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Solder Interconnect Predictor (SIP) Software Package

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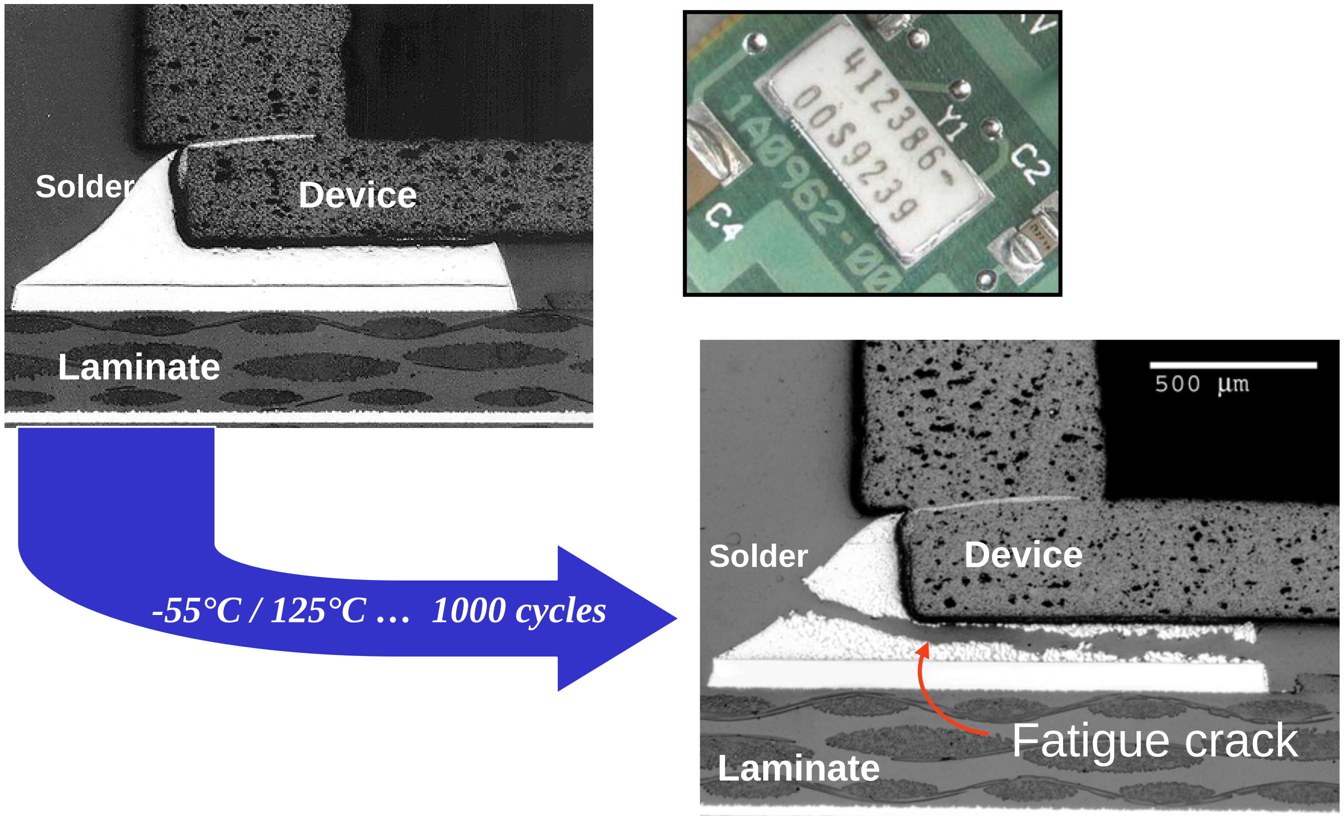
‡Sandia is a multi-program laboratory operated by Sandia Corp, a Lockheed Martin company, for the US Dept. of Energy under contract DE-AC04-94AL85000.

Outline

- Objectives
- Constitutive model for 63Sn-37Pb solder
- Solder Interconnect Predictor (SIP)
- Pb-free (95.5Sn-3.9Ag-0.6Cu) SIP
- Summary

Motivation



Thermal mechanical fatigue causes 63Sn-37Pb solder to coarsen and to eventually fail.

Objectives

- Create software package (SIP) to predict lifetime of soldered interconnections

  - "User-friendly" – use by any product/process engineer

  - Quick turn-around on analyses (less than one hour on desktop

  - Flexibility to address current and near-future packages

  - Easy to add new solder material models, other solder joint types, etc.

Constitutive Model for 63Sn-37Pb Solder

Constitutive Relation $$\dot{\sigma} = \mathbf{E} : (\mathbf{d} - \mathbf{d}^{in})$$

Inelastic Strain Rate $$\mathbf{d}^{in} = \frac{3}{2}\dot{\gamma}\mathbf{n} = \frac{3}{2} f \exp\left(\frac{-Q}{R\theta}\right)\left(\frac{\lambda_o}{\lambda}\right)^p \sinh^m\left(\frac{\tau}{\alpha(c+\hat{c})}\right)\mathbf{n}$$

Normalized Stress Difference Tensor $$\mathbf{n} = \frac{\left(\mathbf{s} - \frac{2}{3}\mathbf{B}\right)}{\tau}$$

von Mises Effective Stress $$\tau = \sqrt{\frac{3}{2}\left(\mathbf{s} - \frac{2}{3}\mathbf{B}\right) : \left(\mathbf{s} - \frac{2}{3}\mathbf{B}\right)}$$

Evolution Eq. for State Variable c $$\dot{c} = A_1\dot{\gamma} - (A_2\dot{\gamma} + A_3)(c - c_o)^2$$

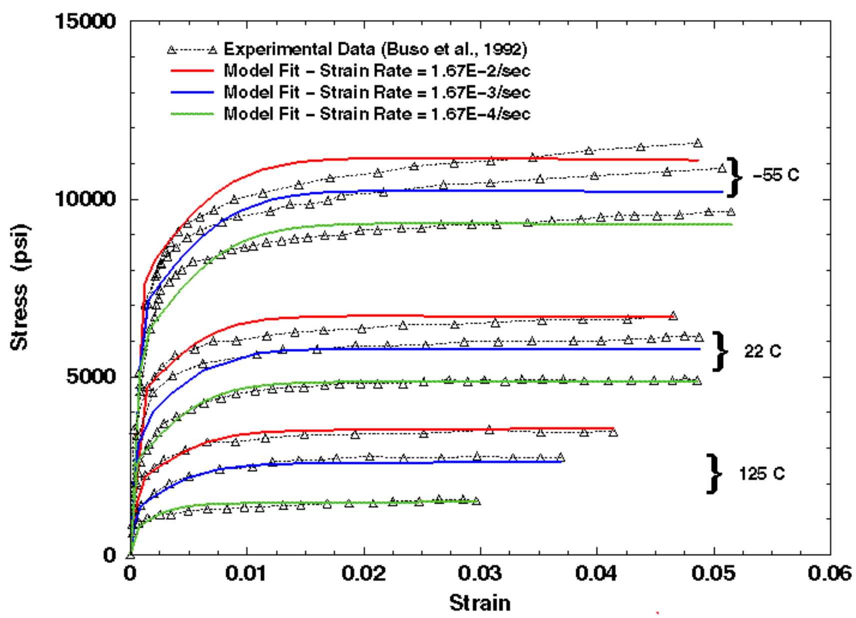
Evolution Eq. for State Tensor B $$\dot{\mathbf{B}} = A_4\mathbf{d}^{in} - (A_5\dot{\gamma} + A_6)\sqrt{\left(\frac{2}{3}\mathbf{B} : \mathbf{B}\right)}\,\mathbf{B}$$

Effect of Coarsening on Strength (Hall-Petch Relationship) $$\hat{c} = A_7\left(\frac{\lambda_o}{\lambda}\right)^{A_8} \qquad A_8 = \frac{1}{2}$$

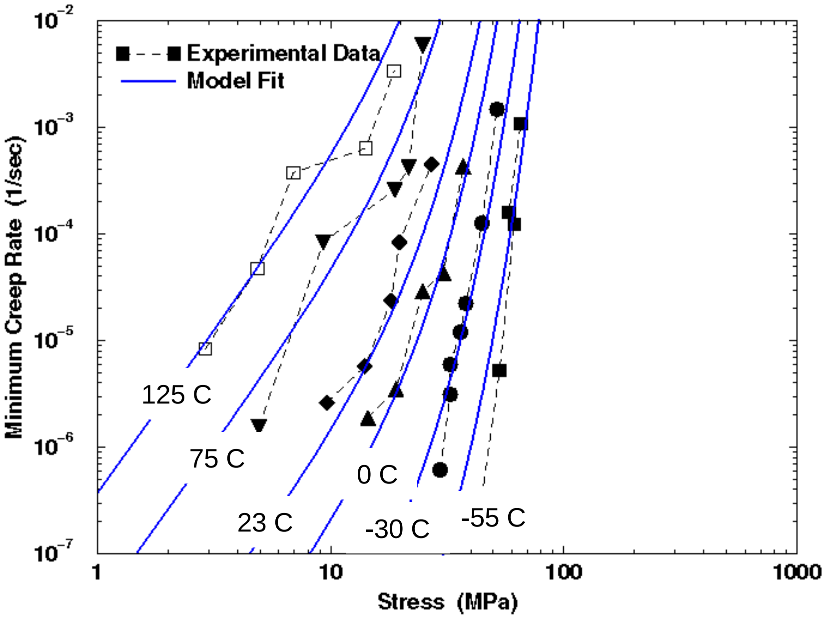
Coarsening Rate (Pb-rich Phase Size) $$\dot{\lambda} = \frac{(A_9 + A_{10}\dot{\gamma})}{(\lambda - \lambda_o)^{A11}}$$

63Sn-37Pb Solder Response to Mechanical Loading

Constitutive Model vs. Experimental Data



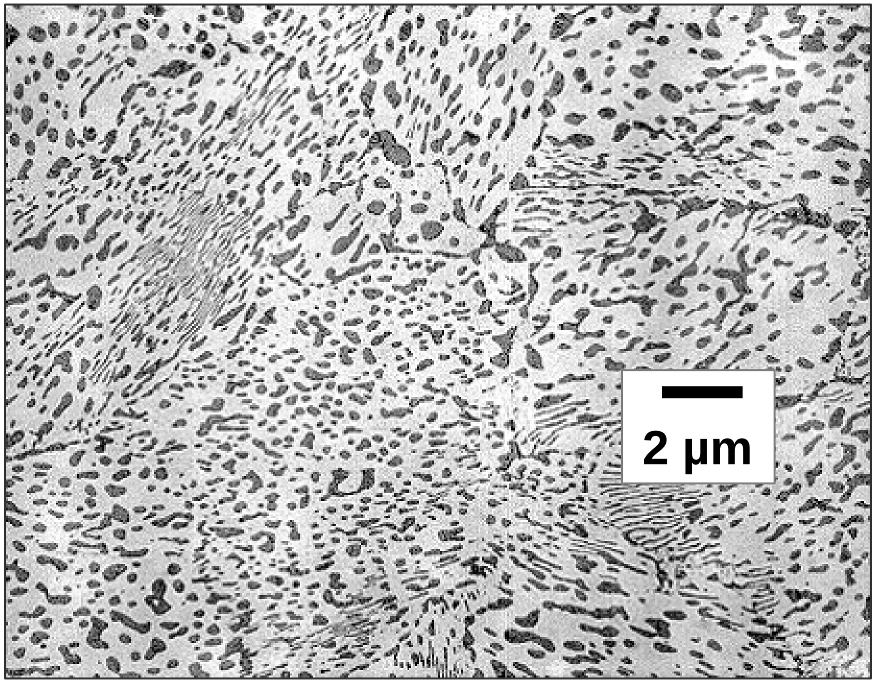
Uniaxial Compression



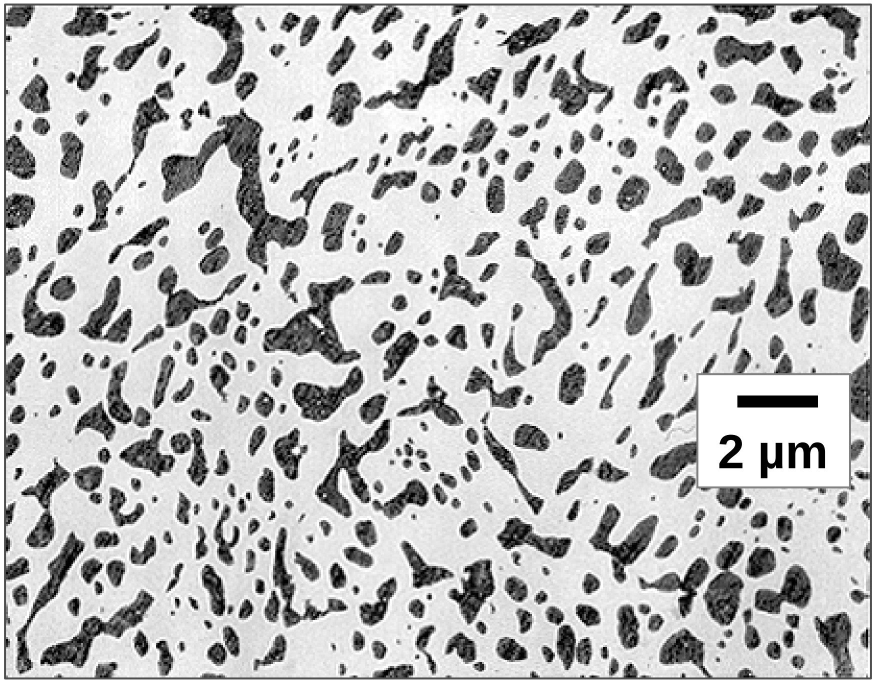
Steady-State Creep

Coarsening of 63Sn-37Pb Solder

Experimental Study of Solder Coarsening
Paul Vianco et al., Journal of Electronic Materials, 1999



As Fabricated



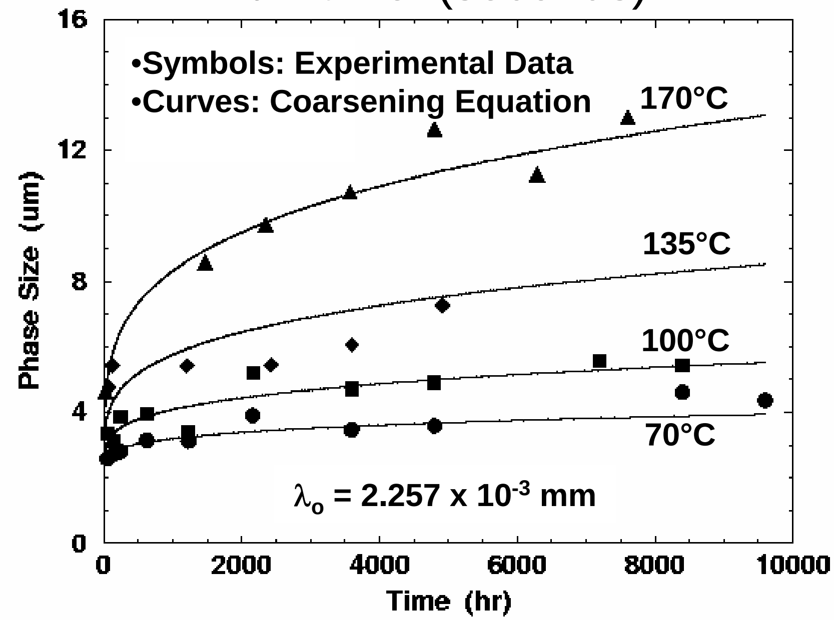
Aged at 100C for 350 Days

Coarsening of 63Sn-37Pb Solder

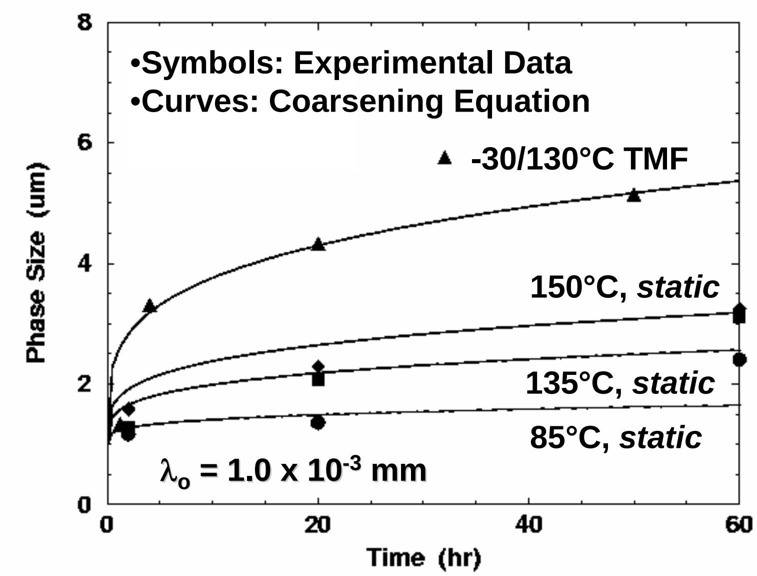
$$\lambda = \lambda_o + \{[4.10 \times 10^{-5} e^{-11023/T} + 15.6 \times 10^{-8} e^{-3123/T} (d\gamma/dt)]t\}^{0.256}$$

λ = Pb-rich phase particle diameter (mm) T = Temperature (°K)

t = time (seconds) γ = inelastic strain



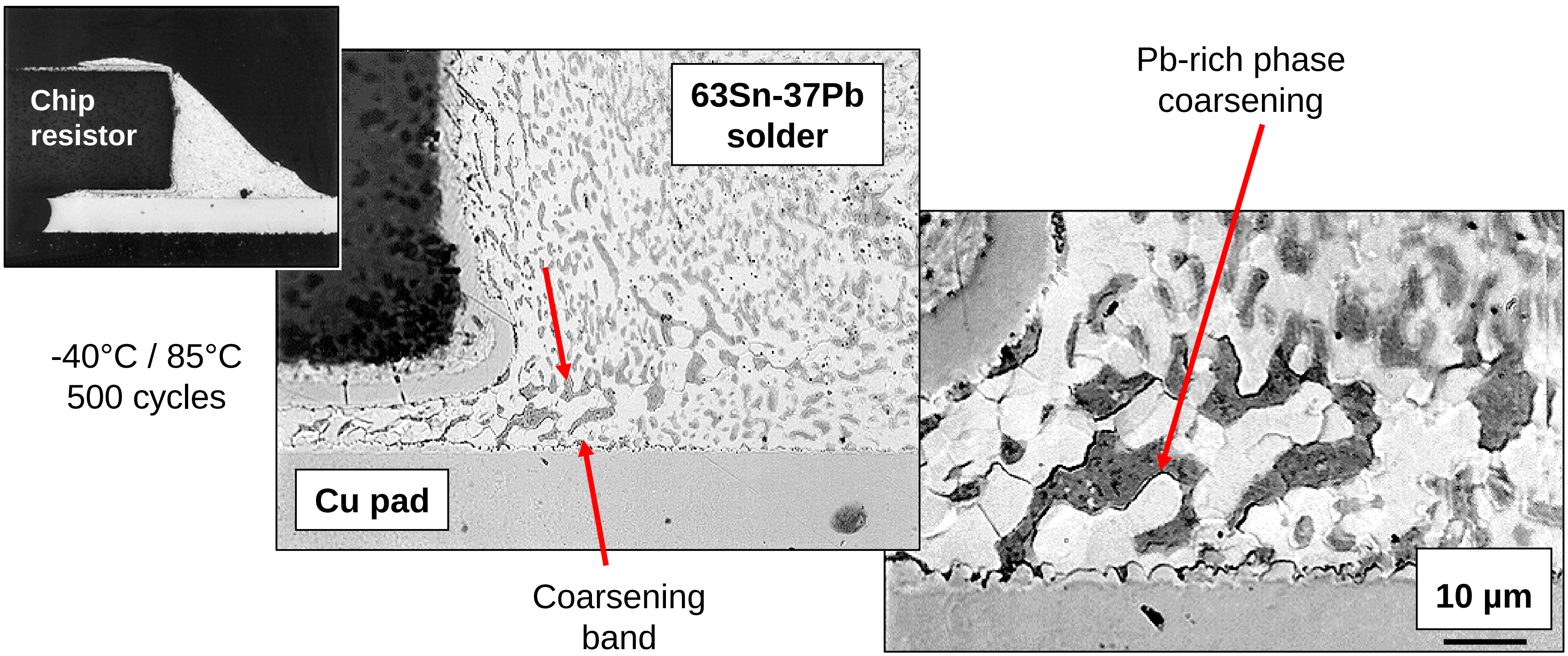
Fit to Vianco et al's Static Anneal Data (Journal of Electronic Materials, 1999)



Fit to Hacke,Sprecher, and Conrad TMF Data (J.E.P. 115 1993)

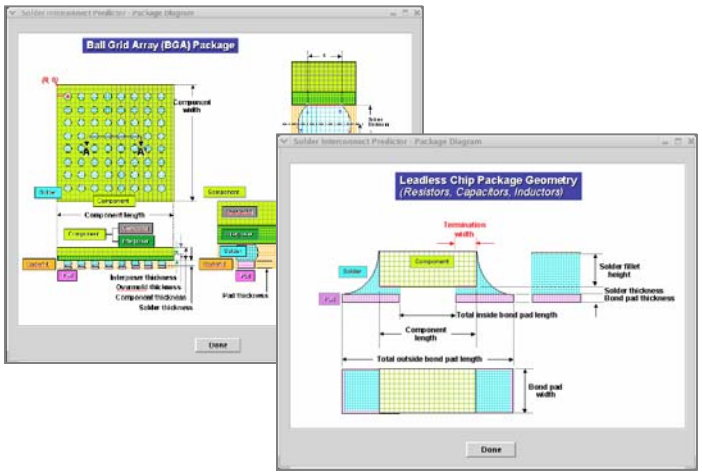
Failure Criteria for 63Sn-37Pb Solder

- Microstructure-based Failure Criterion: fail when $\lambda = \lambda_{critical} = 0.0078$ mm
- Coffin-Manson Criterion: Cycles to failure, N_f , given by: $\Delta\gamma_p N_f^{\alpha} = \theta$



Solder Interconnect Predictor on WindowsXP

Solder
Interconnect
Predictor



Mesh Generation Tools:
Fastq, Gen3d, Gjoin, Grepos

Finite Element Code:
JAS-3D

Material Models:
Eutectic Sn-Pb Solder Model
UCPD Model for Pb-free Solder
…

Post-Processing:
BLOT

SIP software development

Solder Interconnect Predictor (SIP) software was developed under contract with Strikewire Technologies (Louisville, CO).

Package geometries

- Ball grid array (BGA)
- Chip scale package (CSP)
- Gull wing packages (e.g., SOICs, SOTs, QFPs, etc.)
- J-leaded packages
- Flip chip (FC) package
- Diodes
- Passive chip devices (e.g., resistors, capacitors, etc.)
- Leadless ceramic chip carriers (LCCC)

SIP software development

Material types

Component	Alumina (resistors and LCCCs), titanate (capacitors), glass (diodes) overmolding (PEMS), interposer (area array), and Si (die for FC)
Substrate	Epoxy-glass (FR-4), BT epoxy-glass, polyimide-glass, polyimide-quartz, epoxy-aramid, polyimide-aramid, and alumina (HMCs)
Pad	Cu, AuPtPd (hybrid microcircuits)
Leads	Cu, Fe-Ni-Co alloy
Underfill	

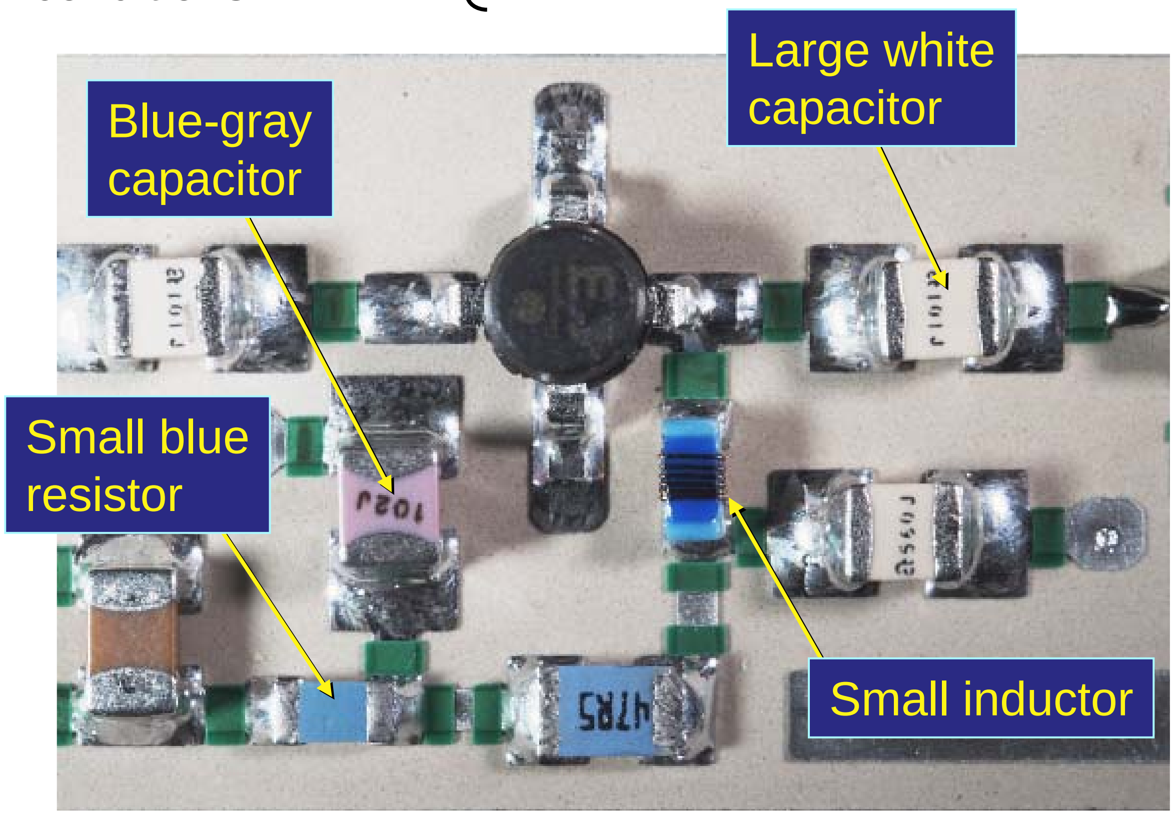
Material properties

- Elastic modulus
- Coefficient of thermal expansion
- Poisons ratio

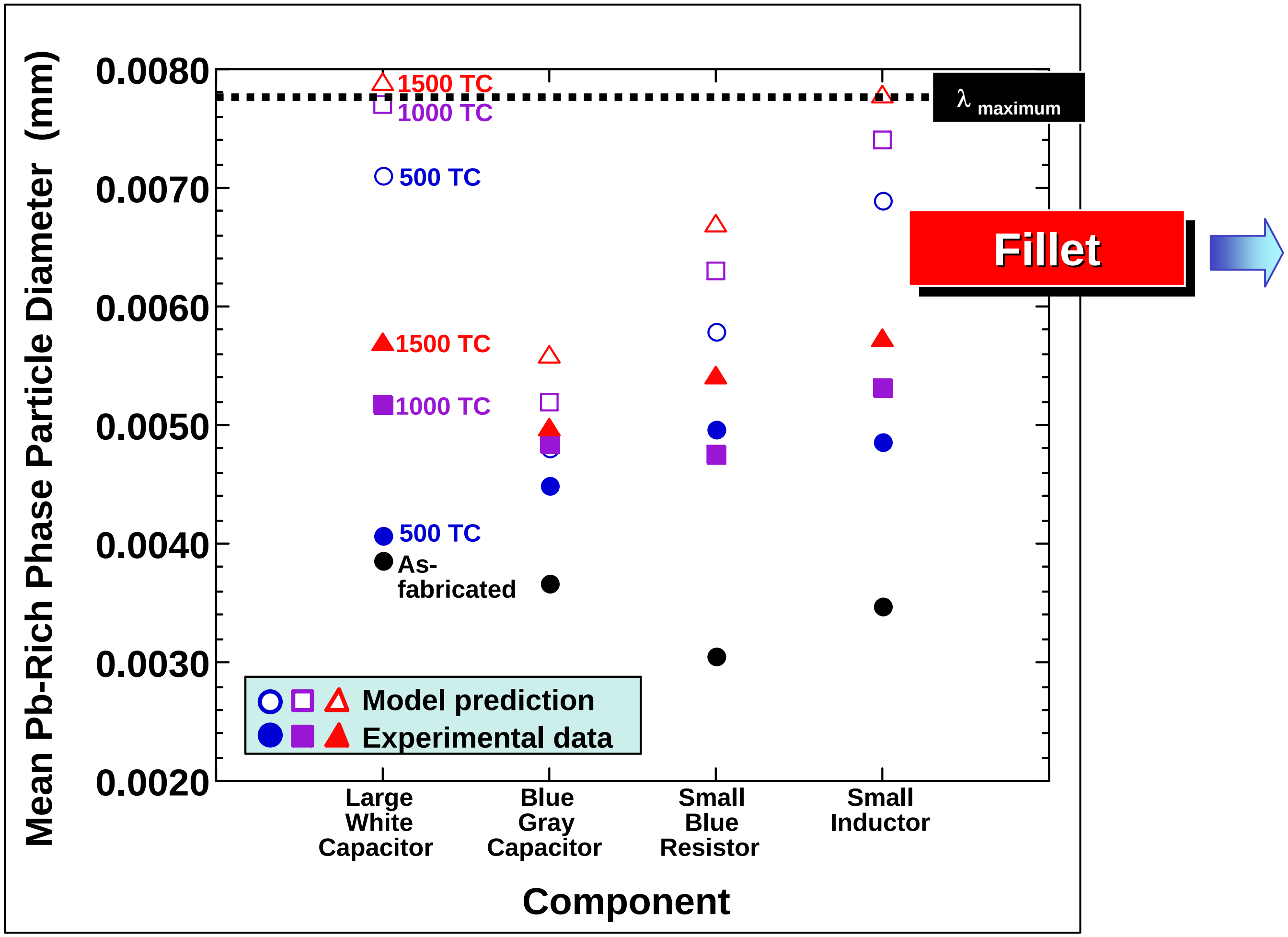
CoMPSIR© model validation hardware

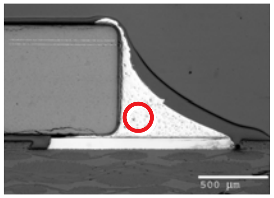
Test vehicle accelerated aging conditions

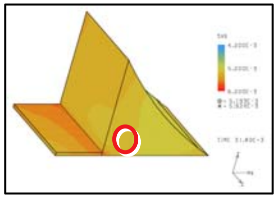
-55°C … 125°C, 20 min holds;
0, 500, 1000, and 1500 cycles



CoMPSIR© model validation







Summary

- A Linux-based version developed by S. Burchett and Strikewire.
- A WindowsXP version developed with Kansas State University
- A new constitutive model for 95.5Sn-3.9Ag-0.6Cu (wt%) lead-free solder developed by Fossum et al.
- This new material model will be implemented into Pb-Free SIP.
- SIP being validated by comparing predictions with existing experimental data and results from test vehicles.

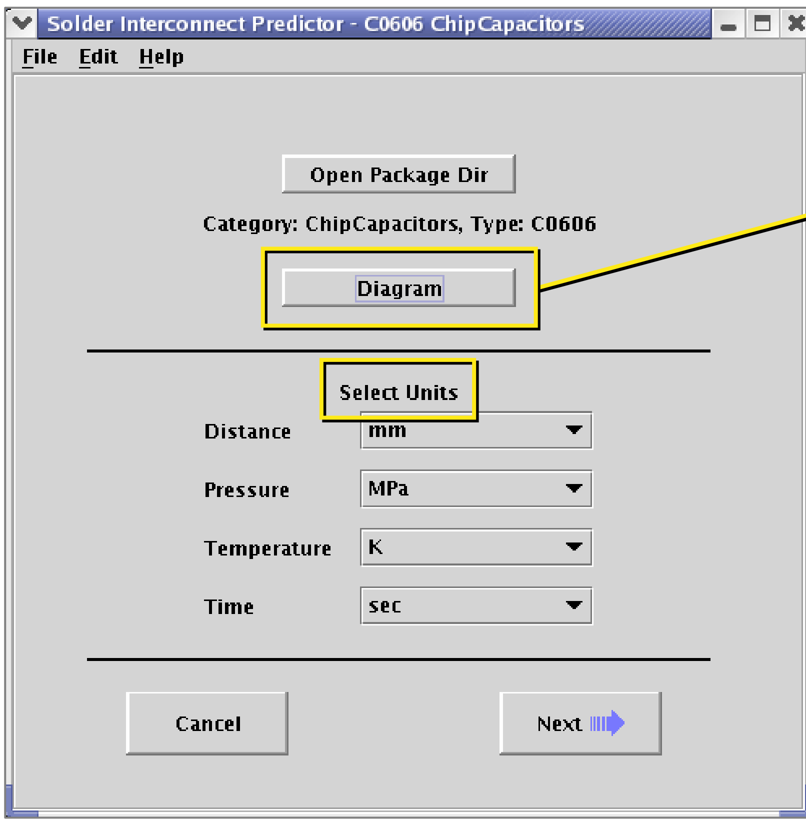
Current Work

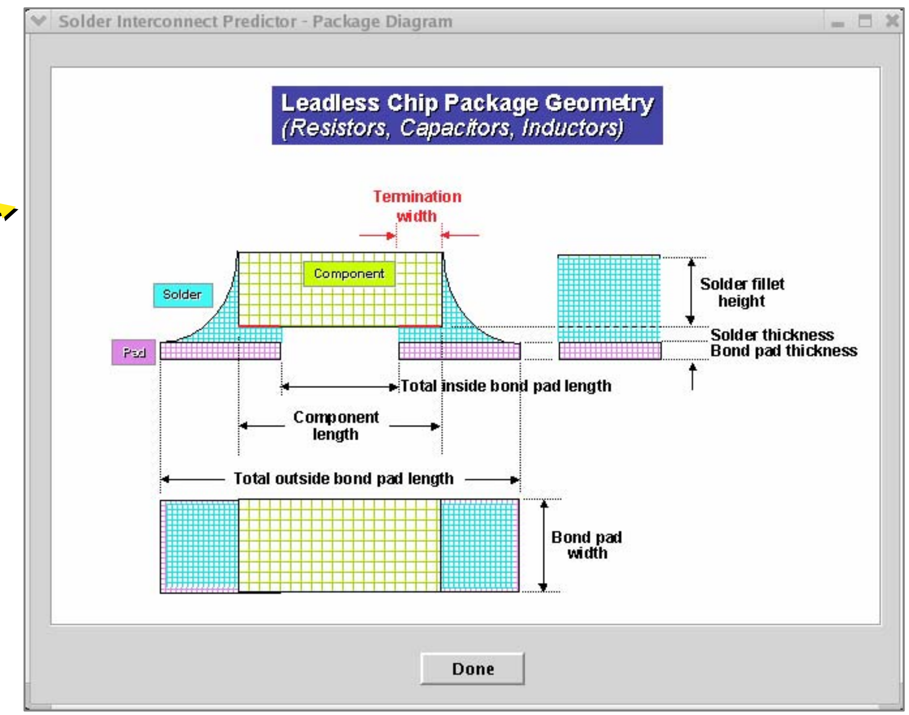
- Development of Windows SIP
  - Fix multiple meshing and JAVA bugs
  - Accuracy of multi-joint model predictions ?
  - Include PTH joint geometry
  - Create Installation sets
- Development of Pb-Free SIP
  - Develop Sip tool for Pb-free solder joints
  - Failure based on volume average (Pierce, Stanford)
- Development of SIPLite
  - Develop initial version of SIPLite
  - Compare SIPLite predictions with thermal cycling experiments
- Validation with Experimental Data (Tom Clifford Round Robin et al)

SIP software development

A brief walk-through will be made of SIP version 0.8.

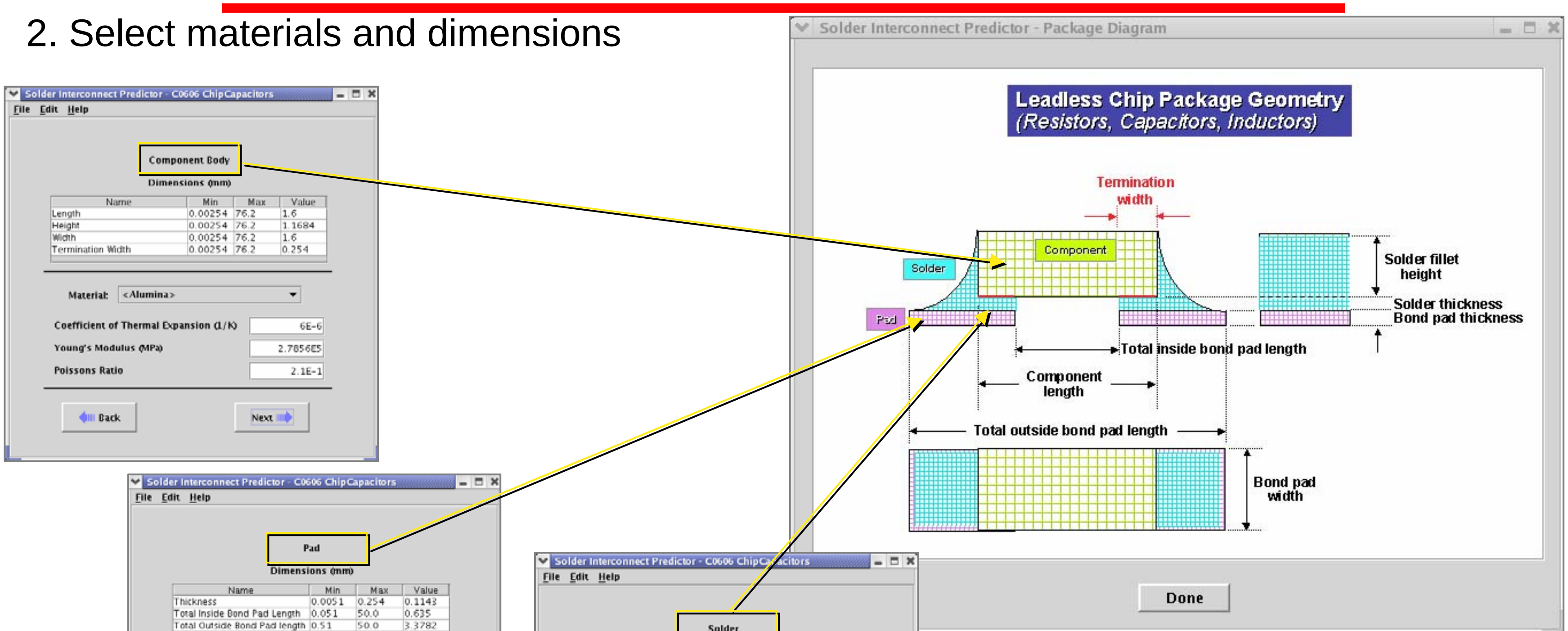
1. Select package type and preferred units system

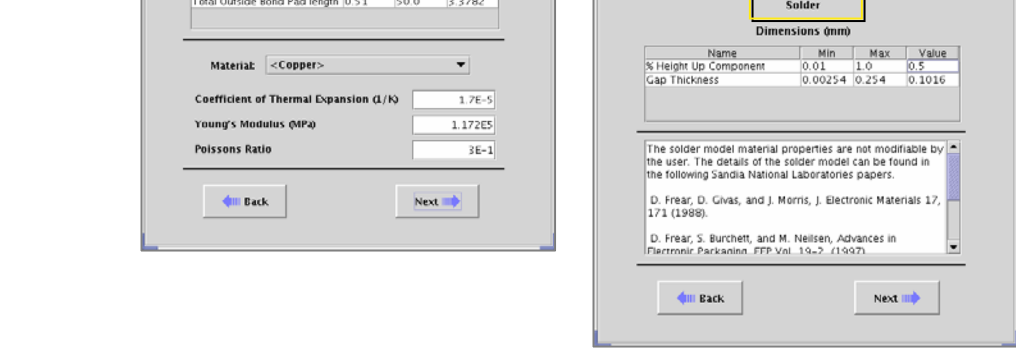




SIP software development

2. Select materials and dimensions

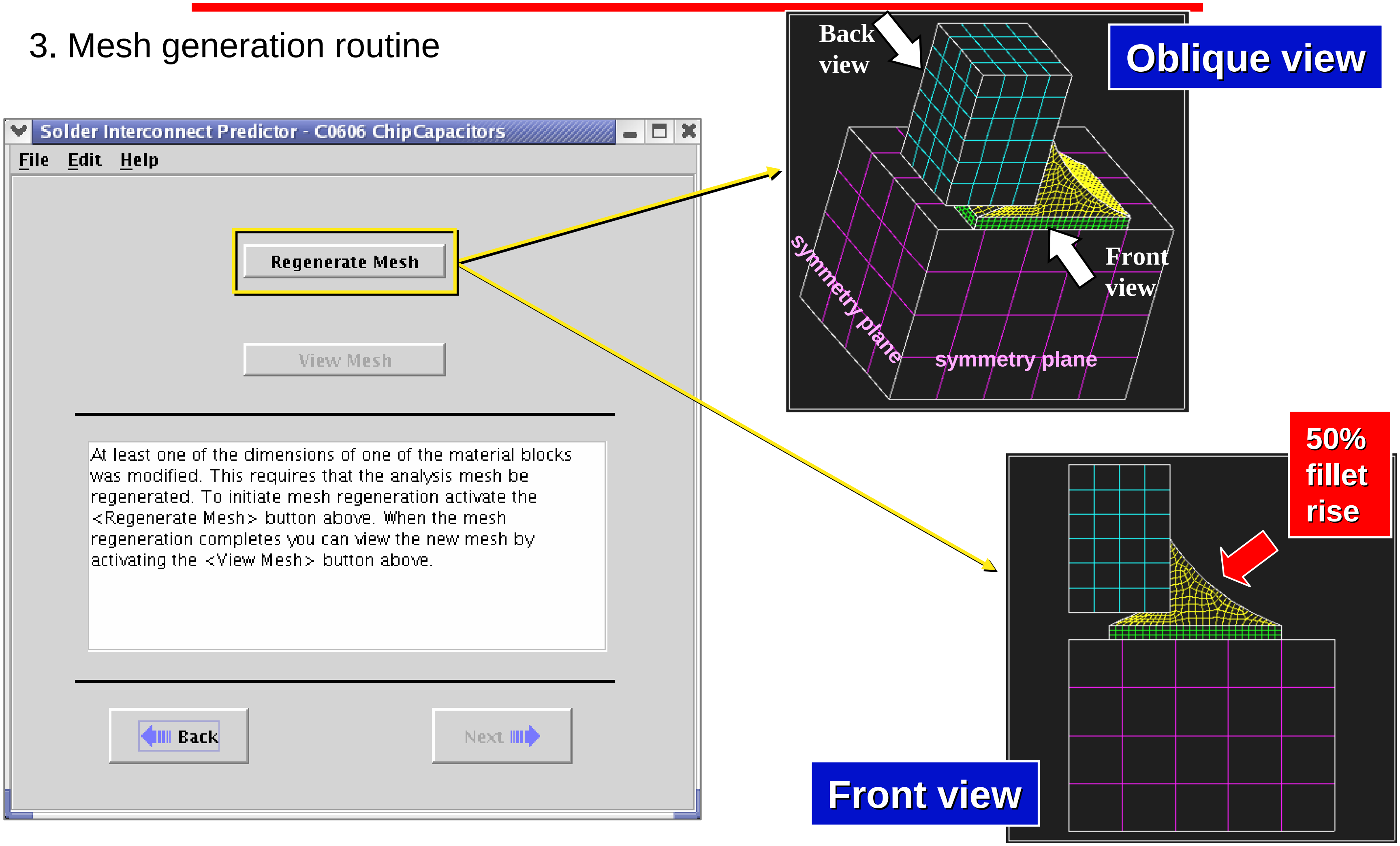




The fillet rise, fillet extent and gap thickness can be changed to reflect variations of manufacturing processes.

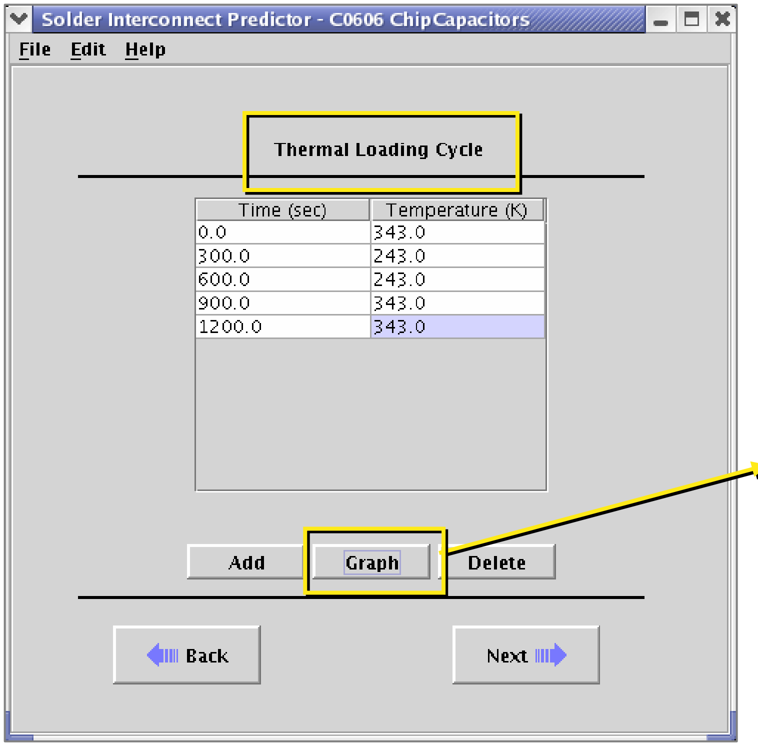
SIP software development

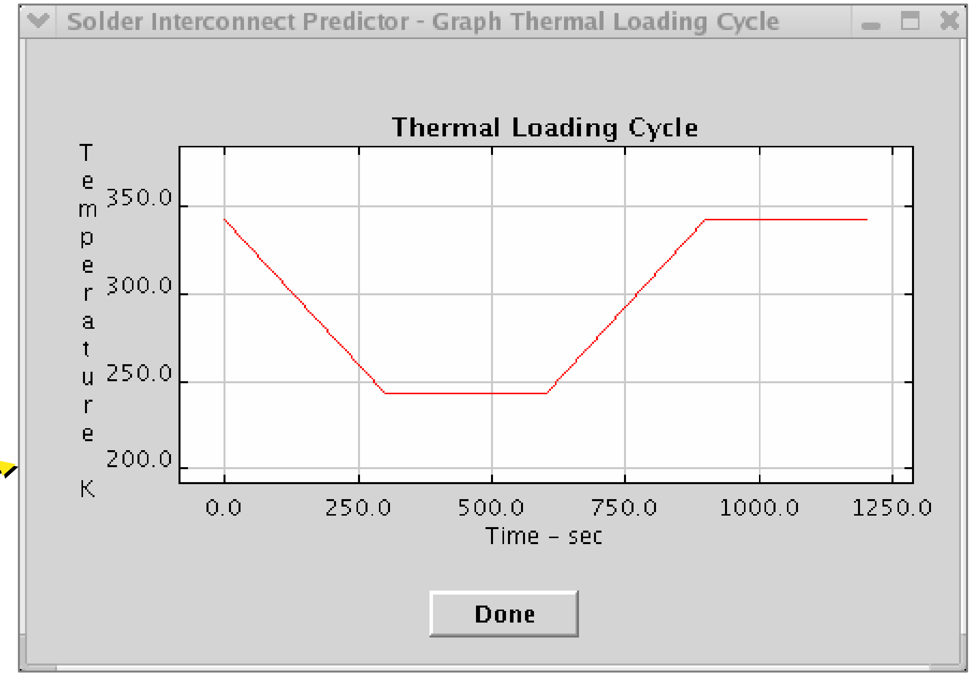
3. Mesh generation routine



SIP software development

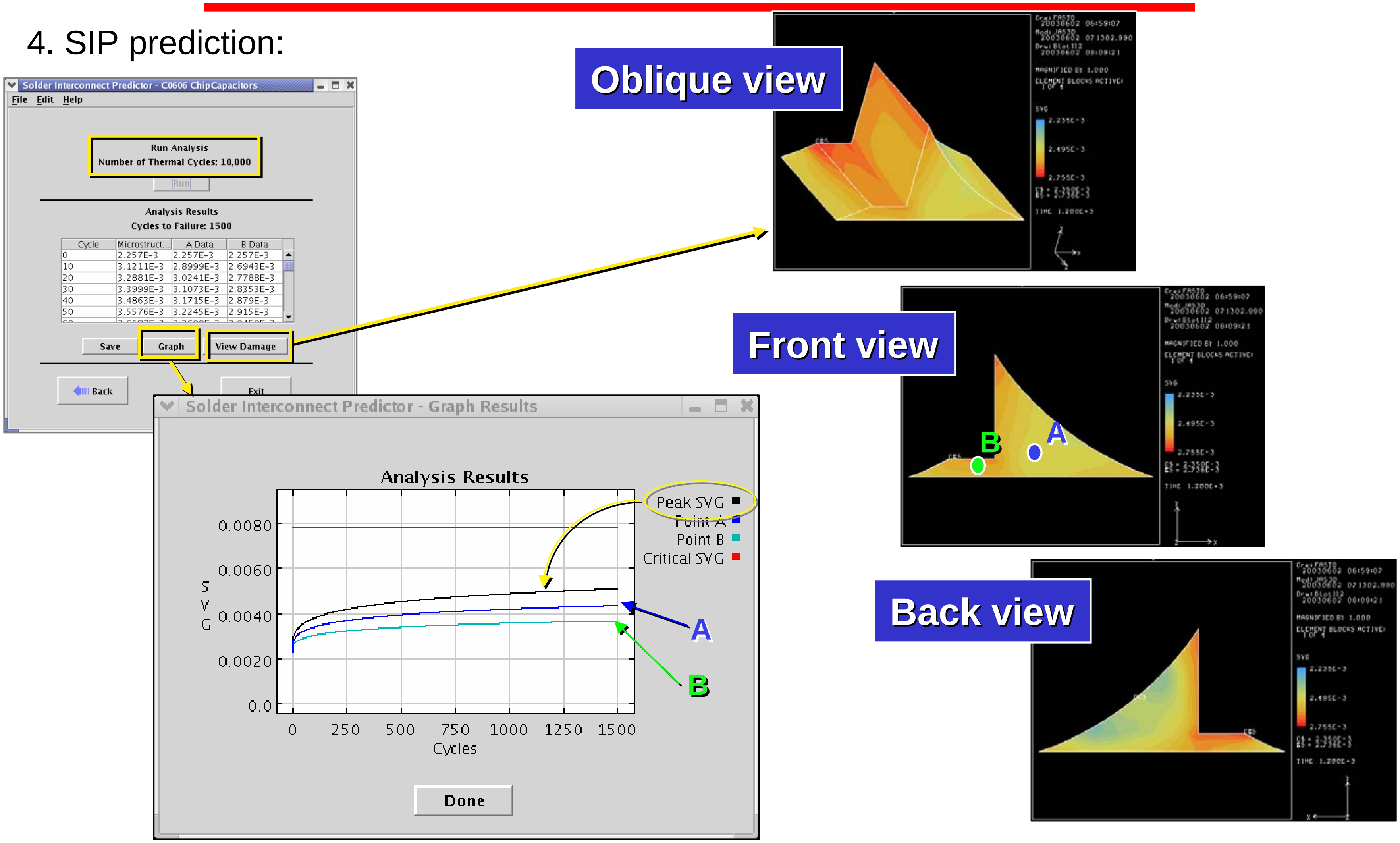
4. Prescribe thermal cycle temperature history.





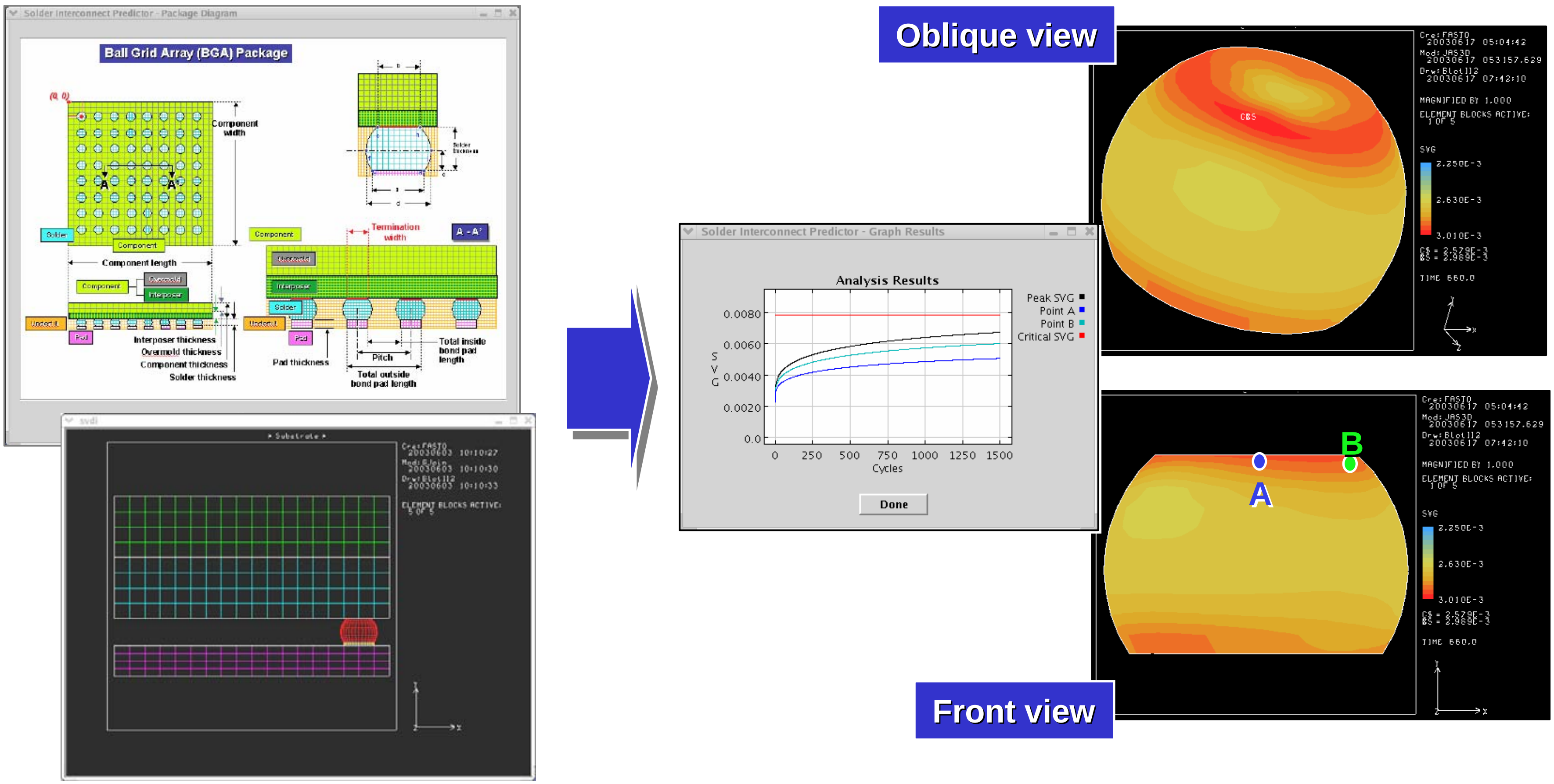
SIP software development

4. SIP prediction:



SIP software development

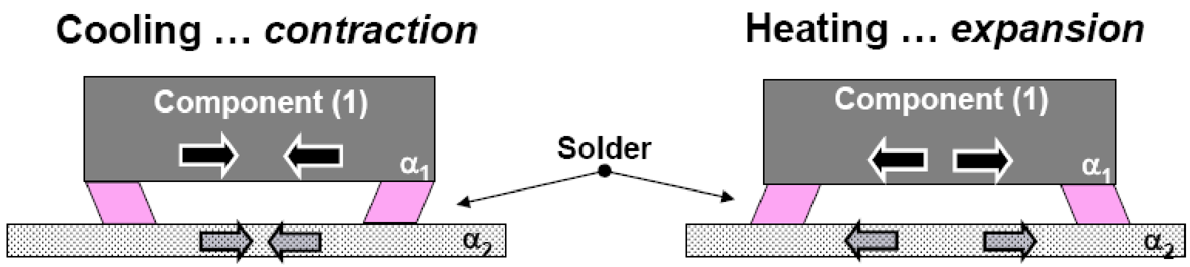
The SIP prediction for a ball-grid array (BGA) solder joint



SIPLite

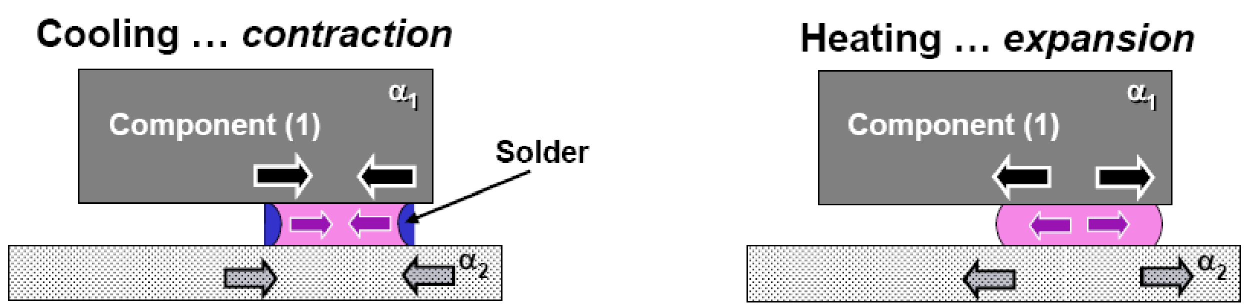
- Just like SIP but with Closed-Form Solutions to get EQPS in place of FEA.
- Based on following assumptions:
  - solder strain is caused by differential expansion of component or lead for FP and QFP and board
  - solder accommodates all differential expansion
  - differential expansion between solder and component/board not included
- Currently 1 EXCEL Spreadsheet and Small Fortran Programs.

SIPLite



Global thermal expansion mismatch: $\alpha_{\text{component (1)}} < \alpha_{\text{circuit board (s)}}$

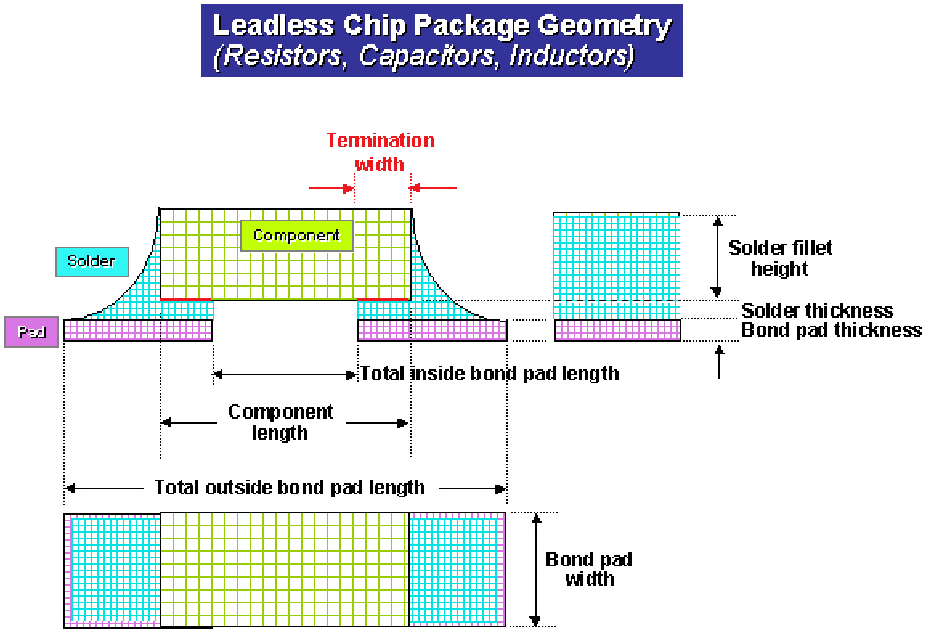
SipLite Captures Global Expansion Mismatch



Local thermal expansion mismatch: $\alpha_{\text{component (1)}} < \alpha_{\text{circuit board (s)}} << \alpha_{\text{solder (3)}}$

SipLite Does NOT Capture Local Expansion Mismatch

SIPLite



Input: Component Length (L)
Component Width (W)
Component TEC (α_C)
Board TEC(α_B)
Temperature History (ΔT)
Solder Thickness (h)

Compute: $X = L/2.0$
$Y = W/2.0$

$$\gamma_{XZ} = (\alpha_B - \alpha_C)\, \Delta T(X/h)$$

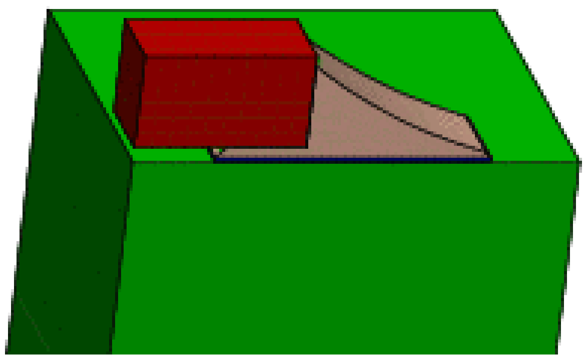
$$\gamma_{YZ} = (\alpha_B - \alpha_C)\, \Delta T(Y/h)$$

$$\Delta EQPS = 2\sqrt{\frac{1}{3}\left(\gamma_{xz}^2 + \gamma_{Yz}^2\right)}$$

$$N_{Coffin-Manson} = \left(\frac{1.31636}{\Delta EQPS}\right)^{1.96078}$$

$$N_{Micro-Parameter} = f(T, \Delta EQPS)$$ numerically

SIPLite



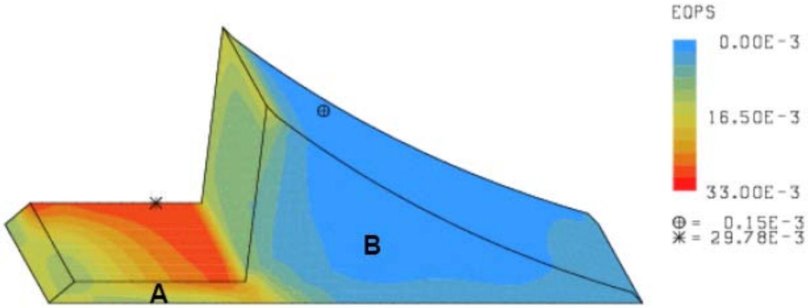
Input: Component Length (L)	0.039 in.
Component Width (W)	0.019 in.
Component TEC (α_C)	6.4 ppm/C
Board TEC(α_B)	17.5 ppm/C
Temperature History (ΔT)	135 C
Solder Thickness (h)	0.0012 in.

Compute: $X = L/2.0$

$Y = W/2.0$

$\gamma_{XZ} = (\alpha_B - \alpha_C)\,\Delta T(X/h)$ 0.02435

$\gamma_{YZ} = (\alpha_B - \alpha_C)\,\Delta T(Y/h)$ 0.01186



$$\Delta EQPS = 2\sqrt{\frac{1}{3}\left(\gamma_{XZ}^2 + \gamma_{YZ}^2\right)}$$ 0.03128

$$N_{Coffin-Manson} = \left(\frac{1.31636}{\Delta EQPS}\right)^{1.96078}$$ 1529

$$N_{Micro-Parameter} = f(T, \Delta EQPS)$$ 2447