

FAST AND SLOW BORDER TRAPS IN MOS DEVICES

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There is a lot of interest in understanding the roles of interface traps, oxide traps, and/or border traps during switched-bias annealing or charge-injection studies after irradiation or high-field stress [1-9]. Changes in inferred interface-trap densities are often reported [6,9]. It is usually not clear whether these changes are truly due to interface traps, or whether some may be due to border traps [7,10,11]. In this summary we apply a "dual-transistor border-trap" (DTBT) technique that combines high-frequency charge-pumping and lower-frequency threshold-voltage measurements to estimate bulk-oxide-trap, interface-trap, and border-trap densities in irradiated MOS transistors [10]. This method takes advantage of the different time scales in which interface traps and border traps exchange charge with the Si to obtain an estimate of the density of faster border traps often mistaken for interface traps. Effects of slower border traps are also inferred from changes in the "bulk" oxide-trap charge density through switched-bias annealing. To our knowledge, this is the first time fast and slow border-trap effects have been separated quantitatively in MOS devices. Possible microstructures for fast and slow border traps are suggested.

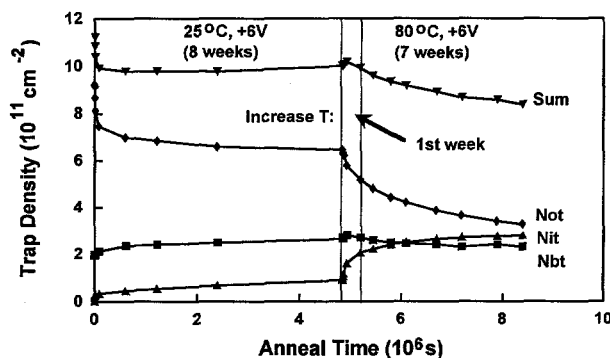


Fig. 1: ΔN_{it} , ΔN_{bt} , and ΔN_{ot} vs. anneal time for transistors with soft 45-nm oxides irradiated to 45 krad(SiO_2) with 10-keV x rays.

In Fig. 1 we show bulk-oxide-trap, interface-trap and fast border-trap densities (ΔN_{ot} , ΔN_{it} , and ΔN_{bt}) for MOS transistors with soft 45 nm oxides. Immediately after irradiation, there are very few interface traps (triangles) for these devices. Almost all effects that would be attributed to interface traps by midgap and/or subthreshold techniques (not shown) during irradiation and 25°C anneal in Fig. 1 are really due to border traps (squares). When the anneal temperature is increased to 80°C, the density of border traps decreases slightly and the density of interface traps increases dramatically. This leads to nearly equivalent interface and border trap densities following the ~ 5.7 -wk 80°C anneal at +6 V.

We now focus on changes in defect densities during the first week after the temperature is raised to 80°C, where much of the increase in ΔN_{it} occurs. At the same time, there is a large drop in bulk-oxide-trap charge density. In fact, the decrease in ΔN_{ot} during this period ($\sim 1.2 \times 10^{11} \text{ cm}^{-2}$) is approximately equal to the increase in ΔN_{it} ($\sim 1.1 \times 10^{11} \text{ cm}^{-2}$). During this interval, the border-trap density is essentially unchanged, as is the total defect density. These data and their possible relevance to (1) "latent" interface-trap buildup [12] and (2) trapped positive-charge to interface-trap conversion models will be discussed at the SISC.

Figure 2 shows successive -6 V, +6 V, and -6 V annealing periods at 80°C that follow the data of Fig. 1 chronologically. Comparing endpoints of Fig. 1 to the beginning of Fig. 2, one can see switching to negative bias moves the border-trap density from just under the interface-trap density to just above it. Border traps remain more significant than interface traps for the rest of the annealing periods.

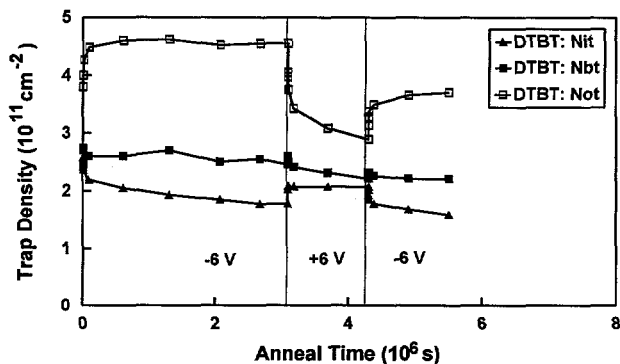


Fig. 2: ΔN_{it} , ΔN_{bt} , and ΔN_{ot} vs. anneal time for the devices of Fig. 1. The anneal temperature was 80°C.

Consistent with previous work [1-9], ΔN_{ot} increases after the switch to -6 V bias at the beginning of the first interval in Fig. 2. Upon return to +6 V in the second interval, ΔN_{it} increases, and ΔN_{bt} and ΔN_{ot} decrease. A return to negative bias leads to a decrease in ΔN_{it} , an increase in ΔN_{ot} , and little change in ΔN_{bt} . As in previous studies, the reversibility in ΔN_{ot} is attributed to the exchange of negative charge with the Si due to the presence of border traps too slow to exchange charge with the Si during threshold-voltage measurements [1,3,6-9]. These may be metastable electron traps associated with trapped holes [1,3,7,9-11], and/or anomalous positive charge (APC) [4,8]. The value of ΔN_{it} appears to show a clearer trend toward reversibility (going up when the bulk-oxide-trap charge goes down, and vice versa) than fast border traps during the switched-bias anneals.

We now discuss what defects may cause the two types of border-trap effects in Figs. 1 and 2. First, there are faster border traps whose density is estimated via the DTBT technique. These switch like interface traps, but on slower time scales [7,10,11]. Their density increases by $\sim 30\%$ during the initial 25°C anneal in Fig. 1, and decreases $\sim 15\%$ during the 80°C anneals in Fig. 2 without much dependence on bias. The second type of border trap is a slower defect responsible for the reversibility of ΔN_{ot} . The reversible portion of the ΔN_{ot} in Fig. 2 (less than $\sim 1.5 \times 10^{11} \text{ cm}^{-2}$) due to slow border traps is smaller than ΔN_{bt} , and has a much different dependence on anneal bias, suggesting that fast and slow border traps may differ in microstructure.

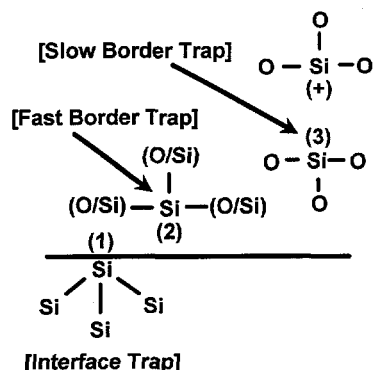


Fig. 3: Interface traps (P_b defects), and possible O-vacancy-related fast ($O_{3-x}Si_xSi\bullet$) and slow (E'_y) border traps in SiO_2 . Sites (1) and (2) are positively charged at large negative bias and negatively charged at large positive bias. Site (3) is neutral at large negative bias and negatively charged at large positive bias.

Figure 3 shows a schematic illustration of interface traps and O-vacancy-related fast and slow border traps that is consistent with the results of Figs. 1 and 2. The interface trap (site 1) is the classic P_{b0} center [5]. A strong correlation between slow border traps and E'_y centers (site 3) was demonstrated in oxides processed similarly to those of Figs. 1 and 2 by Warren et al. [13]. The slow border trap depicted in Fig. 3 is a version discussed by Lelis et al., where the defect may be altered by strain [3] or high electric fields near the interface.

One candidate for the fast border trap in Fig. 3 is the $O_{3-x}Si_xSi\bullet$ family of defects. For $x = 0$, the Si atom above Site 2 is surrounded by three O atoms. This is the E'_s defect [13-15], which is also sometimes called the hemi- E' center [13] because it is essentially one half of the E'_y center (Fig. 3). This center is known to have gap states, which are emphasized by O'Reilly and Robertson to be electrically similar to those of the E'_y center [14]. For $x = 3$, the Si atom above Site (2) is surrounded by three Si atoms, forming the so-called D center [16], which is a Si cluster in the oxide that looks very much like a P_b ! So it should not be surprising that such a defect might act like an interface trap, only switching more slowly since it is in the near-interfacial oxide instead of at the interface. Cases for $x = 1$ or 2 are similar to

structures invoked to describe the P_{b1} center at the (100) Si/SiO₂ interface by Poindexter [5], though this interpretation has been questioned. It would be interesting to consider the possibility of these centers acting as border traps, rather than interface traps. Further comparisons with electron paramagnetic resonance data and defect-energy calculations will be presented at the SISC.

The defects in Fig. 3 can explain many aspects of Figs. 1 and 2. However, much of the switching response is similar to classic bias-temperature instabilities in SiO₂. These are often attributed to the polarization and/or decomposition of water near the interface [5,17], suggesting that some results in Figs. 1 and 2 may be due to the motion of charged hydrogen species, e.g., $(OH)^-$ and/or H^+ , liberated by bond breaking during irradiation. These may be exchanged between the near-interfacial oxide and near-surface Si during switched-bias anneals. This may be consistent with the association of hydrogen with APC in some oxides [4,6], though H-related defects also can interact with trapped holes [6]. Similar hydrogen chemistry is likely responsible for the reversibility of ΔN_{it} in Figs. 1 and 2. The nature of these defects and their impact on MOS radiation response and reliability will be discussed further at the SISC.

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