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CERAMIC-POLYMER COMPOSITE FOR HIGH ENERGY DENSITY CAPACITORS

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Abstract

The U.S. Department of Defense vision for future directed energy weapons systems (e.g., high power microwave systems) requires the development of electrical pulsers that exceed current state-of-the-art in energy storage density by an order of magnitude or more. Capacitors made from composite dielectric materials consisting of ceramic nanoparticles embedded in a polymer matrix show promise for attaining these goals. Sandia National Laboratories (SNL) and TPL Inc. (TPL) have teamed to investigate the limits of these new materials for use in high energy density and high power capacitor designs. The major challenges encountered thus far are quality control in the processing of the materials as well as mechanical stresses resulting from the thermal curing process while forming prototype capacitor devices. This paper reports on the current status and results achieved by this investigation.

I. INTRODUCTION

There are at least two commercially available capacitor technologies capable of ~10MW/J discharge powers: oil/paper/film/metal foil windings [1] and $BaTiO_3$/$SrBaTiO_3$ single layer ceramic blocks (e.g., "door knob" capacitors [2]). Typical energy densities achievable by these technologies are 0.1J/cc and 0.05J/cc, respectively.

An alternative to these conventional technologies and the focus of SNL and TPL's collaborative effort involves the use of a unique dielectric material in a novel capacitor design. From Maxwell's equations, the energy density of an electrostatic field is $\varepsilon E^2/2$, where ε is the permittivity and E is the electric field. Although energy density scales quadratically with electric field but only linearly with permittivity, high permittivities are still desired so that devices with useful capacitance values (e.g., tens of nF) can be made with practical electrode geometries.

Through a combination of polymer science and ceramic processing, TPL has engineered a composite material that possesses the electrical properties required for a substantial increase in capacitor energy density. The composite dielectric material includes a combination of high dielectric constant ceramic nanoparticles uniformly dispersed in an epoxy resin system. Previous studies of similar composite materials have shown that nanoparticles may be introduced into a polymer matrix with significantly less degradation of the dielectric strength than for microscale particle fillers [3].

In this study, the nanoparticles (Fig.1) are formulated and surface modified in an effort to maintain the dielectric strength of the polymer resin while increasing the dielectric constant. High concentrations of the nanoparticles incorporated into the thermal setting polymer are then cast as a liquid and cured in electrode

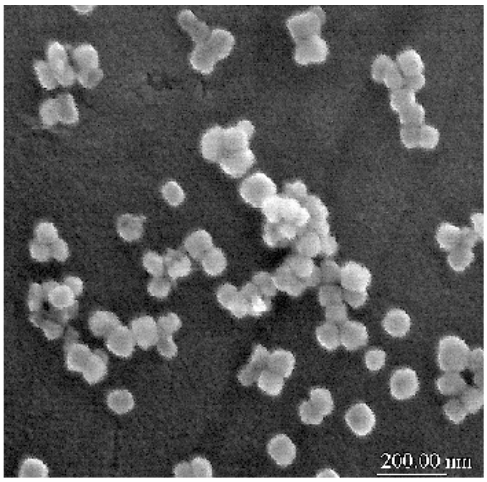

Figure 1. SEM image of the ceramic nanoparticles used in this investigation (the image shows an area approximately 1.4 microns by 1.4 microns).

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[2] Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

assemblies to generate compact capacitors. Multi-layer electrode geometries allow for efficient use of the high energy density material system. And although thin electrodes are desired to minimize electrode volume, which cannot store electrostatic energy, electric field enhancements due to the smaller edge radius of thin electrodes limit the average electric field that may be applied to the bulk of the dielectric material. In addition, a low inductance electrode geometry is also required for high power discharge. Finally, a low aspect ratio form factor is desired to facilitate compact Marx pulser geometries based on these capacitors.

For this development effort, the nominal design objective is to develop a 100kV, 400J capacitor capable of ~4GW discharge power that has an energy density of 1J/cc – an order of magnitude advance over commercially available high power capacitor technologies. This study involves four general areas: capacitor design, dielectric materials development, capacitor assembly procedures, and device testing. It is important to note that a viable capacitor device must represent a design compromise between the requirements and limitations of each respective area. The major challenges encountered thus far are quality control in the processing of the materials as well as mechanical stresses resulting from the thermal curing process while forming prototype capacitor devices. This paper reports on the current status and results achieved by this investigation.

II. DIELECTRIC & SINGLE-LAYER CAPACITOR DEVELOPMENT

The first year of this study focused on addressing issues related to composite material processing and electrode material selection and preparation. Evaluations were performed in simple, single-layer capacitor structures, with nominal capacitance values of 1.0nF and a breakdown voltage between 50kV and 100kV. Typical dielectric layer thicknesses for these devices were between 0.5mm and 1mm. A variety of dielectric material process parameters were varied, including nanoparticle dispersion, filtering, and pressure/ temperature conditions during casting and curing. In addition, electrode material and processes for finishing the surface and edges were adjusted to minimize electric field enhancements at electrode edges. The result of the process and design optimization was single layer capacitors with average voltage capability of 3.8 kV/mil (1mil = 25.4μm). The typical measured dielectric constant of this material was 50, corresponding to a material energy density of approximately 5.0 J/cc. Note that the electrode volume and encapsulation volume reduced the finished single layer capacitor energy density by approximately 50%.

Consistent voltage stress capability between 3.5kV/mil and 4.0kV/mil concluded the process development and design evaluations on single layer capacitor geometries. The measured voltage performance agreed well with small area evaluations used to determine intrinsic dielectric strength in combination with modeled field enhancements at the electrode edge. Average dielectric strength of the composite using 16mm diameter spherical electrodes was 8.5kV/mil. Due to a field enhancement factor of approximately 2 at the electrode edges, the voltage stress capability of the single layer capacitor was limited to approximately half the intrinsic dielectric strength of the material (as expected.)

III. MULTI-LAYER CAPACITOR DEVELOPMENT

Continued development of the ceramic-polymer composite capacitor focused on increased capacitance (5nF to 10nF) geometries with increased packaging efficiency. Thus, a low inductance multi-layer design was developed during the second year. The multi-layer geometry increases electrode area in a compact manner, facilitating capacitance scaling to a useful value for Marx bank applications. A CAD rendering of a prototype multi-layer design is shown in Fig. 2 below. The nominal size of the prototype device is approximately 6cm by 6cm by 2cm. Note that this geometry is easily scaled to the desired voltage and capacitance by adjusting the number of electrodes, electrode area, and electrode separation.

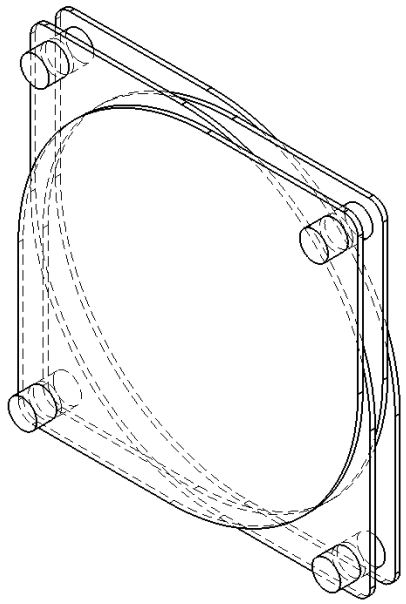

Figure 2. Prototype multi-layer electrode geometry. Nominal plate spacing is 1.27mm. The composite dielectric (not shown) infiltrates the electrode structure as a liquid and is then thermally cured.

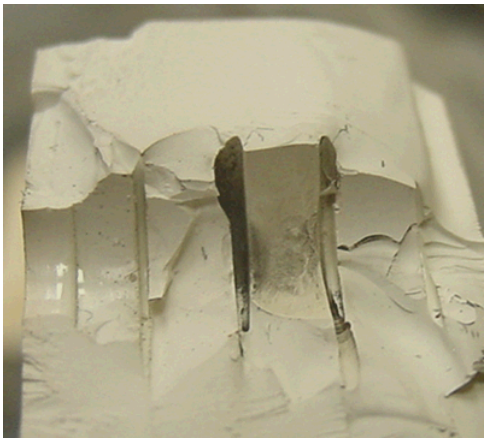

Figure 3. Dielectric material (electrodes removed) after device failure. Carbon on material adjacent to center electrode is evidence of partial discharge and/or arcing. In this device, the distance between electrodes was approximately 1.27mm.

As in the case of single layer capacitors, the fabrication process for multi-layer capacitors included five general steps. First, the multi-layer electrode structure was assembled in a mold with spacers to provide uniform separation between electrodes. Second, the ceramic nanoparticle dispersion was produced in the two part resin system and the composite dielectric material was prepared for casting. Third, the liquid dielectric was infiltrated into the mold assembly, displacing the air between the electrodes. Fourth, the thermal setting resin system was cured under moderate temperature (<100˚C) to form the final capacitor structure. Finally, the cast part was removed from the mold and a common set of electrical contacts were made between alternating electrodes to establish the capacitor terminals.

During this phase of development, it was found that the mechanical constraints of the multi-layer structure were not highly compatible with the dielectric material developed in the first year. For example, poor flow of the composite liquid limited the ability to uniformly infiltrate the electrode structures. Also, incorporation of air during the casting process resulted in voids in the dielectric, representing a voltage-limiting defect. In addition, shrinkage of the dielectric during the cure as well as thermal expansion coefficient mismatch between the dielectric and electrodes led to residual mechanical stress in the dielectric. In severe cases, delamination of the dielectric from the spacers and electrode occurred within the device. High voltage testing, failure, and postmortem examination of these devices yielded evidence of partial discharge in the form of carbonization at the electrode edges (see Fig. 3), resulting in cumulative damage to the dielectric. Single event failures in this dielectric system do not produce this level of carbonization.

Further examination of the partial discharge phenomena revealed that recent electrode edge preparation did not meet earlier processing standards and

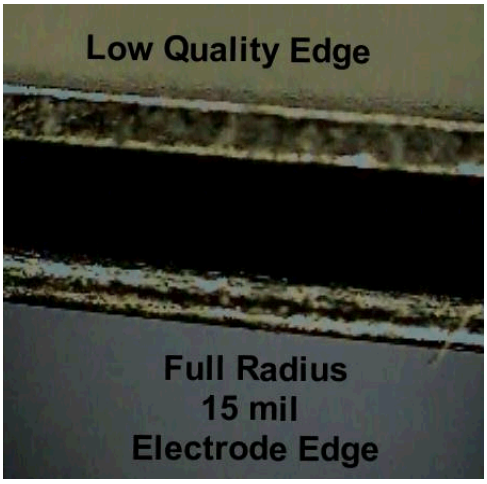

Figure 4. Electrodes with low quality edge preparation (top) compared against those with high quality edge preparation (bottom) were found to contribute to initial device failures.

probably contributed to low lifetime partial discharge induced failures (see Fig. 4). Additionally, the formulation, assembly procedure, and cure process for the dielectric material was adjusted in effort to minimize residual mechanical stress in the final structure. For example, the magnitude of shrinkage during cure is proportional to the concentration of polymer in the composite. Higher loading percentages of the ceramic nanopowder have the desirable effect of reducing shrinkage and increasing permittivity while having the undesirable effect of increasing viscosity during electrode infiltration. Modifications to the formulation and material preparation process were successful in achieving higher particle loading and achieving a reduced viscosity. Further, the cure process was optimized toward achieving full cure of the resin with reduced stress. A time-temperature profile was developed to reduce the rate of cure and limit the peak processing temperature.

IV. TESTING & EVALUATION

For testing of materials and capacitor devices produced by this investigation, an automated test bed was designed and constructed. In this system, a Glassman LX series 150kV power supply charges the device under test though an isolation resistor that also determines the charge current and charge time. The voltage on the device under test (DUT) is monitored via a Northstar VD-200 resistive probe. For simple dielectric strength tests, the DUT is discharged via a Ross relay. For high power testing, the DUT is discharged through a series combination of an inductor and resistor via an SF_6 spark gap. In this case, the load current is monitored via a T&M Research coaxial CVR. The CVR data is recorded by a Tektronix TDS3000B series oscilloscope. A

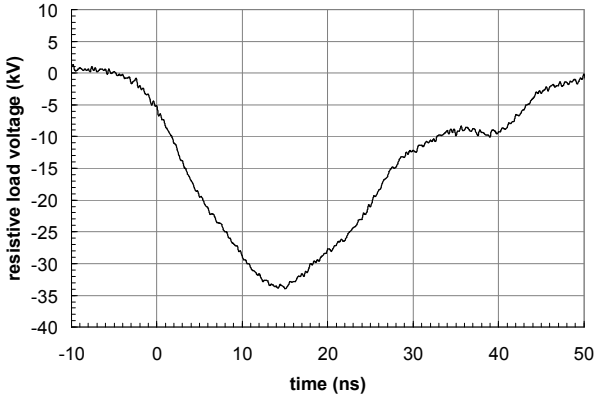

Figure 5. Preliminary high power discharge data from the composite dielectric material stressed at a moderate field (~1.5kV/mil) into a resistive load.

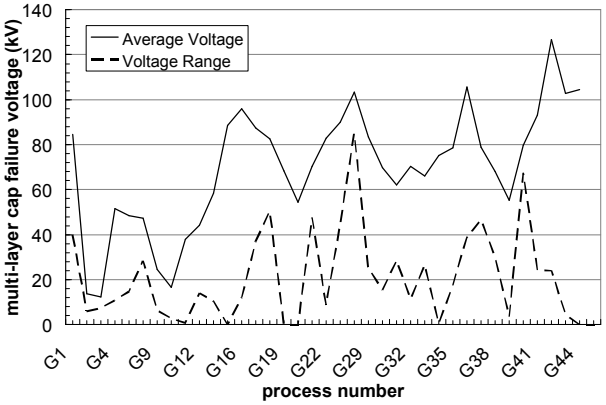

Figure 6. Multi-layer capacitor failure voltage performance for each subsequent process modification. Averaged data represents the mean failure voltage of three devices produced by each process modification while range data represents the difference between the maximum and minimum failure voltages of the three devices.

computer running LabVIEW controls the entire test, including the charge voltage, the spark gap pressure, the spark gap trigger, and dump relay. The computer records the test data, including the CVR waveform acquired by the oscilloscope.

Because the electrostatic energy storage occurs predominantly in the atomic polarization of the ceramic nanoparticles, the dielectric system should be capable of very high power discharge, although extensive tests in this aspect of the material have not yet been completed. Fig. 5 shows preliminary high power discharge data collected with this test bed. Here, a single layer of the composite dielectric material was discharged into a resistive load. A ~10ns risetime indicates that the material depolarizes fast enough for use in high power applications.

Fig. 6 quantifies the development progress of this investigation by showing the average and range of failure voltages of prototype composite dielectric multi-layer capacitors to date. The number of layers and capacitances of these devices are comparable; each new data point largely represents the results of composite dielectric and assembly/cure process refinements. Because the parameter space is large, setbacks and advances have typified the development process. However, an overall upward trend in failure voltage is clearly evident.

V. SUMMARY AND FUTURE WORK

Currently, the finished devices produced by this investigation consistently achieve 0.6J/cc energy density at maximum breakdown voltage, representing a factor of 5-6 improvement over other commercially available high power capacitor technologies. However, significant work remains to achieve 1J/cc energy density with high yields and useful device lifetimes. Future work will be directed towards mitigating the effect of dielectric material stresses introduced during the thermal cure process described above. In addition, investigation of high power discharge and lifetime performance of these devices will be completed. Subsequent scaling of device capacitances to values more useful for Marx bank applications (e.g., 80nF to 100nF) and application of this dielectric material to other compact pulsers (e.g., stacked Blumleins) may then proceed.

VI. REFERENCES

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