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Radiation Effects in MOS Oxides

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I. INTRODUCTION

From MOSFETs to bipolar ICs, oxides and insulators are a key component of many electronic devices. Ionizing radiation can induce significant charge buildup in these oxides and insulators leading to device degradation and failure. In space systems (and other harsh radiation environments, e.g., high-energy particle accelerators), exposure to high fluxes of electrons and protons can significantly reduce system lifetime due to total ionizing dose. Over the last thirty years, the effects of total ionizing dose on radiation-induced charge buildup in oxides have been investigated in detail. In addition to total ionizing dose effects, the energetic particles of space can also induce degradation by other mechanisms. For example, the heavy ions in space environments can reduce long-term reliability and lead to catastrophic device failure.

In this paper, we review the effects of radiation on oxide-induced device degradation and failure. The effects of total ionizing dose radiation-induced charge buildup in gate, field isolation, and silicon-on-insulator (SOI) buried oxides, and alternate high-K dielectrics are first reviewed. After that, the mechanisms and properties of heavy ion-induced single-event gate rupture (SEGR) will be discussed, followed by a brief discussion of the effects of heavy-ion exposure on long-term reliability.

II. TOTAL DOSE EFFECTS

A. Overview

High-energy electrons (secondary electrons generated by photon interactions or electrons present in the environment) and protons can ionize atoms, generating electron-hole pairs. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional electron-hole pairs. In this manner, a single, high-energy incident photon, electron, or proton can create thousands of electron-hole pairs.

When an MOS transistor is exposed to high-energy ionizing irradiation, electron-hole pairs are created in the oxide. Electron-hole pair generation in the oxide leads to almost all total dose effects. The generated carriers induce the buildup of charge, which can lead to device degradation. The mechanisms by which device degradation occurs are depicted in Figure 1. Figure 1 is a plot of an MOS band diagram for a p-substrate capacitor with a positive applied gate bias. Immediately after electron-hole pairs are created, most of the electrons will rapidly drift (within picoseconds) toward the gate and holes will drift toward the Si/SiO_2 interface. However, even before the electrons leave the oxide, some of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is called the electron-hole yield or charge yield. Those holes which escape "initial" recombination will transport through the oxide toward the Si/SiO_2 interface by hopping through localized states in the oxide. As the holes approach the interface, some fraction will be trapped, forming a positive oxide-trap charge. It is believed that hydrogen ions (protons) are likely released as holes "hop" through the oxide or as they are trapped near the Si/SiO_2 interface. The hydrogen ions can also drift to the Si/SiO_2

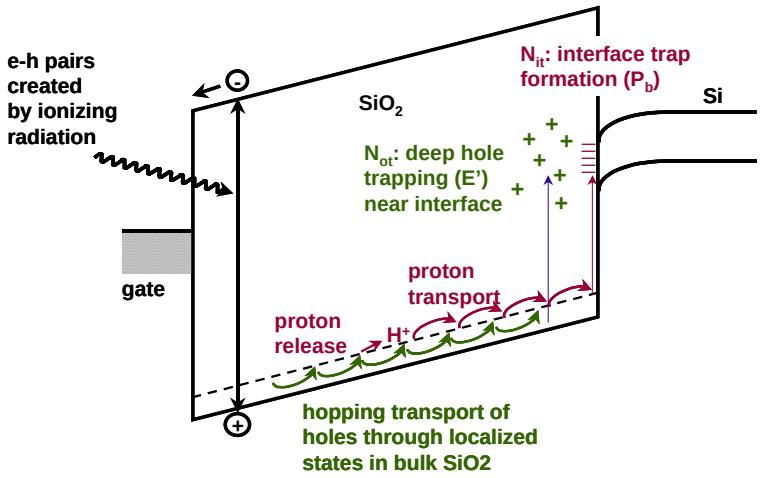

Figure 1: Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation.

where they may react to form interface traps. At threshold, interface traps are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors.

In addition to oxide-trapped charge and interface-trap charge buildup in gate oxides, charge buildup will also occur in other oxides including field oxides, silicon-on-insulator (SOI) buried oxides, and alternate dielectrics. The radiation-induced charge buildup in these insulators can cause device degradation and circuit failure. Positive charge trapping in the gate oxide can invert the channel interface causing leakage current to flow in the OFF state condition (V_{GS} = 0 V). This will result in an increase in the static power supply current of an IC and may also cause IC failure. In a similar fashion, positive charge buildup in field and SOI buried oxides can cause large increases in IC static power supply leakage current (caused by parasitic leakage paths in the transistor). In fact, for advanced ICs with very thin gate oxides, radiation-induced charge buildup in field oxides and SOI buried oxides normally dominates the radiation-induced degradation of ICs. Large concentrations of interface-trap charge can decrease the mobility of carriers and increase the threshold voltage of n-channel MOS transistors. These effects will tend to decrease the drive of transistors, degrading timing parameters of an IC. In the rest of this section, we present the details of oxide-trap and interface-trap charge buildup in MOS transistors.

B. Charge Yield

If an electric field exists across the oxide of an MOS transistor, once generated, electrons in the conduction band and holes in the valence band will immediately begin to transport in opposite directions. Electrons are extremely mobile in silicon dioxide and are normally swept out of silicon dioxide in picoseconds [1,2]. However, even before the electrons can leave the oxide, some fraction of the electrons will recombine with holes in the oxide valence band. This is referred to as initial recombination. The amount of initial recombination is highly dependent on the electric field in the oxide and the energy and type of incident particle [3]. In general, strongly ionizing particles form dense columns of charge where the recombination rate is relatively high. On the other hand, weakly ionizing particles generate relatively isolated charge pairs, and the recombination rate is lower [3]. The dependence of initial recombination on the electric field strength in the oxide for low-energy protons, alpha particles, gamma rays (Co-60), and x rays is illustrated in Figure 2 [4,5]. Plotted in Figure 2 is the fraction of unrecombined holes (charge yield) versus electric field in the oxide. The data for the Co-60 and 10-keV x-ray curves were taken from Ref. [5]. The other two curves were taken from Ref. [4]. For all particles, as the electric field strength increases, the probability that a hole will recombine with an electron decreases, and the fraction of unrecombined holes increases. Taking into account the effects of

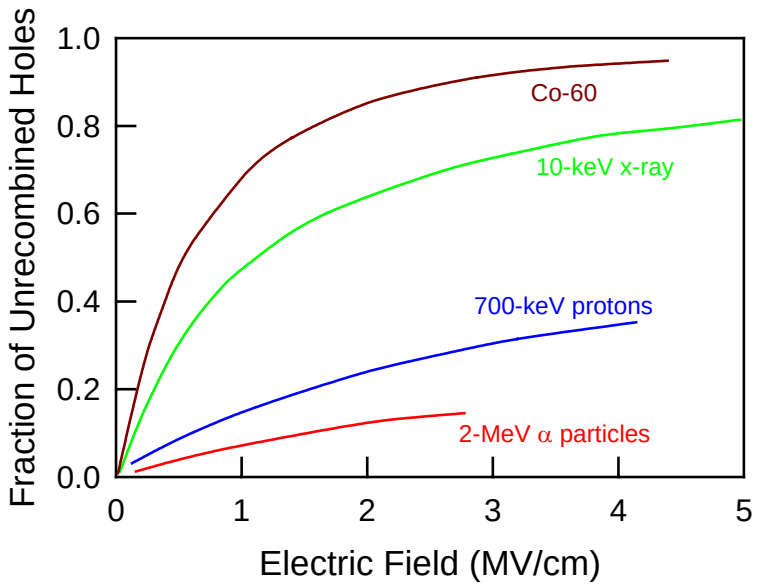

Figure 2: The fraction of holes that escape initial recombination (charge yield) for x rays, low-energy protons, gamma rays, and alpha particles. (After Refs. [4] and [5])

hole yield and electron-hole pair generation, the total number of holes generated in the oxide (not including dose enhancement effects [3,4]) that escape initial recombination, N_h, is given by [4]

$$N_h = f(E_{ox}) g_0 D t_{ox} ,$$

where $f(E_{ox})$ is the hole yield as a function of oxide electric field, D is the dose, and t_{ox} is the oxide thickness (in units of cm). g_0 is a material-dependent parameter giving the initial charge pair density per rad of dose (g_0 = 8.1×10^{12} pairs/cm^3 per rad for SiO_2).

C. Oxide Traps

Holes generated in the oxide transport much slower through the lattice than electrons [1]. In the presence of an electric field, holes can transport to either the gate/SiO_2 (negatively applied gate bias) or Si/SiO_2 interface (positively applied gate bias). Due to its charge, as a hole moves through the SiO_2 it causes a distortion of the local potential field of the SiO_2 lattice. This local distortion increases the trap depth at the localized site, which tends to confine the hole to its immediate vicinity. Thus, in effect, the hole tends to trap itself at the localized site. The combination of the charged carrier (hole) and its strain field is known as a polaron [6]. As a hole transports through the lattice, the distortion follows the hole. Hence, holes transport through SiO_2 by "polaron hopping" [4,7,8]. Polarons increase the effective mass of the holes and decrease their mobility. Polaron hopping makes hole transport dispersive (i.e., hole transport occurs over many decades in time after a radiation pulse) and very temperature and oxide thickness dependent [4,7,8].

With the application of a positive gate bias, holes transport to the Si/SiO_2 interface. Close to the interface there are a large number of oxygen vacancies due to the out-diffusion of oxygen in the oxide [9] and lattice mismatch at the surface. These oxygen vacancies can act as trapping centers. As holes approach the interface, some fraction of the holes will become trapped. The number of holes that are trapped is given by the capture cross-section near the interface, which is dependent on the applied field and is very device fabrication dependent, with only a few percent of the holes being trapped in hardened oxides to as much as 50 to 100% for soft oxides. The positive charge associated with trapped holes causes a negative threshold-voltage shift in both n- and p-channel MOS transistors.

The effect of the capture cross-section on trapped-hole buildup can be observed in the electric field dependence of the buildup of oxide traps shortly after irradiation. Figure 3 is a plot of the threshold-voltage shift due to oxide-trap charge, ΔV_{ot}, versus oxide electric field [10]. The circles are the measured data, the squares are the measured data adjusted for charge yield, and

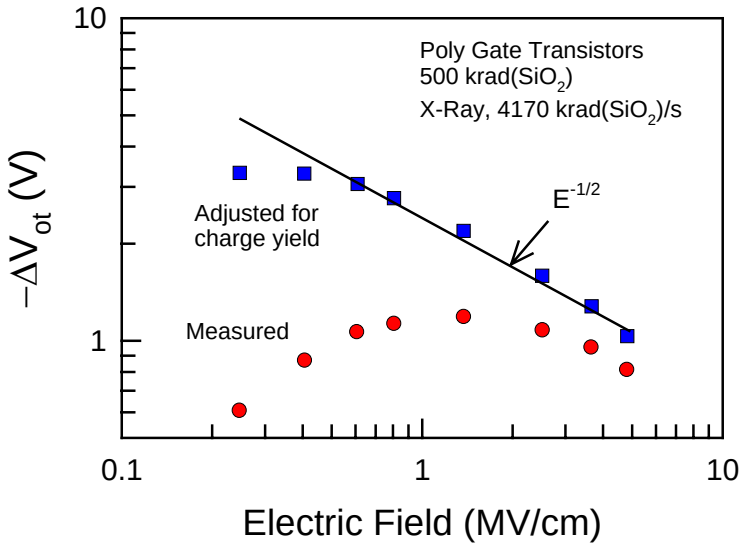

Figure 3: Electric field dependence of ΔV_{ot} versus electric field. Shown are the measured data (circles) and the measured data corrected for charge yield (squares). (After Ref. [10])

the solid line is a plot of $E^{-1/2}$. For electric fields greater than 0.5 V/cm, ΔV_{ot} adjusted for charge yield decreases with approximately an $E^{-1/2}$ electric field dependence. This is the same electric field dependence as is observed for the hole capture cross-section near the Si/SiO_2 interface [11-16]. This indicates that the field dependence of oxide-trap charge buildup is determined primarily by the hole capture cross-section.

Immediately after charge is trapped in oxides it begins to be neutralized. The time dependence of trapped-hole neutralization at room temperature is illustrated in Figure 4 [17], where the voltage shift due to oxide-trap charge, ΔV_{ot}, is plotted versus time for hardened n-channel polysilicon gate transistors irradiated to 100 krad(SiO_2) at dose rates from $6x10^9$ to 0.05 rad(SiO_2)/s and then annealed under bias at room temperature. The bias during irradiation and anneal was 6 V and the gate oxide thickness of the transistors was 60 nm. During anneal, the decrease in the magnitude of ΔV_{ot} follows a logarithmic time dependence. At each dose rate, ΔV_{ot} falls on the same straight line. Thus, the rate at which ΔV_{ot} is neutralized is dose-rate independent. The actual rate at which ΔV_{ot} is neutralized can depend on the details of the device fabrication process [18].

The neutralization of oxide-trapped charge occurs primarily by one of two mechanisms: 1) the tunneling of electrons from the silicon into oxide traps [18-23], and/or 2) the thermal emission of electrons from the oxide valence band into oxide traps [19,23-26]. The spatial and energy distributions of the oxide traps will strongly affect the rate at which charge neutralization occurs. For tunneling, the spatial distribution of the oxide traps must be close to the Si/SiO_2 interface. For thermal emission, the energy levels of the oxide traps must be close to the oxide valence band. Not only will the spatial and energy distributions of the oxide traps affect the rate of neutralization at room temperature and constant bias, but they will also affect its temperature and bias dependence.

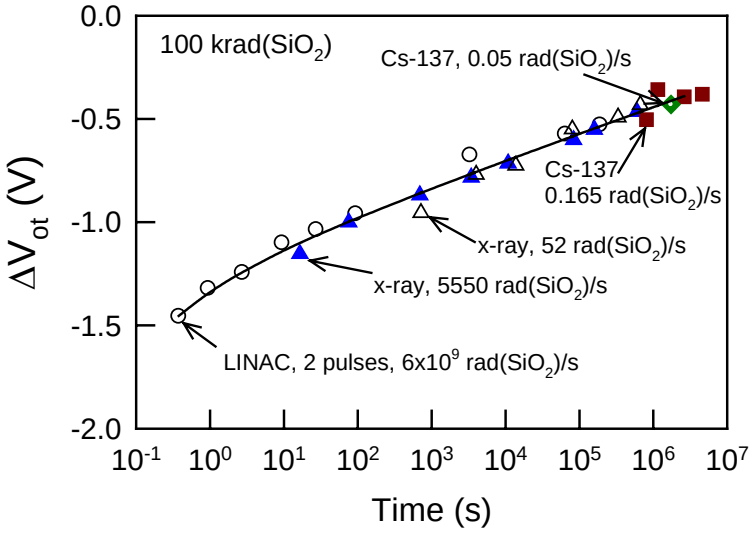

Figure 4: Oxide-trapped charge neutralization during anneal at room temperature for transistors irradiated at dose rates from $6x10^9$ to 0.05 rad(SiO_2)/s. (After Ref. [17])

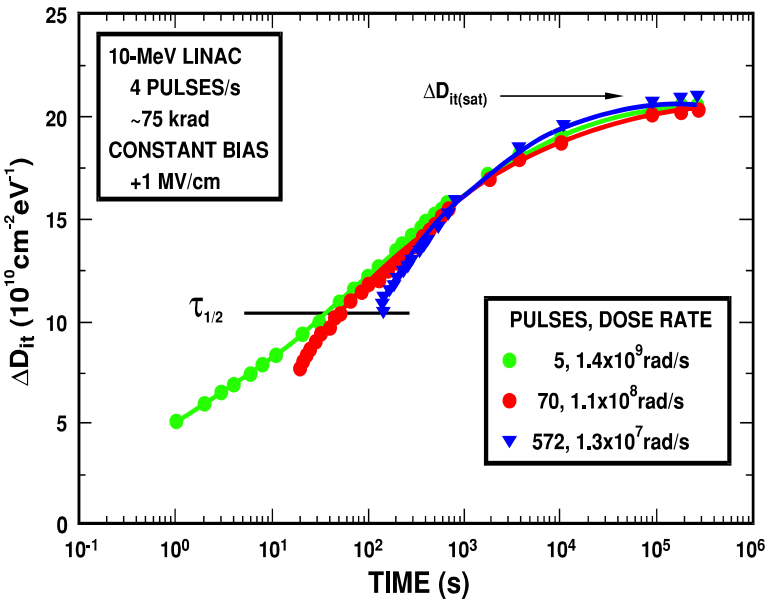

Figure 5: Interface-trap buildup as a function of time after irradiation. (After Ref. [33])

D. Interface Traps

In addition to oxide traps, radiation also leads to the formation of interface traps at the Si/SiO_2 interface [27]. Interface traps exist within the silicon band gap at the interface. Because of their location at the interface, the charge of an interface trap can be changed easily by applying an external bias.

Interface traps can be positive, neutral, or negative. Traps in the lower portion of the band gap are predominantly donors, i.e., if the Fermi level at the interface is below the trap energy level, the trap "donates" an electron to the silicon. In this case, the trap is positively charged. P-channel transistors at threshold are affected primarily by interface traps in the lower region of the band gap. Therefore, for a p-channel transistor, interface traps are predominantly positive, causing negative threshold-voltage shifts. Conversely, traps in the upper portion of the band gap are predominantly acceptors, i.e., if the Fermi level is above the trap energy level, the trap "accepts" an electron from the silicon. In this case, the trap is negatively charged. Interface traps predominantly in the upper region of the band gap affect an n-channel transistor at threshold. Therefore, for an n-channel transistor, interface traps are predominantly negative, causing positive threshold-voltage shifts. At midgap, interface-trap charge is approximately neutral [28-31]. Because oxide-trap charge is positive for both p- and n-channel transistors, oxide-trap charge and interface-trap charge compensate each other for n-channel transistors and add together for p-channel transistors.

Interface-trap buildup occurs on time frames much slower than oxide-trap charge buildup. Interface-trap buildup can take thousands of seconds to saturate after a pulse of ionizing radiation [32,33]. Figure 5 [33] is a plot of the increase in density of interface-traps, ΔD_{it}, versus time after high-dose-rate pulses of ionizing radiation. The density of interface traps is the average number of traps in a given interval of the band gap, and has the units of traps/cm^2-eV. The data for this plot were taken on polysilicon gate transistors irradiated to 75 krad(Si) in 5, 70, and 572 pulses at a 4-Hz repetition rate using an electron linear accelerator (LINAC). The gate oxide thickness was 47 nm and the electric field across the oxide during irradiation and anneal was 1 MV/cm. For these measurements, interface-trap buildup had begun by the time of the first measurement (1 s for the data taken with 5 pulses). However, interface-trap buildup does not begin to saturate until ~10^5 s. This curve is typical of that for interface-trap buildup. For the curve taken with 5 pulses, the time for 50% buildup ($\tau_{1/2}$) is approximately 35 s.

For polysilicon-gate transistors, the electric field dependence of interface-trap buildup is very similar to the electric field dependence of oxide-trap charge buildup [10,34]. When measured data are adjusted for charge yield, the adjusted data follow an $E^{-0.6}$ field dependence,

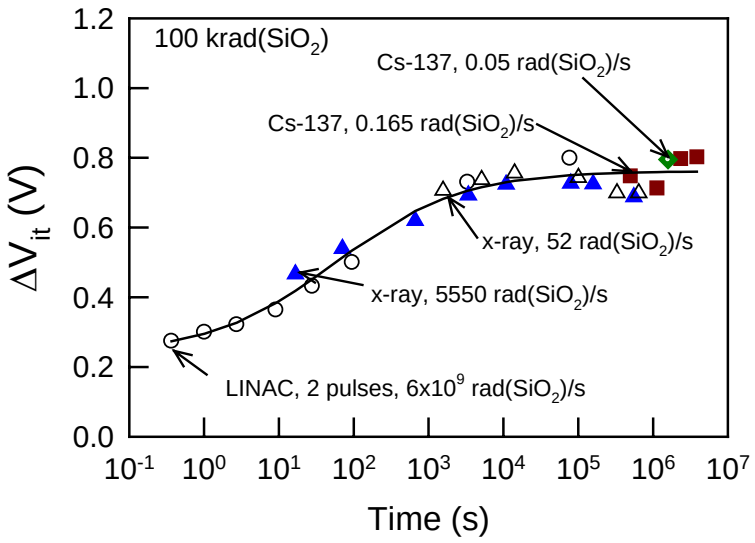

Figure 6: Interface-trap buildup for transistors irradiated at dose rates from $6x10^9$ to 0.05 rad(SiO_2)/s and annealed under bias (+6 V) at room temperature. (After Ref. [17])

within experimental uncertainty equal to the electric field dependence of oxide-trap charge and the hole capture cross-section near the interface. This is an indication that both oxide-trap charge and interface-trap charge buildup are linked to hole trapping near the Si/SiO_2 interface. Little or insignificant buildup of interface traps occurs if a negative bias is maintained during irradiation and anneal, consistent with the lack of hole trapping near the interface under these conditions.

There does not appear to be a "true" dose-rate dependence for the buildup of interface traps in MOS devices [17]. Figure 6 [17] is a plot of ΔV_{it} versus time for transistors irradiated to a total dose of 100 krad(SiO_2) at dose rates from $6x10^9$ to 0.05 rad(SiO_2)/s. After irradiation each transistor was annealed under bias. The bias during irradiation and anneal was 6 V. Note that as long as the total irradiation plus anneal time is the same, the same threshold-voltage shift due to interface traps is measured, regardless of the dose rate of the radiation source. If there were a "true" dose-rate dependence, the data taken at different dose rates would not fall on the same response curve.

Unlike oxide-trap charge, interface traps do not readily anneal at room temperature. Some interface-trap annealing at 100°C has been reported by several workers [35-38]. However, higher temperatures are normally required to observe significant interface-trap annealing [39,40]. These properties make interface-trap charge effects very important for low dose-rate applications, e.g., space. For n and p-channel MOS transistors, interface-traps affect device performance primarily through an increase in threshold voltage and a decrease in channel mobility. Both of these degradation mechanisms tend to reduce the drive current of "ON" transistors, leading to increases in timing parameters of an IC.

E. Device Properties

For a gate oxide transistor, parasitic field oxide transistor, or back-channel transistor of an SOI device (discussed below), the total threshold-voltage shift is the sum of the threshold-voltage shifts due to oxide-trap and interface-trap charge, i.e.,

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} . \qquad \textbf{(2)}$$

ΔV_{ot} and ΔV_{it} can be determined from

$$\Delta V_{ot,it} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} \rho_{ot,it}(x) x dx \,, \quad \textbf{(3)}$$

where $\rho_{ot,it}(x)$ is the charge distribution of radiation-induced oxide-trapped or interface-trap charge. Note the change in sign between the charge distribution and the threshold-voltage shift. For positive charge, the threshold-voltage shift is negative; conversely, for a negative charge, the threshold-voltage shift is positive. Thus, for devices where oxide-trap charge dominates, the threshold-voltage shift will be predominantly negative.

At high dose rates and short times, little neutralization of oxide-trap charge will occur and ΔV_{ot} can be large and negative. Conversely, interface-trap charge will have had insufficient time to build up and ΔV_{it} is normally small. Thus, at high dose rates and short times for either n- or p-channel transistors, the threshold-voltage shift can be large and negative. For an n-channel transistor (gate or parasitic field oxide transistor), large negative threshold-voltage shifts can significantly increase the drain-to-source leakage current, which in turn causes significant increases in IC static supply leakage current, I_{DD}, leading to potential IC failure.

At moderate dose rates, some neutralization of oxide-trap charge will take place and some buildup of interface traps will also occur. Thus, for this case, both ΔV_{ot} and ΔV_{it} can be large. For an n-channel transistor, ΔV_{ot} and ΔV_{it} tend to compensate each other. Therefore, at moderate dose rates, even though the individual components (ΔV_{ot} and ΔV_{it}) of the threshold-voltage shift can be large, the net threshold-voltage shift for an n-channel transistor can be small and the radiation-induced failure level of an IC may be relatively high.

For the long times associated with low-dose-rate irradiations, a large fraction of the oxide-trap charge in transistors may be neutralized during irradiation. Thus, ΔV_{ot} is often small. In contrast, the long times associated with low-dose-rate irradiations allow interface-trap buildup to saturate. This results in a positive increase in threshold voltage in n-channel transistors and a decrease in carrier mobility. The buildup of interface traps in gate oxides is primarily important for older technologies and other device types (e.g., power MOSFETs) with relatively thick oxides. For present-day gate oxides, the gate oxide thickness is normally very thin. As will be shown below, radiation-induced charge buildup rapidly decreases with decreasing oxide thickness. As a result, interface-trap buildup (and oxide-trapped charge buildup) in gate oxides is often not a concern and total dose effects are dominated by oxide-trapped charge buildup in field oxides.

For p-channel transistors, both ΔV_{ot} and ΔV_{it} are negative and they add together. At high dose rates, ΔV_{ot} can be large. At low dose rates, ΔV_{ot} can still be large because standard bias conditions for a p-channel transistor do not lead to significant oxide-trap charge neutralization via tunneling. In addition, ΔV_{it} can also be large, especially for thick oxides (e.g., parasitic field oxides). Therefore, for both high and low dose rates, the threshold-voltage shift for p-channel transistors can be large and negative. The net result is that for parasitic p-channel field oxide transistors, the threshold becomes larger, decreasing the effect of radiation-induced charge buildup in parasitic field oxides (over p-type regions) on radiation-induced degradation.

III. OXIDE HARDENING

In this section, we examine process conditions that affect oxide hardness. Although we will focus on process conditions that affect gate oxide hardness, the process conditions discussed

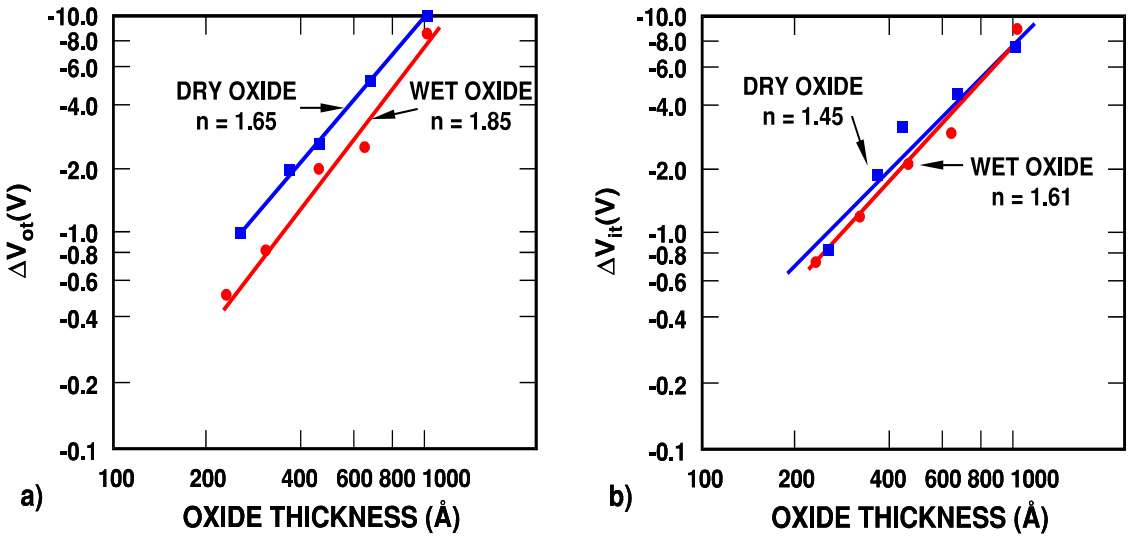

Figure 7: The dependence of the threshold-voltage shift due to a) oxide-trap and b) interface-trap charge on oxide thickness.

have similar effects on radiation-induced charge buildup in field isolation insulators and silicon-on-insulator buried oxides. A key process condition that has a very large effect on gate-oxide hardness is oxide thickness. Fortunately, as the thickness of the gate oxide decreases, radiation hardness improves. Figure 7 is a plot of the threshold-voltage shifts due to interface-trap and oxide-trapped charge for dry and steam grown (wet) oxides. The threshold-voltage shifts due to both types of charge decrease with slightly less than a t_{ox}^2 thickness dependence ($t_{ox}^{1.5}$ to $t_{ox}^{1.8}$). For very thin oxides (<20 nm), there is evidence that the amount of radiation-induced oxide-trap charge decreases with an even faster dependence on oxide thickness [41]. Because of the improvement in hardness with decreasing thickness, gate oxides in advanced commercial technologies can be extremely radiation hard.

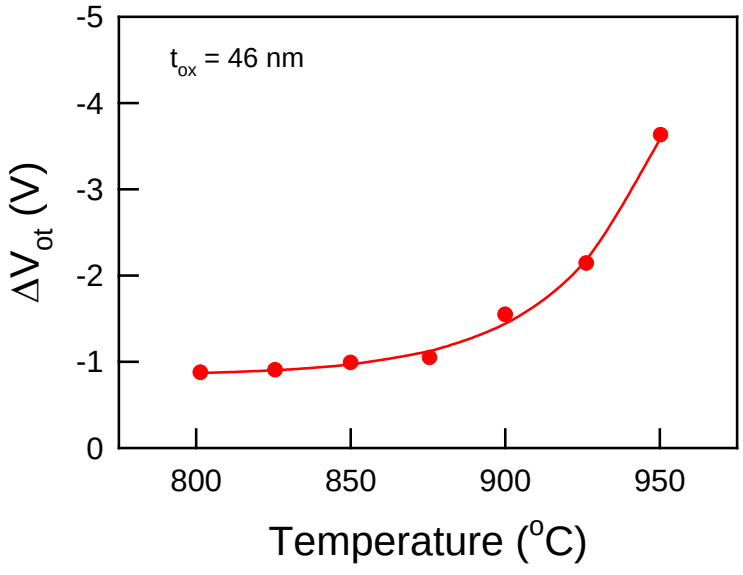

Figure 8: The effect of anneal temperature on radiation-induced oxide-trapped charge. (After Ref. [42])

In addition to oxide thickness, other process conditions can affect hardness. For example, high-temperature anneals can significantly degrade device hardness due to the creation of oxygen vacancies in the oxide. Figure 8 is a plot of ΔV_{ot} for capacitors annealed in nitrogen at temperatures from 800 to 950°C and irradiated to 1 Mrad(SiO_2) [42]. Anneal temperatures above 875° result in significant increases in ΔV_{ot}. The trend in advanced commercial IC technologies is to minimize the time and temperature of anneals and oxidations to minimize the amount of dopant

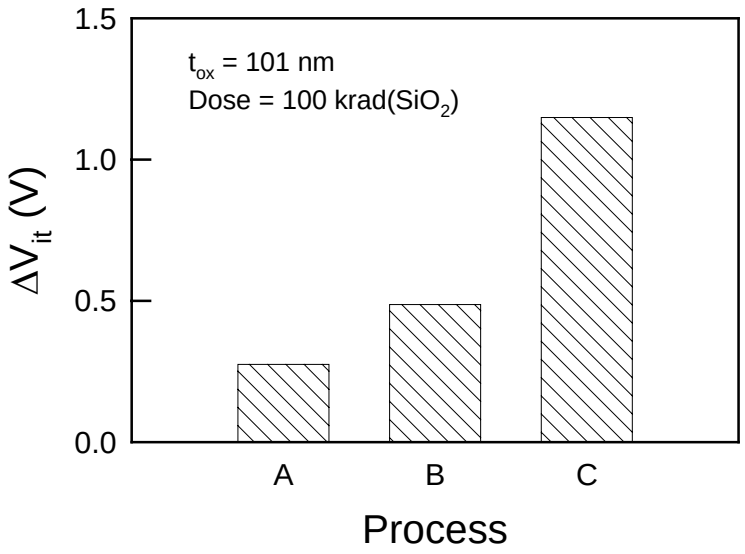

Figure 9: Effect of hydrogen on radiation-induced interface-trap buildup. Capacitor A was exposed to the least amount of hydrogen during processing and Capacitor C was exposed to the most amount of hydrogen. (After Ref. [43])

redistribution. Thus, minimizing anneal temperatures to improve radiation hardness is consistent with the present trend for manufacturing commercial ICs. Nitrogen anneals over the same temperature range have a much smaller effect on ΔV_{it}. However, annealing in ambients containing hydrogen after depositing the gate material (e.g., polysilicon or metal) can significantly increase the amount of radiation-induced interface-trap charge. Figure 9 is a plot of ΔV_{it} for capacitors annealed in varying amounts of hydrogen after deposition of the polysilicon gate and irradiated to 100 krad(SiO_2) [43]. Capacitor A was exposed to the least amount of hydrogen and capacitor C was exposed to the greatest amount of hydrogen. Increasing the amount of hydrogen used in processing resulted in increasing concentrations of interface-trap charge. Thus, to optimize hardness, process temperatures after gate oxidation should be kept at or below 850°C (except perhaps for a few brief rapid thermal anneals) and ambients containing hydrogen should be minimized.

IV. ALTERNATE DIELECTRICS

Silicon dioxide has been the primary gate insulator since MOS ICs were first developed. To achieve the drive currents required by advances in IC technology, the thicknesses of SiO_2 gates are becoming extremely thin. They are reaching a point where electron tunneling can cause prohibitively large increases in power consumption. To circumvent this problem, alternate gate dielectrics with high dielectric constants (also referred to as "high-K" dielectrics) are being explored. By using a high-dielectric-constant gate material, a much thicker dielectric can be used to obtain the equivalent capacitance of much thinner SiO_2 gates. For these thicker high dielectric constant insulators, electron tunneling is reduced and oxide-trap charge may be more significant.

At the present time, there is relatively little information on the radiation hardness of the dielectrics under consideration for replacing SiO_2. Because the dielectric gates will be physically thicker and deposited or grown using different techniques, it is possible that these dielectrics could trap significantly more charge than thinner thermally-grown SiO_2 gates. As a result, the radiation-induced charge trapping in the gate insulator may once again affect IC radiation hardness. The radiation hardness of hafnium oxide, HfO_2, has been explored [44-48]. Hafnium oxide has a relatively high dielectric constant (~25) compared to SiO_2 (3.9), is less reactive with polysilicon than many of the other dielectrics being pursued, and has shown encouraging results

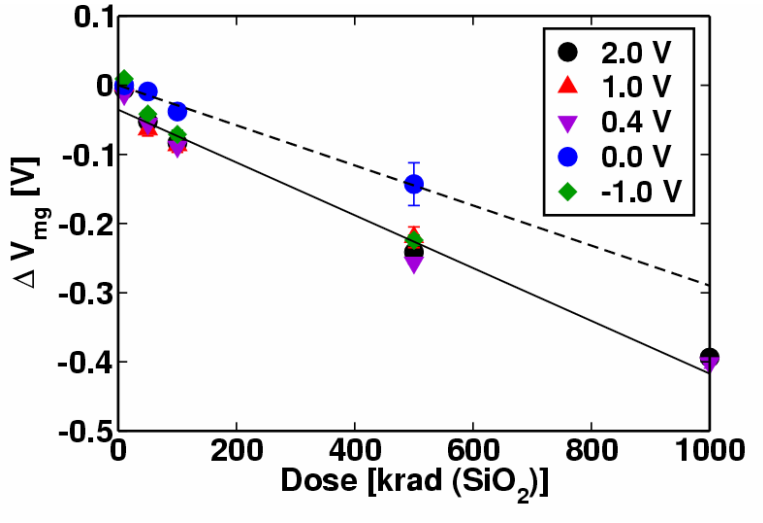

Figure 10: Midgap voltage shift versus total dose for hafnium silicate capacitors irradiated with 10-keV x-rays with applied biases from -1 to 2 V. The equivalent oxide thickness (EOT) is 4.5 nm and the physical thickness is 29 nm. (After Ref. [44])

in measurements of reliability such as stress-induced leakage current, time-dependent dielectric breakdown, and mean time to failure [49-52].

Figure 10 is a plot of the midgap voltage shift for hafnium silicate capacitors irradiated with 10-keV x rays with an applied bias (-1 to 2 V) during irradiation [44]. The physical oxide thickness of the hafnium silicate gates is 29 nm. This corresponds to an equivalent oxide thickness (EOT) of 4.5 nm. Assuming interface-trap charge is neutral at midgap (which needs to be confirmed for hafnium oxides), the midgap voltage shift is equal to the oxide-trap charge voltage shift. The midgap voltage shift is relatively large. After irradiating to 1 Mrad(SiO_2), the voltage shift is ~-0.4 V for capacitors irradiated with either a positive or negative bias and is approximately -0.3 V for capacitors irradiated with a 0 V bias. These shifts correspond to approximately a 28% hole trapping efficiency [44] (similar to some non-hardened SiO_2 thermal oxides). For a more practical hafnium oxide thickness (<2 nm EOT), as will be required by advanced technologies, the voltage shift may be considerably less, assuming that the radiation hardness of hafnium oxide dielectrics improves in a manner similar to that for silicon dioxide dielectrics.

Although the radiation hardness of thin EOT HfO_2 gate oxides appears to relatively good, recent results have shown that the combined effects of irradiation and bias temperature stress can lead to enhanced degradation [48]. The amount of enhanced degradation was found to depend on the irradiation and anneal bias conditions. Worst-case bias was for pMOS transistors irradiated in their "OFF" states, and annealed in their "ON" states.

Another alternative dielectric that has been explored in much more detail is reoxidized nitrided oxides (RNO) [53-58]. Nitrided oxides have a lower pin-hole density than SiO_2, can be grown at high temperatures permitting better uniformity and less compressive stress and fixed charge, and can retard the diffusion of dopants through the insulator which can affect the channel resistivity [54]. These properties make nitrided and RNO dielectrics attractive for ultra-thin gate-oxide commercial and hardened devices [54]. Indeed, most advanced commercial CMOS technologies in production today employ nitrided oxides. RNO oxides have been shown to be superior to thermal oxides in radiation hardness [59,60] and hot-carrier degradation [61].

The primary difference between thermal and RNO dielectrics in ionizing radiation environments is the nearly total lack of interface-trap buildup for RNO dielectrics [62]. RNO dielectrics can be fabricated in which there is no measurable interface-trap buildup for transistors irradiated to total doses in excess of 50 Mrad(Si) [62]. For those cases where some interface-trap buildup was observed, the number of interface traps does not increase in time after irradiation [59]. This likely occurs because hydrogen released in the bulk of the dielectric or near the

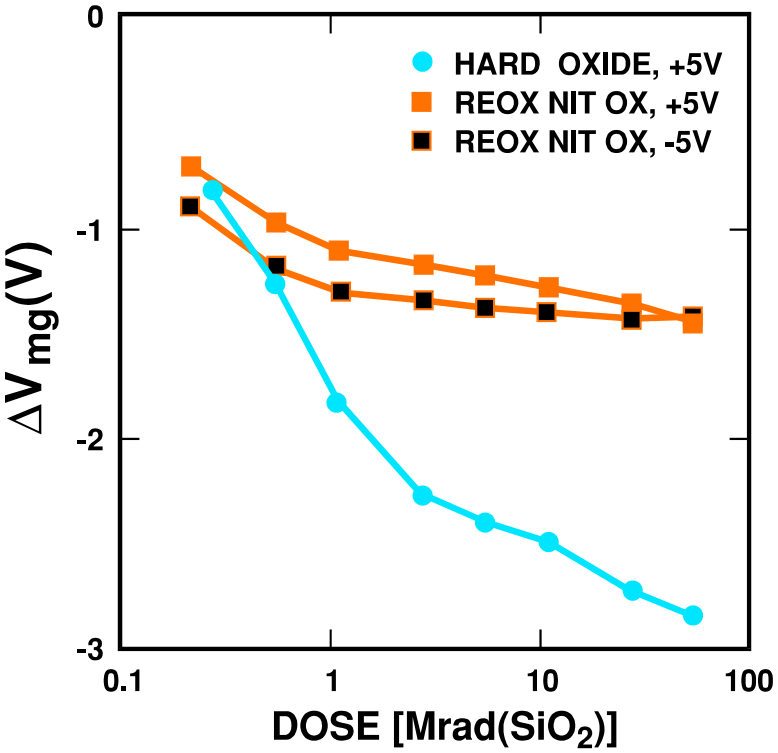

Figure 11: The change in midgap voltage measured on 37-nm RNO and thermal oxide transistors versus dose. The midgap voltage shift corresponds to the threshold-voltage shift due to oxide-trapped charge. (After Ref. [62])

interface (which is responsible for interface-trap buildup in thermal oxides), cannot penetrate the nitrogen rich oxynitride layer near the interface and create an interface trap [59].

RNO dielectrics can be fabricated so that the amount of oxide-trap charge buildup for a RNO oxide is lower to or comparable to that for a thermal oxide. Figure 11 [62] is a plot of the threshold-voltage shift at midgap for p-channel transistors fabricated with a hardened oxide and with a RNO oxide versus dose. The oxide and RNO dielectric thicknesses were 37 nm and the preirradiation fixed charge levels were ~$3x10^{10}$ and 10^{11} cm^{-2}, respectively. At midgap, interface-trap charge is neutral, thus the threshold-voltage shift at midgap corresponds to the threshold-voltage shift due to oxide-trap charge. The bias during irradiation for the hardened thermal oxide was +5 V and the bias for the RNO oxides was either +5 or -5 V. After irradiating to 10 Mrad(SiO_2), the amount of oxide-trap charge buildup in the hardened thermal oxides is more than twice that for the RNO oxides. Note that for the RNO oxide transistors, the shifts are nearly equal for biases of +5 and -5 V.

V. Parasitic Field Oxide Transistor Leakage

Even though the radiation hardness of commercial gate oxides may improve as the IC industry tends towards ultra-thin oxides, field oxides of advanced commercial technologies will still be relatively thick and may still be very soft to ionizing radiation. A relatively small dose in a field oxide (~10 krad(Si) for some commercial devices) can induce sufficient charge trapping to cause field-oxide induced IC failure. Because of this, radiation-induced charge buildup in field oxides is the main cause of IC failure in advanced commercial technologies.

Field oxides are much thicker than gate oxides. Typical field-oxide thicknesses are in the range of 100 nm to 1000 nm. Unlike gate oxides, which are routinely grown by thermal oxidation, field oxides are produced using a wide variety of deposition techniques. Thus, the trapping properties of a field oxide may be poorly controlled and can be considerably different than for a gate oxide.

Even for thermally grown thick oxides, the buildup of charge in gate and field oxides can be qualitatively different [63,64]. For example, in thick SiO_2 capacitors (>100 nm), interface-trap

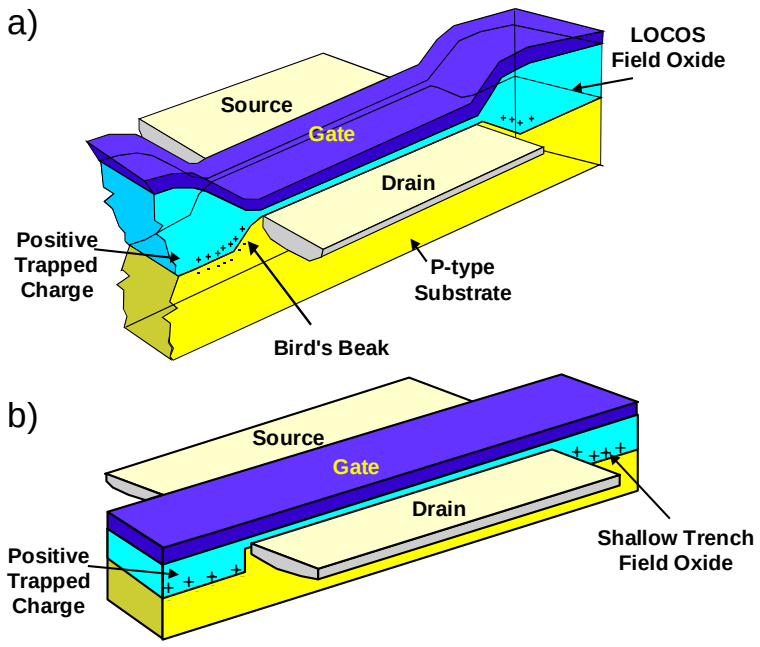

Figure 12: Cross section of a) a LOCOS isolated and b) shallow-trench isolated transistor. (After Ref. [65])

buildup has been observed within 4 ms following a pulse of ionizing radiation [63]. The buildup was found to be independent of oxide field and polarity and occurred with approximately the same efficiency at room temperature and 77 K. This suggests that some "prompt" interface traps could have been created directly by radiation. This is in contrast to thinner gate oxides, where little or no prompt interface traps are normally observed. On similar devices, a significant amount of hole trapping was observed in the bulk of the oxide [64].

Two common types of field oxide isolation used today are local oxidation of silicon (LOCOS) and shallow-trench isolation (STI). LOCOS isolation has been used for many years. Within the last ten years, most commercial IC suppliers have replaced LOCOS isolation with STI for advanced submicron technologies. Figure 12a [65] shows the cross-section of an n-channel transistor with LOCOS isolation, illustrating positive charge buildup in the bird's beak regions. Similar charge buildup will occur for STI, as illustrated in Figure 12b [65]. As positive radiation-induced charge builds up in the field oxide overlying a p-type surface, it can invert the surface, forming an n-type region underneath the field oxide. As the surface inverts, conducting paths can be generated that will greatly increase the leakage current. Figure 13 depicts two possible leakage paths for STI [65]. One leakage path occurs at the edge of the gate-oxide transistor between the source and drain. Another leakage path could occur between the n-type source and drain regions of a transistor and the n-well of adjacent p-channel transistors. These two leakage paths will cause an increase in static power supply current of an IC with radiation. Because radiation-induced charge

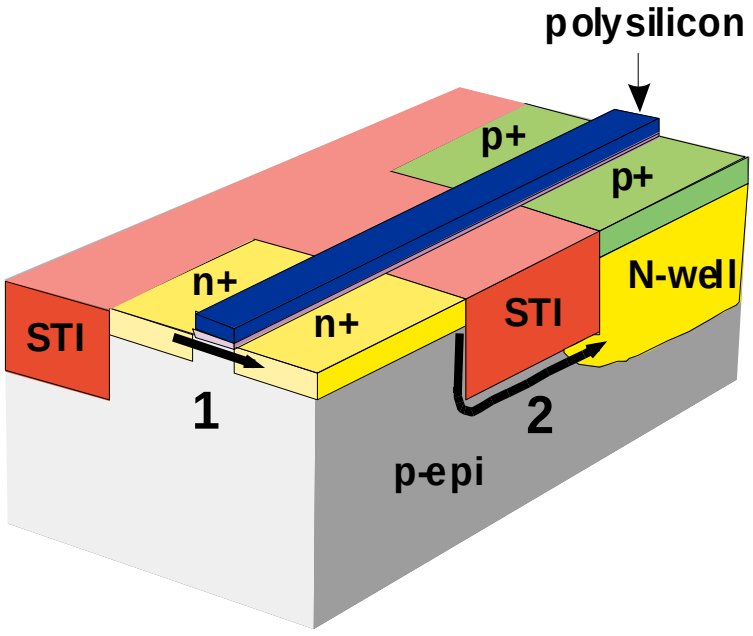

Figure 13: As indicated by the arrows, two possible leakage paths in a shallow-trench isolation technology. (After Ref. [65])

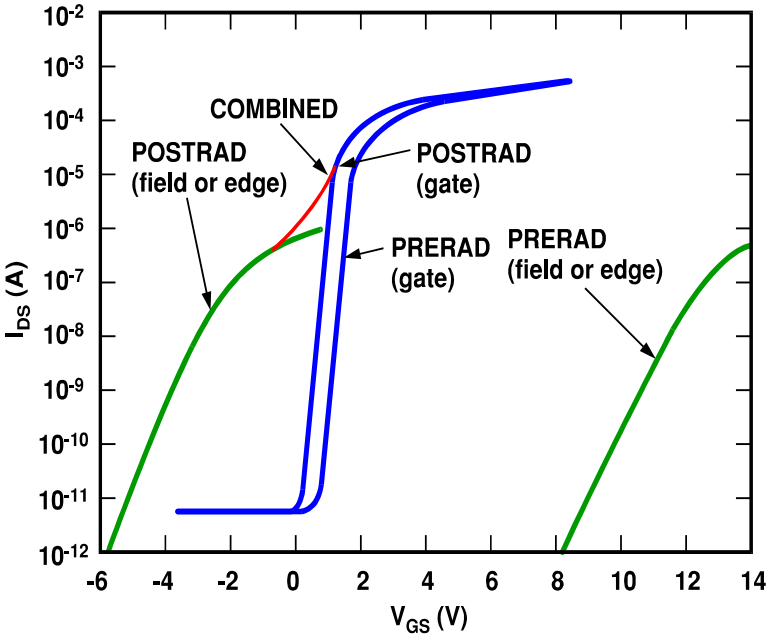

Figure 14: I-V curves for a gate-oxide transistor and a parasitic field-oxide transistor showing the increase in leakage current of the gate-oxide transistor caused by the parasitic field-oxide transistor.

buildup in field oxides is predominantly positive, its effect is usually most important for n-channel transistors.

The field oxide forms a parasitic field-oxide transistor in parallel with the gate-oxide transistor. For example, at the edges of the gate transistor the gate polysilicon extends over the field oxide region, as shown in Figure 12. The parasitic field-oxide transistor consists of the gate polysilicon, a portion of the field oxide, and the source and drain of the gate transistor. The effect of the excess leakage current from a parasitic field oxide transistor on the gate oxide transistor is illustrated in Figure 14. Plotted in Figure 14 are the drain-to-source leakage current versus gate-to source voltage curves for an n-channel gate-oxide transistor with (combined curve) and without field-oxide leakage and for a parasitic field-oxide transistor. Because of the large thickness of the field oxide, the preirradiation threshold voltage of the parasitic field oxide transistor is relatively large, but as positive radiation-induced charge builds up in the field oxide, it can cause a very large negative threshold-voltage shift of the parasitic field-oxide transistor. If the threshold-voltage shift of the parasitic field oxide transistor is large enough (as depicted in Figure 14), it will cause an "OFF" state leakage current (I_{DS} @ V_{GS} = 0 V) to flow, which can significantly add to the drain-to-source current of the gate oxide transistor. Thus, the field-oxide leakage prevents the gate oxide transistor from being completely turned off. This will greatly add to the static supply leakage current of an IC.

The amount of field-oxide leakage depends greatly on IC process and topography. For example, for STI the topography of the shallow trench and process conditions inherently lead to variations in the trench sidewall insulator thickness between the silicon trench and overlying conductors (e.g., polysilicon). This is especially pronounced at the top corner of the trench. At the top corner, the shallow insulator thickness can result in very high fields across the insulator. These high fields in trench corner regions have been shown to reduce gate oxide integrity [66], to cause anomalous humps in the subthreshold I-V characteristics of non-irradiated commercial ICs [66-71], and to severely limit the irradiation hardness [65]. As the magnitude of the electric field across the trench corner increases, the magnitude of the threshold-voltage shift of the parasitic field-oxide transistor increases [65].

The worst-case bias condition for radiation-induced charge buildup in field oxides is the bias condition that maximizes the electric field across the field oxide. This is clearly shown in Figure 15, which is a plot of the total threshold-voltage shift (plotted as ΔV_{FB}) and the threshold-voltage shift due to oxide and interface-trap charge versus applied electric field for transistors

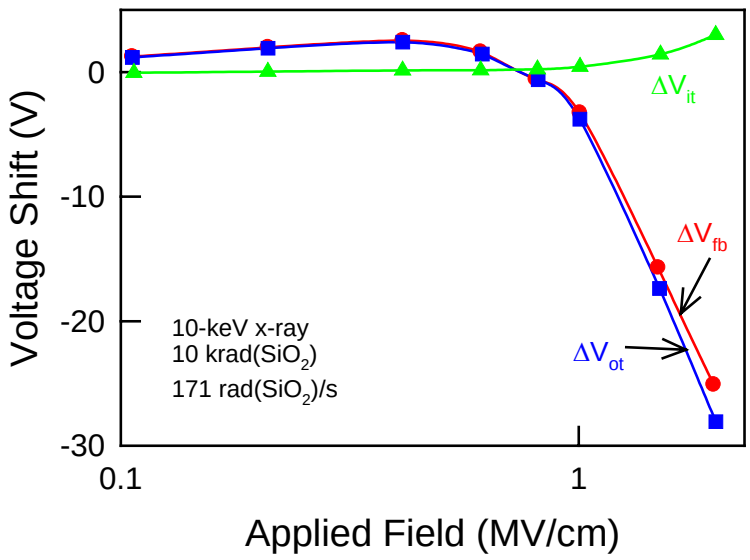

Figure 15: Flatband voltage shift and the threshold-voltage shift due to oxide and interface-trap charge versus applied field during x-ray irradiation for an n-channel transistor fabricated using a traditional field oxide insulator as the gate dielectric. (After Ref. [65])

fabricated using a field oxide as the gate dielectric [65]. The gate dielectric was deposited using a traditional shallow-trench isolation process. The transistors were irradiated with 10-keV x rays to a total dose of 10 krad(SiO_2). For these bias and irradiation conditions, there is no significant buildup of interface-trap charge in the field oxide. However, at the higher electric fields, there is a very large radiation-induced buildup of oxide-trapped charge, which causes a very large threshold-voltage shift of the field oxide transistor. After irradiating to a total dose of 10 krad(SiO_2), the threshold-voltage shift was greater than 25 V for electric fields greater than 2 MV/cm. Depending on the initial threshold voltage of the field oxide transistor, this radiation-induced threshold-voltage shift may be large enough to cause large increases in transistor leakage current. These data demonstrate that one must reduce the electric field in the field oxide to avoid large increases in radiation-induced field oxide leakage current. Even though traditional process techniques were used to deposit the gate dielectric, the topology of the gate dielectric for these transistors is considerably different than for standard STI. Very high electric fields can occur at the corners of STI, leading to very large radiation-induced threshold-voltage shifts of parasitic STI transistors . In a typical layout of STI, a polysilicon line connected to the gate of a transistor can extend over the STI. Thus, the bias condition that will result in the maximum electric field across the STI is the bias condition that gives the maximum voltage drop between the gate and the substrate. This bias condition is normally the "ON" bias condition, where the gate is at the bias supply voltage, V_{DD}, and the source, drain, and substrate are grounded. Although these results were demonstrated for STI, similar results have been obtained for ICs with LOCOS isolation.

VI. SOI TECHNOLOGIES

A. General

Silicon-on-insulator (SOI) technology has been actively pursued for use in radiation-hardened systems for more than twenty years. More recently, it is quickly becoming a mainstream technology for commercial applications. The cross sections of SOI (top) and bulk-silicon (bottom) n-and p-channel transistors are shown in Figure 16. The main feature that has made SOI technology attractive for radiation-hardened and commercial applications is that SOI transistors are built on top of an oxide instead of a silicon substrate. As will be discussed below, this property gives SOI technology advantages over equivalent bulk-silicon (or epitaxial) circuits. In a standard thin-film SOI transistor, the source and drain extend completely through

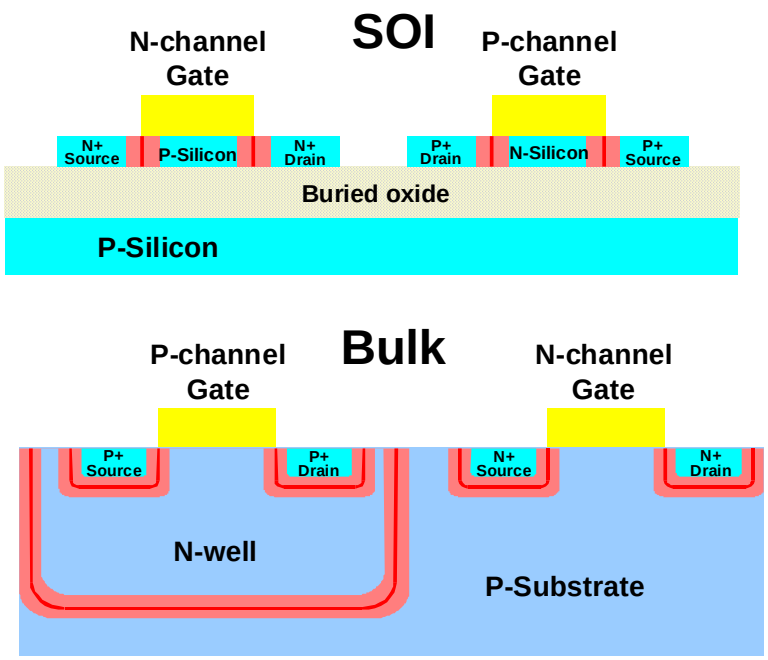

Figure 16: Cross sections of SOI (top) and bulk-silicon (bottom) n- and p-channel transistors.

the top-silicon layer, which is typically less than 200 nm thick. Except for the fact that SOI transistors are built on an oxide, SOI process technology is very similar to that for bulk-silicon technologies. Each SOI transistor inherently includes two transistors: a standard top-gate transistor consisting of the source, drain, and gate oxide, and a back-gate parasitic transistor consisting of the source and drain of the top-gate transistor and the buried oxide. For the back-gate transistor, the substrate acts as the gate contact. Two generic types of SOI transistors (top gate) are partially-depleted and fully-depleted transistors. In a partially-depleted transistor, the depletion region in the body region (the region underneath the gate) formed by the top-gate transistor does not extend completely through the top-silicon layer. Because there is a non-depleted silicon region between the top-gate depletion region and the silicon/buried oxide interface, the top-gate transistor characteristics of a partially-depleted transistor (i.e., threshold voltage) are not directly affected by charge buildup in the buried oxide. In a fully-depleted transistor, the depletion region formed by the top-gate transistor extends completely through the top-silicon layer. For a fully-depleted transistor, the top gate transistor is electrically coupled to the back-gate transistor and radiation-induced charge buildup in the buried oxide will directly affect the top-gate transistor characteristics. Whether a transistor is a partially or fully-depleted transistor depends primarily on the thickness of the silicon layer and the doping concentration of the body region. A fully-depleted transistor must have a very thin silicon layer and/or be lightly doped.

B. Total-Dose Effects

The total-dose hardness of an SOI transistor depends on the radiation hardness of three oxides: 1) gate, 2) field oxide or sidewall isolation, and 3) buried oxide. The mechanisms for the radiation-induced degradation of the gate oxide of a MOS/SOI transistor are identical to the mechanisms for the gate oxide of a MOS transistor fabricated on a bulk silicon substrate as discussed above. Most present-day SOI circuits use shallow-trench isolation for transistor isolation. The radiation hardness of STI was discussed above.

The biggest difference between the total-dose response of SOI and bulk-silicon technologies is radiation-induced charge buildup in the buried oxide of SOI transistors. As SOI buried oxides are exposed to ionizing radiation, radiation-induced charge will become trapped in the buried oxide. This radiation-induced trapped charge is predominantly positively charged. As illustrated in Figure 17a, this charge buildup in the buried oxide can invert the back-channel interface, forming a leakage path between the source and drain of the top-gate transistor. For

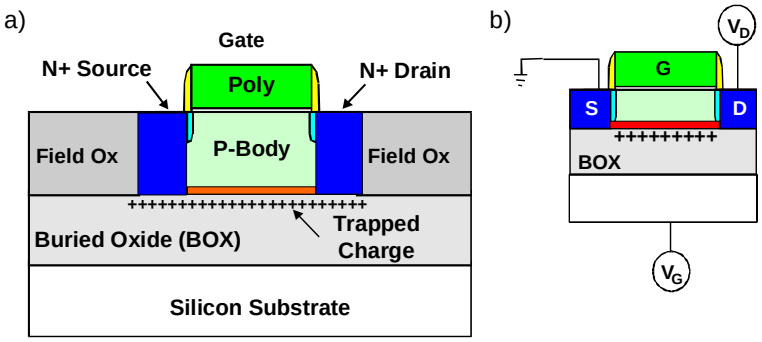

Figure 17: Cross section of an SOI transistor illustrating a) charge buildup in the buried oxide inverting the back-channel and b) bias conditions for measuring the back-channel threshold voltage.

simplicity, the charge buildup as illustrated in Figure 17a is shown to be located close to the buried oxide/back-channel interface. However, in general, charge will be trapped throughout the buried oxide. Inversion of the back-channel interface can lead to large increases in the leakage current of a partially-depleted transistor. Because the top-gate transistor is electrically coupled to the back-gate transistor in a fully-depleted transistor, radiation-induced charge buildup in the buried oxide of a fully-depleted transistor will cause a decrease in the threshold voltage of the top-gate transistor. In the remainder of this section, we examine the effects of radiation-induced charge buildup in the buried oxide on transistor radiation hardness.

A simple method for quantifying the amount of radiation-induced charge buildup in the buried oxide is to measure the threshold voltage of the back-gate transistor. The bias configuration for measuring the back-gate I-V characteristics is shown in Figure 17b. The bias configuration and measurement conditions are identical to those for measuring the top-gate I-V characteristics, except that the gate bias is applied to the substrate. Typical I-V curves for the back-gate transistor are shown in Figure 18a. The transistors were irradiated with Co-60 gamma rays in the OFF (V_{GS} = V_S = 0 V; V_{DS} = 5 V) bias condition. As noted in the figure, positive charge buildup in the buried oxide can cause large negative shifts in the back-gate transistor I-V curves. As the radiation-induced charge buildup becomes sufficiently large to cause an increase in the leakage current at zero back-gate bias, the top-gate leakage current will begin to increase as illustrated in Figure 18b. This leakage current resulting from radiation-induced charge buildup in the buried oxide will prevent the top-gate transistor from being completely turned off. If it is large enough, it can cause parametric and potentially functional failure.

The radiation response of buried oxides has been found to be highly dependent on the fabrication process [72,73]. Two common methods for fabricating SOI substrates are separation by implanted oxygen (SIMOX) and by wafer bonding. SIMOX substrates are formed by implanting a silicon substrate with oxygen ions to very high fluence levels and then annealing the substrate at very high temperatures (e.g., 1350°C) to form the buried oxide. Bonded SOI substrates are formed by growing an oxide on the surface of one wafer and then bonding the wafer to a second substrate. There are numerous methods for producing the thin top silicon layer of the SOI substrate. Common to all bonded wafer

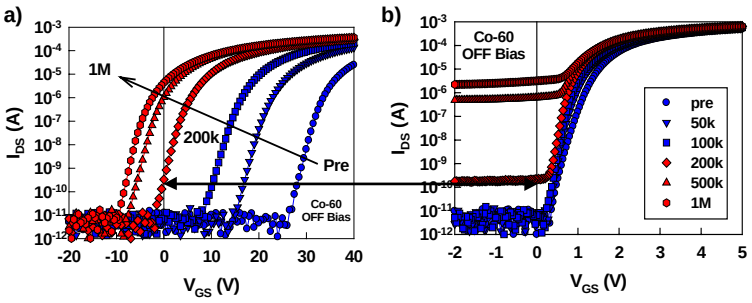

Figure 18: I-V characteristics for a) a back-gate transistor irradiated to 1 Mrad(SiO2) and its effect on b) the top-gate transistor leakage current. The transistors were irradiated in the OFF (VGS = VS = 0 V; VDS = 5 V) bias condition.

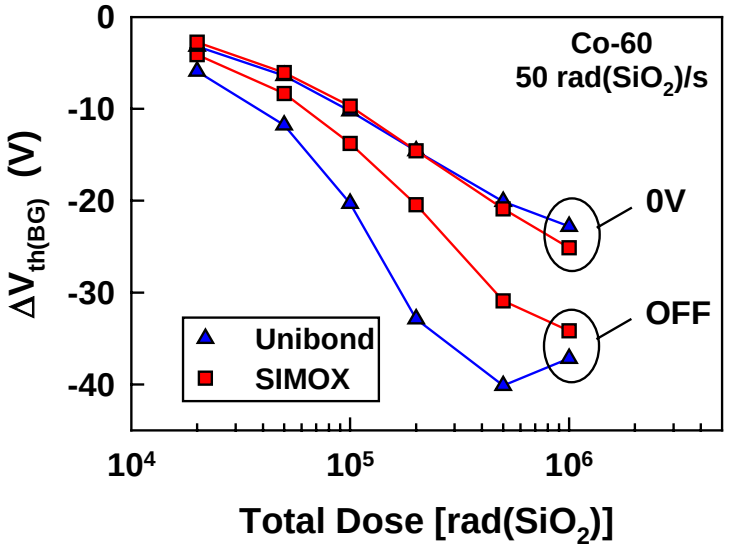

Figure 19: Back-gate transistor threshold-voltage shift for SOI transistors fabricated using Unibond and SIMOX buried oxides. (After Ref. [78])

processes is a high temperature bond strengthening anneal (e.g., 1100°C). The high temperature anneals used to fabricate SOI substrates (both SIMOX and bonded) cause oxygen to out-diffuse from the buried oxide, leaving behind numerous oxide defects. These defects can lead to radiation-induced trapped charge. It is natural to expect that the high-fluence implants used to fabricate SIMOX substrates (and some bonded oxide substrates) may cause numerous implant-related defects throughout the buried oxide. Previous works [73-77] have shown that up to 100% of the radiation-generated holes are trapped in the bulk of the oxide at deep trap sites close to their point of origin. An example of the threshold-voltage shifts for two SIMOX and bonded wafers is shown in Figure 19 [78]. Data are shown for the back-gate threshold-voltage shift for transistors fabricated using SIMOX and Unibond (made by SOITEC) substrates, irradiated using Co-60 gamma rays in the 0 V ($V_{GS} = V_S = V_{DS} = 0$ V) and OFF ($V_{GS} = V_S = 0$ V; $V_{DS} = 5$ V) bias conditions. The Unibond substrates show larger back-gate transistor threshold-voltage shifts for the OFF bias condition than the SIMOX substrates. Once trapped, some of the holes are slowly neutralized by electrons by thermal detrapping at room temperature [73-77]. In addition to hole trapping, electrons are also trapped throughout the bulk of the buried oxide [73]. Most of the trapped electrons are thermally detrapped within <1 s after a pulse of radiation. After the electrons are detrapped, the resultant charge is due to a high concentration of trapped holes causing large negative threshold-voltage shifts of the buried oxide.

Liu et al. [79], was the first to examine in detail the electric field conditions in a partially-depleted SOI buried oxide that lead to worst-case bias conditions. Similar to field oxides, the buildup of radiation-induced charge in SOI buried oxides is dominated by positive oxide-trapped charge. Therefore, the electric field condition that results in the maximum back-gate threshold-voltage shift in an SOI transistor is the bias condition that causes the most radiation-induced hole trapping near the back Si/SiO_2 interface. This will be the bias condition that results in the maximum electric field strength in the buried oxide underneath the channel region. Liu et al. [79], and subsequently Ferlet-Cavrois et al. [80], have simulated the electric field distributions in the buried oxide for numerous radiation bias conditions. Both showed that for typical gate lengths and buried oxide thicknesses the bias condition that produces the largest electric fields underneath the channel and the most hole trapping is the transmission gate (pass gate) bias configuration for partially-depleted transistors. The transmission gate (TG) bias configuration is defined as source and drain biased at V_{DD} and gate and body contact (if available) grounded. Simulations and data [80] have also shown that the OFF bias condition (drain at V_{DD} and all other contacts grounded) can result in very large back-gate threshold-voltage shifts. The bias

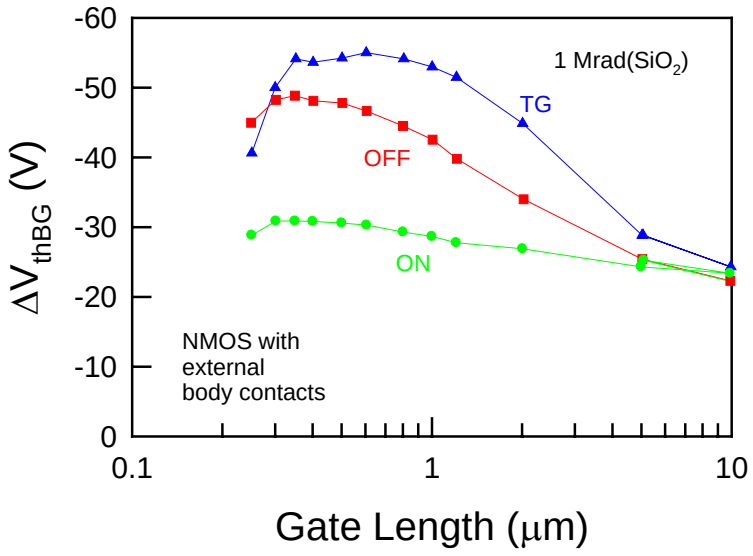

Figure 20: Back-gate threshold-voltage shift versus gate length for an n-channel SOI transistor irradiated with x rays to a total dose of 1 Mrad(SiO2). Transistors were biased in the ON, OFF, and TG bias configurations. (After Ref. [80])

configuration that results in the largest back-gate threshold-voltage shifts depends on the ratio of the transistor gate length to the buried oxide thickness [80]. These simulations have been experimentally verified [78-80]. Figure 20 is a plot of the measured back-gate threshold-voltage shifts versus gate length for n-channel transistors irradiated with 10-keV x rays to a total dose of 1 Mrad(SiO_2) [80]. The buried oxide thickness was 413 nm. The technology used for fabricating the transistors was a 0.25-μm technology. The largest back-gate threshold-voltage shifts observed were in transistors irradiated in the TG bias configuration. However, for transistors with gate lengths near the standard technology gate length of 0.25 μm, the back-gate threshold-voltage shifts were approximately the same for transistors irradiated in the TG and OFF bias configurations. The smallest back-gate threshold-voltage shifts were for transistors irradiated in the ON bias configuration. These results for the worst-case bias configuration for partially-depleted SOI transistors are just the opposite of that for the worst-case bias configuration for radiation-induced charge buildup in field oxides.

For fully-depleted SOI transistors, the worst-case bias is not as well defined as for partially-depleted SOI transistors. Similar to the case for partially-depleted SOI transistors, Jenkins and Liu [81] showed that for some fully-depleted SOI technologies, the worst-case bias for radiation-induced charge trapping in the buried oxide was the transmission gate bias configuration. However, for other technologies, the worst-case bias was determined to be the ON bias configuration [82]. The mechanism causing these differences is unknown. However, for the technologies of Ref. 82, the radiation-induced increase in leakage current caused by charge trapping may be partly due to inversion of the back-channel interface and partly due to a "total-dose latch" effect [83-85]. The total-dose latch effect is caused by charge trapping in the buried oxide modulating the body potential. As the body potential is lowered relative to the source, electrons can be injected into the body region and be collected at the drain. If the electric field near the drain is high enough to cause impact ionization, this could lead to a current run away condition causing snapback (in SOI technology, snapback is often called single transistor latch).

C. Hardening

Several techniques have been proposed to mitigate the effects of radiation-induced charge trapping in the buried oxide on transistor performance. These techniques can be grouped into two general categories: techniques that reduce the amount of net positive radiation-induced trapped charge and techniques that reduce the effects of radiation-induced trapped charge on transistor

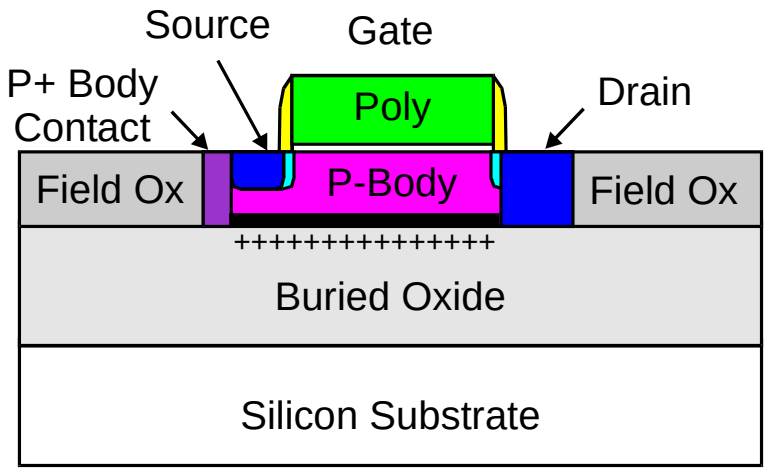

Figure 21: Cross section of a BUSFET transistor illustrating the shallow source. For a BUSFET transistor, inversion of the back-channel interface by charge trapping in the buried oxide does not form a conducting path between source and drain. (After Ref. [88])

performance. One technique that has been proposed to reduce the amount of net radiation-induced positive trapped charge is to implant the buried oxide with silicon [86,87]. The silicon implant creates electron traps throughout the buried oxide. When filled, these electron traps will compensate the trapped positive charge, decreasing the net positive charge in the oxide.

A transistor structure that reduces the effect of radiation-induced charge trapped in the buried oxide on transistor performance is the body-under-source field effect transistor (BUSFET) [88]. The BUSFET is similar to a standard SOI transistor, except that the source penetrates only partially through the top silicon layer. (If the drain also penetrates only partially through the top-silicon layer, there could be a large decrease in dose rate and single-event upset hardness due to additional junction area.) The cross section of a BUSFET is shown in Figure 21. Inherent to the BUSFET is a body tie that connects the body region to a p+ body contact at all positions along the width of the channel. This makes the BUSFET body tie more effective than conventional body ties. As radiation-induced charge is trapped in the buried oxide, the charge will invert the back-channel interface. However, because the source penetrates only partially through the buried oxide, the inverted layer cannot form a conducting path between the source and drain and no increase in top-gate transistor leakage current occurs. As long as the depletion region formed by the electron layer does not come into contact with the source depletion region, there will be no conducting path between source and drain.

VII. HEAVY-ION EFFECTS

A. Single-Event Gate Rupture (SEGR)

A single-event gate rupture can occur as a single heavy ion passes through a gate oxide. SEGR occurs at high oxide electric fields, such as those during a write or clear operation in a nonvolatile SRAM or E^2PROM [89-91]. SEGR was first observed [90,91] for metal nitride oxide semiconductor (MNOS) dielectrics used for memory applications. Since then, SEGR has been observed in power MOSFETs, MOS transistors [92], and more recently in high-density DRAMs [93] and field-programmable gate arrays [94].

SEGR is caused by the combination of the applied electric field and the energy deposited by the ion [92,95]. As an ion passes through a gate oxide it forms a highly conducting plasma path (conducting pipe) between the silicon substrate and the gate contact [89,91,92]. With an electric field across the oxide, charge will flow along the plasma path depositing energy in the oxide. The average resistance of the conducting pipe depends on the mobility of carriers and their density in the pipe. There are two sources of charge carriers in the conducting pipe: charge

injected from the anode due to the electric applied across the oxide and charge generated in the oxide by the passage of a heavy ion [95]. If the energy deposited is high enough, it can cause localized heating of the dielectric and potentially a thermal runaway condition. If thermal runaway occurs, the local temperatures along the plasma will be high enough to cause thermal diffusion of the gate material, cause the dielectric to melt, and evaporate overlying conductive materials [89,92]. The resistance of the initial ion track is inversely proportional to the ion LET. If the LET is increased, resistance is lowered and the required voltage across the device to sustain conduction is reduced [92].

For thermal SiO_2 oxides with the incident ion normal to the surface, Wheatley et al. [96] showed that the critical electric field, E_{cr}, for SEGR is given by

$$E_{CR} = \frac{E_0}{1 + L/B}, \tag{4}$$

where E_0 is the breakdown field of the oxide in the absence of ion exposure in MV/cm, L is the ion LET in MeV-cm^2/mg, and B is a fitting parameter. Sexton et al. [95] has derived an expression for B,

$$B = \frac{\mu_1 n(V)}{\mu_2 K}, \tag{5}$$

where μ_1 and μ_2 are the mobilities of carriers generated by high field injection and by the heavy ion, respectively, $n(V)$ is the electron density from high field injection, and K is a proportionality constant determined assuming that the density of carriers is proportional to LET. For oxides with thicknesses from 6 to 18 nm, Sexton et al. [97] found that B varies from 48 to 72. As illustrated in Figure 22, Eq. 4 does fit experimental data. This figure is a plot of $1/E_{CR}$ versus LET for data taken from several different works [92,96-98]. All of the data were taken on capacitors. In this figure, $1/E_0$ is the y-axis intercept of the line and the slope of the line is equal to $1/(E_0B)$. The data show a pattern of increasing breakdown field with decreasing oxide thickness, even at high LET [97], suggesting for a given LET that advanced technologies should become less susceptible to SEGR as gate oxide thickness decreases. Sexton et al [97] have shown that E_0 determined from the y-axis intercept is close to the experimentally measured pre-irradiation breakdown field (at least for the oxides explored in [97]). This is an indication that the improvement in SEGR for decreasing oxide thickness is fundamentally a function of the

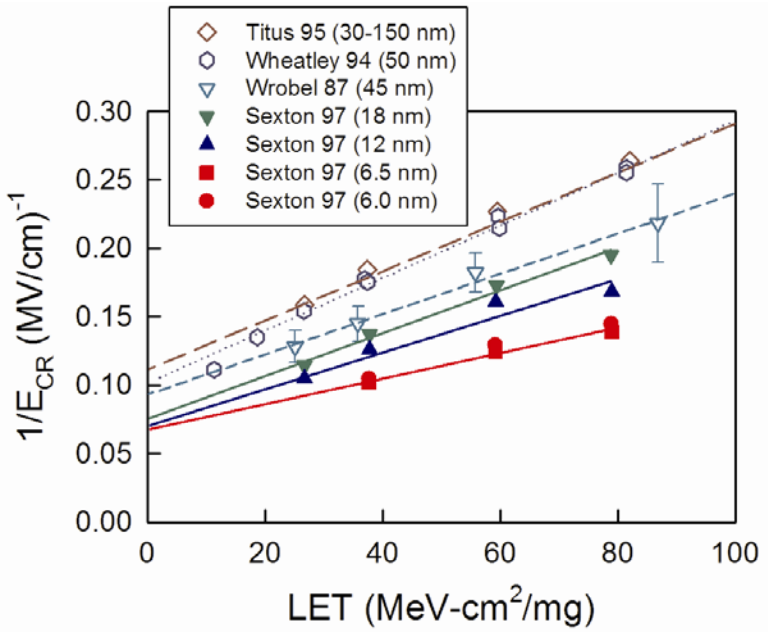

Figure 22: 1/ECR versus LET for capacitors with thicknesses from 6 to 150 nm. Data compiled from Refs. 92,96-98.

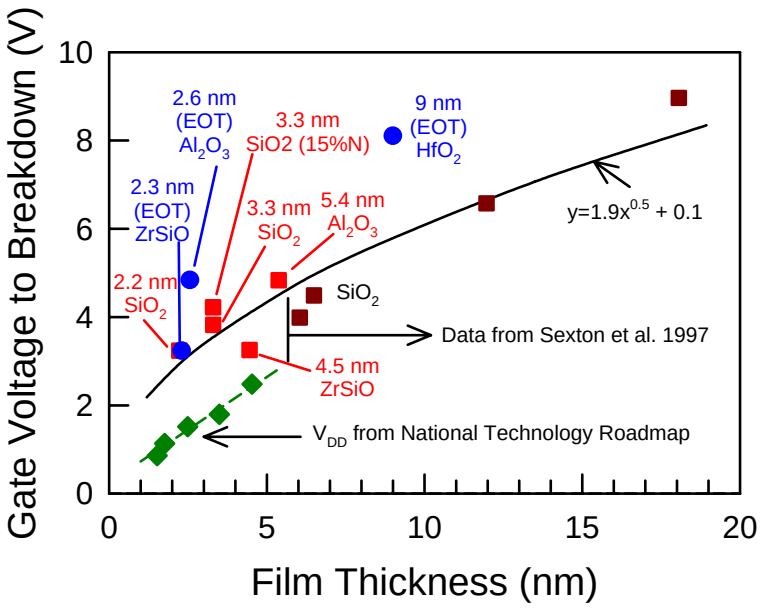

Figure 23: Trends for voltage to radiation-induced hard breakdown (RHB) with physical dielectric film thickness for exposure to 342-Au ions. (After Ref. [100])

quality of the oxides prior to exposure to heavy ions.

For thin oxides and insulators, there are two types of breakdown; radiation-induced soft breakdown (RSB) and radiation-induced hard breakdown (RHB) [95,100]. RHB is discussed above. As insulators are exposed to heavy ions, some insulators exhibit a gradual increase in leakage current. This type of breakdown is referred to as soft breakdown [95,99-103]. Although in soft breakdown the oxide is clearly damaged, the oxide (insulator) has not ruptured. It can be the dominant stress-related breakdown mode in emerging oxides [100,101]. While the probability for heavy-ion induced hard breakdown can be very low in ultra thin gate oxides, soft breakdown (increase in gate leakage current) can occur at relatively low gate voltages and ion fluences [95,100,101]. RSB is a cumulative effect, but is normally observed for the most energetic ions [100]. Whether or not soft breakdown affects device performance will depend on circuit application [101]. For some circuits, even small increases in leakage cannot be tolerated, while for other circuits very large increases in leakage current can be tolerated. RSB and RHB have been found to be relatively unrelated events [95], i.e., exposure to high ion fluence can greatly increase gate leakage current (RSB), but does not increase the probability for RHB.

Electrically-induced soft breakdown has been postulated to be due to a conducting pipe that is stable, but does not have sufficient thermal energy to expand [100]. Alam et al. [104] have explained soft breakdown as a conduction path across the dielectric, which dissipates power (V^2/R_{path}) below the threshold for irreversible thermal damage, with a crossover to hard failure given by a specific power (not energy) level. A similar power-related threshold has been observed for single-ion-induced hard breakdown [100].

To determine whether or not advanced IC technologies will indeed be sensitive to RHB, several works have investigated the susceptibility of ultrathin oxides and high-K dielecrics to heavy ion strikes [95,97,99,100]. In one of these works, Massengill et al. [100] exposed SiO_2 capacitors with oxide thicknesses down to 2.2 nm and high-K dielectric capacitors with equivalent oxide thicknesses (EOT) down to 2.3 nm to 342-MeV Au ions. The results of this work are summarized in Figure 23. Plotted is the gate voltage to breakdown, V_{BD}, versus film thickness (EOT for high-K dielectrics). Also included in the figure are the gate oxide breakdown results of Sexton et al. [97] for thin SiO_2 capacitors. V_{BD} does decrease with film thickness. However, as film thickness decreases, the normal operating voltage for that film thickness will decrease correspondingly. Also shown in Figure 23 are the expected operating voltages (out to 2009) for future IC technologies according to the 1999 National Technology Roadmap for

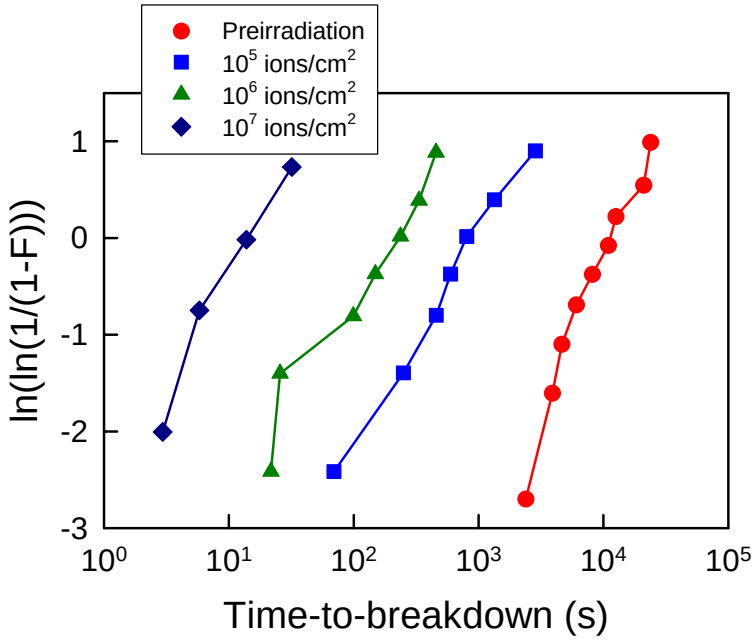

Figure 24: Weibull lifetime distributions of test capacitors following heavy-ion irradiation (After Ref. [105])

Semiconductors. Although this roadmap has been updated, the general bias trends are still true. Comparing the experimentally breakdown results to the operating bias voltages expected as film thickness decreases, it is clear the ion-induced SEGR breakdown voltage remains well above the expected normal operating voltage as film thickness is decreased.

It has been shown on test structures that ions can have a significant impact on gate oxide response. For a non-volatile memory transistor, the probability of a SEGR will depend on the time that the device is in a write, clear, or other high-electric field mode of operation. For a number of nonvolatile memory applications, this may be only a small percentage of the total operation time. Clearly the probability of a SEGR is highly dependent on the system application.

B. Latent Effects

Although there does not appear to be any correlation between RHB and RSB, heavy-ion exposure can lead to electrically-induced latent breakdown. Figure 24 is a plot of the Weibull lifetime distribution subjected to constant-voltage time dependent dielectric breakdown (TDDB) tests preirradiation and after irradiating to fluences of 10^5, 10^6, and 10^7 ions/cm^2. The capacitors had an oxide thickness of 3 nm and an area of 10^{-4} cm^2, and were irradiated with 823-MeV Xe-129 ions. The TDDB tests were performed with a -4.9 V bias. The intrinsic TDDB life dramatically decreases as the ion fluence is increased. For the smallest fluence (10^5 ions/cm^2), the intrinsic lifetime decreased by over an order of magnitude. For these capacitors, a fluence of 10^5 ions/cm^2 corresponds to approximately 10 ion hits. It has been suggested that the reduction in lifetime is caused as heavy ions produce damage tracks that weaken areas in the oxide film where defect generation is enhanced during constant voltage stress [105].

C. Enhanced Degradation in Power MOSFETs

Recent heavy-ion irradiations of n-channel power MOSFETs have shown enhanced degradation [106]. Figure 25 shows I-V characteristics for power MOSFETs irradiated with a) Co-60 gamma rays and b) 333-MeV Au ions. The device in Figure 25a was irradiated to 20 krad(SiO_2) at a dose rate of 103 rad(SiO_2)/s. During irradiation these devices were biased with 15 V applied to the gate and all other terminals grounded. Similarly, the device in Figure 25b was irradiated at BNL's heavy ion test facility to a fluence of 10^7 ions/cm^2 at a flux of 2.3×10^5 ions/cm^2/s. The dose deposited during this shot was 13 krad(SiO_2). Comparing these data, it is observed that the device in Figure 25a has a small, and nearly parallel shift in the I-V

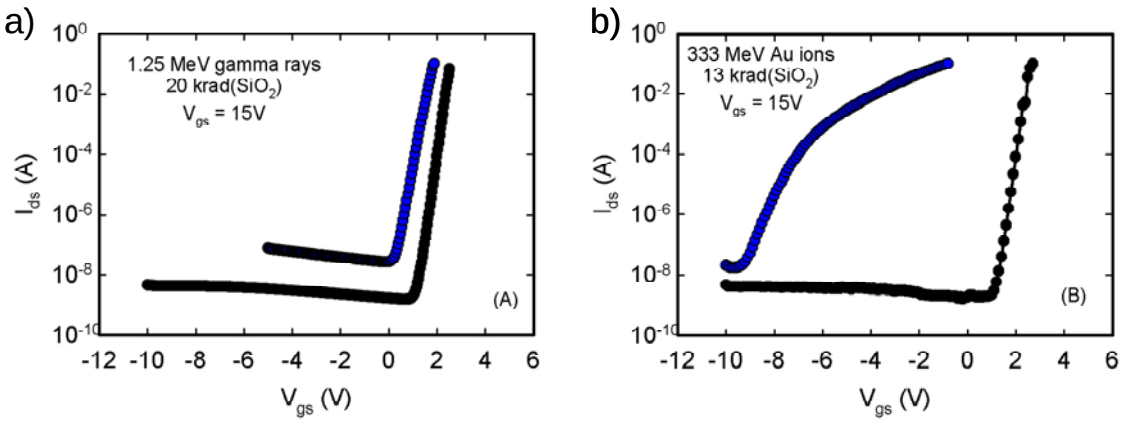

Figure 25: Pre and post irradiation IV curves for IRF3704ZCS power MOSFETs irradiated with a) Co-60 gamma rays and b) 333-MeV Au ions with 15V applied to the gate during irradiation. (After Ref. [106])

characteristics (ΔV_{th} = 1.06 V), whereas the device in Figure 25b has a much larger shift and a humped-shaped I-V curve (ΔV_{th} = 10.2 V). Thus for nearly the same total dose, the radiation-induced threshold voltage shift is an order of magnitude larger for heavy ions than for Co-60 gamma rays. This is a surprising result when considering that the charge yield for heavy ion irradiation is expected to be significantly lower than for gamma ray irradiation [4,5]. Although not shown here, it should be noted that there was no increase in the gate leakage current for either of these devices for these radiation conditions. This indicates that the large shift induced by heavy ion irradiation is not due to some degradation mechanism that impacts the insulating properties of the gate oxide in these devices. As suggested in [106], one possible mechanism that may explain these data is a combined effect of total dose ionization damage and ion-induced displacement damage.

VIII. SUMMARY

The harsh radiation environment of space can subject electronics to numerous energetic particles. These particles can substantially degrade the performance of electronics. Oxides are particularly susceptible to radiation-induced damage. The electrons and protons in space can lead to radiation-induced total-dose effects. The two primary types of radiation-induced charge are oxide-trapped charge and interface-trap charge. With a positively applied gate bias, holes will transport toward the Si/SiO_2 interface, where some fraction of the holes will be trapped at defects near the Si/SiO_2 interface, forming a positive oxide-trap charge. Immediately after oxide-trap charge is formed, it begins to be neutralized by electrons tunneling from the silicon or by the thermal emission of electrons from the oxide valence band. As holes "hop" through the oxide or as they are trapped near the Si/SiO_2 interface, hydrogen ions are likely released. These hydrogen ions can drift to the Si/SiO_2 interface where they may react to form interface traps. Interface-trap buildup can take thousands of seconds to saturate. There does not appear to be a "true" dose rate dependence for the buildup of interface traps. Unlike oxide-trap charge, interface traps do not normally anneal at room temperature. At threshold, interface traps are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors. Thus, interface-charge charge tends to compensate oxide-trap charge for n-channel transistors and add

together for p-channel transistors. Fortunately, the amount of buildup of radiation-induced charge rapidly decreases as oxide thickness is decreased. As a result, the importance of radiation-induced charge buildup in gate oxides is rapidly decreasing and the total dose hardness of present-day technologies is dominated by radiation-induced charge buildup in parasitic field oxides and the buried oxides of SOI devices.

Two alternate dielectrics that have been investigated for replacing silicon dioxide are hafnium oxides and reoxidized nitrided oxides (RNO). Hafnium oxides show relatively large hole trapping efficiencies (~28%). However, for gate insulator thicknesses expected for the advanced technologies, which may employ alternate dielectrics, the radiation-induced voltage shifts in these insulators may be negligible. RNO transistors can be fabricated such that there is no measurable interface-trap buildup and with less oxide-trap charge buildup than comparable thermal oxides.

A technology that is seeing increased use in space is silicon-on-insulator (SOI). SOI transistors are built on an insulating layer, which reduces the amount of p-n junction area. The reduced junction area leads to lower parasitic capacitance and faster device operation. The absence of a conducting path underneath the MOS transistor completely eliminates parasitic pnpn paths that can cause latchup. The biggest difference between the radiation response of MOS transistors fabricated on bulk silicon substrates and SOI transistors is due to the buried oxide of SOI transistors. Up to 100% of the holes generated by irradiation can be trapped in defects in the bulk of the buried oxide. The buildup of charge can invert the bottom surface of the silicon channel of a MOS/SOI transistor, creating a back-channel leakage current. However, techniques are available that can mitigate the effects of charge trapping in the buried oxide. One transistor design that has been successfully applied to reduce the effects of radiation-induced trapped charge in the buried oxide is the BUSFET.

Heavy ions in space can also degrade the oxides in electronic devices through several different mechanisms. One type of mechanism is single-event gate rupture. SEGR can cause both soft and hard breakdowns. In single-event gate rupture the oxide can be physically destroyed. However, for ultrathin oxides and insulators, heavy ions more predominantly cause radiation-induced soft breakdown, resulting in potentially large increases in gate oxide leakage current. In any case, it has been shown that the radiation-induced hard breakdown voltage for ultrathin voltages oxides and insulators should stay well above normal operating voltages as technologies advance. Unfortunately, even for cases where heavy-ion exposure does not lead to SEGR, it may decrease device lifetime.

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