SAND2007-4349C

Sacrificial Surface Micromachining and SUMMiT ™

(NINE Short Course)

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

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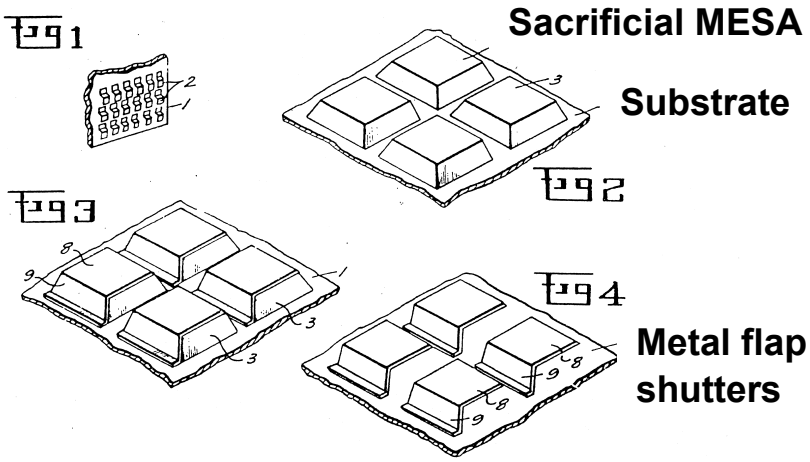
Outline

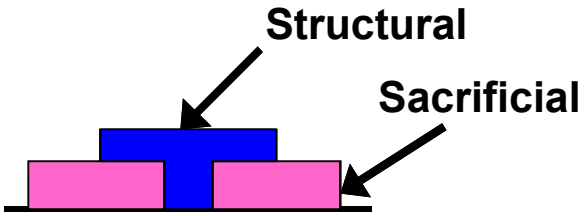
- Overview
- Key concepts of surface micromachining
- Major processing steps for integrated circuit fabrication
  - Deposition, oxidation, CVD, PECVD, LPCVD, photolithography
  - Etching — wet and dry, CMP
- Surface micromachining — multilayer processing
- Release, packaging, reliability

Surface Micromachining



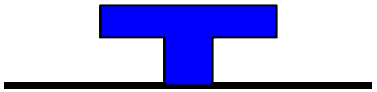
Definition

Fabrication of structures through alternate deposition and patterning of sacrificial and structural materials



First demonstrated in 1956 patent

US Patent 2,749,598: "Method of Preparing Electrostatic Shutter Mosaics," Filed Feb. 1, 1952, Issued June 12, 1956



Released Structure

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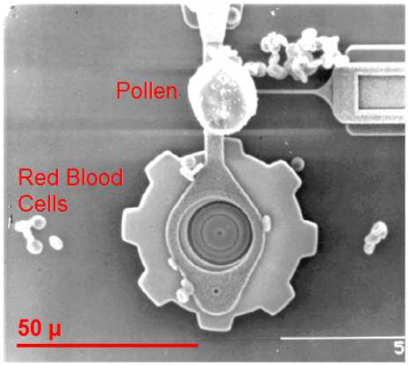
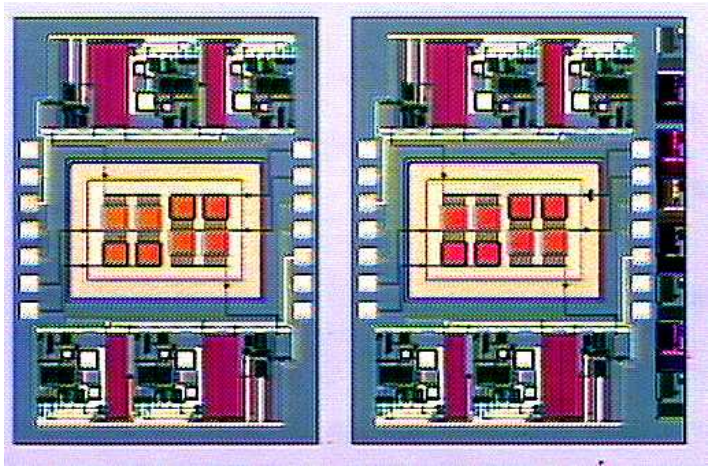
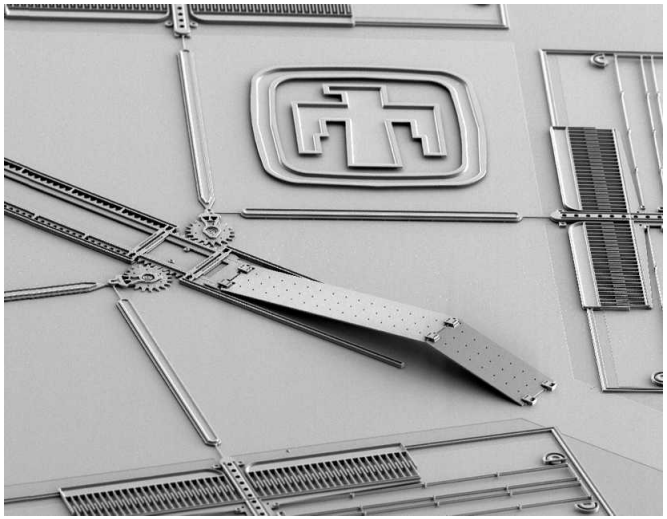
Merits of Surface Micromachining (SMM) Technology



- Complex miniaturized mechanical systems with micron feature sizes
- Batch fabricated with no assembly required
- Can integrate with silicon microelectronics
- Technology exploits microelectronics infrastructure for sensors, actuators etc.





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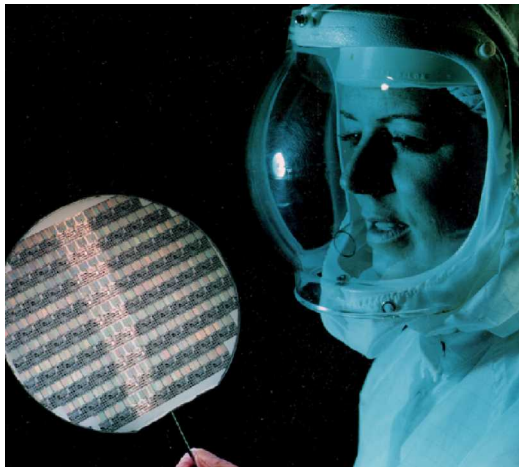
Microelectronics Fabrication Processes for Silicon Surface Micromachining



- **Why make micromachines using IC fabrication technology???**
  - **Low cost batch fabrication**
  - **Design flexibility**
  - **Repeatability, reliability, high yield**
  - **Build on existing manufacturing infrastructure**
  - **Small geometries with precise dimensions**
  - **Interface with control electronics**
  - **Si is a good mechanical material**

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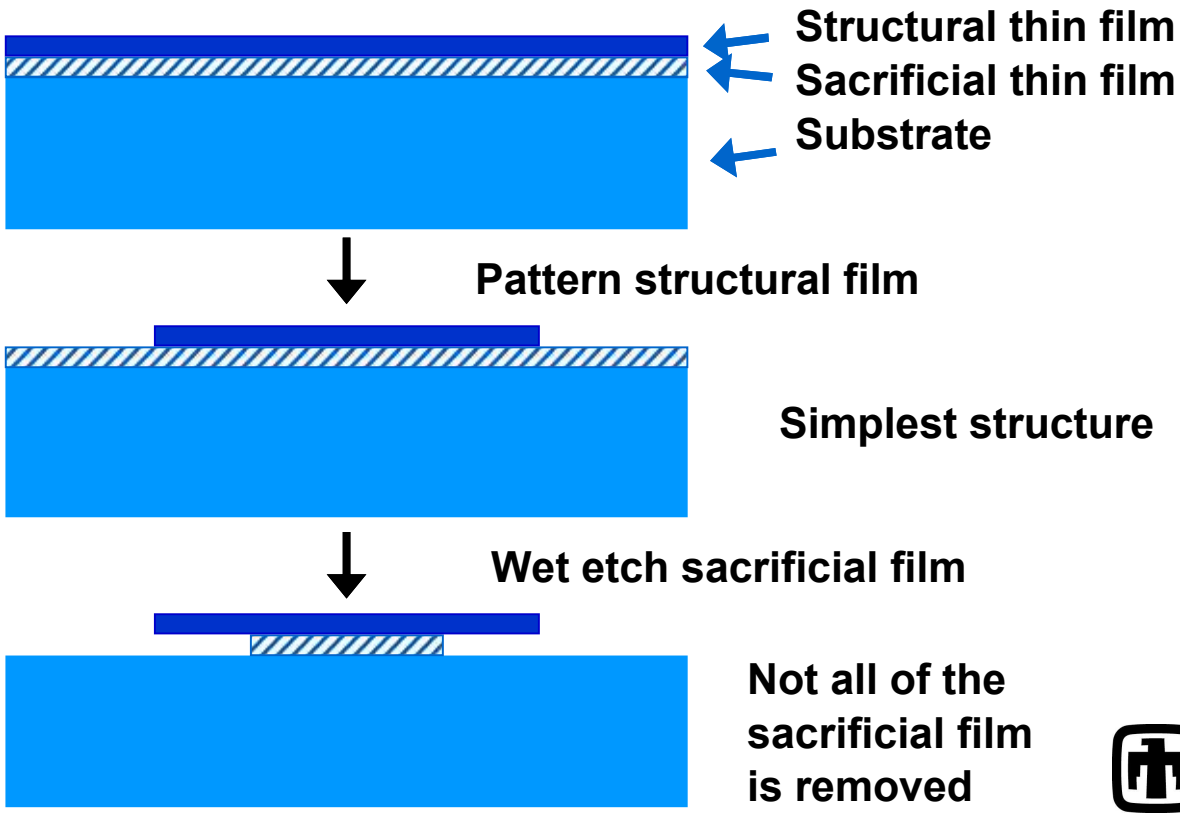
Surface Micromachining

- **Key Concepts:**
  - **Mechanical part is formed out of deposited thin films**
  - **Need one structural and one sacrificial material**



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Materials for Surface Micromachining

Material system requirements:

- Structural film must have desirable mechanical and electrical properties (low stress, conductivity, etc.)
- Sacrificial film must be stable under structural film deposition conditions and etch readily in an etchant that doesn't attack the mechanical film or the substrate
- Both films must be compatible with fabrication environment (generally silicon IC fab)

Examples from the literature:

Structural	Sacrificial
Polysilicon	SiO_2 (most common), porous Si
Low-stress (Si rich) SiNX	Polysilicon
Tungsten	SiO_2
Aluminum	Polyimide
SiGe	SiGe
	Photoresist

Fundamental Processing Steps in Integrated Circuit Fabrication

Crystal growth & wafer slicing

Wafer Slicing

Single Crystal Silicon Ingot

Wafer

Repeat N times

Thin film formation

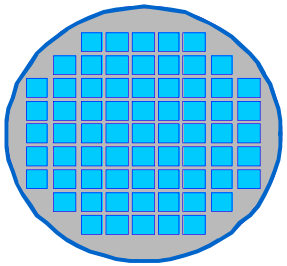
Impurity doping

Photolithography

Etching

Mask set

Dicing and Packaging



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Thin-film Formation or Growth: Oxidation

Silicon grows silicon dioxide when exposed to dry oxygen or steam at high temperatures

Thermal oxidation of silicon proceeds by the following chemical reactions:

Species	***Reaction***	***Relative Growth Rate***
Dry Oxygen	$Si + O_2 \longrightarrow SiO_2$	**Slow** **for <100> Si at 800°C, 0.01 µm takes approx. 150 min.**
Steam	$Si + 2\,H_2O \longrightarrow SiO_2 + 2H_2$	**Fast** **for <100> Si at 800°C, 0.01 µm takes approx. 12 min.**

Standard oxidation processes - utilize either dry or wet

Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

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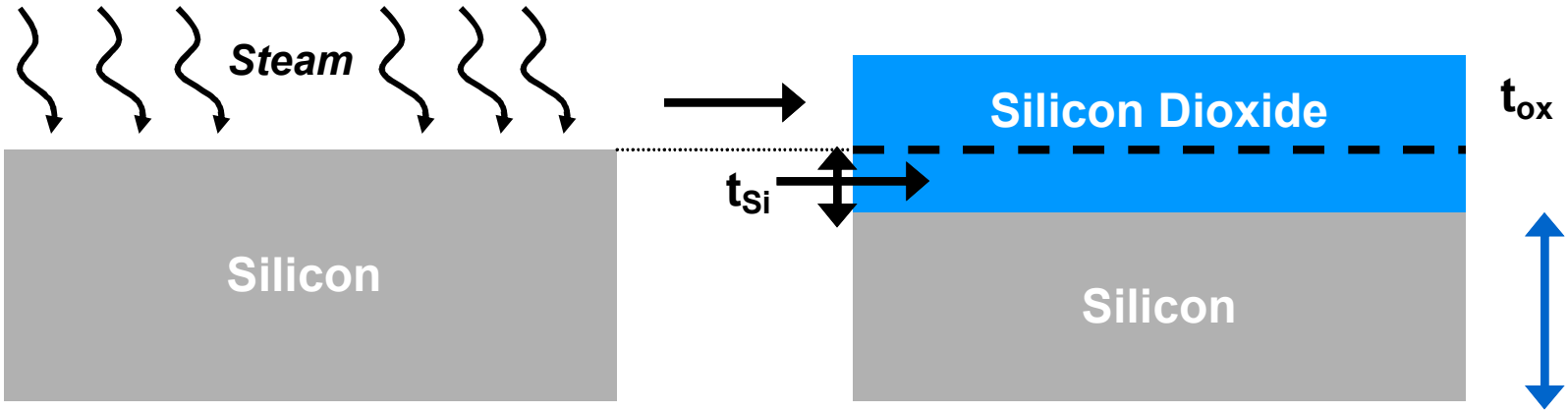
Thin-film Formation or Growth: Oxidation (2)

The oxidation process consumes silicon from the wafer during the formation of the silicon dioxide layer

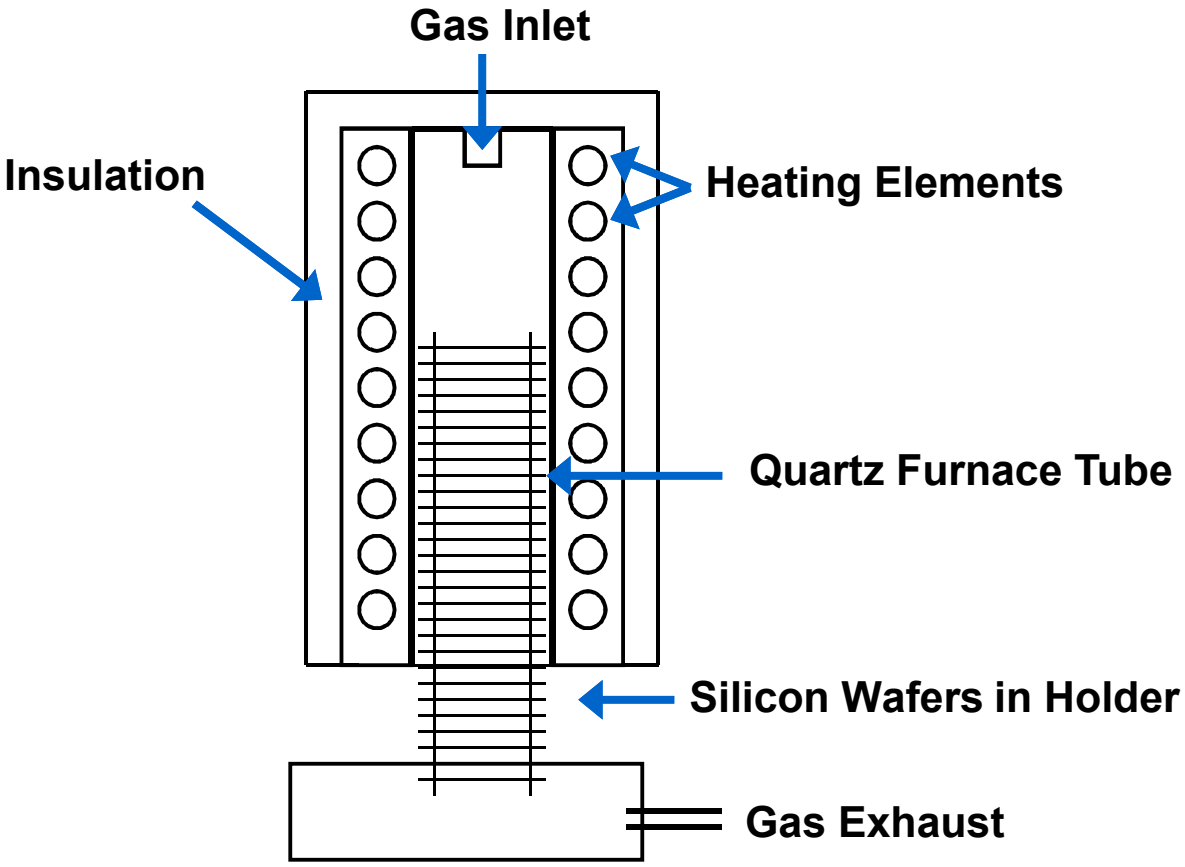
The resulting oxide film is thicker than the amount of silicon consumed in that part of the wafer



The oxide thickness (t_{ox}) is easily measured, the amount of silicon consumed (t_{Si}) can be calculated for single crystal and polycrystalline silicon by the following equation:

$$t_{Si} = 0.45 t_{ox}$$

Thin-film Formation or Growth: Oxidation (3)



Vertical Oxidation Furnace

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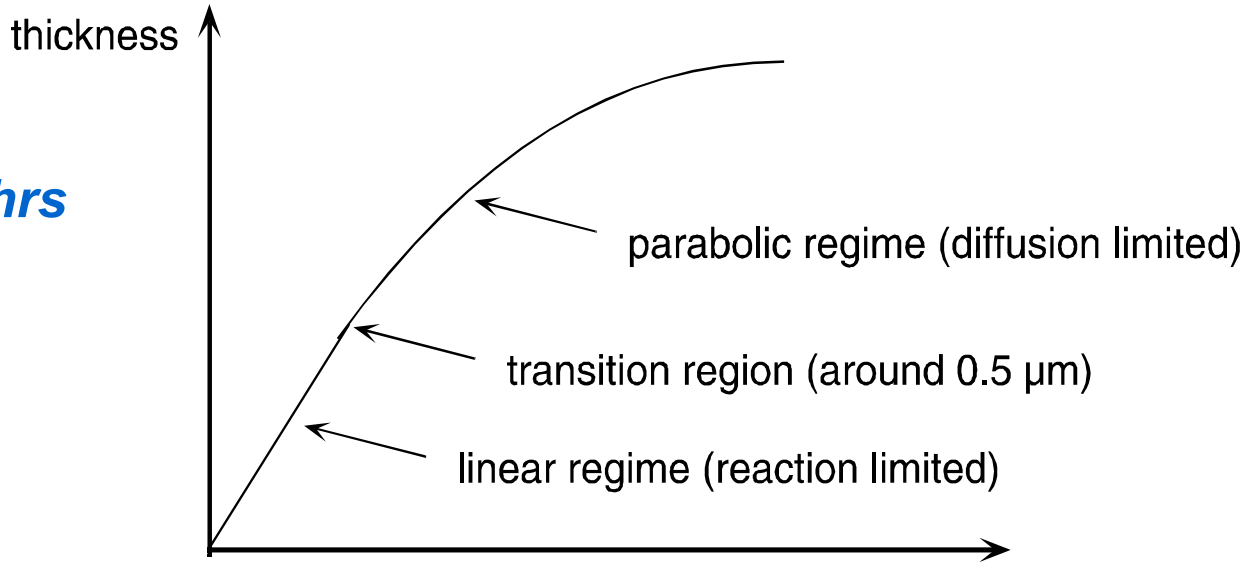
Thin-film Formation or Growth: Oxidation (4)

- **Typical "thick" oxide processes are done at 1050°C, for 100 min, in steam to get approximately 6300 Å oxide grown**
- **Typical IC oxide thicknesses range from 50 Å (gate oxide) to 6300 Å (field oxide)**
- **Typical MEMS oxide thickness requirements range from 6300 Å to 2 microns**

Practical limit in oxide thickness » 2μm » 15 hrs (diffusion limited)



Thin-film Deposition: Chemical-vapor Deposition (CVD)

- CVD is the deposition of a stable layer of material on a partially processed substrate by the chemical reaction of gaseous species
- The constituents forming the deposited layer do not come from the silicon wafer itself (like oxide growth)
- CVD is used to deposit polysilicon, SiO_2 (both high- and low-temp varieties HTO and LTO), SiN_X, other dielectrics, metals
- Reactants are introduced in vapor phase and react at wafer surface to form the thin film
- CVD provides conformal or nearly conformal step coverage

CVD Tool
(Applied Materials)

CVD Tool
(Applied Materials)

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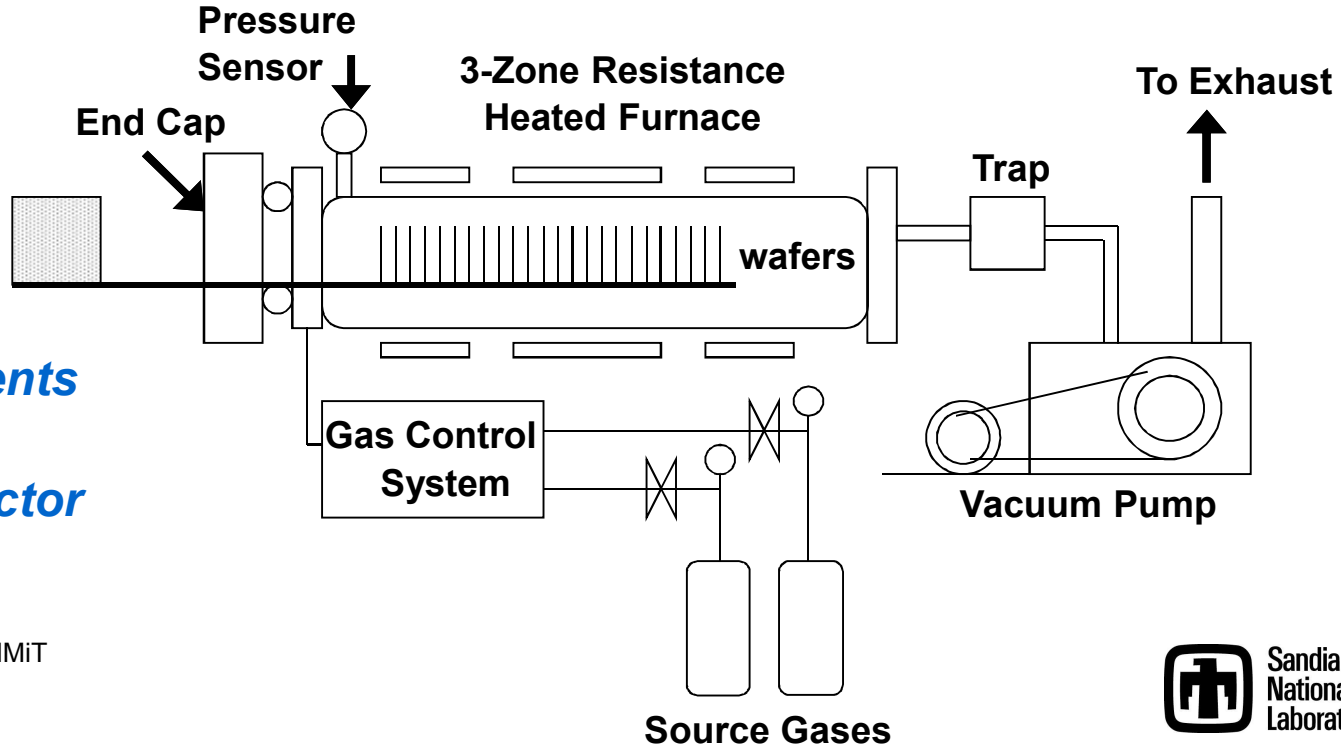
Thin-film Deposition: LPCVD

- LPCVD (low-pressure CVD)
- Operates at 0.1 to 1 torr
- Provides the best quality films
- Provides conformal step coverage
- Typically used to deposit HTO, PolySi, W, high-quality SiN_X



Basic elements of an LPCVD Reactor

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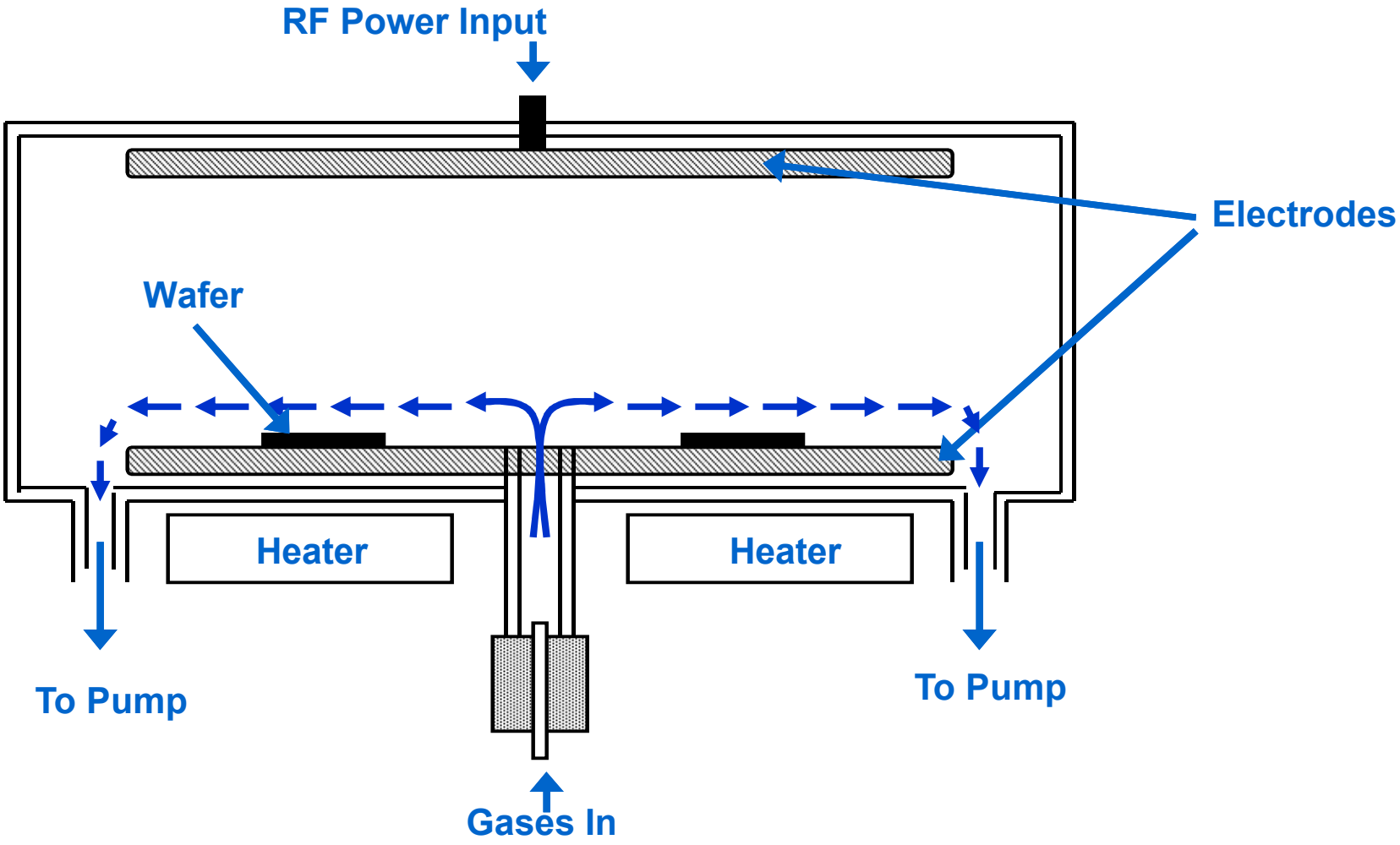
Thin-film Deposition: PECVD

- Plasma Enhanced CVD
- Operates at lower temperatures
- Provides good step coverage
- Films etch quickly
- Primarily used for nitride passivation in ICs or interlevel dielectrics

Thin-film Deposition: PECVD (2)



Horizontal Parallel Plate PECVD Reactor

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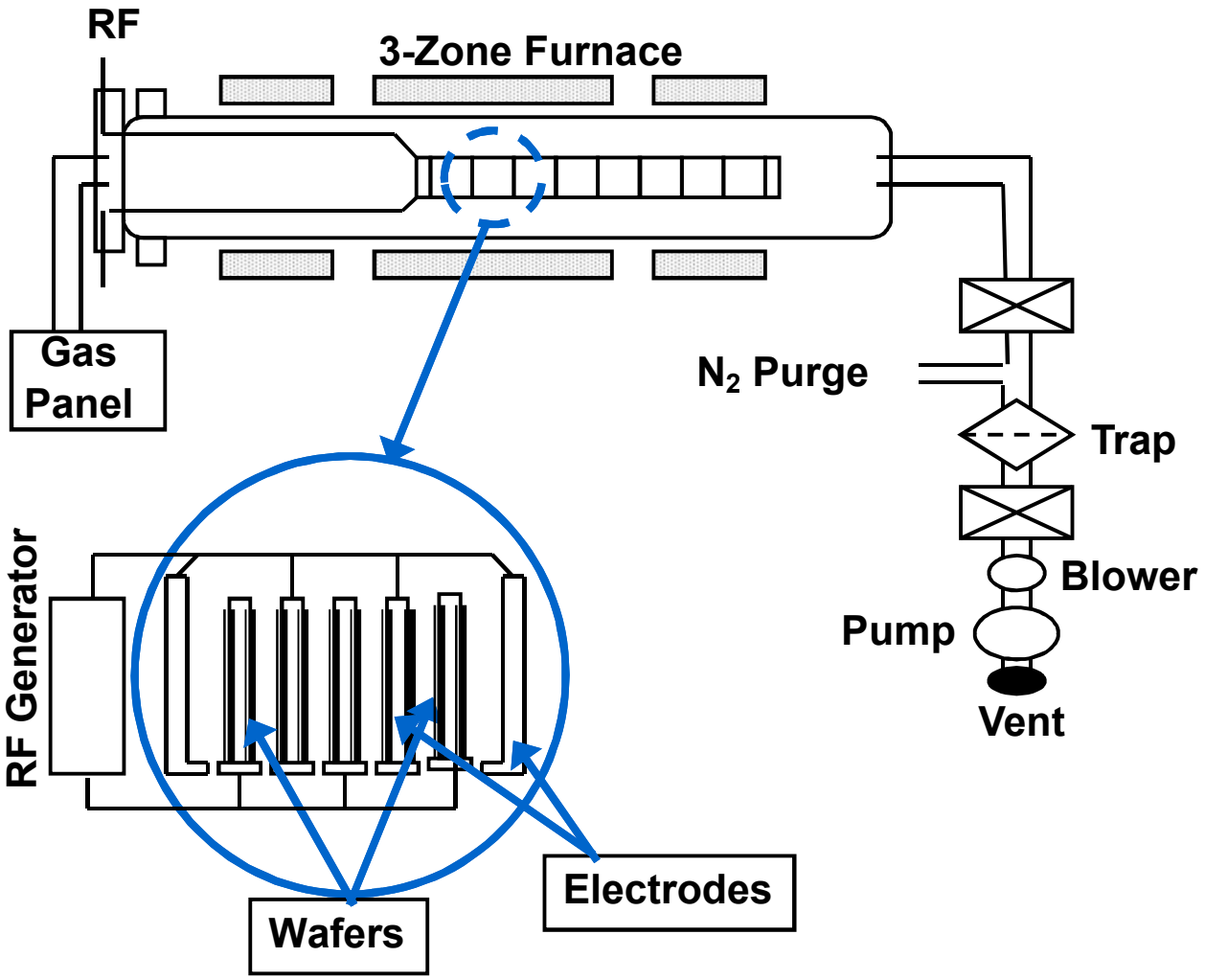
Thin-film Deposition: PECVD (3)



High Capacity PECVD Reactor

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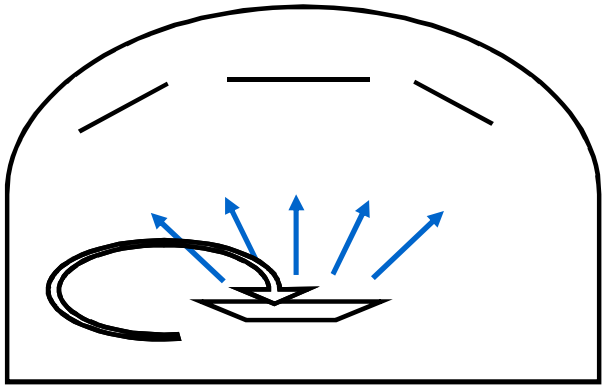
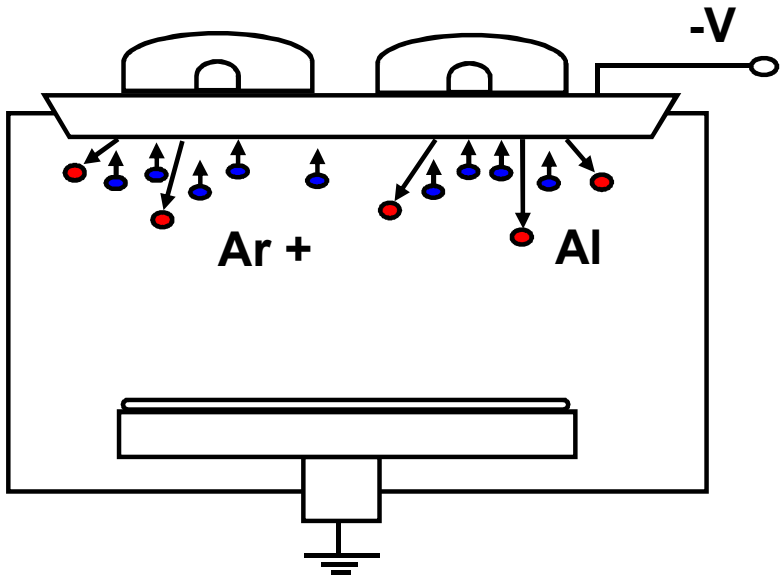
Thin-film Deposition: PVD



Evaporation



Conventional Magnetron Sputtering

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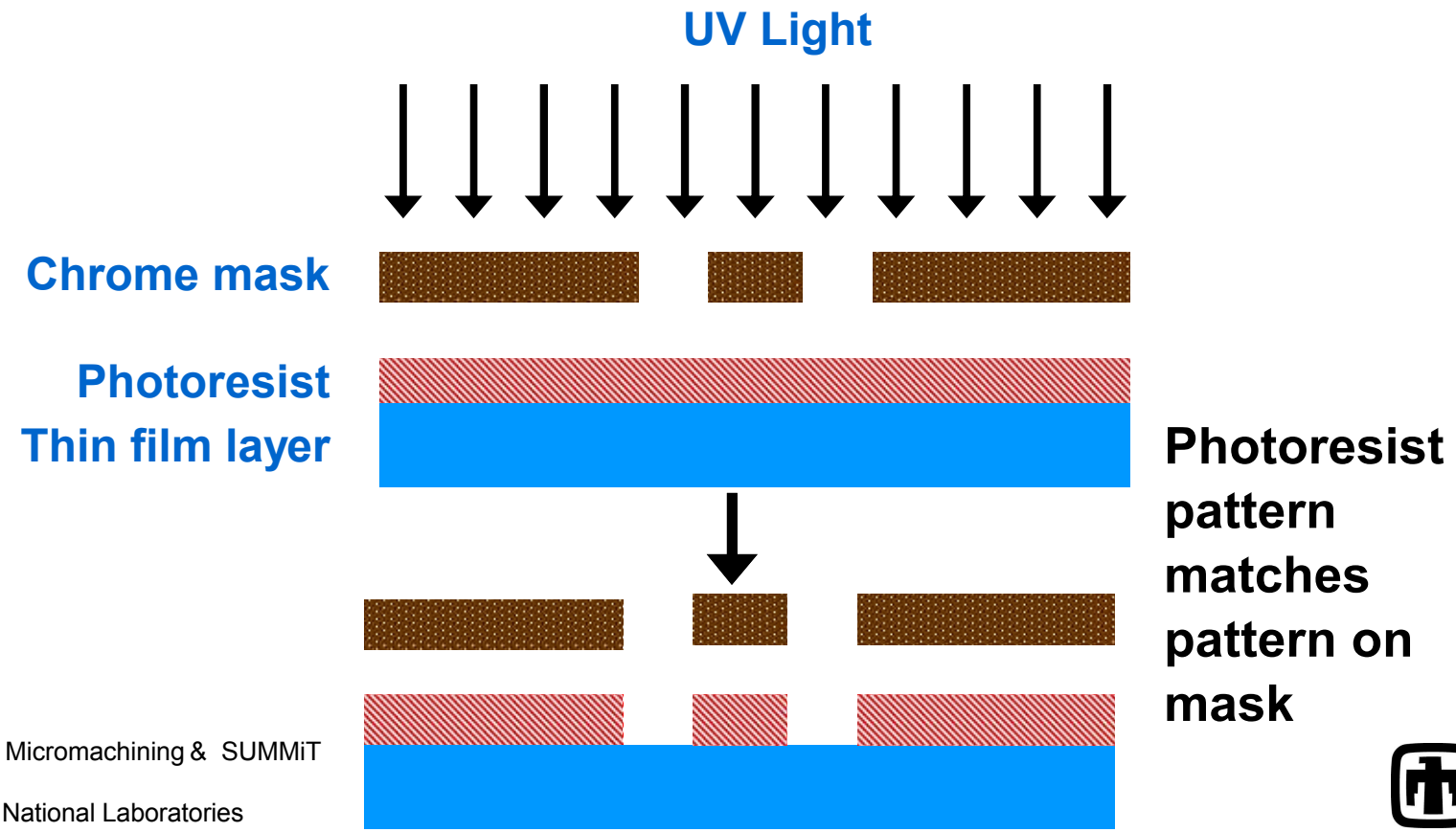
Photolithography

- Photolithography is used to pattern the thin-film layers
- IC industry uses positive photoresist — becomes soluble in developer when exposed to UV light



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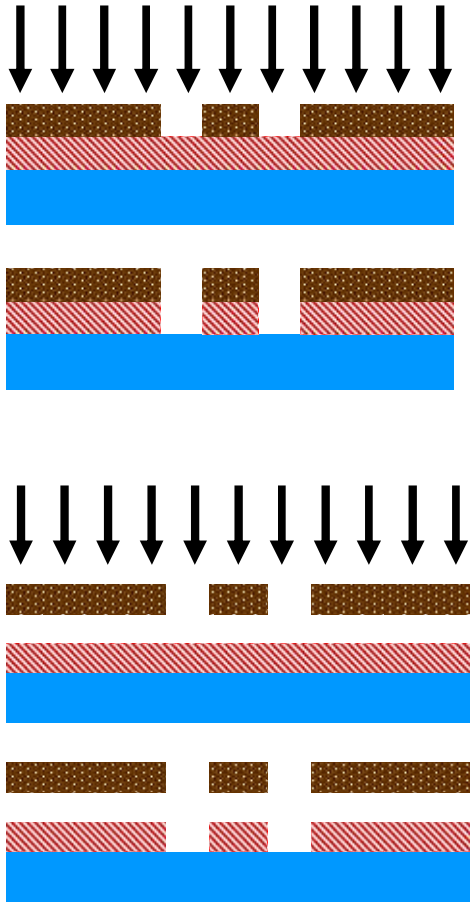
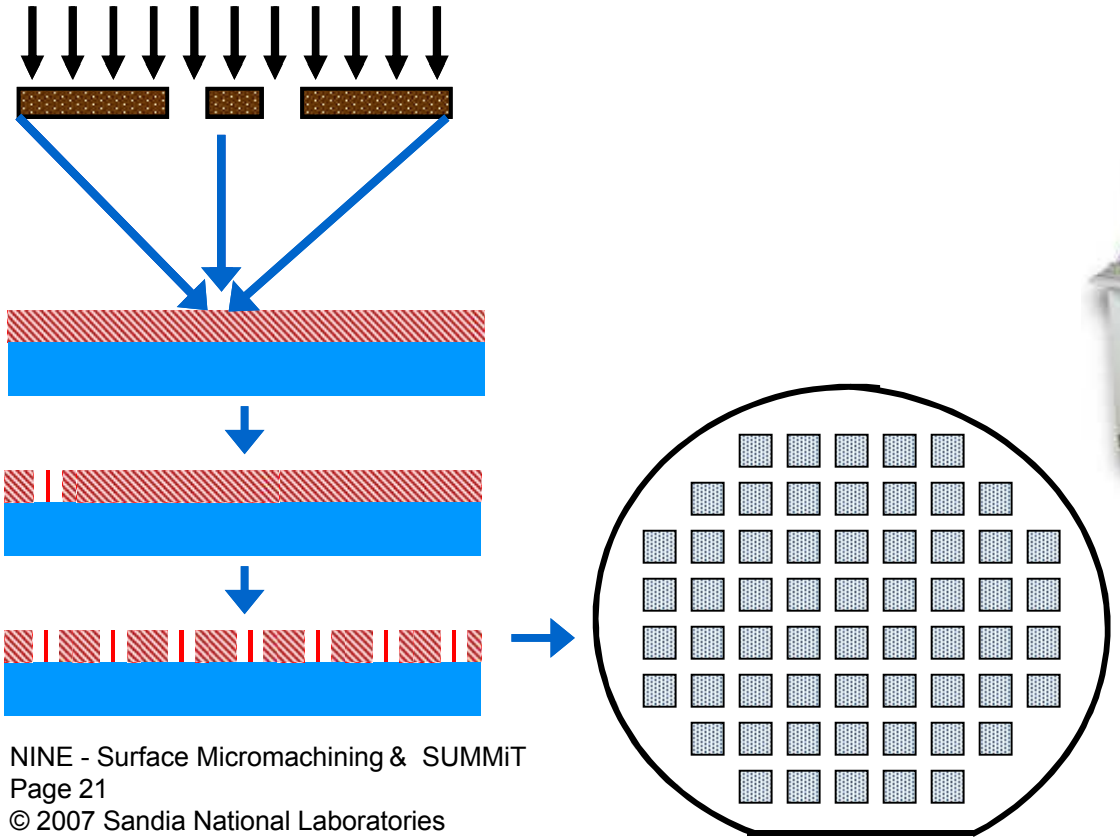
Photolithography Aligners

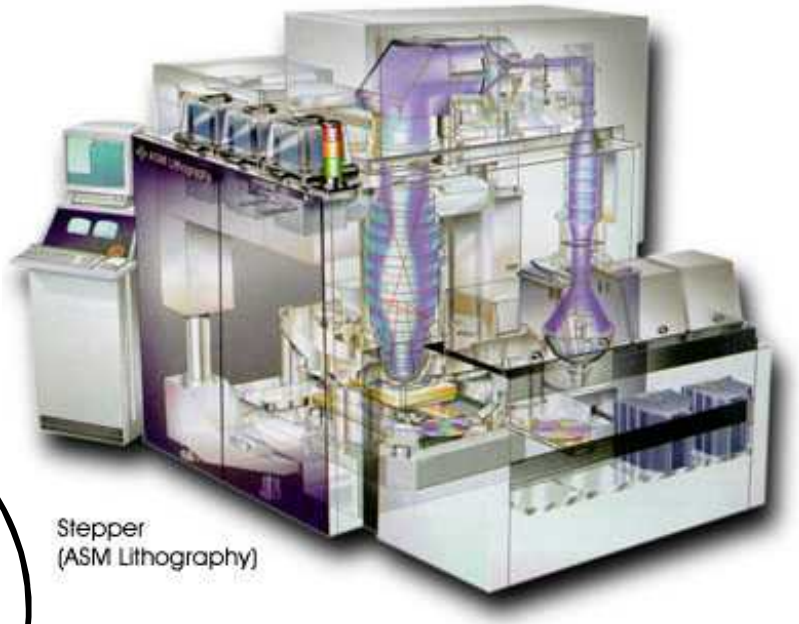
- Types of aligners used in IC industry:
- Contact aligner
  - 1:1 pattern transfer (mask covers entire wafer)
  - Mask contacts photoresist directly
  - ~ 2 µm resolution
- 1:1 projection aligner
  - 1:1 pattern transfer (mask covers entire wafer)
  - No direct contact between mask and resist
- ~ 2 µm resolution



Photolithography Aligners (2)

- **Stepper (UV projection aligner)**
  - **Generally 5:1 pattern transfer**
  - **Mask defines single die and pattern is stepped across wafer**
  - **~ 0.3 µm resolution**





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Microelectronics Fabrication Processes: Etching

Two methods for etching in IC fabrication:

1) Wet Chemical Etching **2) Dry (or Plasma) Etching**

1) Wet Chemical Etching

- Has been in use for over 30 years
- Has very high selectivity
- Has the ability to remove undesirable ions and contaminants from the wafer surface
- Has an isotropic etch profile
- Used to form pin joints in the SUMMiT™ Process

Isotropic Etch

2) Dry Etching

- Can etch anisotropically using energetic plasma
- Is capable of higher resolution
- Used for patterning both polysilicon and silicon dioxide in SUMMiT™ Process

Anisotropic Etch

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IC Fabrication Processes: Dry (Plasma) Etching

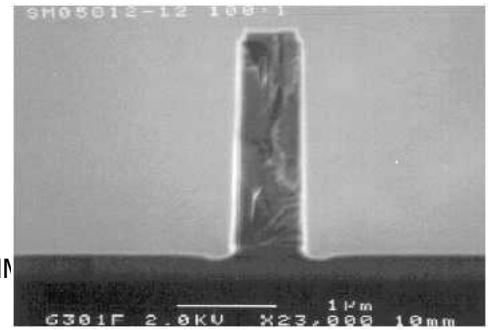
Reactive Ion Etching (RIE)

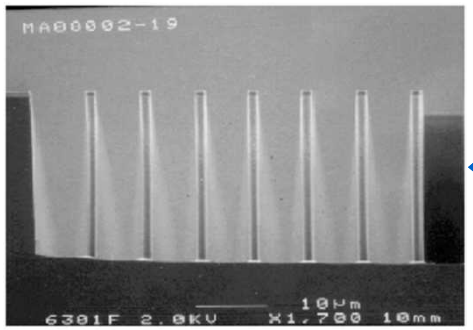
- Uses an energetic plasma to create an anisotropic etch profile
- Requires relatively low temperatures (–30°C to 20°C)
- Sidewall profile, selectivity, & etch rate depend on many parameters
- Physics and chemistry complex; control challenging but doable

Chemistries:

Silicon	Chlorine & fluorine-base, with or without oxygen
	Some variations give good selectivity to SiO_2
	Cold SF_6:0_2 particularly good for trenching
SiO_2, SiN_X	Fluorine-based
(Aluminum	Chlorine-based)
(Tungsten	Fluorine-based)

2.5 micron poly etch in chlorine (SiO_2 hard mask) →





← 40 micron Si etch in SF_6:O_2 (SiO_2 hard mask)

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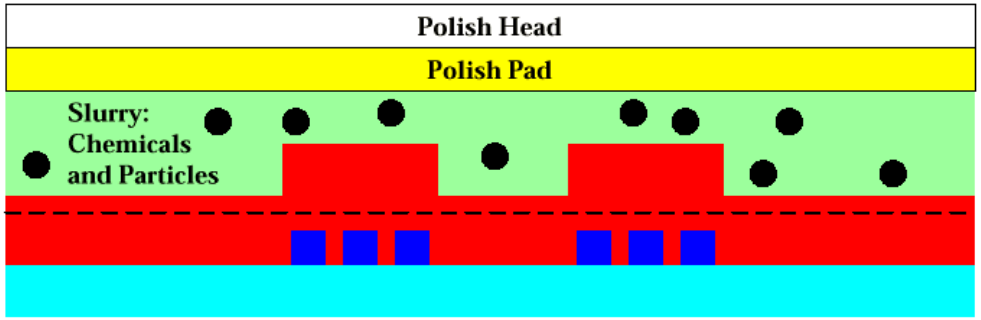
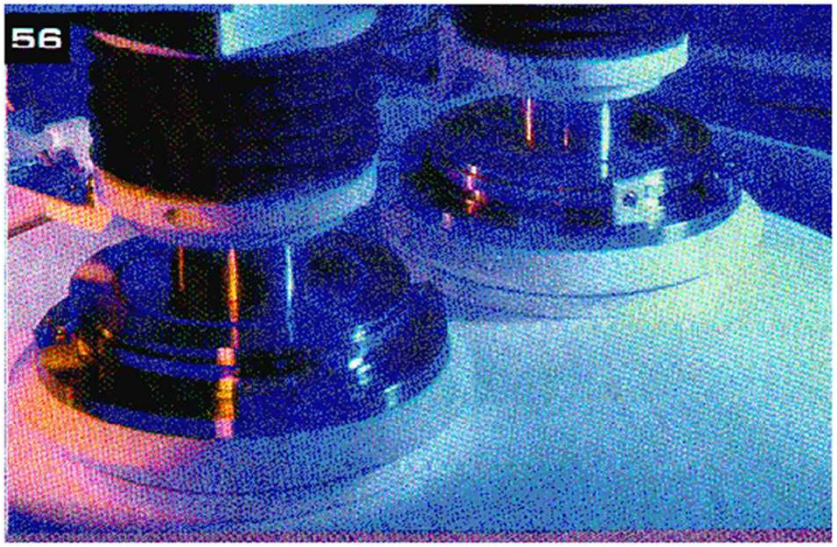
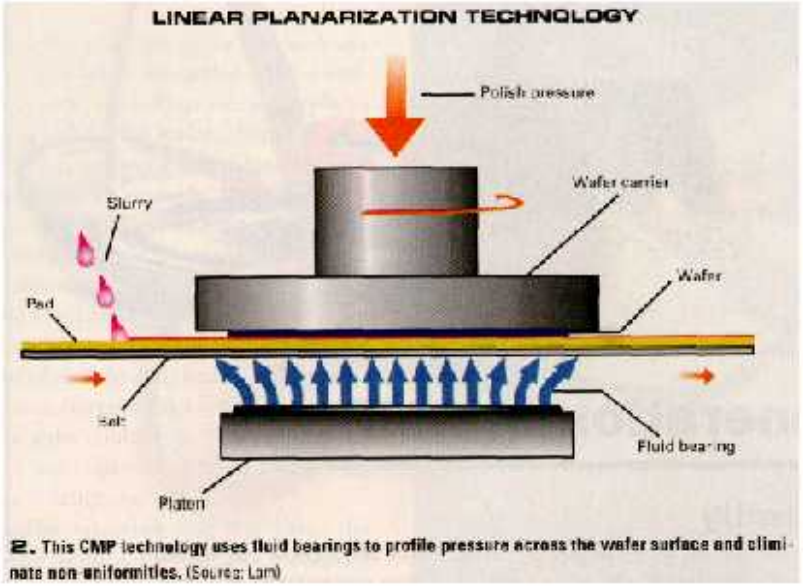
Chemical-mechanical Polishing (CMP)







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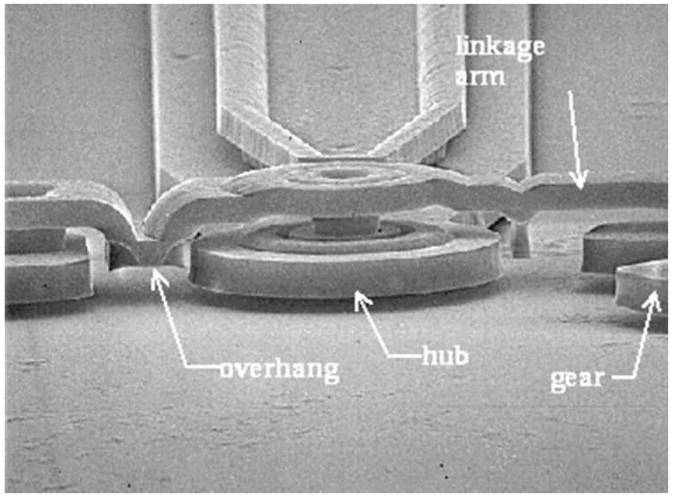
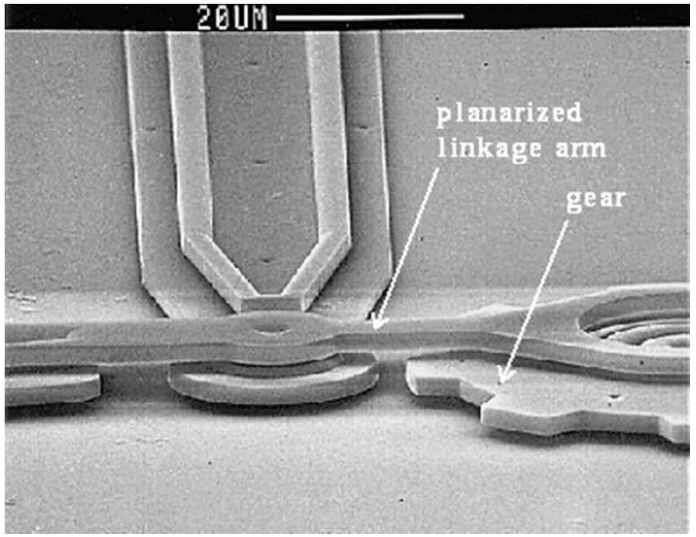
CMP Process Comparison

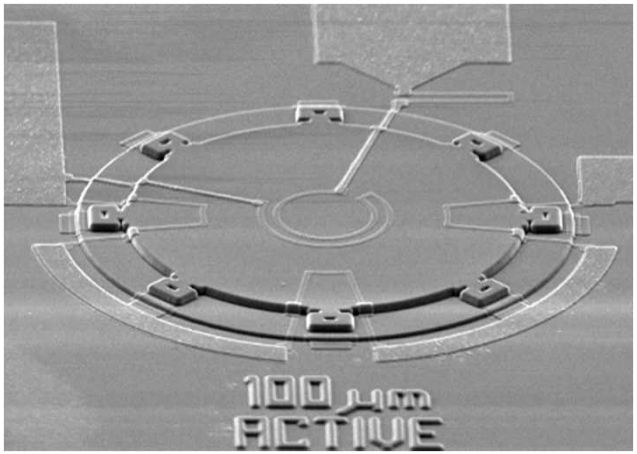
Non-planar Process

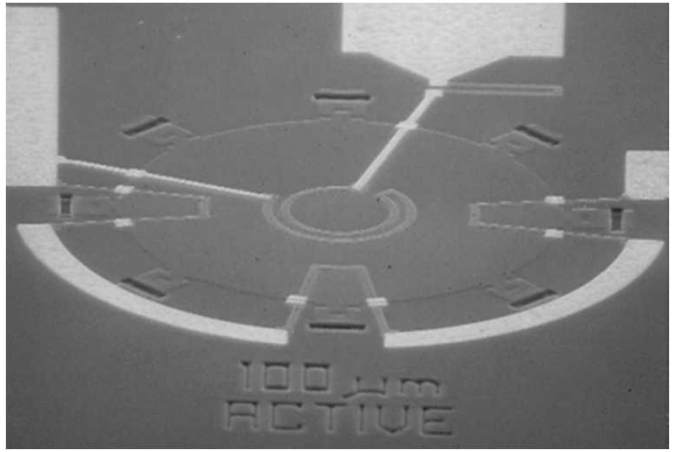


Planarized Process



Pressure sensor





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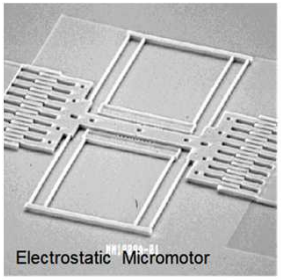
Planarization Enables a New Generation of Micromachines

2*-Level

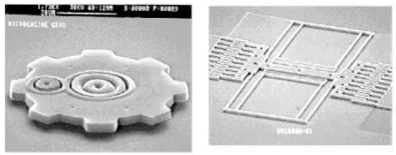


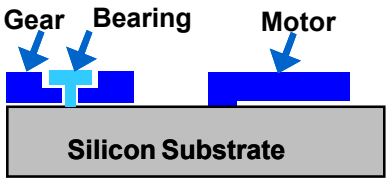
Polysilicon Level #1

Sensors

*** First Poly level is a ground plane**

3-Level

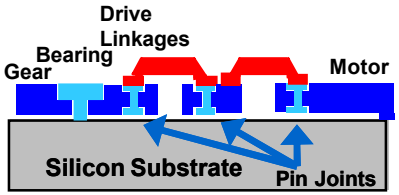




Polysilicon Level #1
Polysilicon Level #2

Advanced Sensors / Simple Actuators

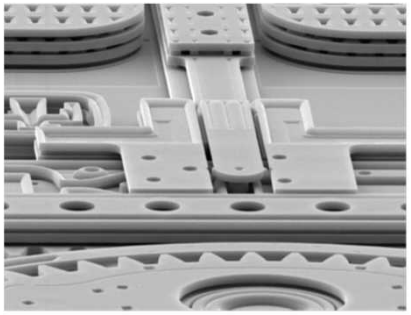
4-Level

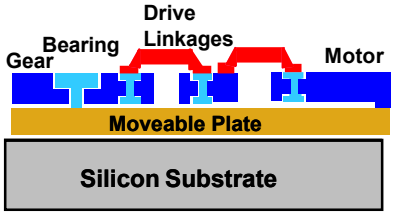


Polysilicon Level #1
Polysilicon Level #2
Polysilicon Level #3

Advanced Actuators

5-Level





Polysilicon Level #1
Polysilicon Level #2
Polysilicon Level #3
Polysilicon Level #4

Complex Systems

Most competing technologies limited to two poly levels

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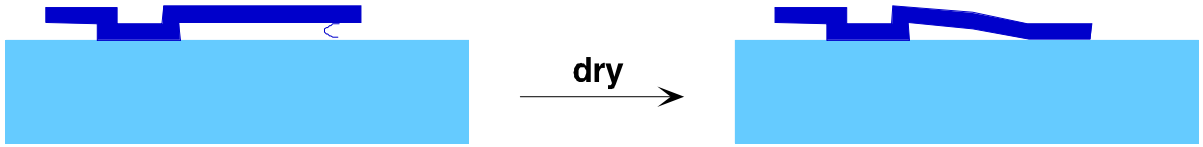
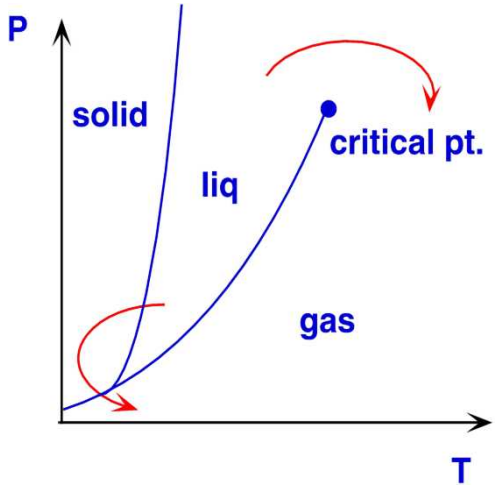
Release Processes

- **Meniscus between hydrophilic surfaces pulls surfaces together (stiction):**



- **Solutions:**
  - **Make structures stiffer in the z-direction ("high-aspect ratio")**
  - **Add bumps (dimples) to reduce surface area in contact**
  - **Treat surfaces to make them hydrophobic (e.g. SAMs)**
  - **Avoid creating the meniscus by**
    - **Drying in supercritical CO_2**
    - **Freezing and sublimating the solvent**



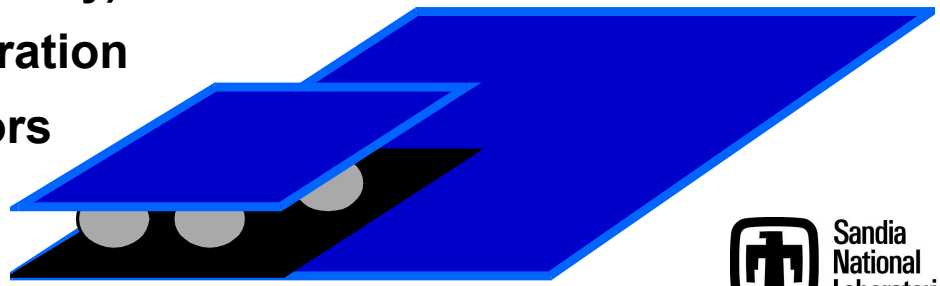
IC Fabrication Processes: Packaging

IC Packaging processes:

- Wafer dicing (diamond saw)
- Wire bonding from pads to pins
- Multi-chip modules and flip-chip bonding
- Hermetic sealing
- Potting to protect from shock and vibration

Of particular interest to MEMS processes:

- Wafer dicing before or after release?
- Multi-chip modules and flip-chip bonding for hybrid integration
- Exposing sensors and actuators to hostile environments (while protecting circuitry)
- Potting to protect from shock & vibration
- Precise orientation of inertial sensors



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Summary

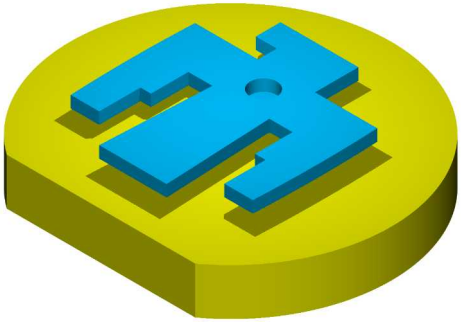
- **Silicon surface micromachining utilizes mature IC infrastructure.**
- **Iterative processes of film deposition, patterning, etch, & CMP used to fabricate complex mechanical structures.**
- **Structural polysilicon layers fabricated on top of sacrificial oxide; “release” etch removes sacrificial films.**
- **Unique considerations required for release processing, reliability, and packaging.**

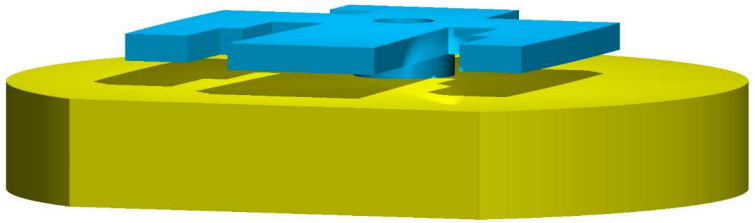
SUMMiT™ Process Details

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

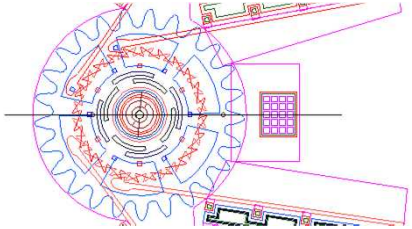
Outline

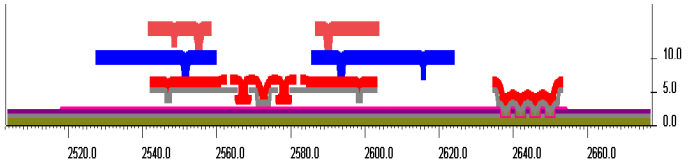
- **SUMMiT™ Process — Building blocks for Sandia Ultra-planar, Multi-level MEMS Technology**





- **SUMMiT V™ Process Layer Descriptions and Mask Level**
- **SUMMiT V™ Process Cross-Sections: Double Ratchet Actuator**





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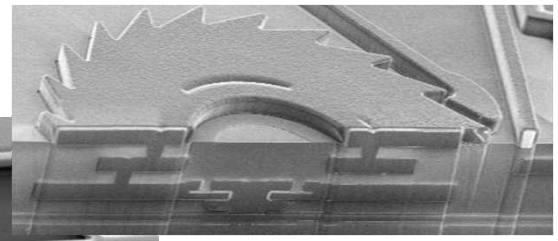
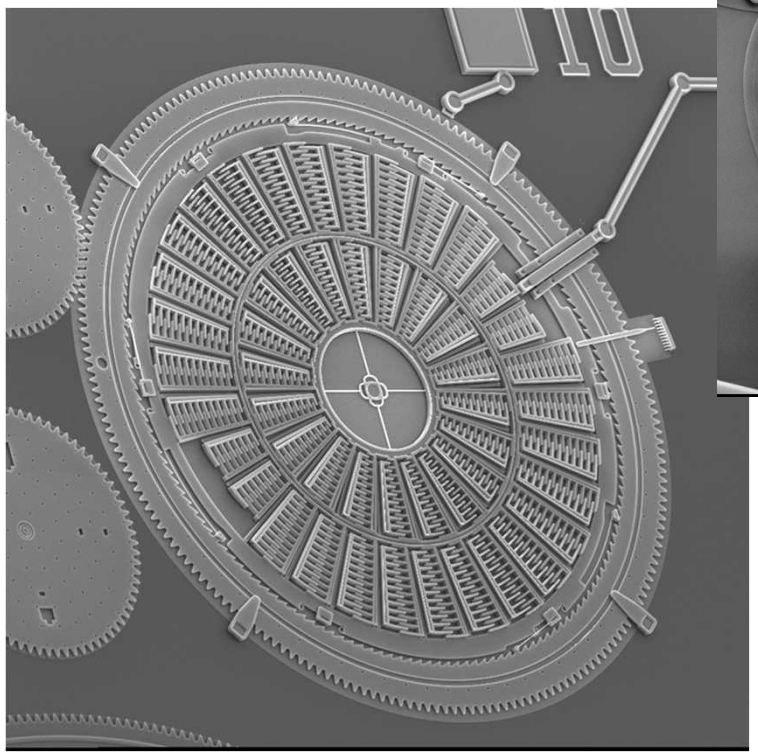
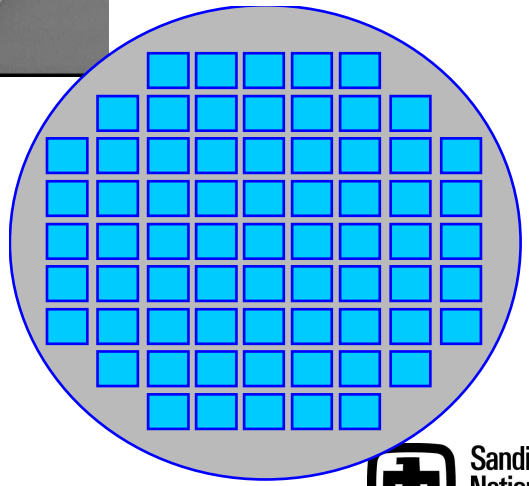
SUMMiT™ Process:
Sandia Ultra-planar, Multi-level MEMS Technology







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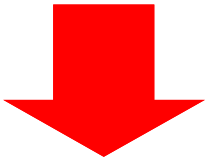
SUMMiT™ Process Layer Descriptions

Layer	Mask level(s)	Film description	Purpose
MMPoly1	(MMPoly1_Cut xor MMPoly1), Pin_Joint_Cut	1.0 µm doped polySi (□ₛ≈22 Ω/sqr)	Mechanical polySi #1, hub for gears
SacOx1	SacOx1_Cut, Dimple1 _Cut	2 µm TEOS	Sacrificial oxide, anchor
MMPoly0	(MMPoly0 xor MMPoly0_Cut)	0.3 µm doped polySi (□ₛ≈40 Ω/sqr)	Ground plane
Nitride	Nitride_Cut	0.8 µm SiN_x over 0.6 µm SiO_2	Electrical isolation



150mm (6”) Silicon Substrate

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SUMMiT™ Process Layer Descriptions (2)

Layer	Mask level(s)	Film description	Purpose
PTNMETAL	(PTNMETAL xor PTNMETAL_Cut)	0.7um AlCu	Wire bonding Anchor
MMPoly4	(MMPoly4 xor MMPoly4_Cut)	2.25 µm doped (Ω_s 9 /sqr), planar poly Si	Mechanical polySi #4
SacOx4	SacOx4_Cut, Dimple4 _Cut	1.5 - 2.0 µm CMP planarized TEOS	Sacrificial oxide, anchor
MMPoly3	(MMPoly3 xor MMPoly3_Cut)	2.25 µm doped (Ω_s 9 /sqr), planar poly Si	Mechanical polySi #3
SacOx3	SacOx3_Cut, Dimple3 _Cut	1.5 - 2.0 µm CMP planarized TEOS	Sacrificial oxide, anchor
MMPoly2	(MMPoly2 xor MMPoly2_Cut)	1.5 µm doped polySi (Ω_s 18 /sqr)	Mechanical polySi #2
SacOx2	(SacOx2 xor SacOx2_Cut)	0.3 µm TEOS	Sac. ox, hub clearance

SUMMiT™ Process Mask Levels

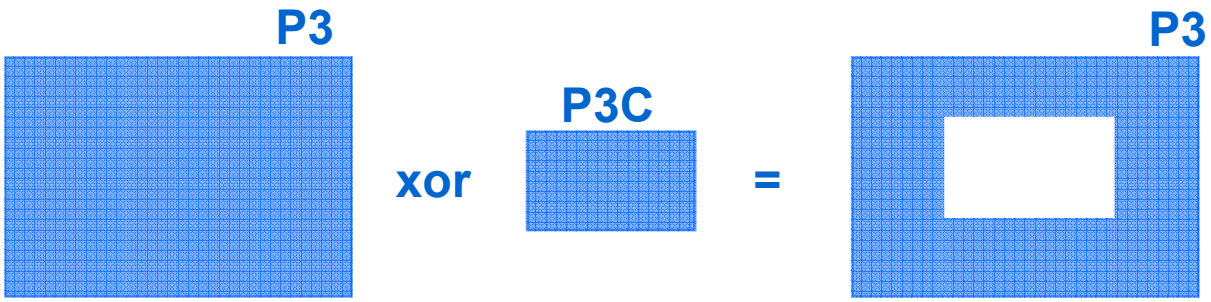
Mask Level	Code	Color	Purpose
21 Nitride_Cut*	NIC	Purple	Substrate contacts
22 MMPoly0	P0	Magenta	Ground plane
23 Dimple1_Cut	D1C	Dk Blue	Dimples in P1
24 SacOx1_Cut	X1C	Green	Anchor P1
25 MMPoly1_Cut	P1C	Black	Holes in P1, no flange
26 Pin_Joint_Cut	PJC	Yellow	Holes in P1 w/ flange
27 SacOx2	X2	Tan	Separate P1 & P2
28 MMPoly2	P2	Red	Define shapes in P2 and/or P1+P2
29 Dimple3_Cut	D3C	Yellow	Dimples in P3
30 SacOx3_Cut	X3C	Black	Anchor P3
31 MMPoly3	P3	Blue	Define shapes in P3
34 Dimple4_Cut	D4C	Orange	Dimples in P4
36 MMPoly4	P4	Peach	Define shapes in P4
42 SacOx4_Cut	X4C	Dk Green	Anchor P4
48 PTNMETALPTN		Gold	Define shapes in PTNMETAL

* Masks with "_Cut" in the name are dark-field masks (closed polygons define holes to be etched in film); others are light-field (closed polygons define structures in film to be left after etch)

SUMMiT™ Drawing Only Mask Levels

Mask Level	Code	Color	Purpose
† 62 MMPoly0_Cut	P0C	Magenta	Define shapes in P0
† 35 MMPoly1	P1	Black	Define shapes in P1
† 37 SacOx2_Cut	X2C	Tan	Define holes in X2
† 38 MMPoly2_Cut	P2C	Red	Define holes in P2
† 41 MMPoly3_Cut	P3C	Blue	Define holes in P3
† 46 MMPoly4_Cut	P4C	Peach	Define holes in P4
† 59 PTNMETAL_Cut	PTNC	Gold	Define holes in PTNMETAL

† These "drawing-only" layers are XORed with their master layers to form the mask (i.e. P1C xor P1 = P1C, X2 xor X2C = X2, P2 xor P2C = P2, P3 xor P3C = P3 P4 xor P4C = P4). Shapes in drawing layers only valid inside shapes in the corresponding master layer!



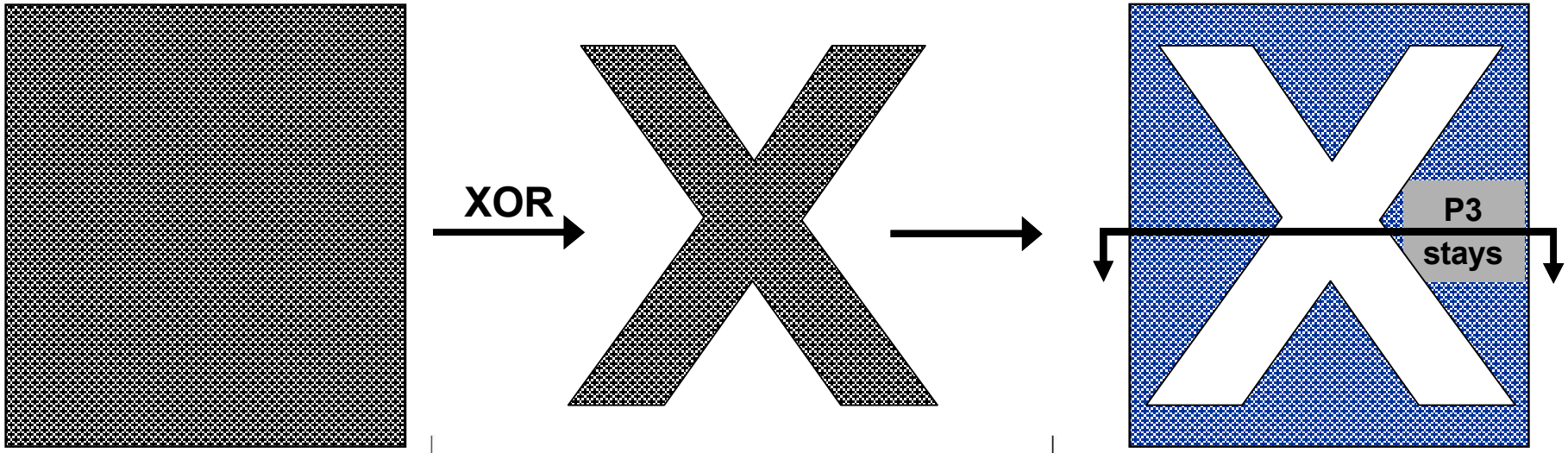
XOR — MMPoly3

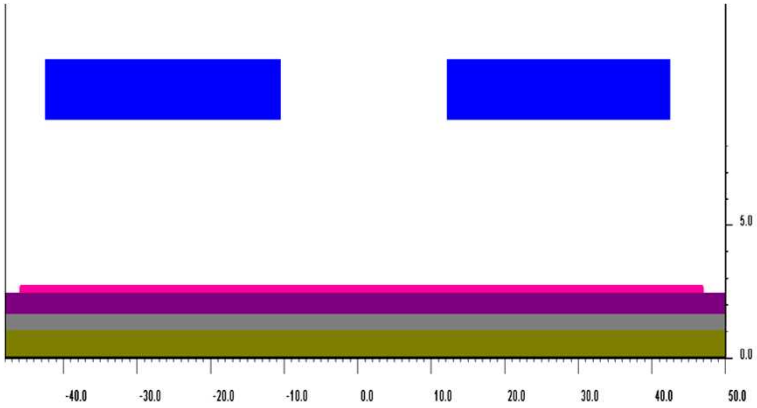
Master Layer

MMPoly3
(P3)

Associated Drawing Layer

MMPoly3_Cut
(P3C)





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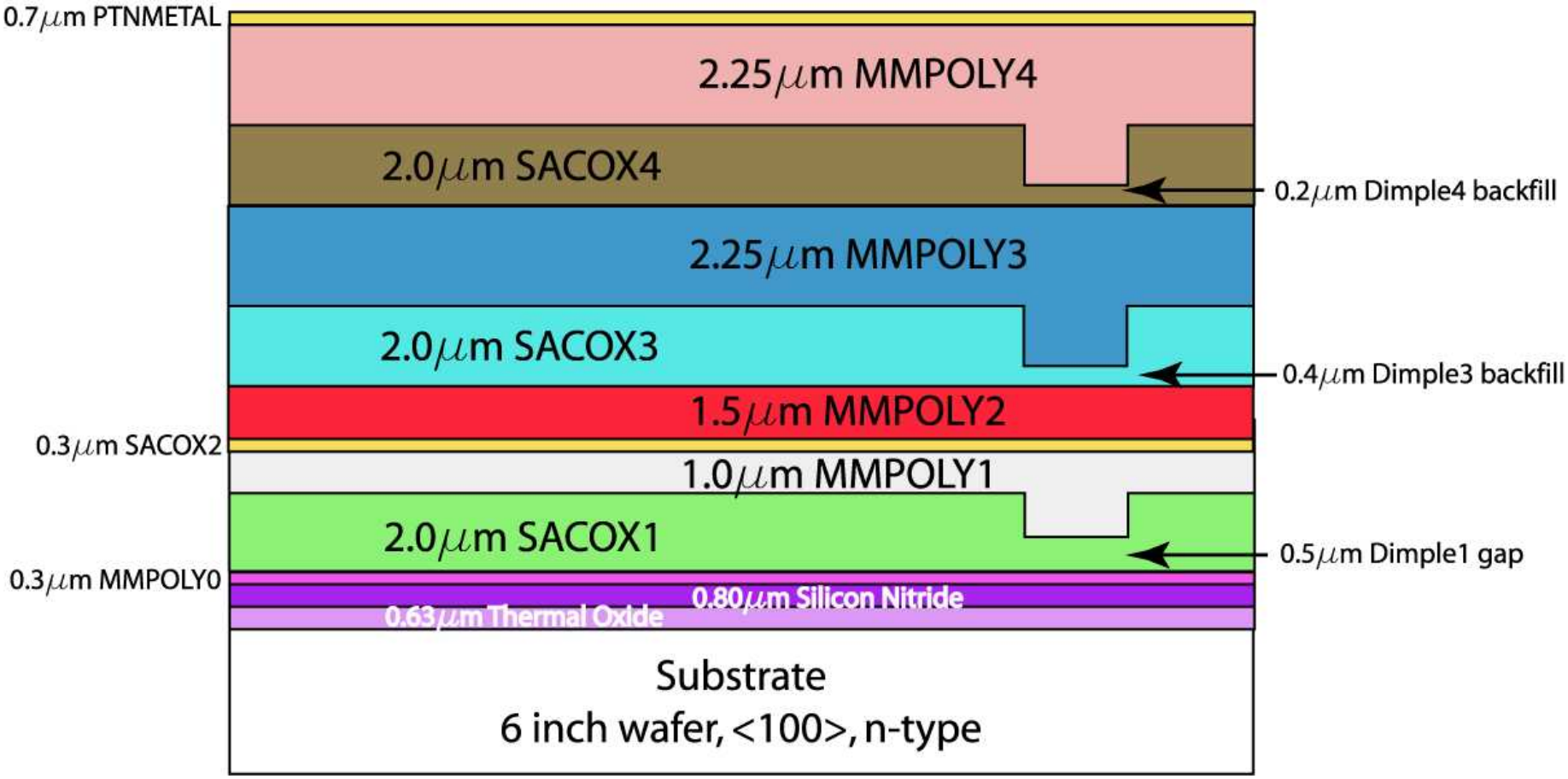
SUMMiT™ Process Layers



**** All PolySi is doped with Phosphorus ****

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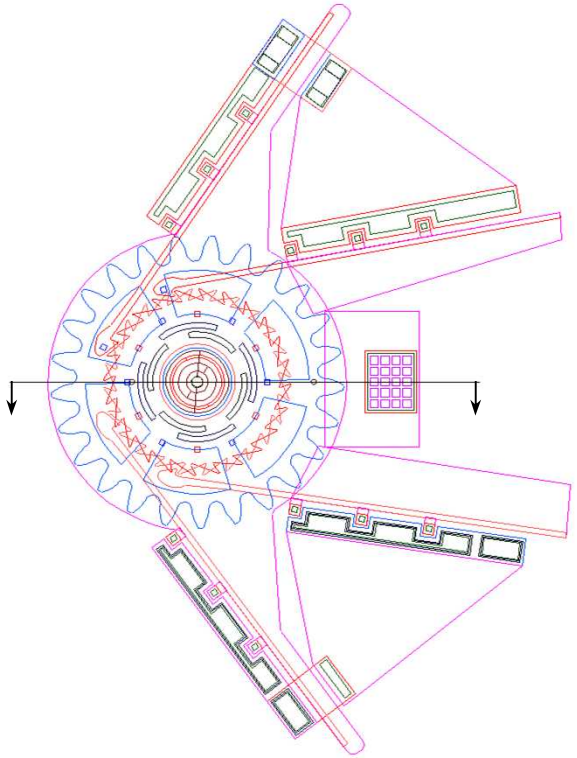
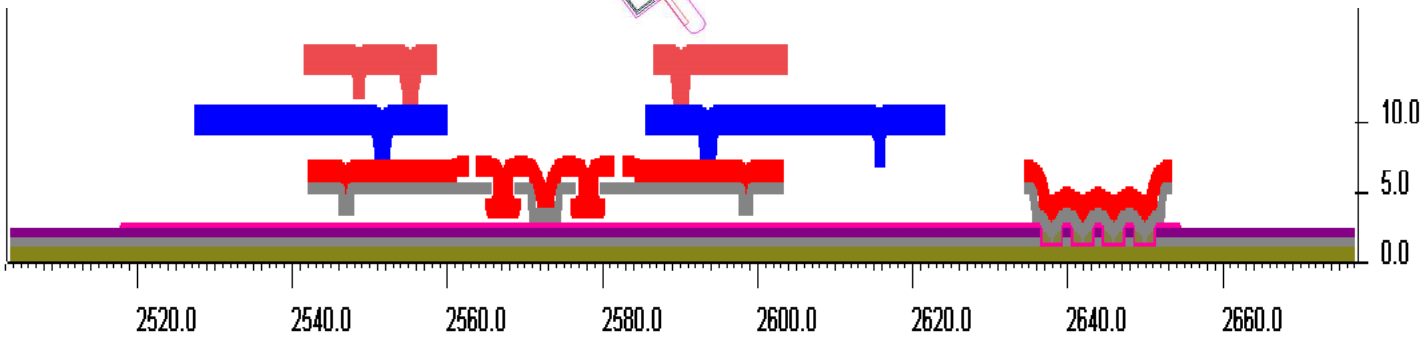
SUMMiT™ Process Cross-sections: Double Ratchet

Plan view
(AutoCad screen capture)



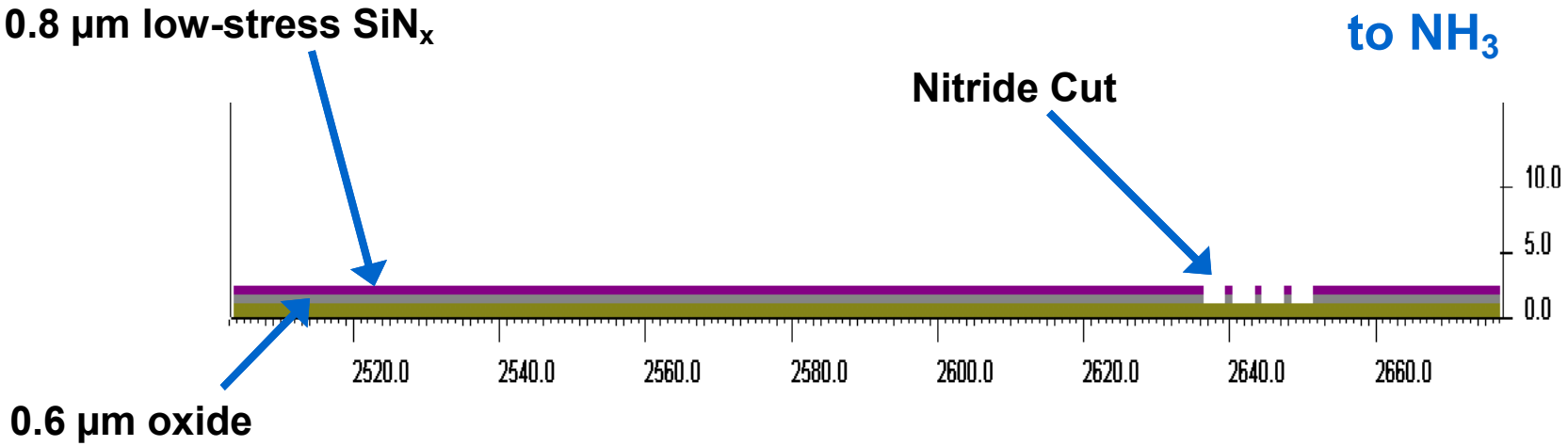
Cross-section
(Along the section line above)



SUMMiT™ Process Cross-sections: Through Nitride Cut

Purpose: Electrical isolation SiN_x — Si rich, controlled by varying $SiCl_2H_2$ to NH_3

Plan view
(AutoCad screen capture)



Cross-section
(Along the section line above)

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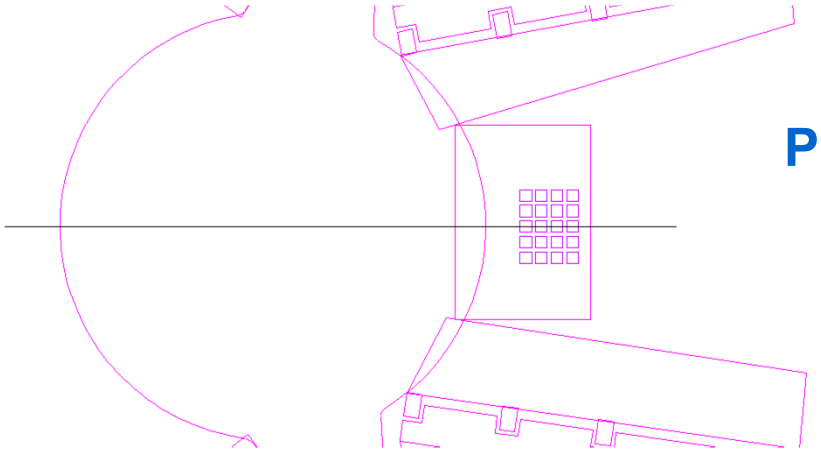
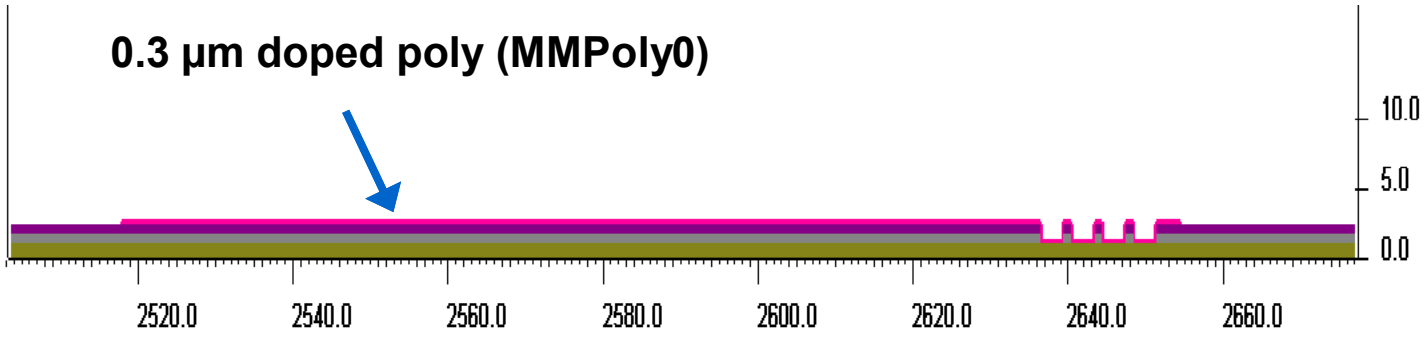
SUMMiT™ Process Cross-sections: Poly0

Plan view (AutoCad screen capture)



Purpose: Ground Plane and electrical contact to substrate

Cross-section (Along the section line above)



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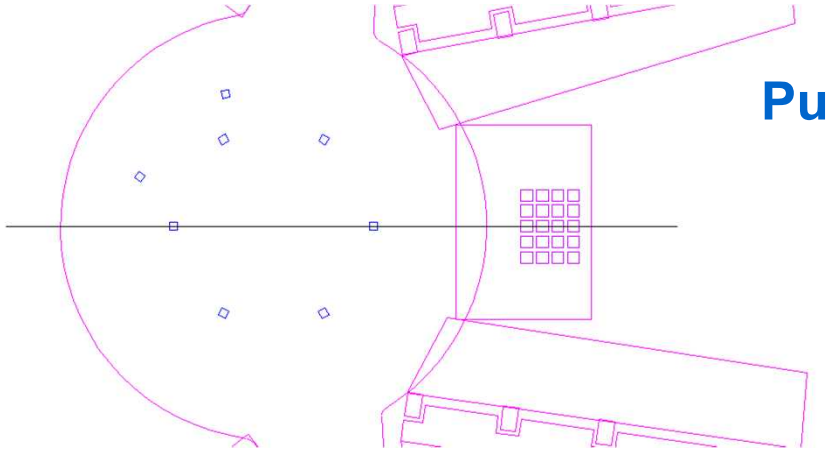
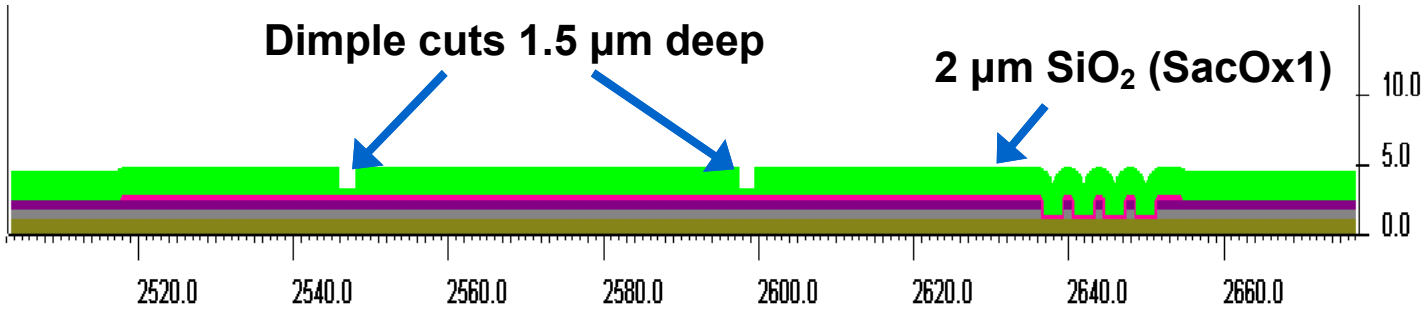
SUMMiT™ Process Cross-sections: Dimple_1 Cut

Plan view
(AutoCad screen capture)



Purpose: Dimple1 — Physical standoff to reduce adhesion

Cross-section
(Along the section line above)



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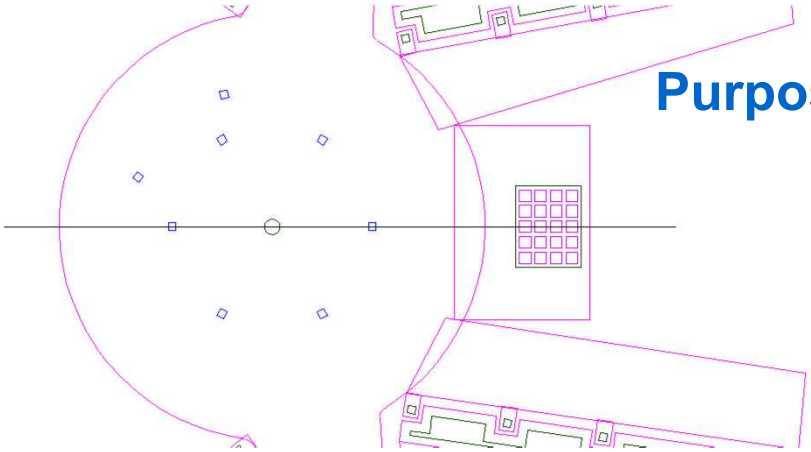
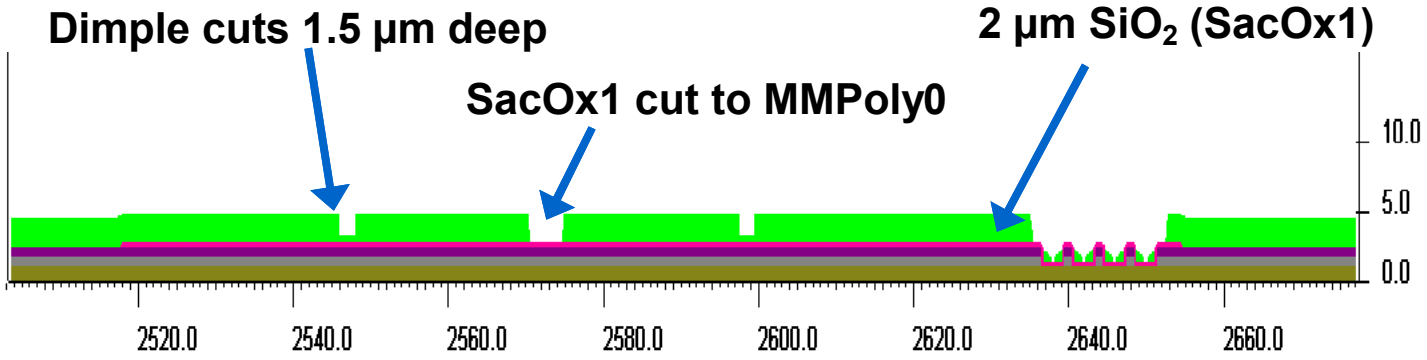
SUMMiT™ Process Cross-sections: SacOx_1 Cut

Plan view
(AutoCad screen capture)



Purpose: Sacox1 — Connects Poly0 to Poly1 deposited using TEOS — tetraethylorthosilicate

Cross-section
(Along the section line above)



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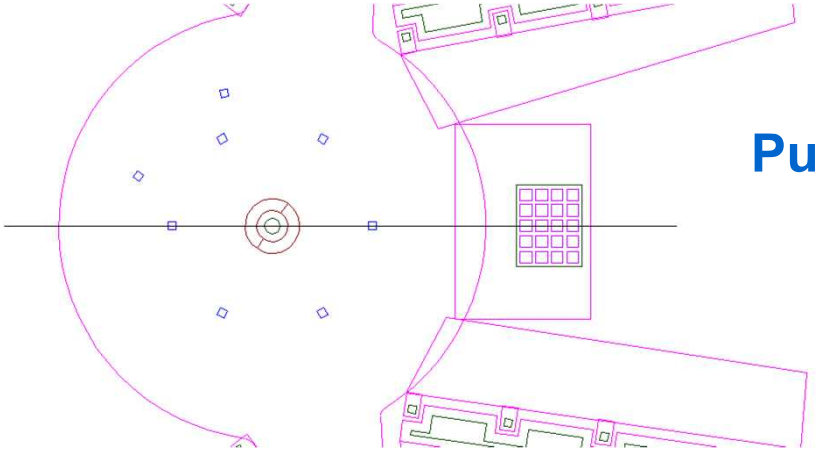
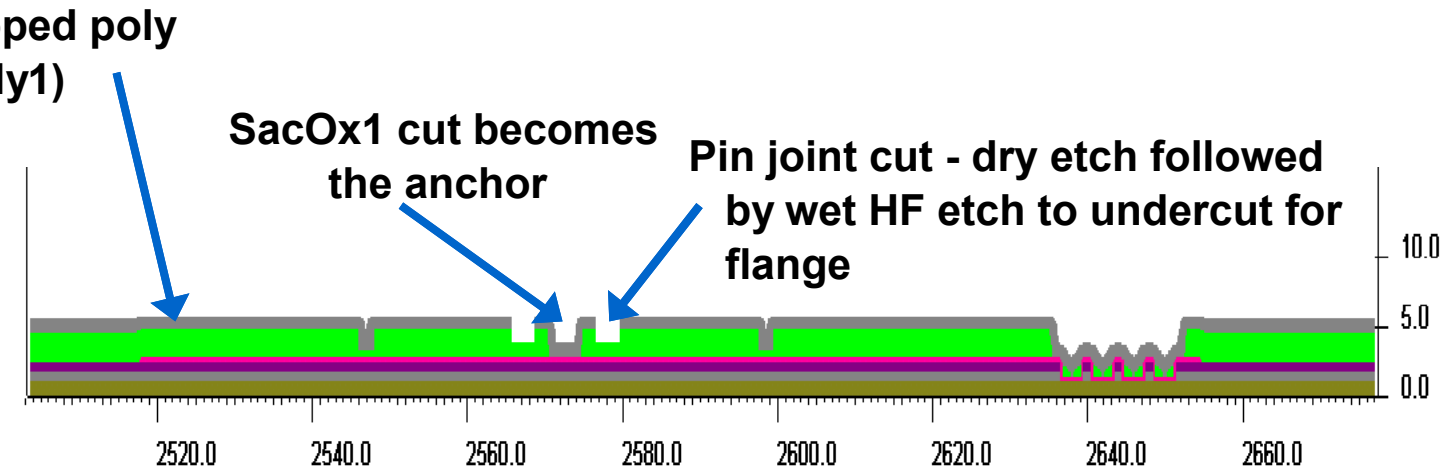
SUMMiT™ Process Cross-sections: Pin Joint Cut

Plan view
(AutoCad screen capture)



Purpose: Mechanical Si hub for gears

Cross-section
(Along the section line above)



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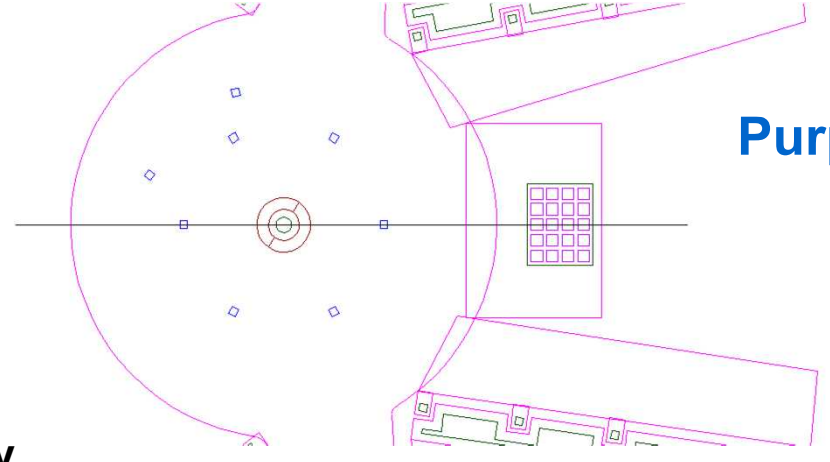
SUMMiT™ Process Cross-sections: Poly1

Plan view
(AutoCad screen capture)

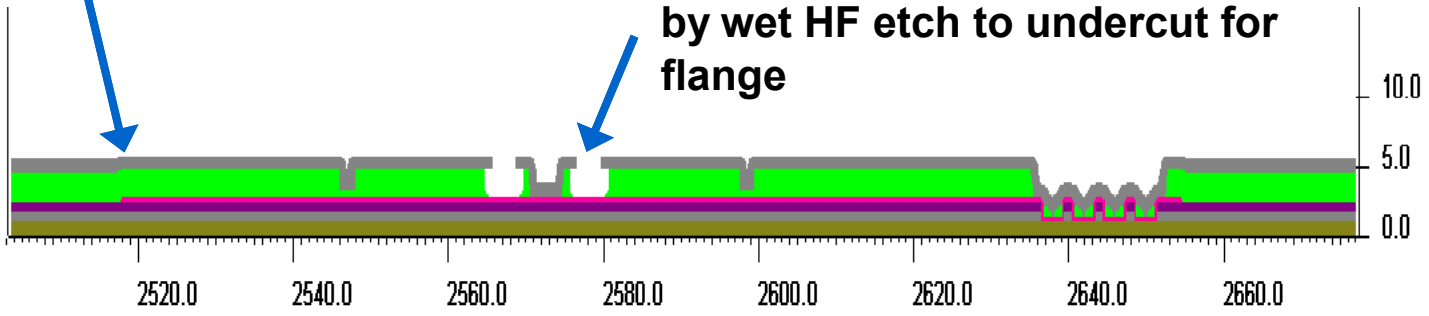


Purpose: Mechanical Si hub for gears

1 µm doped poly (MMPoly1)

Pin joint cut - dry etch followed by wet HF etch to undercut for flange

Cross-section
(Along the section line above)



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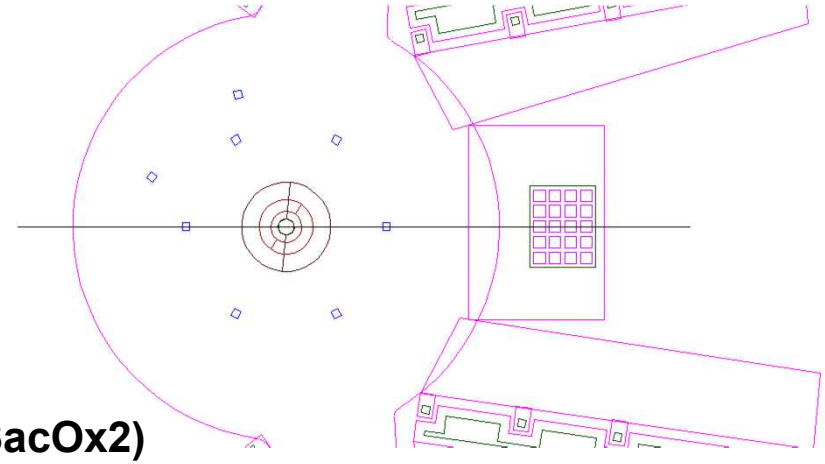
SUMMiT™ Process Cross-sections: SacOx2 Cut

Plan view
(AutoCad screen capture)



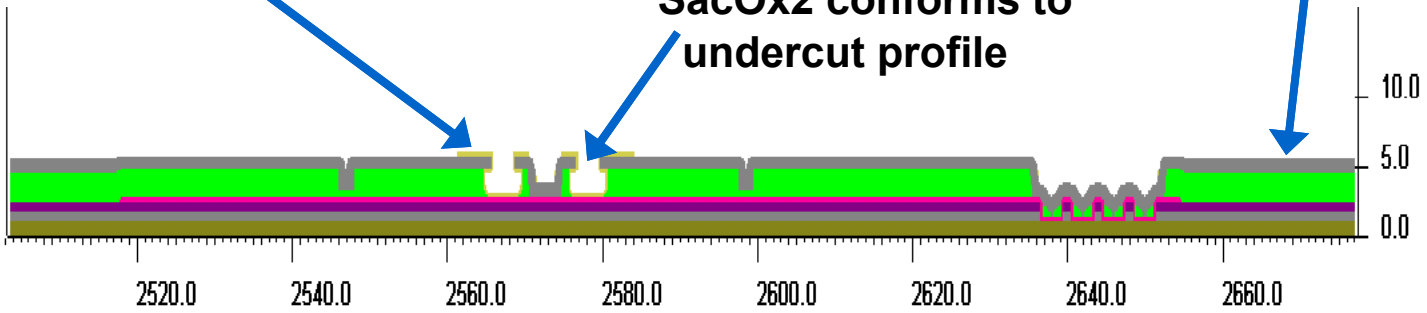
Purpose: Hub clearance

0.3 µm TEOS (SacOx2)

1 µm doped poly (MMPoly1)

SacOx2 conforms to undercut profile

Cross-section
(Along the section line above)



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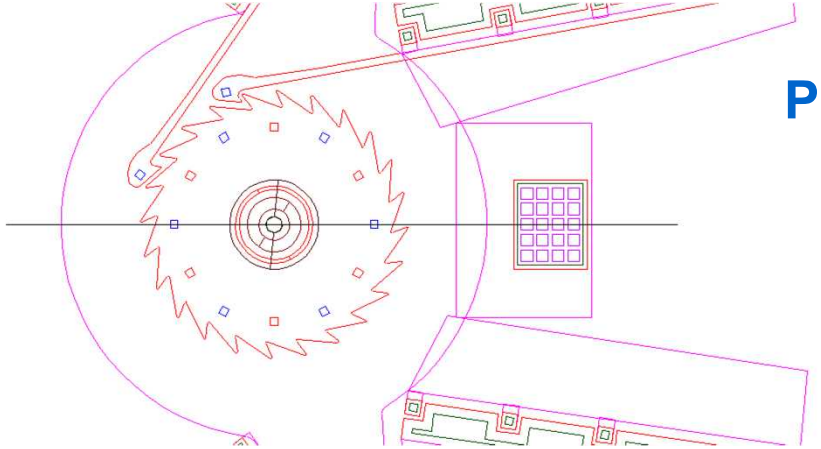
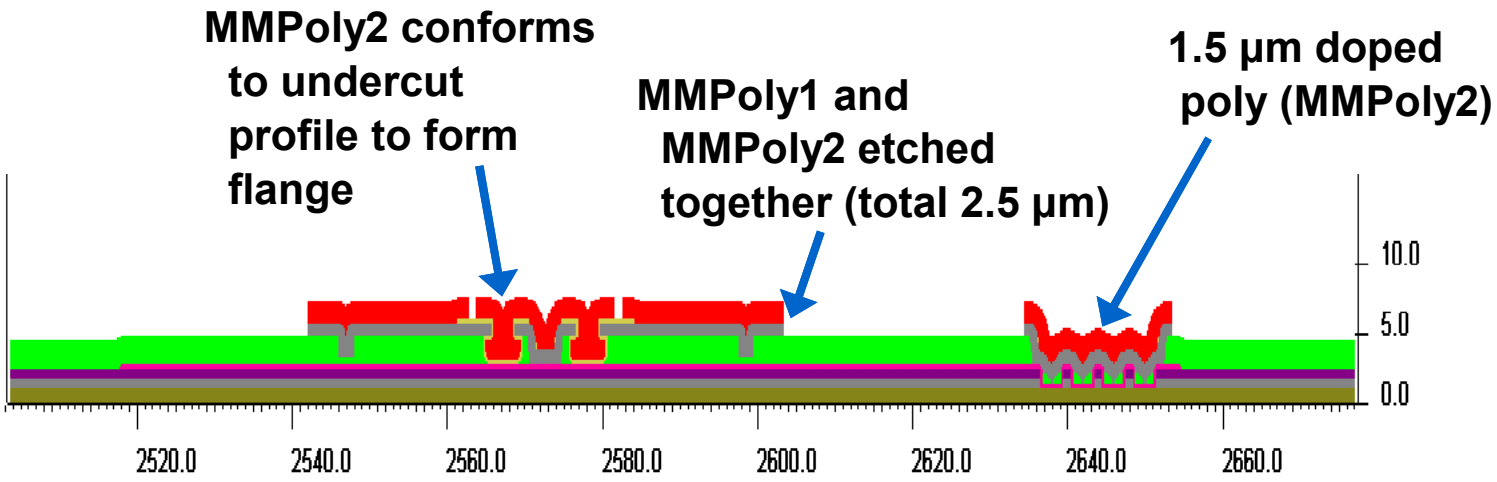
SUMMiT™ Process Cross-sections: Poly2

Plan view
(AutoCad screen capture)



Purpose: Mechanical Si #2 solid hubs and pin joints

Cross-section
(Along the section line above)



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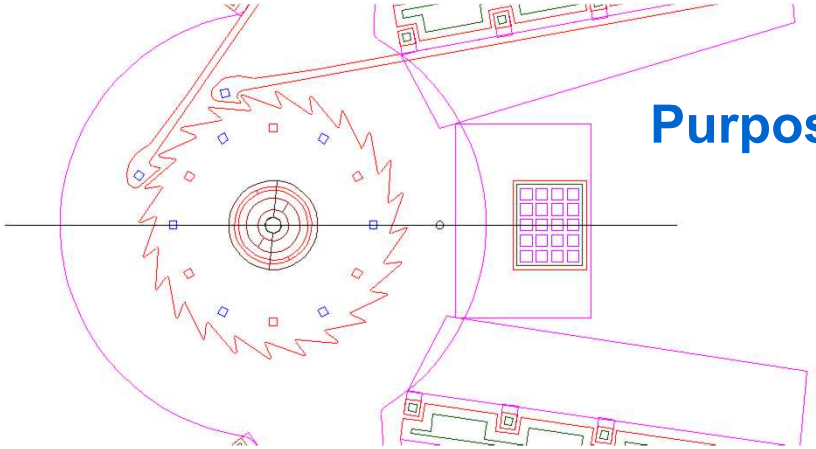
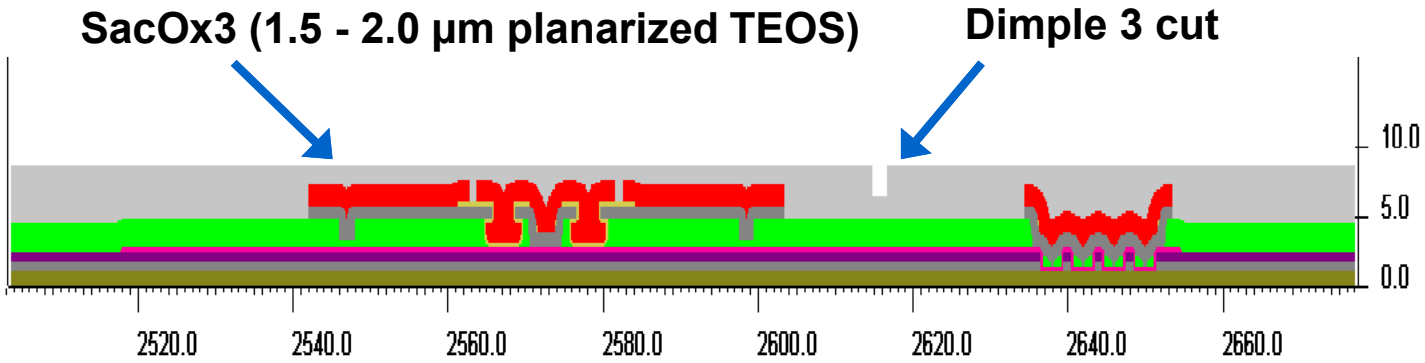
SUMMiT™ Process Cross-sections: Dimple3_Cut

Plan view
(AutoCad screen capture)



Purpose: Dimple3 — Physical standoff to reduce adhesion

Cross-section
(Along the section line above)



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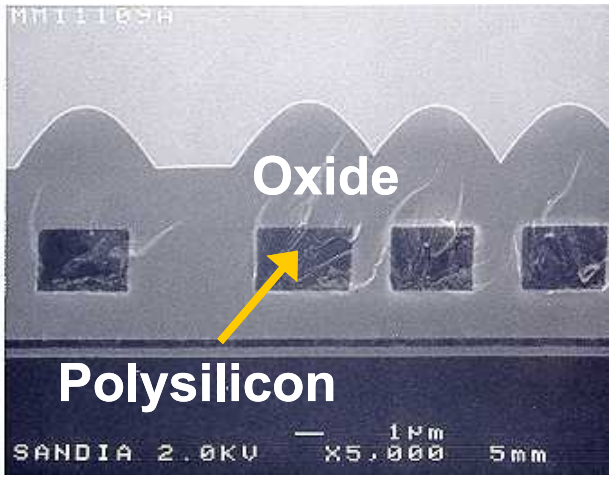
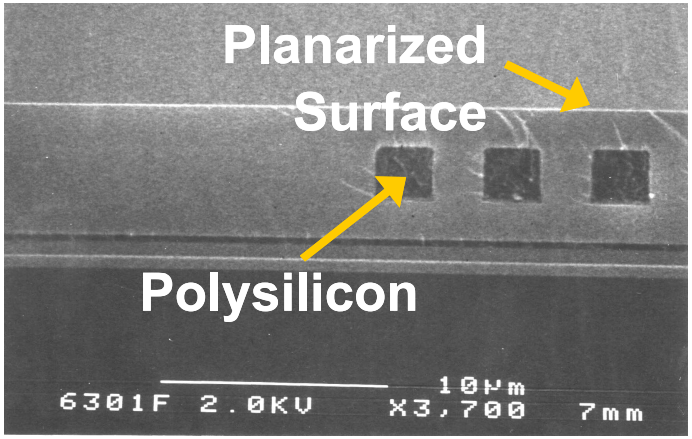
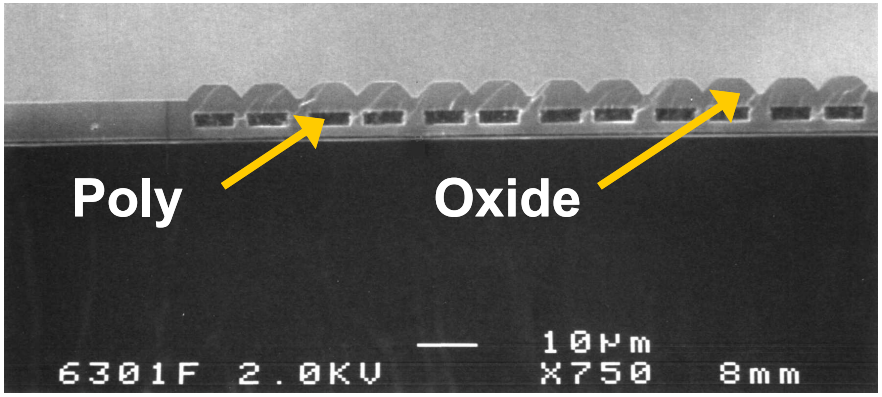
Chemical Mechanical Polishing (CMP)

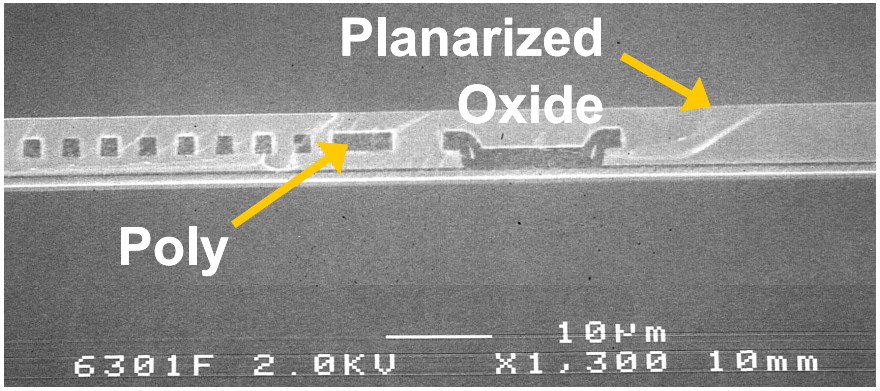
Pre CMP



Post CMP







Complex structures can be built using CMP

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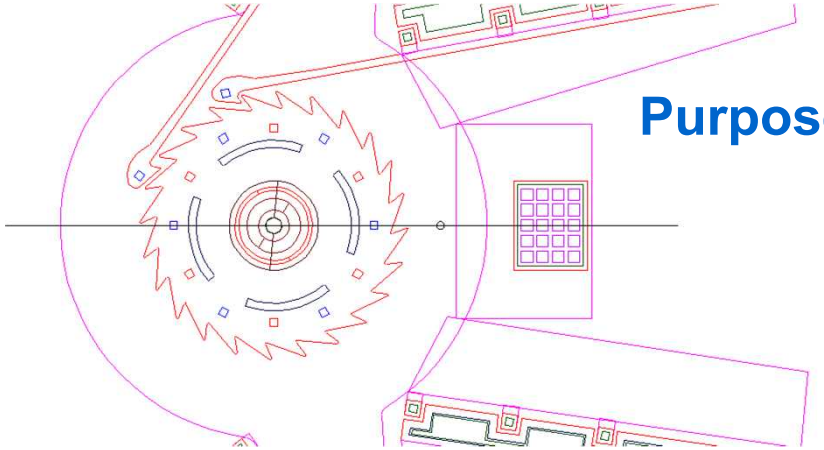
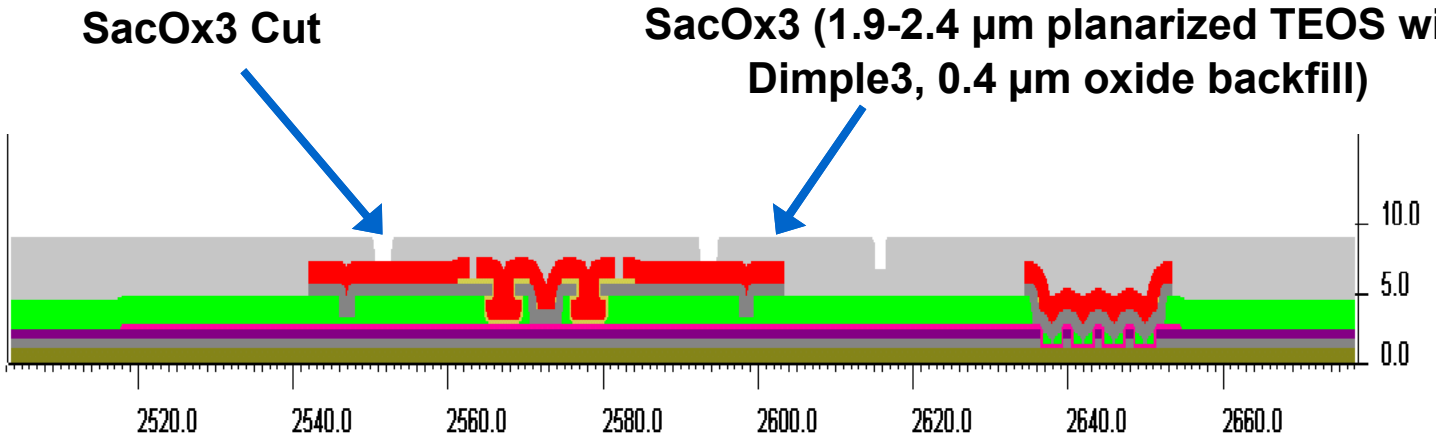
SUMMiT™ Process Cross-sections: SacOx3 Cut

Plan view
(AutoCad screen capture)



Purpose: Sacox3 — Connects Poly3 to Poly2

Cross-section
(Along the section line above)



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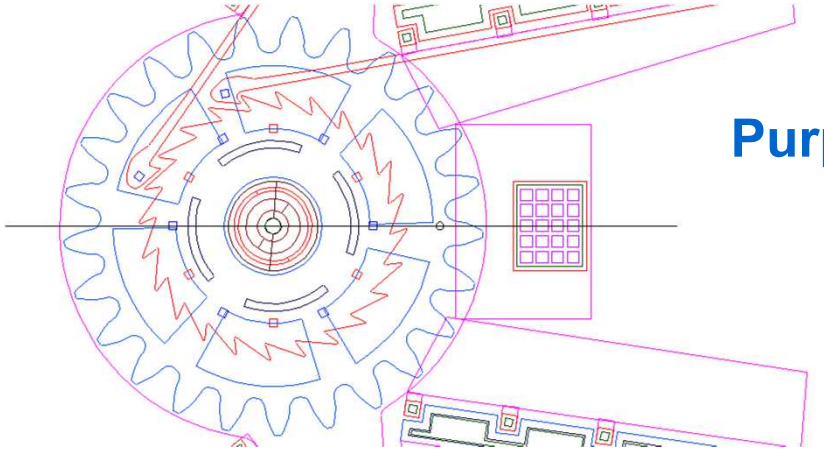
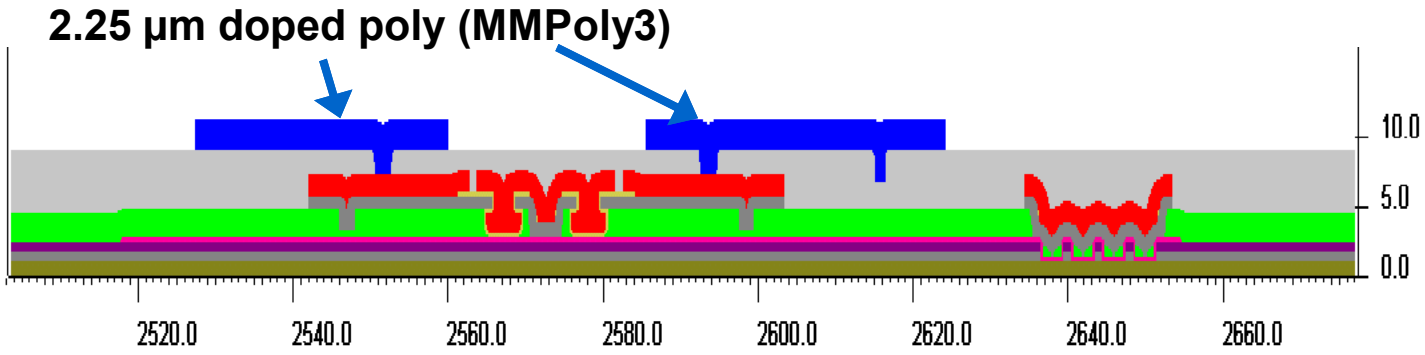
SUMMiT™ Process Cross-sections: Poly3 Cut

Plan view
(AutoCad screen capture)



Purpose: Mechanical Si #3 interlinking element

Cross-section
(Along the section line above)



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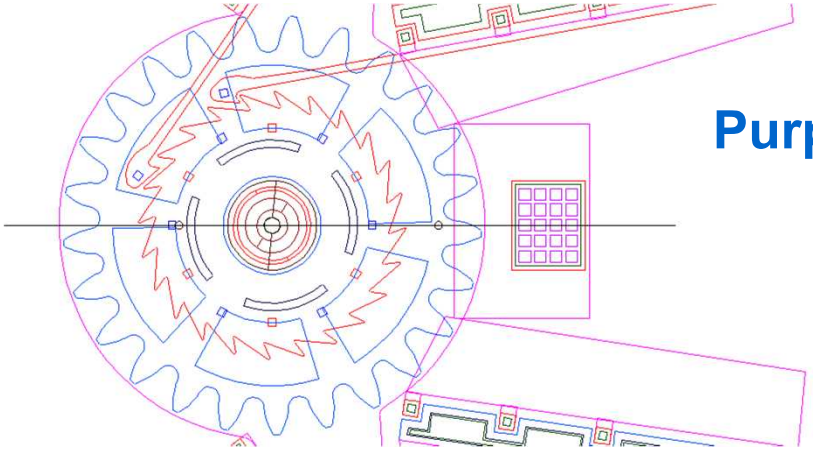
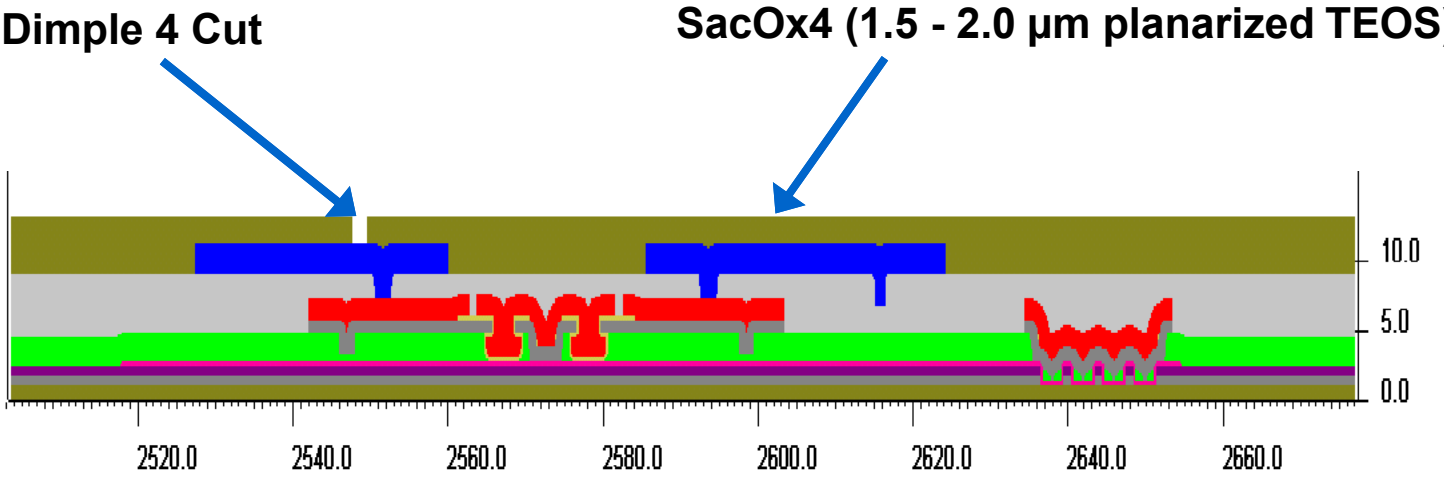
SUMMiT™ Process Cross-sections: Dimple4 Cut

Plan view
(AutoCad screen capture)



Purpose: Dimple4 — Physical standoff to reduce adhesion

Cross-section
(Along the section line above)



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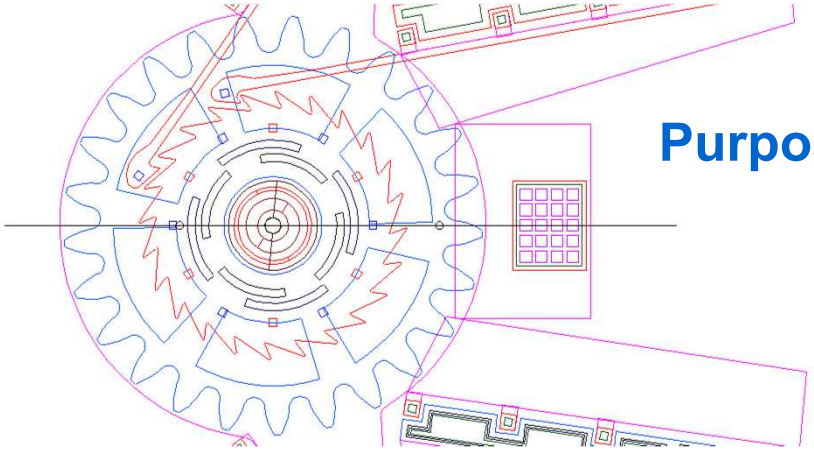
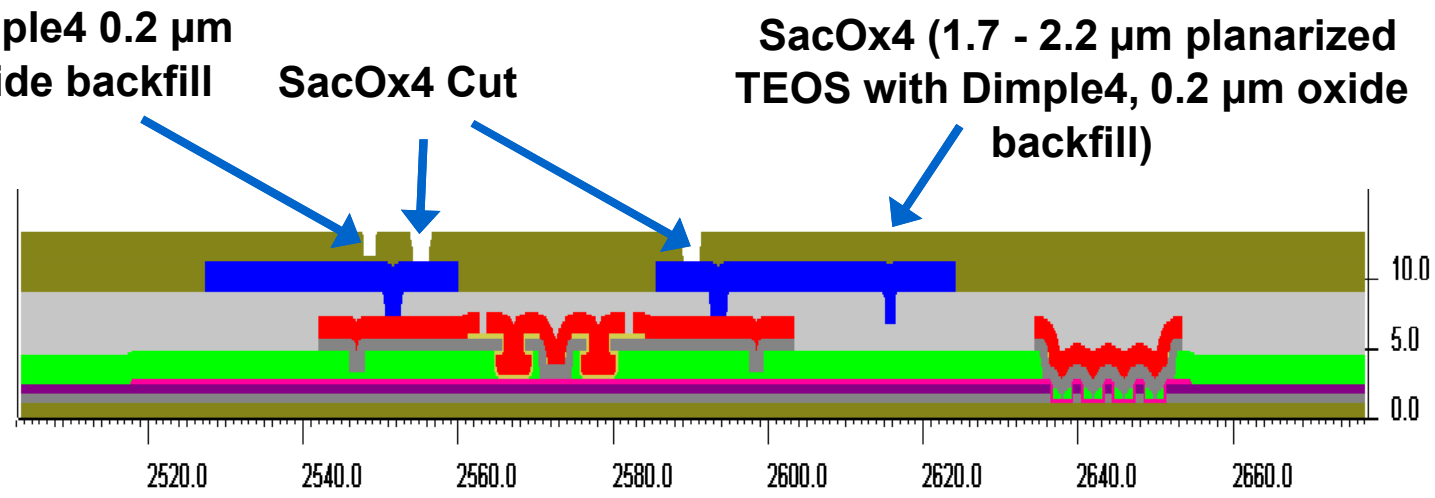
SUMMiT™ Process Cross-sections: SacOx4 Cut

Plan view
(AutoCad screen capture)



Purpose: Sacox4 — Connects Poly4 to Poly3

Cross-section
(Along the section line above)



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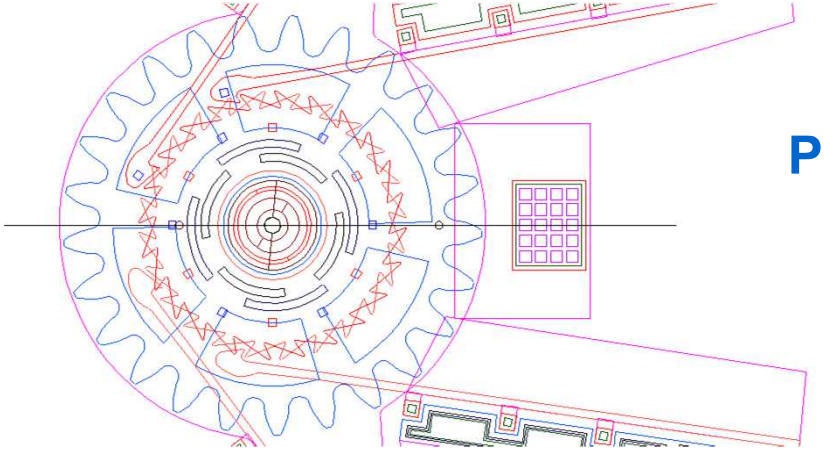
SUMMiT™ Process Cross-sections: Poly4 Cut

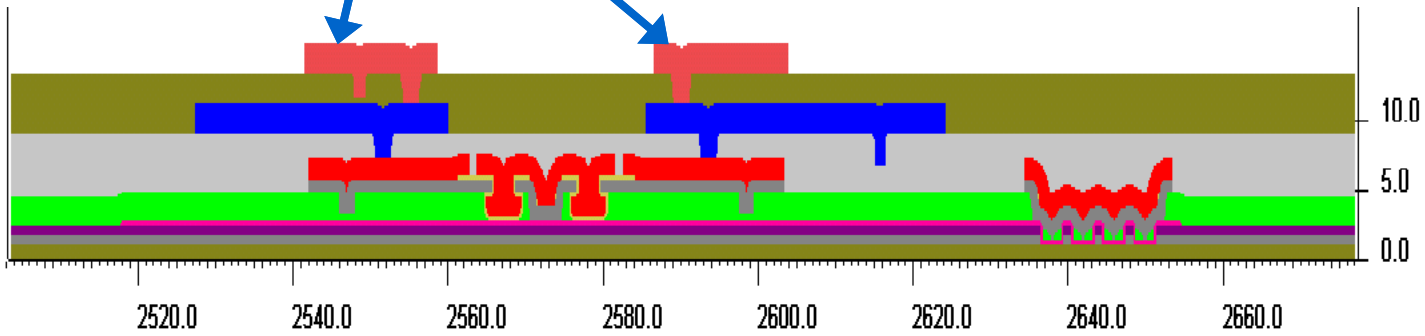
Plan view
(AutoCad screen capture)



Purpose: Mechanical Si #4

2.25 µm doped poly (MMPoly4)

Cross-section
(Along the section line above)



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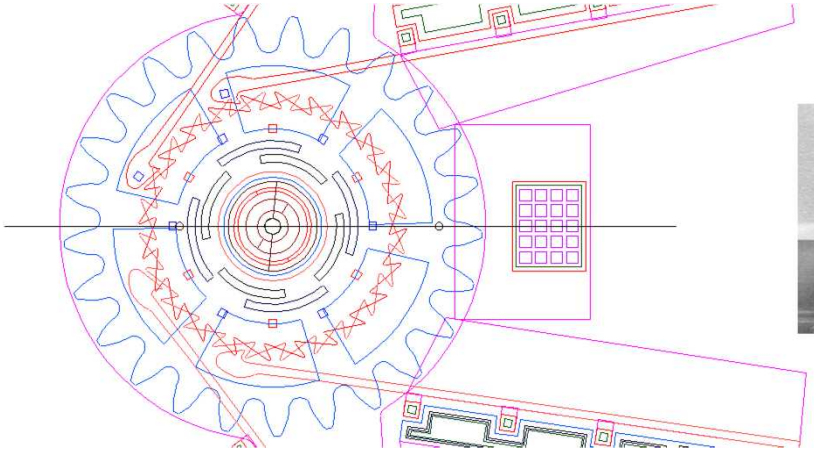
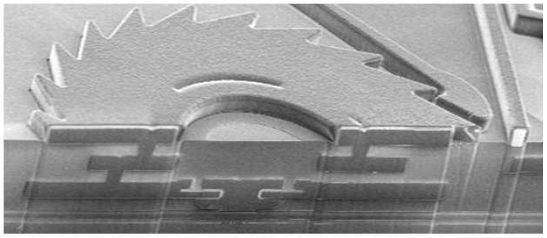
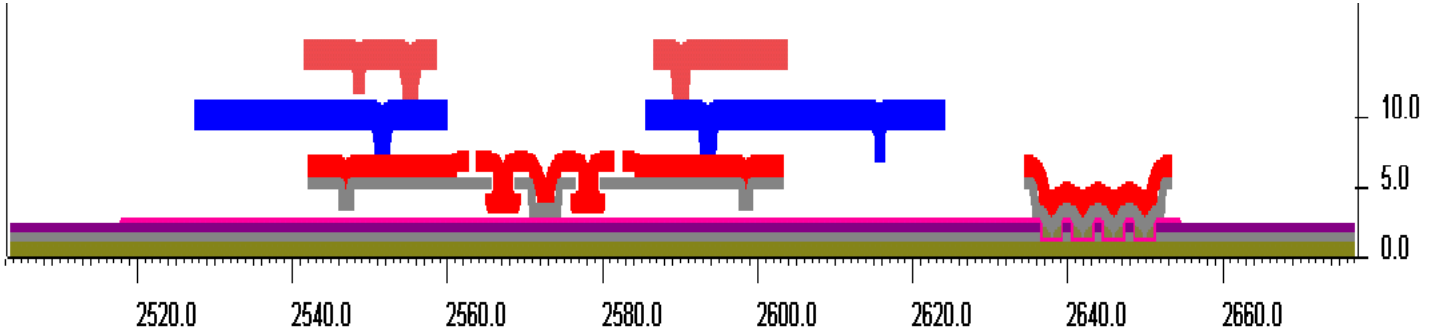
SUMMiT™ Process Cross-sections: Released Structure (Double Ratchet)

SEM perspective view of fabricated device





FIB cross-section of fabricated device



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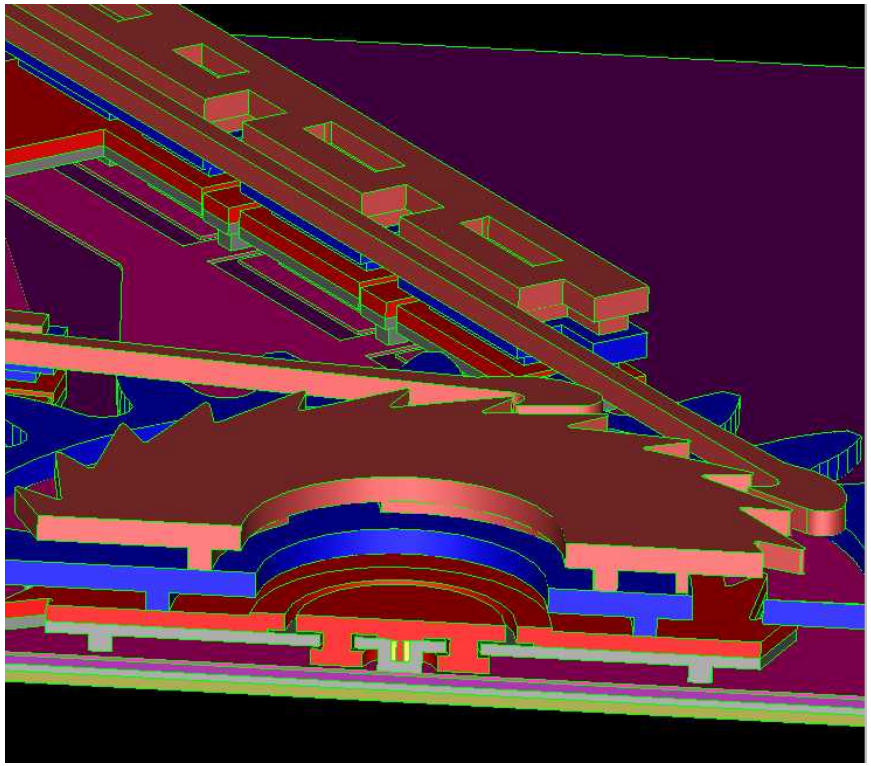
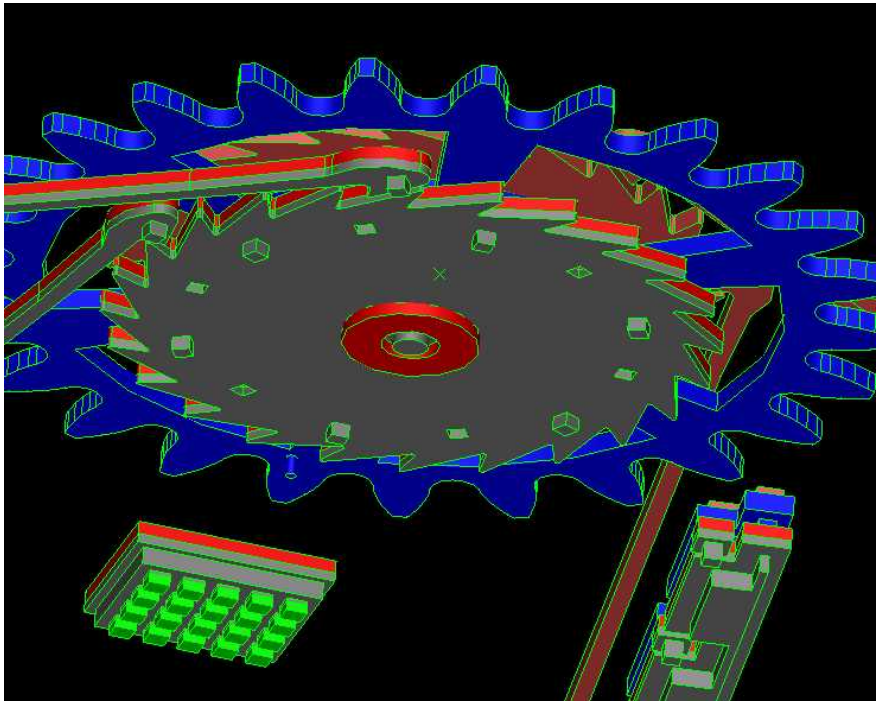
SUMMiT V™ Process Cross-sections: Double Ratchet





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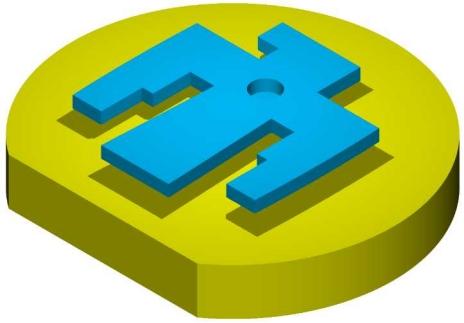
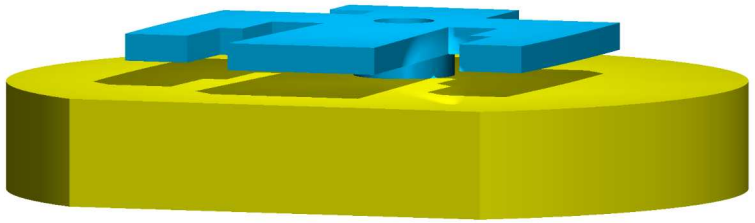
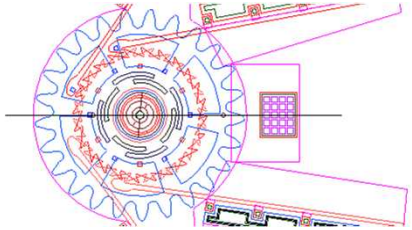
Conclusion

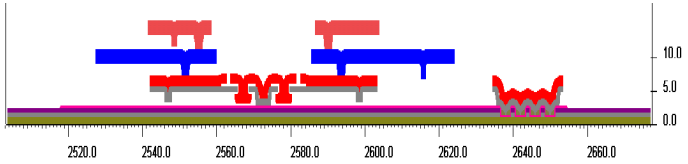
- **SUMMiT™ Process — Five Mechanical Layers Allow Realization of Complex MEMS Structures**





- **Process Layers – Understanding SUMMiT™ Stack is Key to Successful Design Implementation**





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