SAND2007-5301C

Top gated accumulation mode Si MOS quantum devices and oxide charge induced 2DEGs

Wisconsin Silicon Focus Workshop

Eric Nordberg

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Sandia National Laboratories

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- Goal:
  - Gated Quantum Dot in a Silicon/Silicon Dioxide Inversion Layer

- This Talk:
  - Fabrication Process of QD Formation
  - Results and Consequences of oxide charge induced 2DEG
  - Temperature Dependence of Poly-silicon Conduction

Process Flow

- Silicon Wafer
- Gate Oxide Grown
- Source-Drain Lines Implanted
- Poly-silicon Deposited, Doped, and Patterned
- Contacts and Vias Formed
- Second Poly-silicon Lithography
- Second Oxide Deposition (ALD)
- Top Gate Deposition

High Resistivity Silicon Wafer

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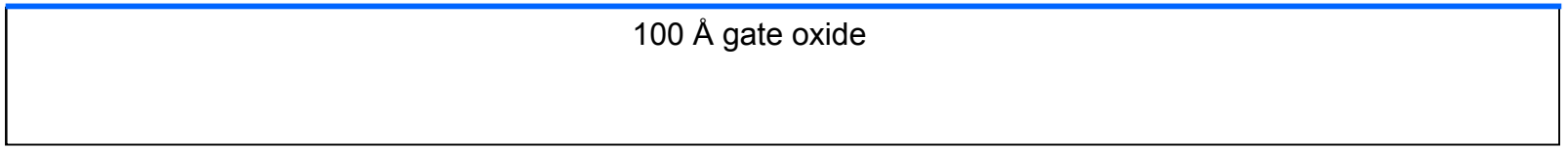

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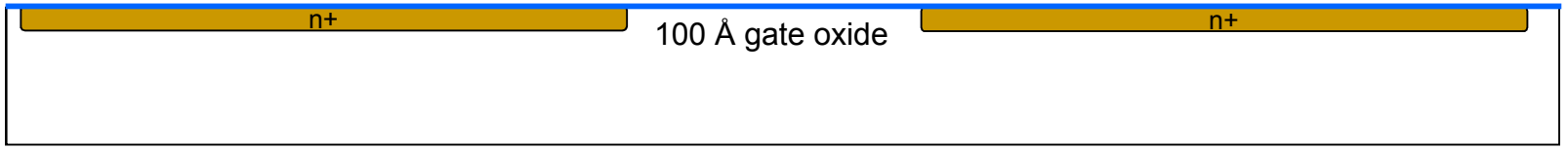

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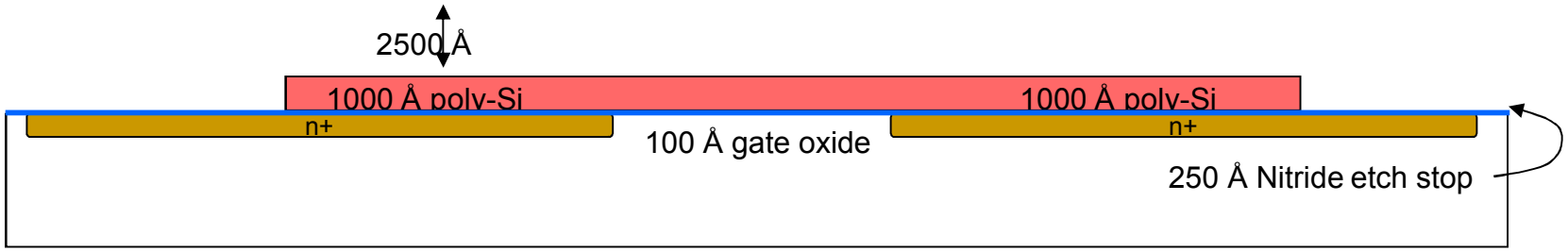

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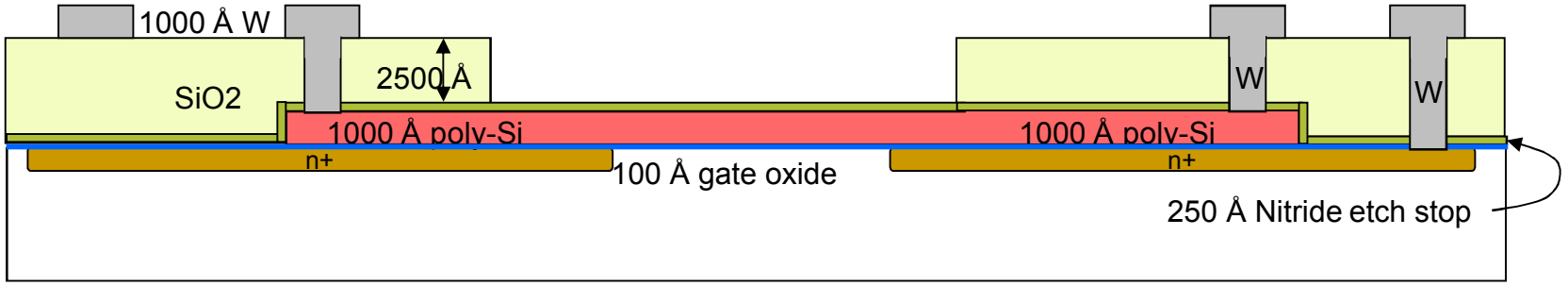

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Si Fab Stop – Front-End

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Back-End Fabrication

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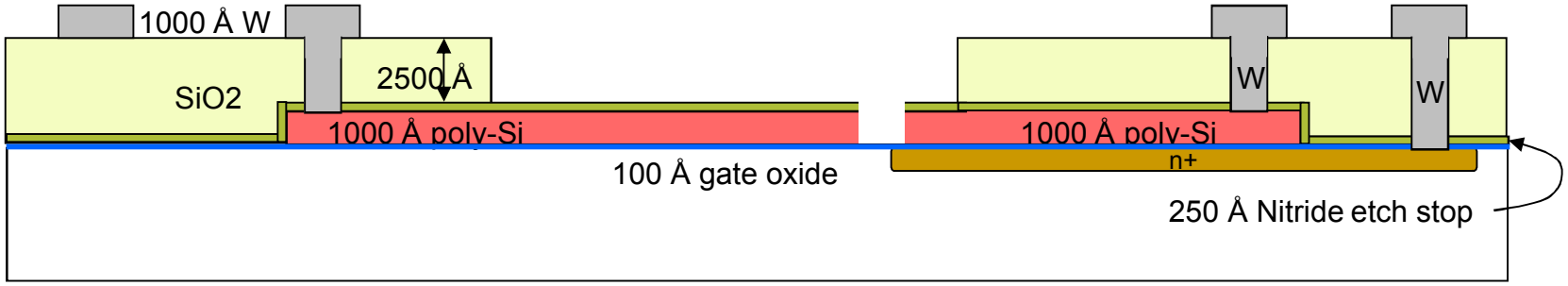

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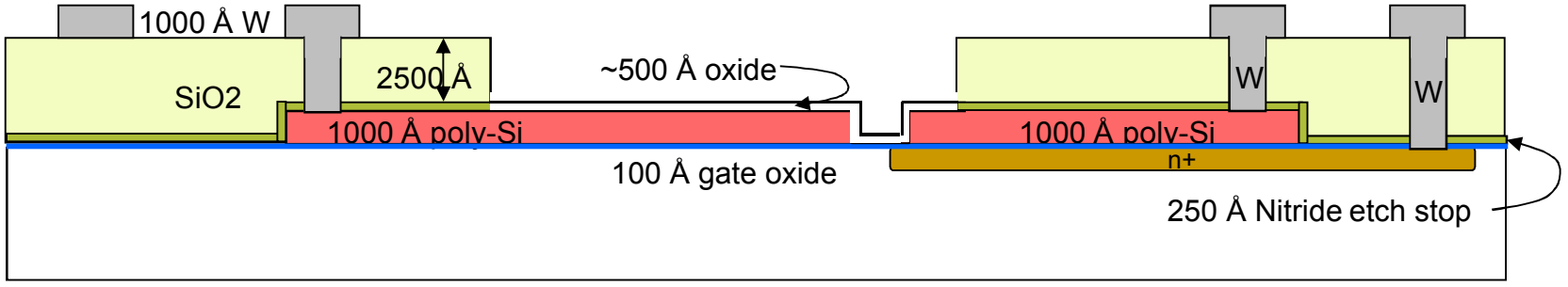

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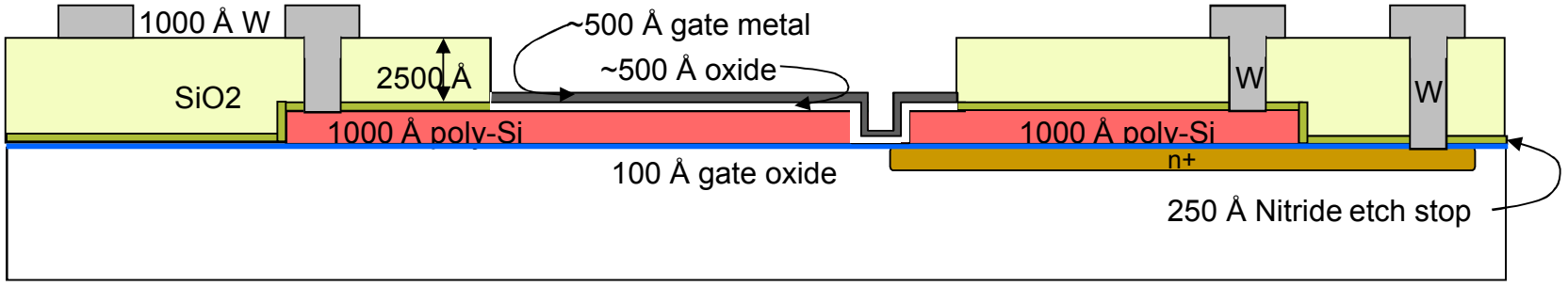
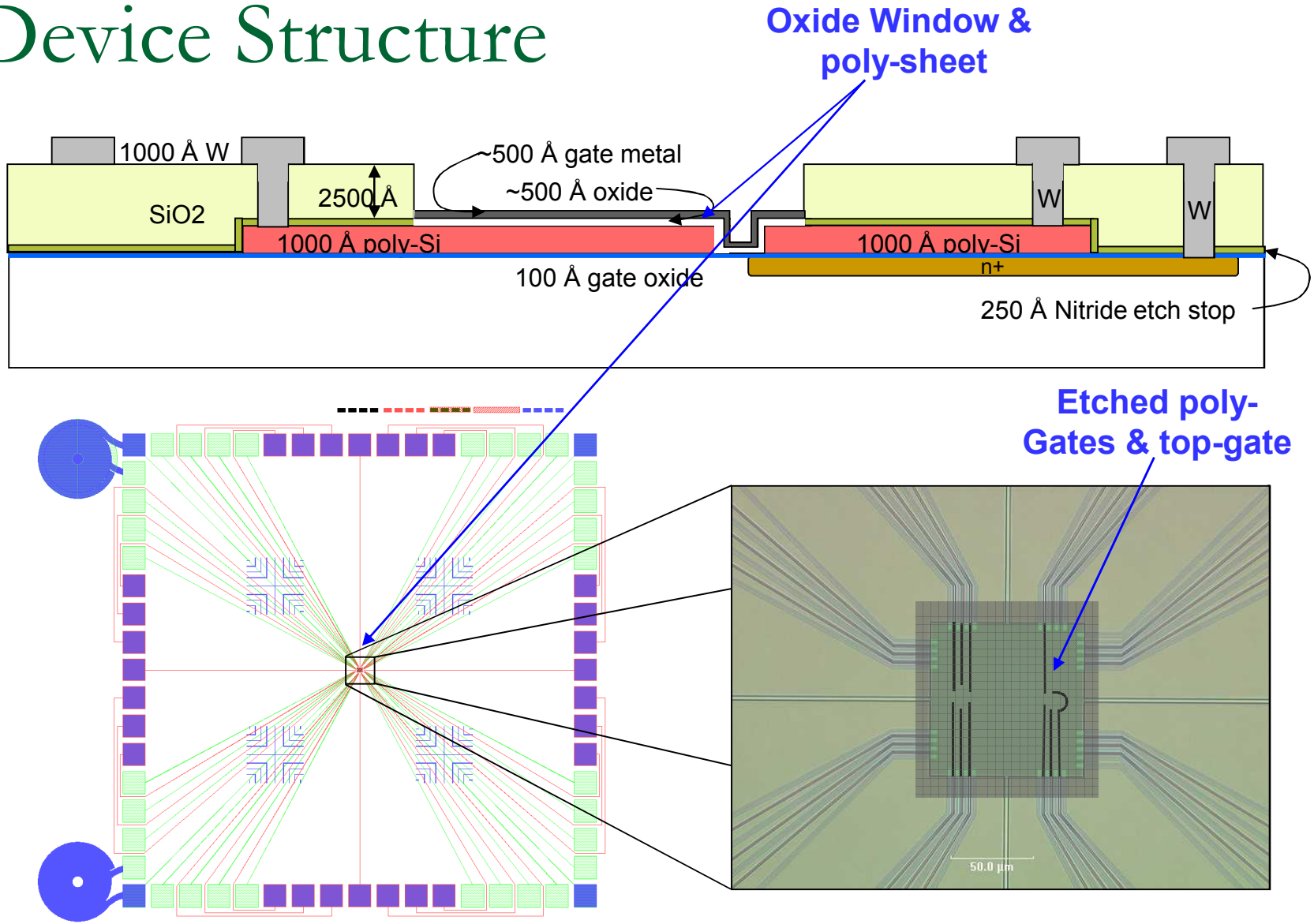
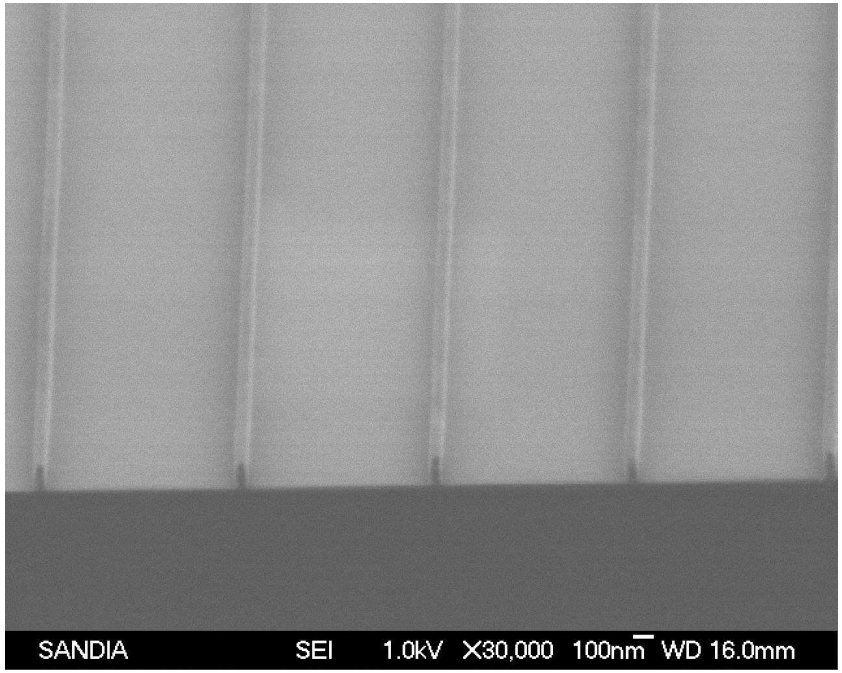
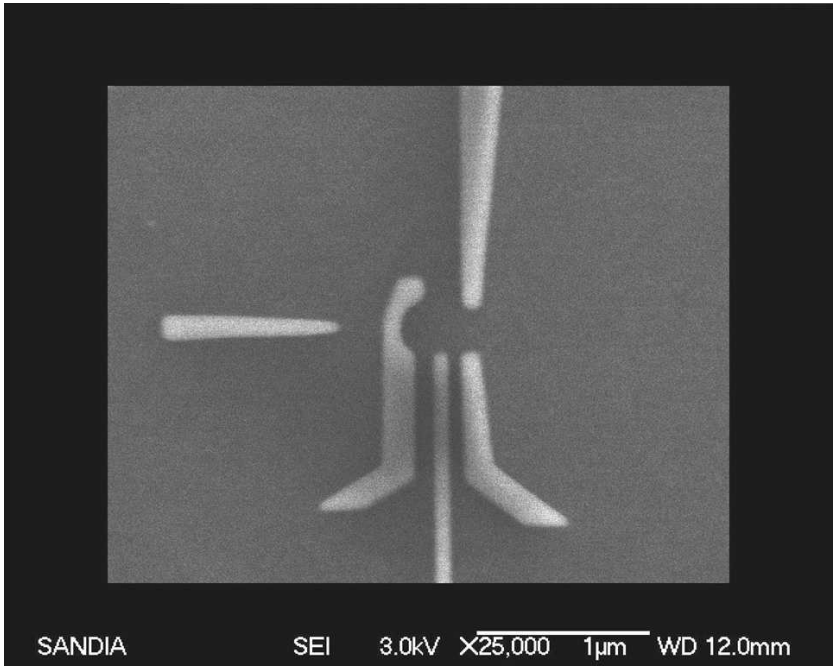


Device Structure



High Selectivity Poly-silicon Etch

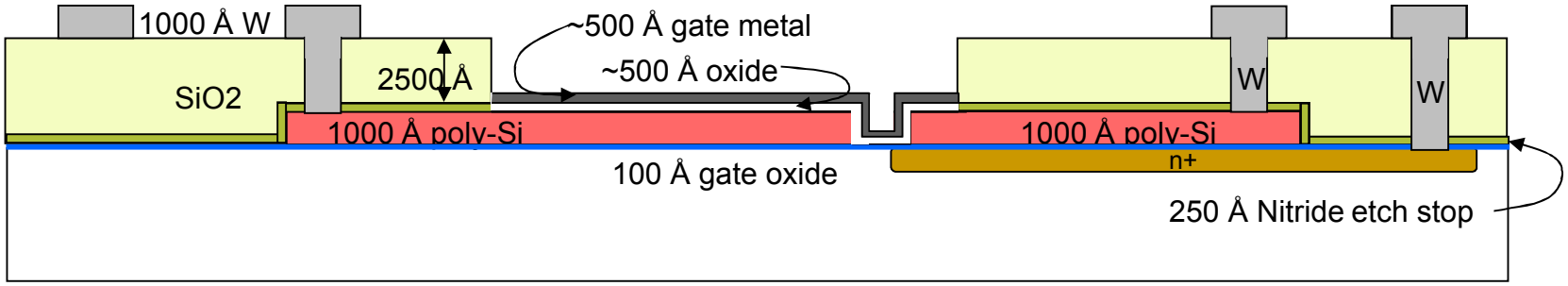




- Depletion gate lay-out follows previously published approaches
- Target poly-Si lines/spaces as small as possible
- Poly-silicon etch done outside Si fab because of need for e-beam lithography (EBL)
- Initial etch development is promising (i.e., 50 nm lines / ~15A oxide loss)

Additional Post Processing

- Atomic Layer Deposition
  - Low temperature deposition (~400°C) minimizes impact on metal contacts and dopant diffusion
  - High quality oxide compared to other oxide deposition techniques – smaller trapped charge, fewer pinholes
- Aluminum Sputter and Liftoff
  - Hypothesis: better than available e-beam, PECVD & thermal deposition capabilities for exposed gate oxide



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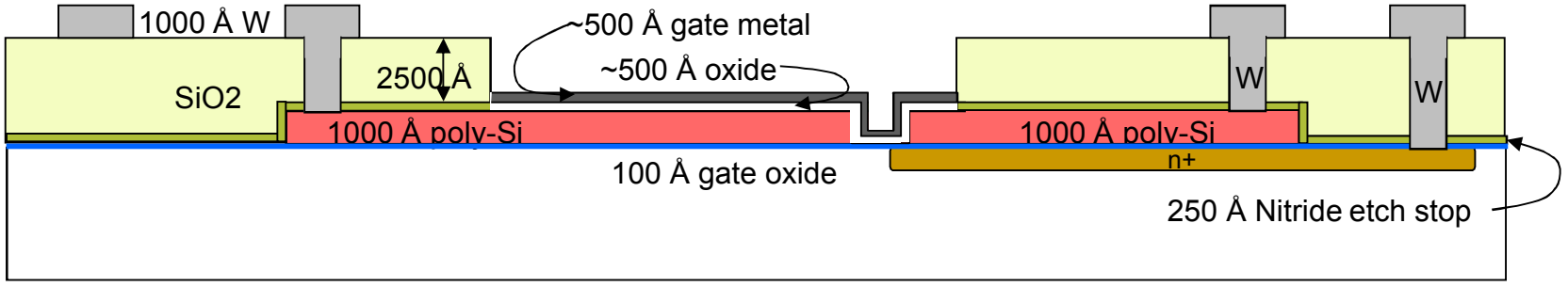
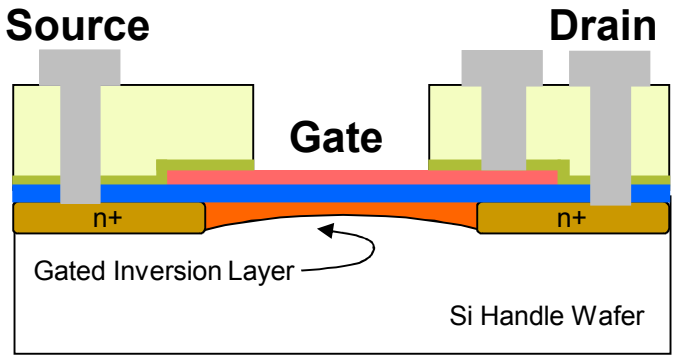
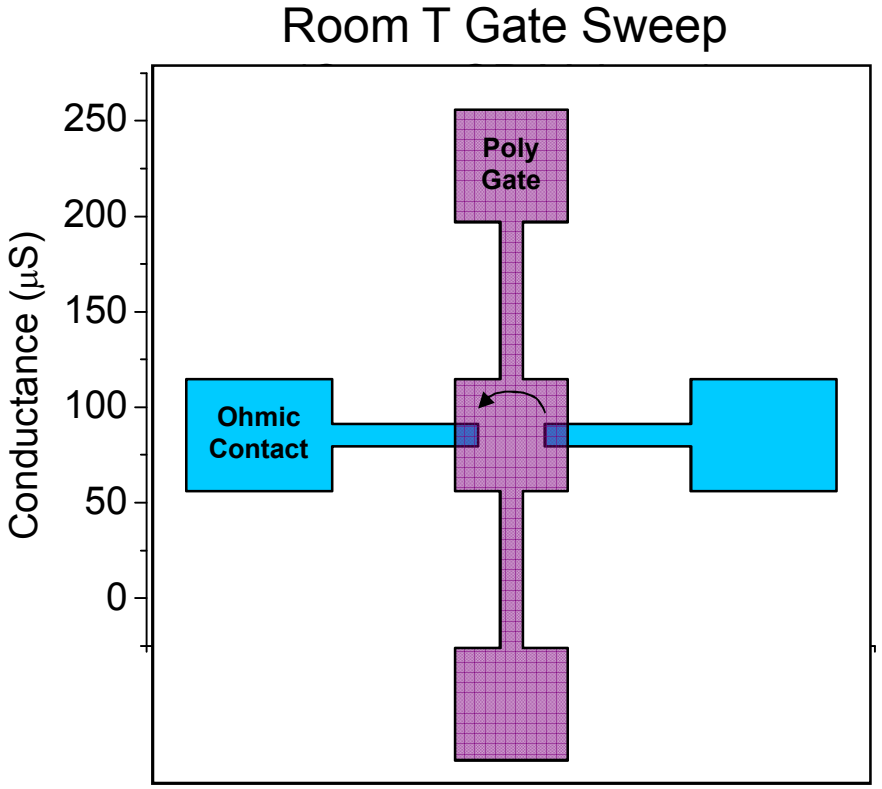


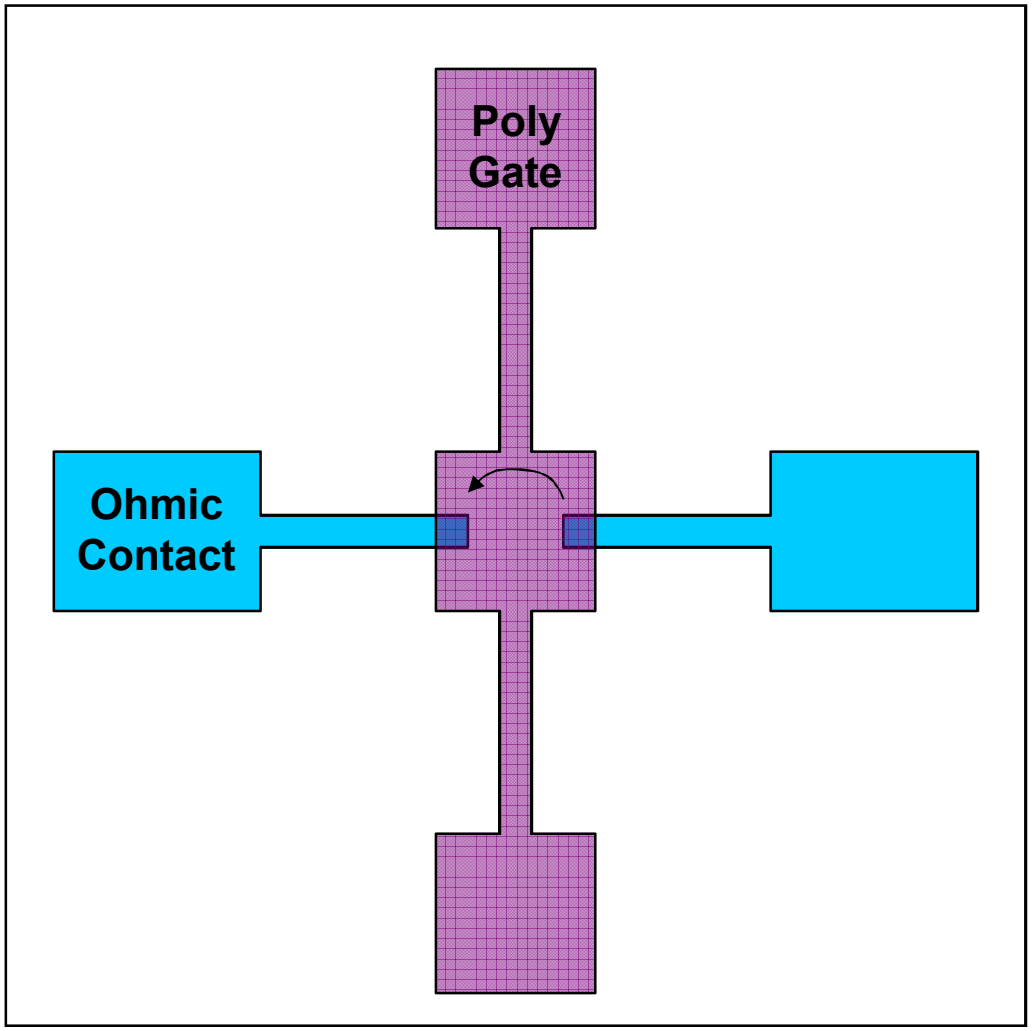
Gate Control





- Zero bias S/D conductance higher than expected for high resistivity wafer
- Minimal conductance variation with increasing V_g
- Current pinched-off w/ negative bias

Geometric Dependence



- For ideal FET, conduction only occurs under the poly-silicon
- Conduction actually occurs everywhere
- Gating depletes only under the poly-silicon limiting possible conduction paths

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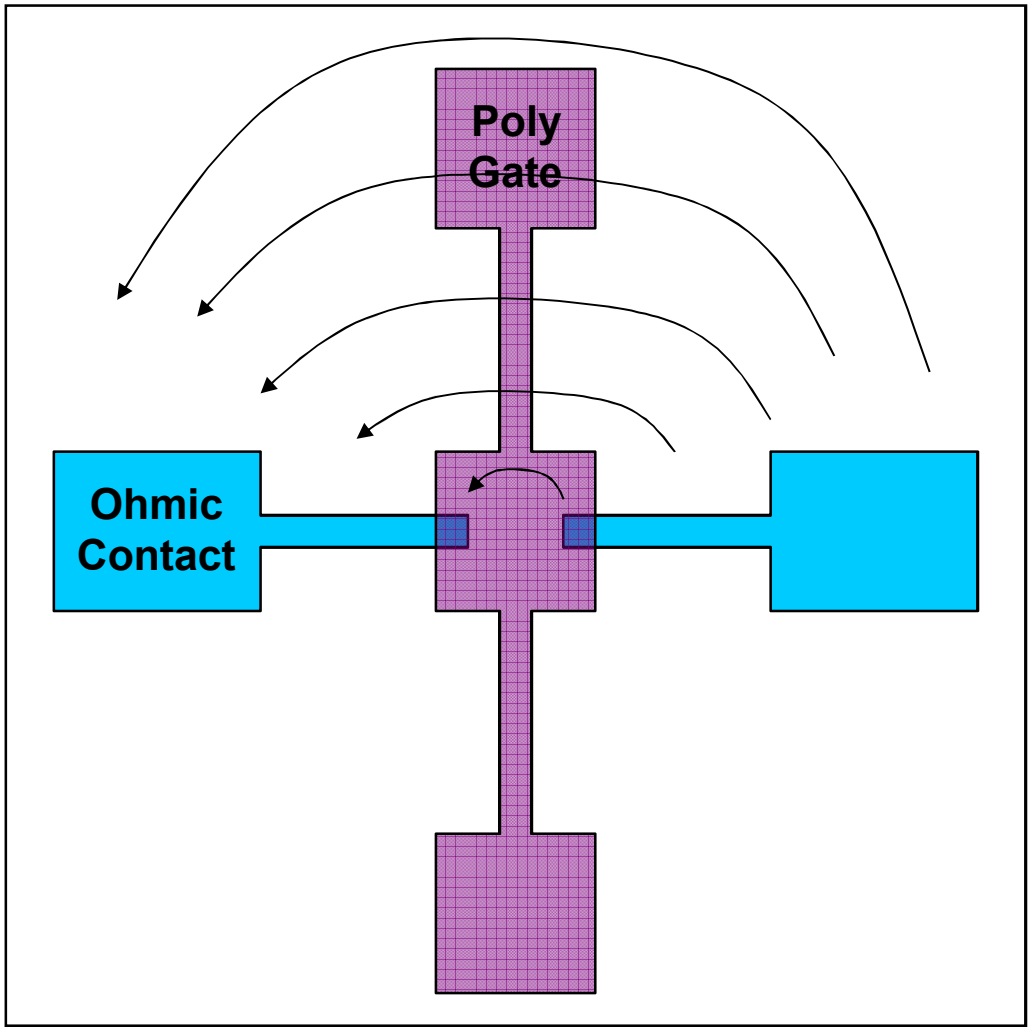

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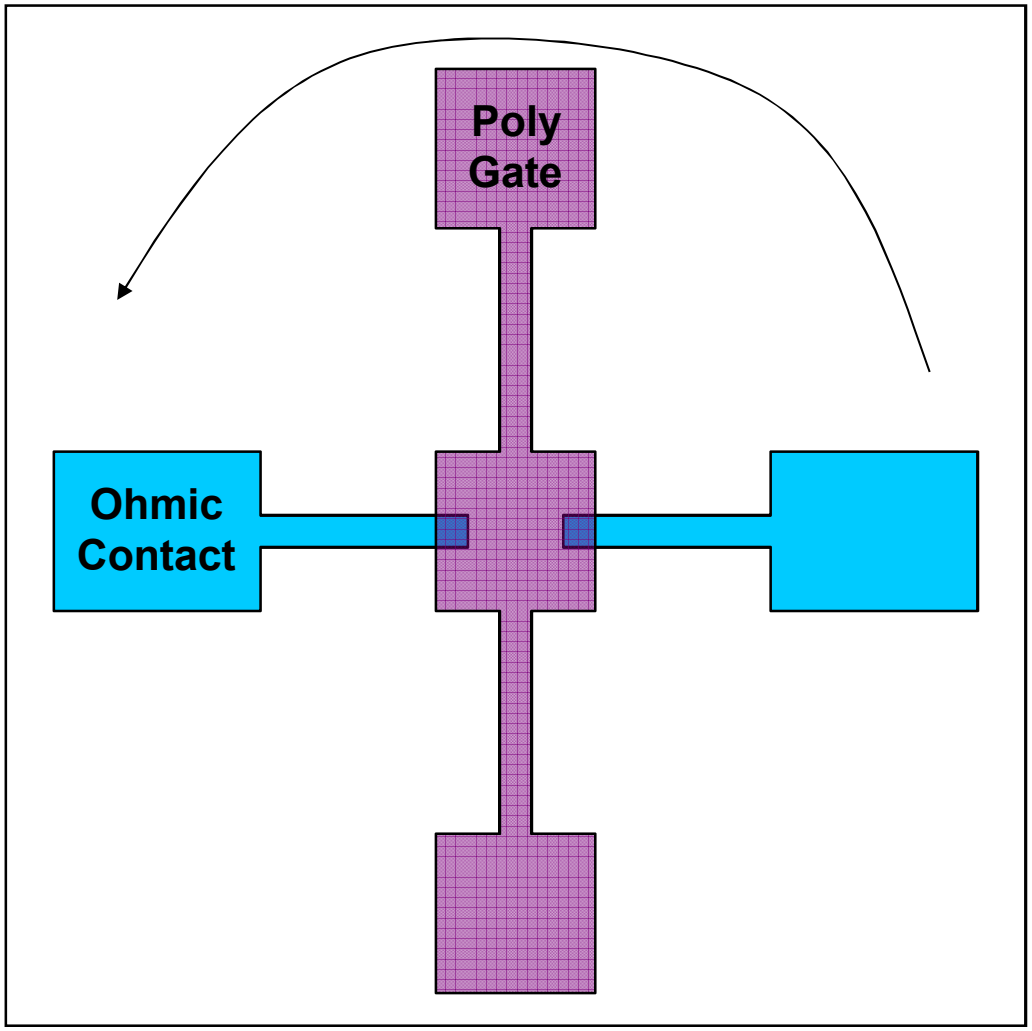

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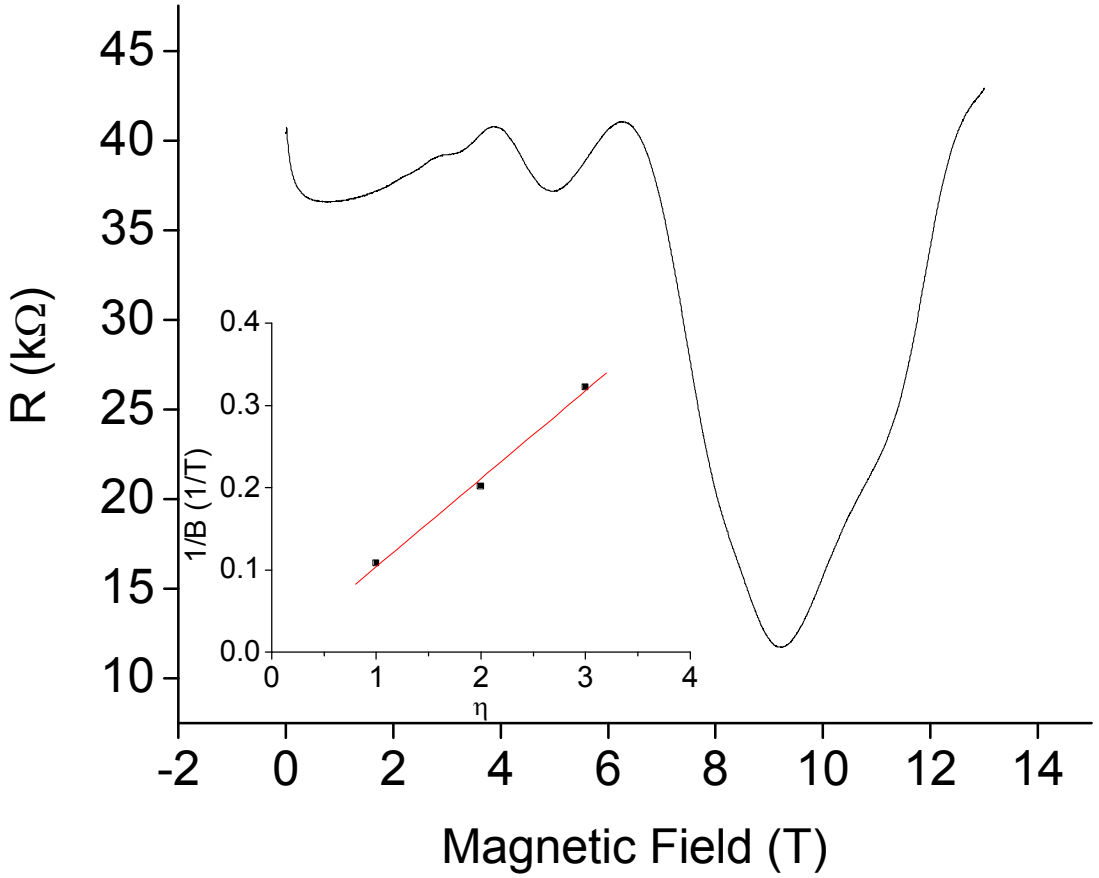
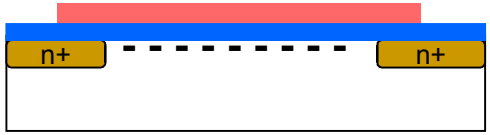
Two-Dimensional Conductivity



Mobility:
2600 $cm^2/V \cdot s$

Carrier Density:
4.5E+11 $/cm^2$

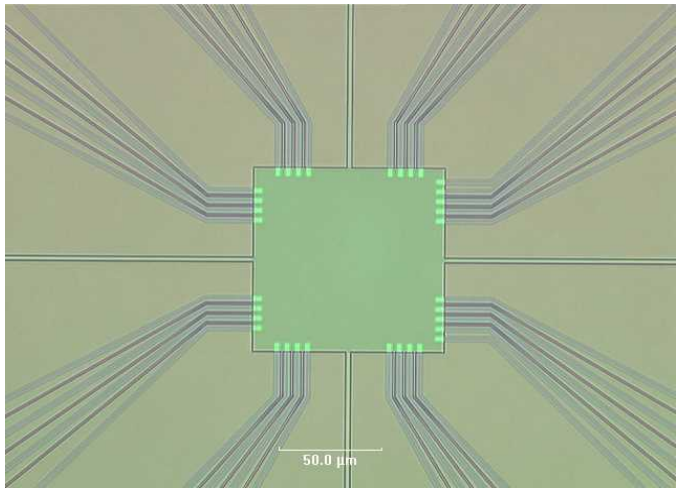
Resistivity:
~5500 Ω/sq

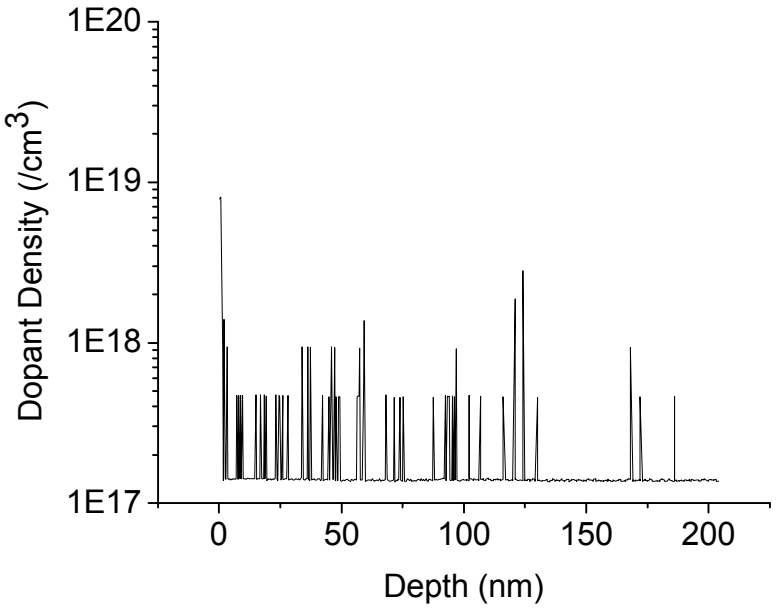


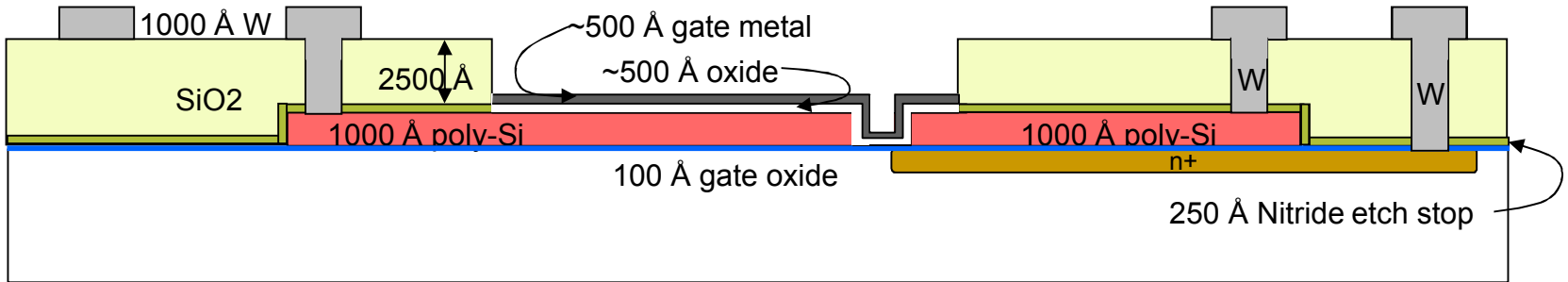
- SdH indicates 2D transport
- Depletion mode gating & hi-resistivity wafer suggests surface channel

Secondary Ion Mass Spectroscopy (SIMS)

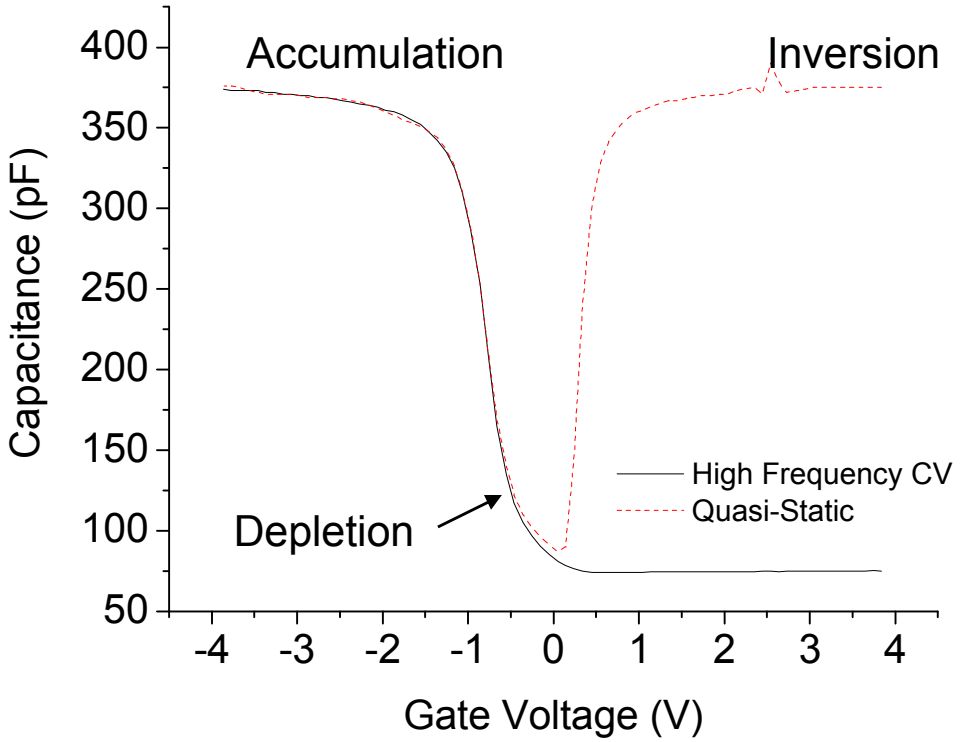
- As and P levels in substrate surface region measured by SIMS
- Concentrations are far below freeze out levels at LHe
- Conductance in field is not due to doping





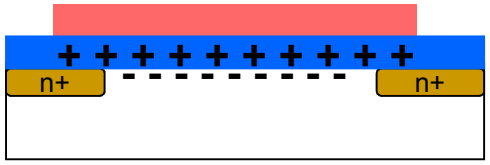


Charge in Monitor Oxide

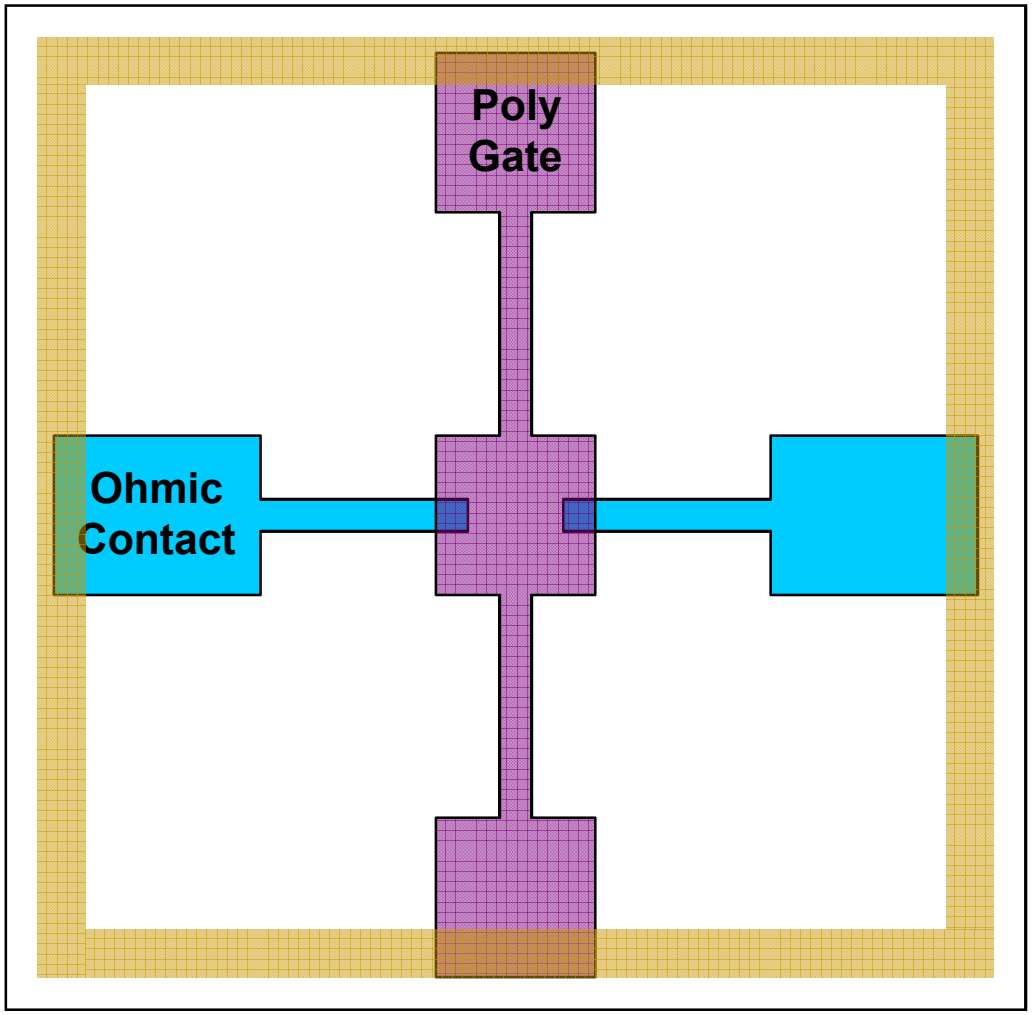


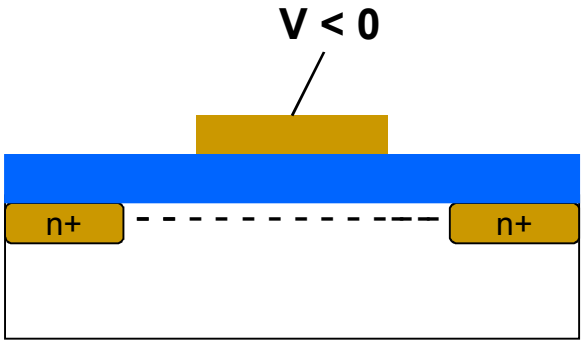
Substrate:
p-type
Doping Level:
1.5E16 /cm^3
D_{IT} (at midgap):
~2.5E10 eV^{-1} cm^{-2}
T_{oxide}: 20 nm
Q_{Ox}: 7.80E-8 C/cm^2
n_{Ox}: 4.87E11 /cm^2

- Positive fixed oxide charge found in typical oxides
- C-V of monitor of SNL oxide detects ~ 5x10^{11} cm^{-2}
- Magnitude offers plausible explanation of 2DEG
  - Effect also previously cited in literature



Approaches for Ohmic Isolation





Additional Top-Gate for Depletion

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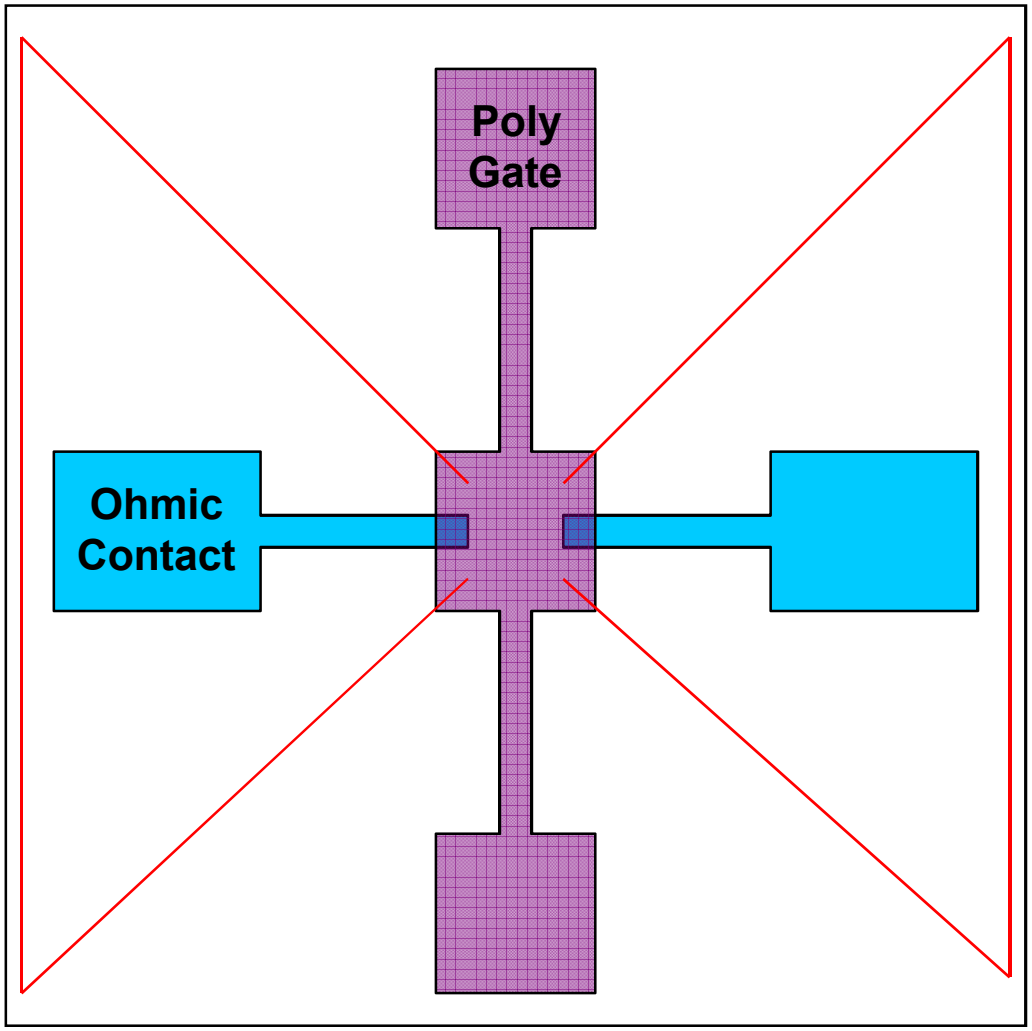
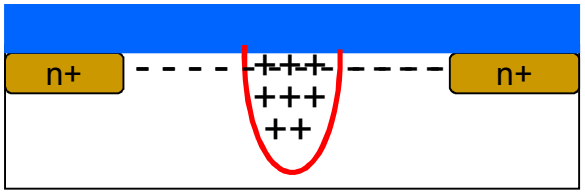
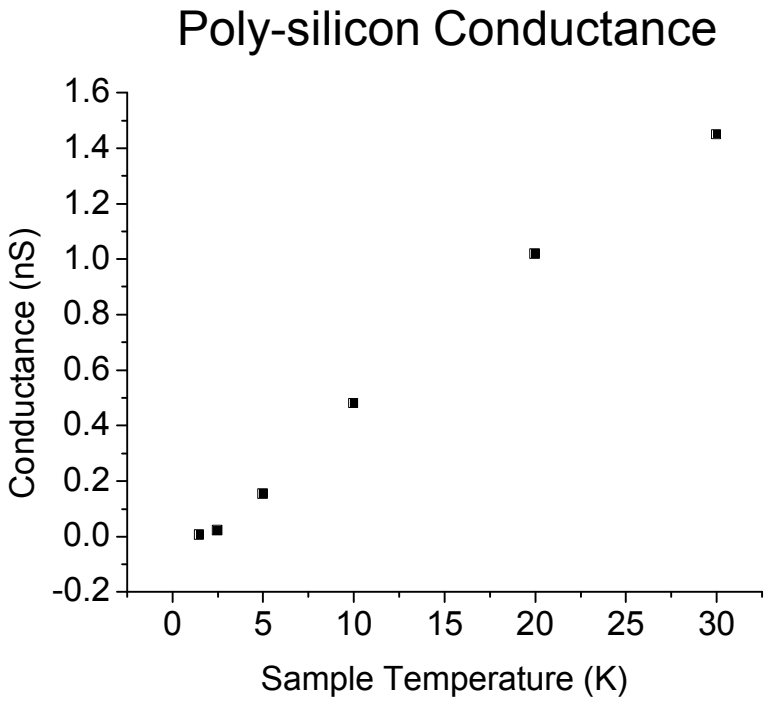
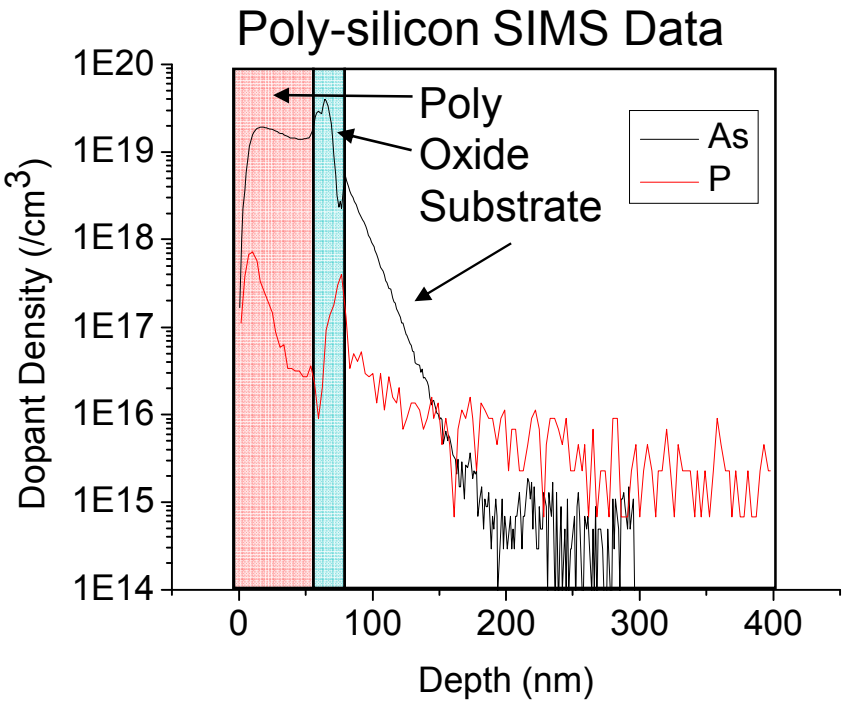




P-type implant lines

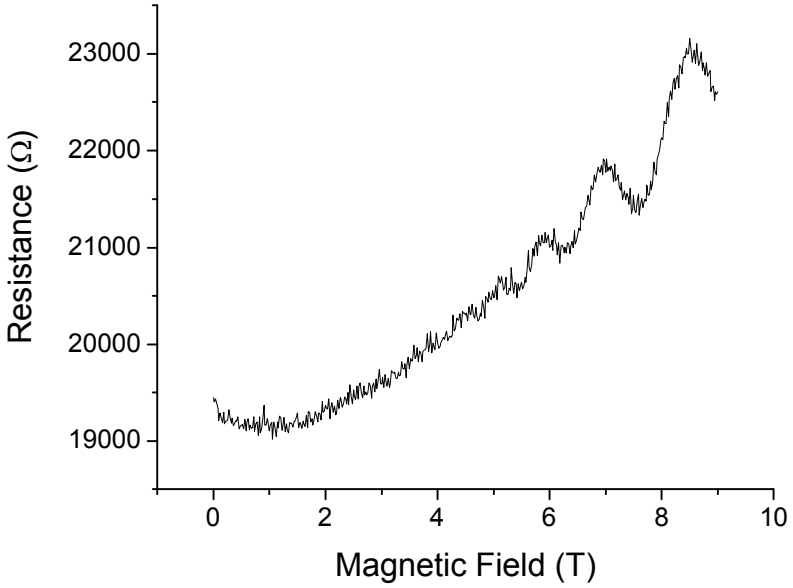
Poly-silicon Conductivity, Mobility

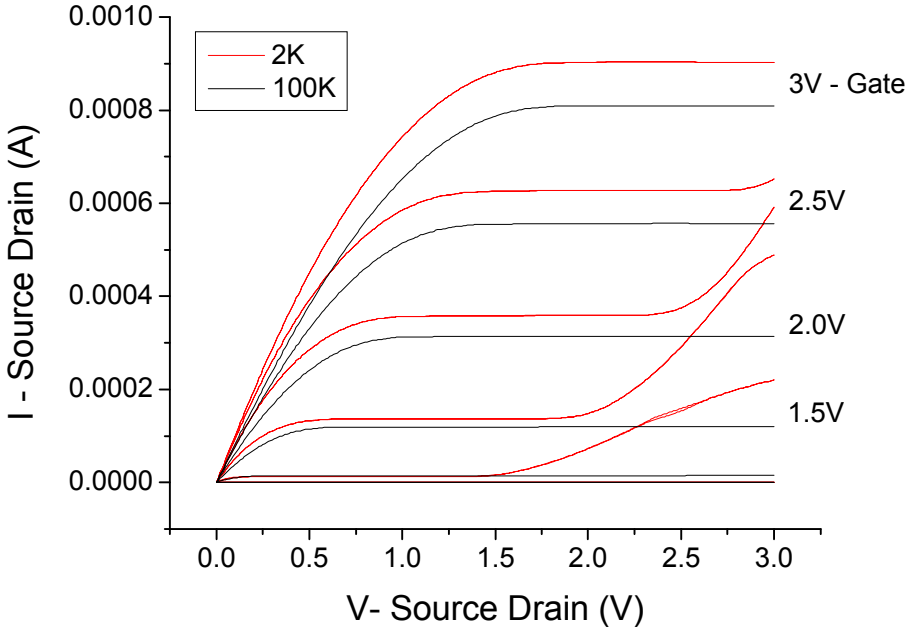




- Poly-silicon conductivity approaches 0 at low T
- Degenerate dopant concentration in poly (SIMS)
- Gating observed at temperature below typical “freeze-out”
- Temperature dependent mobility suggested in literature

Sandia Manufactured MOSFETs





- Sandia CMOS processing seems to be compatible with low temperature measurements (i.e., contacts)
- No evidence of poly-silicon freeze out in MOSFET gate

Summary

- Top gated Si/SiO2 accumulation mode QD structure using SNL fab was described
- Front-end structure completed
  - high resistivity, low resistivity, and SOI cases
- Oxide charge induced 2DEG measured in high resistivity wafer case (~ $5x10^{11}$ cm^{-2})
- Strong poly-Si temperature dependence observed despite degenerate doping levels of ~$2x10^{19}$ cm^{-3}
- Future Goals:
  - Isolate ohmics, increase doping & move on to dot formation

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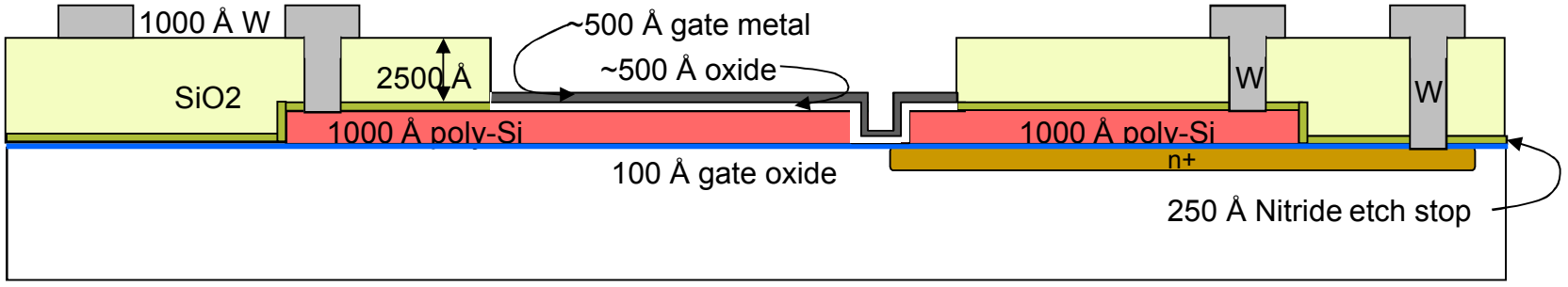
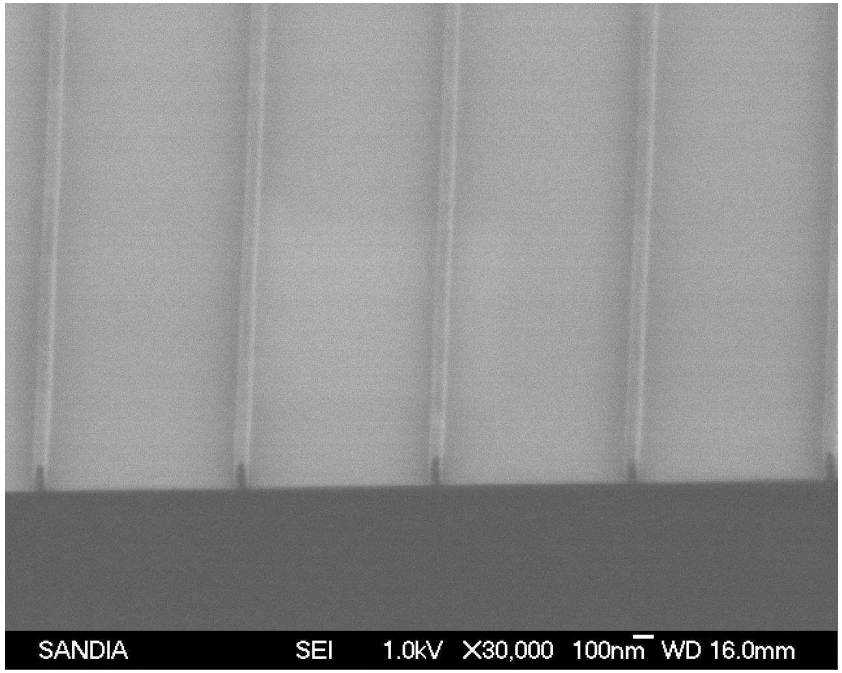


High Selectivity Polysilicon Etch

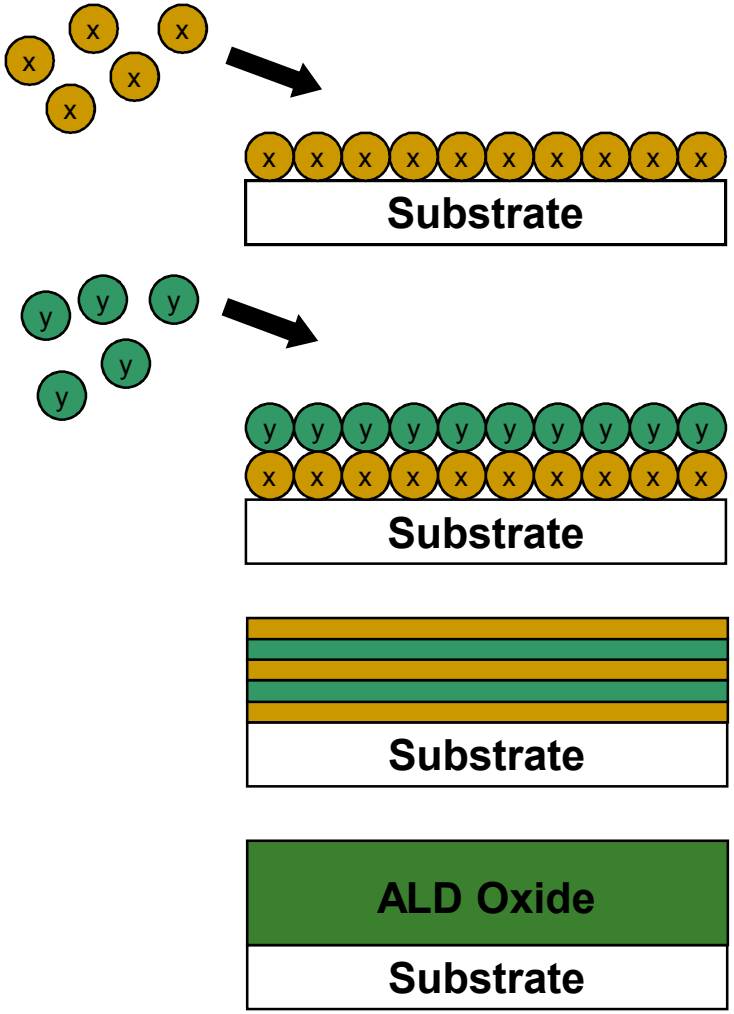


- Br based Poly Silicon Etch
- Etch Selectivity Si/Resist = 0.7
- Oxide remaining = 83 Å (of 100 Å)
- Residual resist post strip
- 50nm features with minimal noise

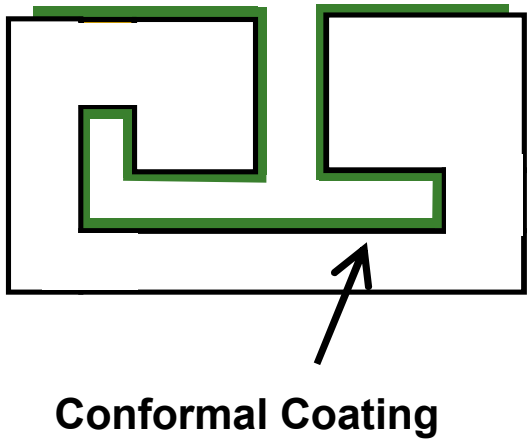
- Al Sputter and liftoff process in place for top-gating
- Low Temperature Deposition
- Oxide Damaged Minimized

PICTURE

Atomic Layer Deposition



- Low Temperature Deposition
- Conformal Coating
- Quality Oxide



PEOPLE?

- Mark Eriksson
- Malcolm Carroll
- Mike Lilly
- Denise Tibbetts
- John Seamons
- Christian Morath
- Dominic Laroche
- Kent Childs (Si fab integration)
- Robert Grubbs (ALD)
- Frank Austin (Sputter Guy)
- Jeff Stevens (Etch Guy)
- Joel Wendt & Aaron Gin (ebeam Guy)

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