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Ultrathin Integrated Multilayer Capacitors by Chemical Solution Deposition

Geoff L. Brennecka, Bruce A. Tuttle, Chad M. Parish, and Luke N. Brewer
Sandia National Laboratories, P.O. Box 5800, MS 1411, Albuquerque, NM, USA 87185-1411
Fax: 01-505-844-9781, e-mail: glbrenn@sandia.gov

ABSTRACT: Continued miniaturization of integrated microsystems as well as the development of novel and advanced energy generation and conversion technologies must be accompanied by comparable advances in capacitive energy storage. The three factors which determine volumetric capacitance are the dielectric constant (K), thickness, and active area of the dielectric layer. Traditionally, capacitor technologies have essentially sacrificed one of these three factors for the optimization of the other two. However, by developing ultrathin high-K dielectrics and integrating them into multilayer structures, we have translated improvements in all three factors into significant advancements in capacitance density. Using spin-coating methods, multilayer capacitors have been fabricated with high dielectric constants (>1000) and individual dielectric layer thicknesses of <50nm. Thus, integrated capacitor structures in excess of 2μF/mm2 can be realized. Further increases in capacitance density can be achieved using a Sandia-developed appliqué process. Discussion will focus on the materials and processing issues in the fabrication of PLZT-based high-K multilayer capacitors, including the increased importance of the electrode/dielectric interface(s) in retaining outstanding properties at the nanoscale. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

Key words: sol-gel, multilayer, PLZT, ultrathin, capacitor

1. INTRODUCTION

As shown in Equation 1, the capacitance of a simple parallel plate structure (C_p) varies linearly with dielectric constant, K, and active electrode area, A, but inversely with dielectric thickness, t,

$$C_p = \frac{KA\varepsilon_0}{t} \qquad (1)$$

where ε_0 represents the permittivity of free space (8.854E-12 F/m). Present capacitor technologies maximize two of the variable parameters at the expense of the third. For example, both wound polymer and electrolytic capacitors achieve very large effective areas with thin dielectric layers, but use materials with K values of approximately 3 and 30, respectively. Similarly, ferroelectric thin films of ~200-500 nm are routinely fabricated with K values >1000, but the effective areas of these capacitors are typically limited to hundreds of square micrometers. By demonstrating multilayer capacitor structures with ultrathin dielectric layers based on high-K ferroelectric materials, this work represents a fabrication scheme that capitalizes on advances in all three basic capacitor parameters.

Presently, fabrication of ultrathin (~5-100nm) films is typically accomplished by deposition from the vapor phase using methods such as molecular bean epitaxy (MBE), pulsed laser deposition (PLD), metal-organic chemical vapor deposition (MOCVD) or sputtering. Studies on ferroelectric films in this category generally focus on the structural aspects of the films in an indirect probe of the effects of film thickness and substrate-related stress on ferroelectric behavior.[1-4] Electrical properties of such films are occasionally determined using scanning probe microscopy, but such films are, in general, not amenable to integration into meso- or macroscopic devices because they are not functional with the relatively large discrete electrodes needed for high-value integrated capacitors. This work reports the fabrication of macroscopically addressable ultrathin capacitors with excellent dielectric and ferroelectric properties. Capacitors based on ferroelectric thin films—whether deposited from the vapor phase or from solution—are generally limited in their active areas because of relatively poor yields traditionally achieved with large electrode areas. A solution-based processing route was developed which has enabled the production of ultrathin layers (<100nm) of perovskite dielectrics of sufficient film quality to result in >80% yield for capacitors with areas of $1mm^2$ across an entire 3” Si wafer using standard CSD spin coating techniques in a simple laboratory laminar flow hood.

This improvement in yield for ultrathin capacitors has also led to the successful fabrication of multilayer capacitors using the same solution-deposition approach. Multilayer structures are the hallmark of the ceramic capacitor industry, and the layer thicknesses which are achievable using tape casting techniques continue to shrink.[5] Eventually, the use of powder-based approaches to produce capacitors with increasingly thinner layers will no longer be feasible. Several groups have reported fabrication of multilayer structures using vapor- or solution-based techniques.[6-11]

We have been able to fabricate capacitors in multilayer structures having active electrode dimensions nearly five orders of magnitude greater than the thickness dimensions

while maintaining dielectric properties similar to those achieved in bulk ceramic capacitors. In this paper, we demonstrate the fabrication of multilayer structures based upon solution-derived PLZT and sputter-deposited Pt with layer thicknesses as small as 20 nm.

2. EXPERIMENTAL PROCEDURES

The versatile lead lanthanum zirconate titanate (PLZT) system was chosen as an appropriate demonstration system for the solution-based multilayer capacitor approach because its superior high-field behavior makes it ideally-suited for integrated high-value capacitor applications and its ferroelectric properties can be tailored over a wide range of behaviors with simple compositional modifications.[12] Solutions were batched assuming B-site compensation for A-site La doping. The nomenclature used here is in the form of La/Zr/Ti, such that 12/30/70, the composition used to fabricate the majority of the multilayer stacks discussed here, refers to a composition with 12% La substitution for Pb and a Zr/Ti ratio of 30/70, resulting in a nominal composition of $Pb_{0.88}La_{0.12}Zr_{0.291}Ti_{0.679}O_3$. The process is general enough to be applicable to any composition that is compatible with chemical solution deposition.

Solutions were prepared according to a slightly modified version of the "inverted mixing order" (IMO) hybrid sol-gel route.[13] The B-site precursors (zirconium butoxide, $Zr(OBu)_4$, 80% in butanol and titanium isopropoxide, $Ti(OiPr)_4$, 99.999%) were mixed and then chelated with glacial acetic acid (HOAc). After mixing, methanol (MeOH) was added as a solvent. The A-site precursors (lanthanum acetate, $La(OAc)_3$, 99.9% and lead (IV) acetate, $Pb(OAc)_4$, 98%) were added and dissolved at approximately 90°C. Once clear, the solutions were cooled to room temperature, and additional MeOH and HOAc were added to adjust solution molarity and improve stability. Pb contents of the solutions were varied from 10% Pb-deficient to 30% Pb-excess. A single solution was used for the deposition of every layer in any given multilayer stack.

Continuous PLZT films were fabricated using a standard photoresist spin-coater across entire 3" platinized silicon wafers (Si // 400 nm SiO_2 // 30 nm Ti // 170 nm Pt). Solutions were dispensed onto the wafer and spun at 4000 rpm for 30 sec, then pyrolyzed on a hot plate at 400°C for 1 min. After the desired number of deposition and pyrolysis steps in a laminar flow hood, the specimens were crystallized by one of two methods: direct insertion into a preheated box furnace at 700°C and removal to a heat sink after 1-60 min, or heating in a box furnace to 650°C for 30-90 min with ±50°C/min ramp rates. For the purposes of this document, the spin-coating of a solution followed by pyrolysis will be referred to as a single 'deposition'. After the desired number of depositions, the film was crystallized and Pt electrodes were sputtered on; each crystallization and electrode process represents a single dielectric 'layer'.

The continuous bottom Pt electrode was sputter deposited by the supplier; subsequent electrodes were fabricated in our lab by RF magnetron sputtering of Pt through shadow masks. The most commonly-used electrode configuration consisted of a 1 mm x 1 mm electrode with a 0.6 mm^2 contact pad offset 0.5 mm from the square electrode. For multilayer stacks, alternate layers of these electrodes were rotated 180° from the previous electrode layer. Electrode thickness was varied simply by adjusting the sputtering time. It was initially thought that achieving complete coverage over discrete electrodes would be problematic for spin-deposited dielectric layers having a thickness similar to or less than that of the electrode. However, the use of low-molarity solutions (typically ~0.04 – 0.2 M) meant that the thickness of the liquid present during spinning was significantly greater than the thickness of the resulting film; thus, dielectric layers were successfully deposited conformally over discrete electrodes several times the thickness of the crystalline dielectric layer.

Alternate electrode layers were connected to one another by etching a small via through the previous two dielectric layers prior to deposition of the next electrode using a wet etch consisting of a dilute mixture of buffered HF and HCl.

Capacitance measurements were made using standard Signatone semiconductor probes connected to an HP 4284A Precision LCR Meter. Polarization vs. field (P vs. E) characteristics were measured using similar probes connected to a Radiant Technologies Precision Workstation. All values reported here were obtained at room temperature; measurements of capacitance and dissipation factor as well as P vs. E measurements were performed at 1kHz. DC resistivity measurements were performed by using one Keithley 237 Source Measure Unit to apply a constant voltage across the sample with a 1kΩ resistor in series and measure the associated current, while another Keithley 237 tracked the voltage drop across the specimen. Data were collected for 10 minutes per capacitor, but only the data from the last five minutes were used to calculate steady state resistivity, in order to eliminate transient effects.

Film thicknesses were determined using a Veeco Dektak contact surface profilometer and verified using cross section transmission electron microscopy (TEM). Specimens of film cross-sections were prepared for TEM by focused ion beam (FIB) milling and were analyzed using a Philips CM30 operated at 300 kV. Scanning electron microscopy (SEM) was also used for microstructural characterization. X-ray diffraction (XRD) was performed using a Siemens D500 powder diffractometer with a Cu Kα radiation source.

2. RESULTS AND DISCUSSION

As previously reported, the yield of 1mm^2 electrodes depends critically on the number of film depositions and shows only a slight dependence upon the actual film thickness.[14] Therefore, high-yield ultrathin films can be fabricated simply by using low-molarity solutions. The limiting factor to thinner films is that each deposition layer must remain continuous and not break up into islands during deposition and/or heat treatment.[14-16]

Multilayer structures were fabricated via sequential deposition of PLZT layers from chemical solution and Pt electrodes by sputtering. Structures with as many as 10 dielectric layers have been built up. As with single-layer specimens,[14] the layer thickness in multilayer specimens varied linearly with the molarity of the deposited solution and with the number of depositions per layer. Multilayer capacitors with layers as thick as 330 nm have been deposited for higher-voltage operation. As shown in Figure 1, multilayer structures have also been successfully fabricated with layer thicknesses as small as ~20 nm.

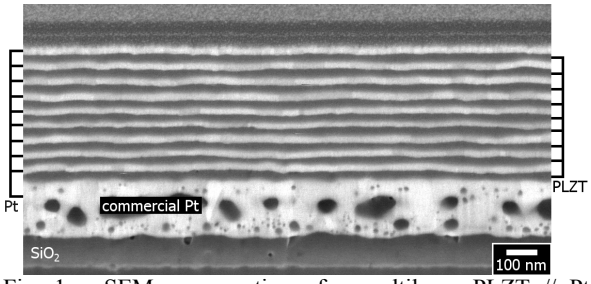

Fig. 1 – SEM cross-section of a multilayer PLZT // Pt structure having layer thicknesses of only 20 nm prepared using focused ion beam milling.

When fabricating a parallel-connected multilayer capacitor structure for maximum capacitance, a single shorting defect across any of the dielectric layers results in a short across the entire stack. This cumulative flaw effect means that the practical fabrication of multilayer stacks with large numbers of layers will require clean room conditions and a method of electrode deposition which minimizes the introduction of flaws in the underlying dielectric layer (i.e., scratches from the sputter mask). Nonetheless, using a basic laboratory laminar flow hood for solution deposition and manual electrode masking and sputtering, we have been able to fabricate functional multilayer capacitors with excellent dielectric properties having as many as 5 active layers.[17] Regardless of film thickness, the measured capacitance of these multilayer structures increased essentially linearly with the number of dielectric layers. Measured ferroelectric behavior and low dielectric losses were indicative of the high quality of the PLZT layers in these multilayer structures.[17]

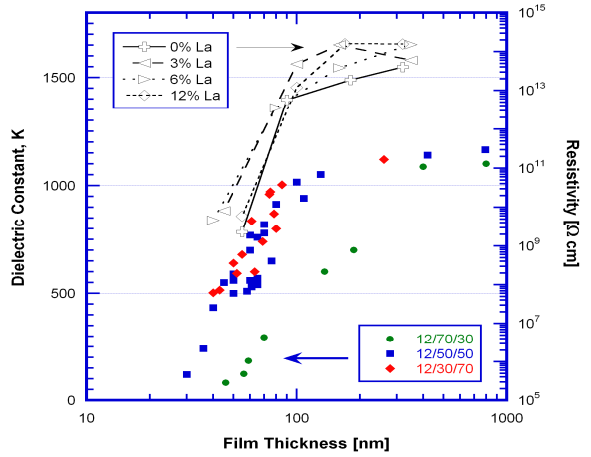

Fig. 2 – Thickness dependence of K (left axis, lower data) and resistivity (right axis, upper data) for PLZT films.

Ultrathin films, however, have been shown to exhibit inferior dielectric properties to those of thicker films, presumably due to increased difficulty controlling Pb stoichiometry.[14] For example, both measured dielectric constant and resistivity decrease dramatically for films below ~100 nm thick. Post-pyrolysis PbO coatings recover some of the dielectric properties for films ~40 nm and greater, but are not successful for thinner films or for improving film resistivity at any thickness (Figure 2).

Grazing incidence XRD (GIXRD) and X-ray reflectivity (XRR) have shown that transient phases are present during heat treatment but that these layers disappear after crystallization. These studies indicated that single-phase perovskite films could be deposited from solution in continuous layers as thin as 9 nm. However, secondary ion-mass spectroscopy (SIMS) studies have revealed that a significant amount of Pb diffuses into the bottom Pt electrode during pyrolysis and subsequent crystallization treatments. Further, high resolution TEM (HRTEM) studies and series dielectric modeling suggest that an interfacial layer of <1 nm may exist between the dielectric PLZT layer and the Pt electrode after crystallization.

Thus, while the use of low-molarity solutions enables the fabrication of ultrathin dielectric layers, the highly-reducing atmosphere at the electrode-film interface associated with the increased organic content of such dilute solutions promotes interaction between the excess Pb in solution and the Pt electrode during heat treatment. Further, as layer thicknesses decrease, it has been observed that more and more excess Pb in solution is required to achieve single-phase perovskite films.[14] Thus, the methods traditionally used to counteract the increased Pb-loss observed during fabrication of thin films (increased Pb excess in solution and post-pyrolysis PbO cover coats) actually worsen the situation when it comes to interactions between the dielectric layer and underlying Pt electrodes.[18]

It has long been known that the crystallization of the ferroelectric perovskite phase of PZT-based materials from solution occurs through an intermediate Pb-rich (O-deficient) fluorite phase. Further, it has been observed that the volatility of the Pb cation can result in the presence of a low-K surface layer in both bulk and thin film forms whose presence leads to significant degradation in electrical properties due to series dilution.[19-20] This metastable Pb-deficient layer can technically have either the disordered fluorite or defect-ordered pyrochlore structure, but since the ordering of the pyrochlore structure is not required for the effects discussed here, the more general 'fluorite' term will be used to describe the cubic, non-ferroelectric Pb phase.

A transformation from the stoichiometric perovskite to the Pb-deficient fluorite phase has previously been observed as a result of Pb-loss at high temperature. While there is no thermodynamic reason that the reverse—a transformation from the metastable Pb-deficient phase back into the stoichiometric perovskite—should not also occur, this has never before been reported.

In order to minimize interactions between the PLZT layer and the underlying Pt electrode, solutions containing Pb deficiencies as large as 10% were prepared and deposited using the same procedures used for other films. Films of two different compositions (PZT 53/47 and PLZT 12/70/30) were used to study the generality of the approach. After crystallization, these severely Pb-deficient films contained a mixture of perovskite and fluorite phases by XRD and exhibited poor dielectric properties. The films were then coated in a PbO solution and annealed at elevated temperatures to promote the incorporation of the excess Pb into the already-crystalline material and conversion to the high-K stoichiometric perovskite phase. Figure 4 shows the improved properties of the resulting single-phase films.

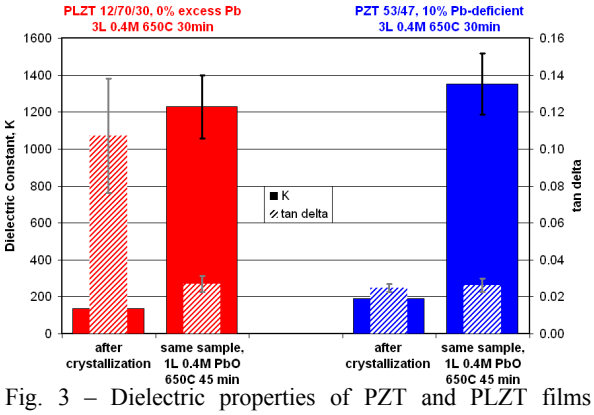

Fig. 3 – Dielectric properties of PZT and PLZT films prepared from Pb-deficient solutions after initial crystallization, then following a Pb-rich annealing step.

TEM studies have verified the conversion of the films from mixed-phase perovskite+fluorite to single-phase perovskite after the Pb-rich annealing step.[21] Figure 5 shows the microstructures associate with the films in each of their mixed-phase and single-phase forms and the dielectric constants measured for the films at each state. The porosity associated with the fine-grain Pb-deficient fluorite phase appears to have been 'pushed out' in the PZT 53/47 film as the perovskite grains grew to incorporate what had been Pb-deficient fluorite. However, some residudal porosity is evident in the PLZT 12/70/30 film after conversion to the stoichiometric perovskite phase.

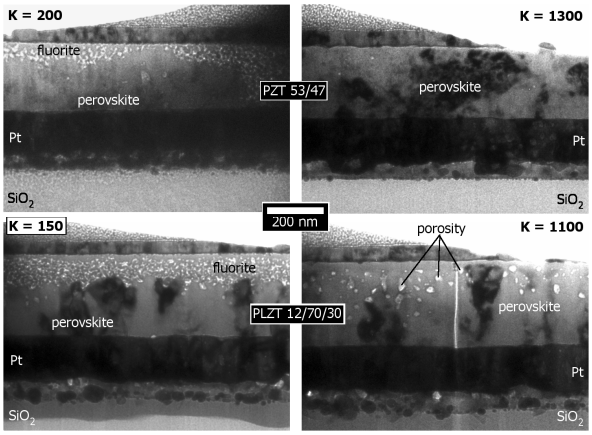

Fig. 4 – Cross-section TEM images of (top) PZT 53/47 and (bottom) PLZT 12/70/30 films (left) after crystallization from Pb-deficient solutions and (right) the same films after annealing in a Pb-rich atmosphere.

3. SUMMARY

Functional nano-scale multilayer capacitors with enhanced areal capacitance were successfully fabricated using chemical solution deposition of PLZT dielectric layers and sputter deposition of Pt electrodes. Multilayer stacks having as many as 10 dielectric layers and stacks with individual layers as thin as 20 nm have been demonstrated. Further, reversibility between the Pb-deficient low-K fluorite phase and the stoichiometric high-K perovskite phase has been demonstrated.

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