National Nuclear Security Administration

Sandia National Laboratories

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BEAM-BASED DEFECT LOCALIZATION TECHNIQUES

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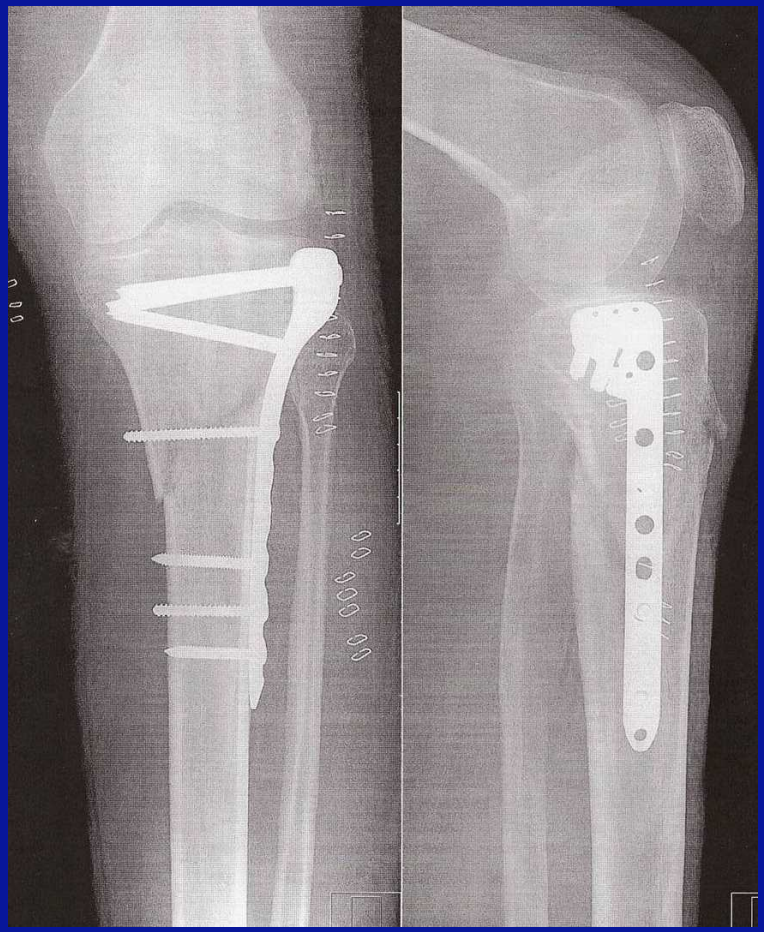
Important Parts of Failure Analysis

Failure Localization

Corrective Action



Purpose

- To describe standard and new SEM and SOM techniques for microelectronic device failure analysis

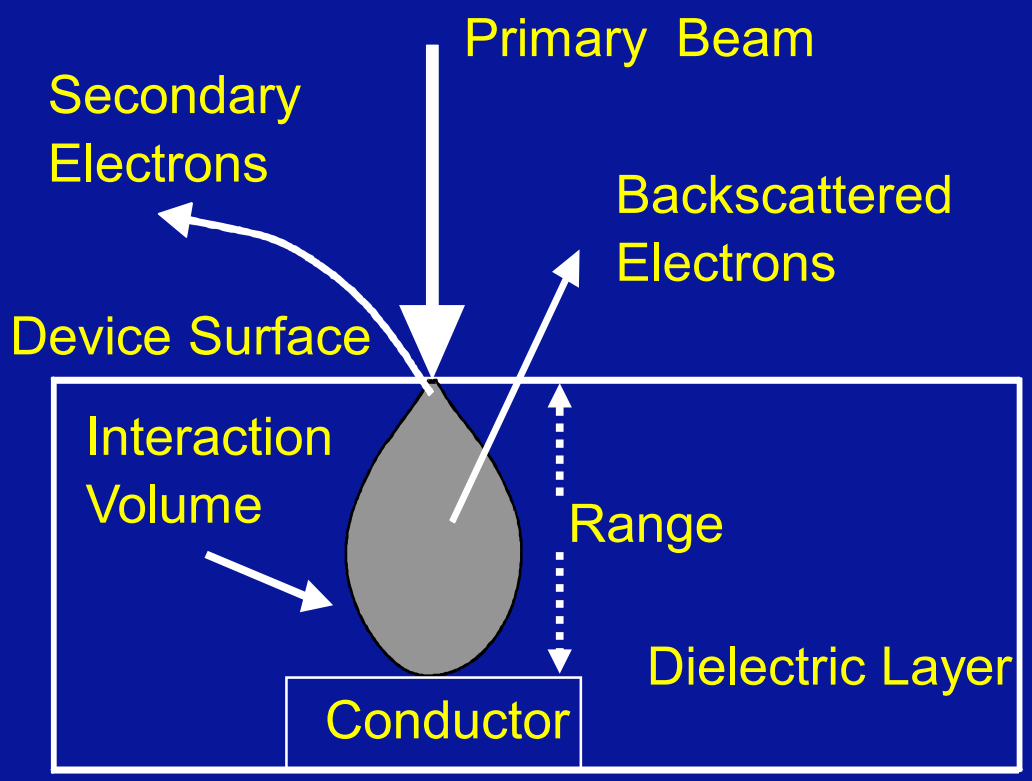
Outline

- Standard SEM techniques:
  - SE imaging, BSE, VC, CCVC, advanced EBT systems, and EBIC
- New SEM techniques:
  - Novel VC applications, RCI, CIVA, LECIVA
- New SOM techniques:
  - LIVA, TIVA/OBIRCH, SEI, SDL/LADA

Secondary Electron (SE) for Surface Morphology

- Information yielded: topology map of the sample, most common SEM mode
- Physics behind use: differences in SE emission efficiency with topology, edge effects
- Implementation: only an SEM is needed, sample prep is optional, lid/plastic removal required, coating to reduce equilibrium charging, choice of PBE (primary beam energy) will reduce charging effects
- IC damage: no direct "physical" damage with e-beam testing, possible MOS damage and annealing, layer removal damage, ESD damage, conductive coating will alter IC performance

Primary Electron Beam/Sample Interaction Products and Beam Range

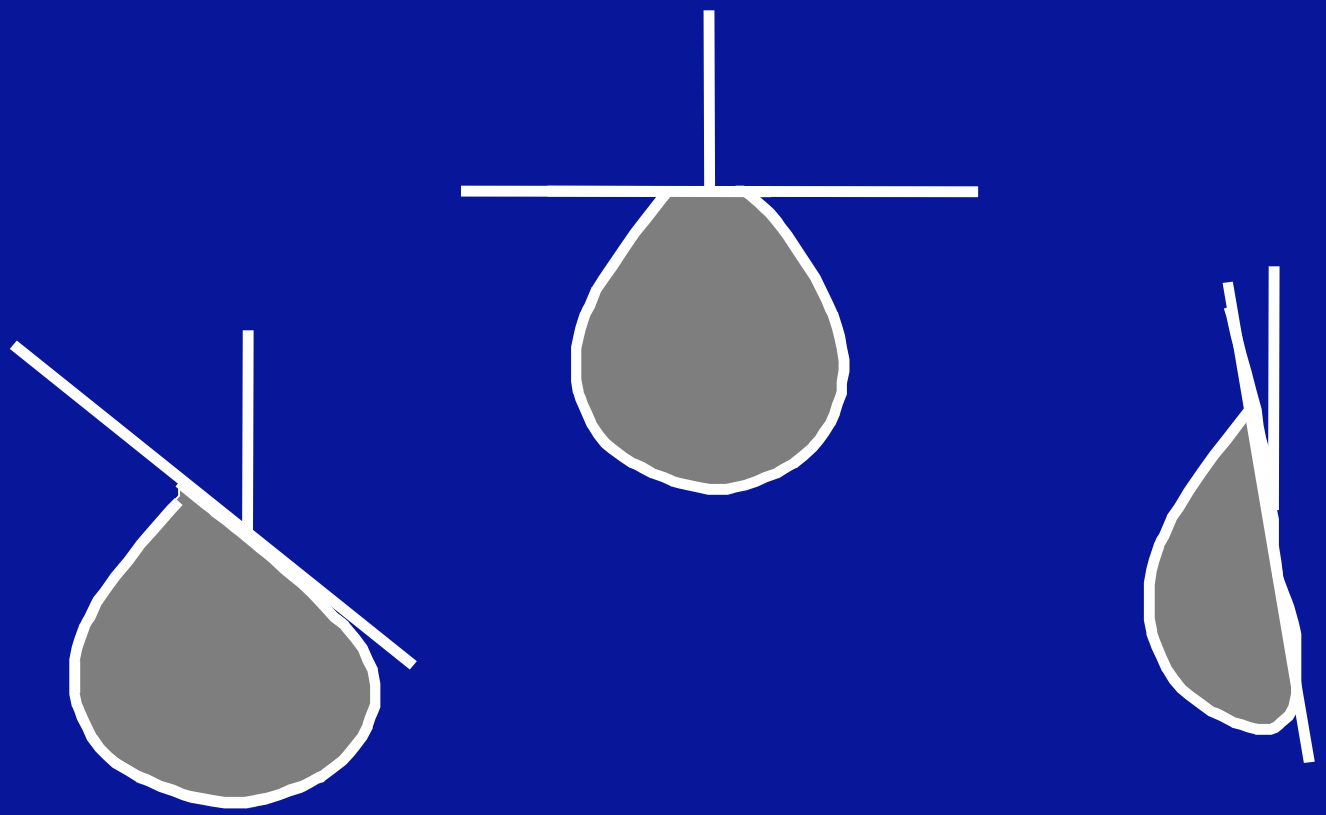


Beam energy (KeV)	Range in Al (μm)	Range* in SiO_2 (μm)
1	0.028	0.036
3.5	0.22	0.29
5	0.41	0.52
10	1.32	1.66
20	4.19	5.23
30	8.24	10.40

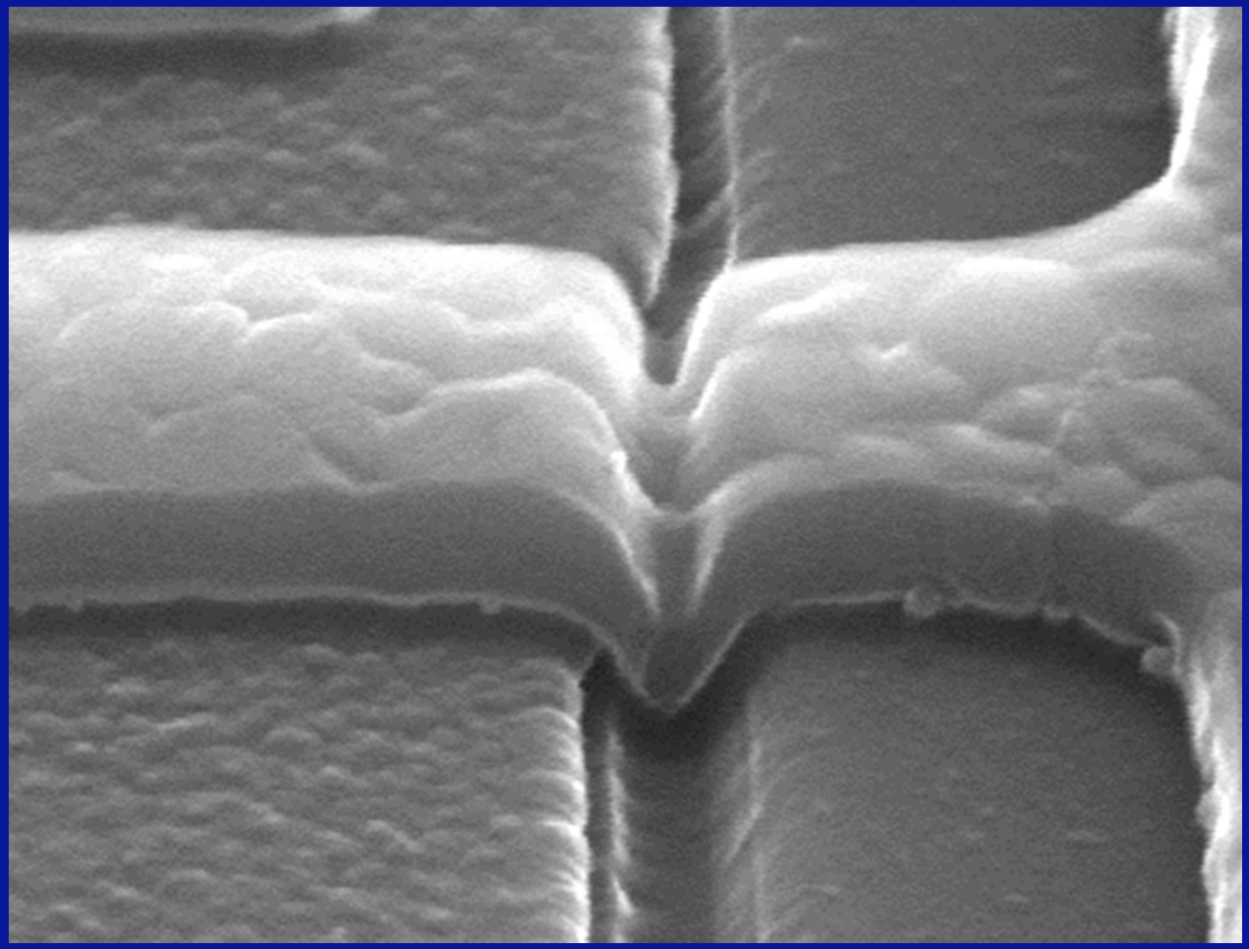
Range calculated from the Kanaya-Okayama formula, courtesy of W. Vanderlinde, LPS

* for a ρ of 2.0 g/cm^3

Electron Beam Interaction Volume Variation With Angle



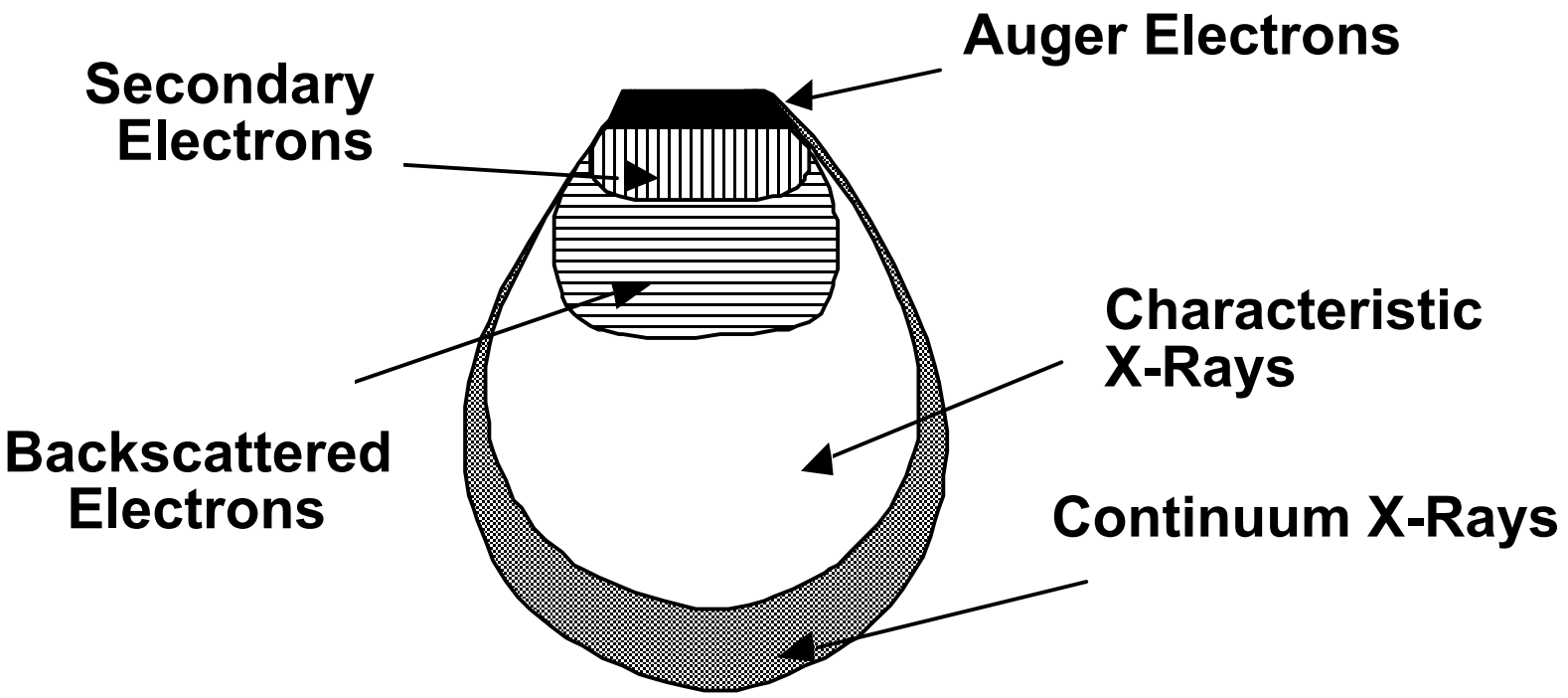
SE Image Example



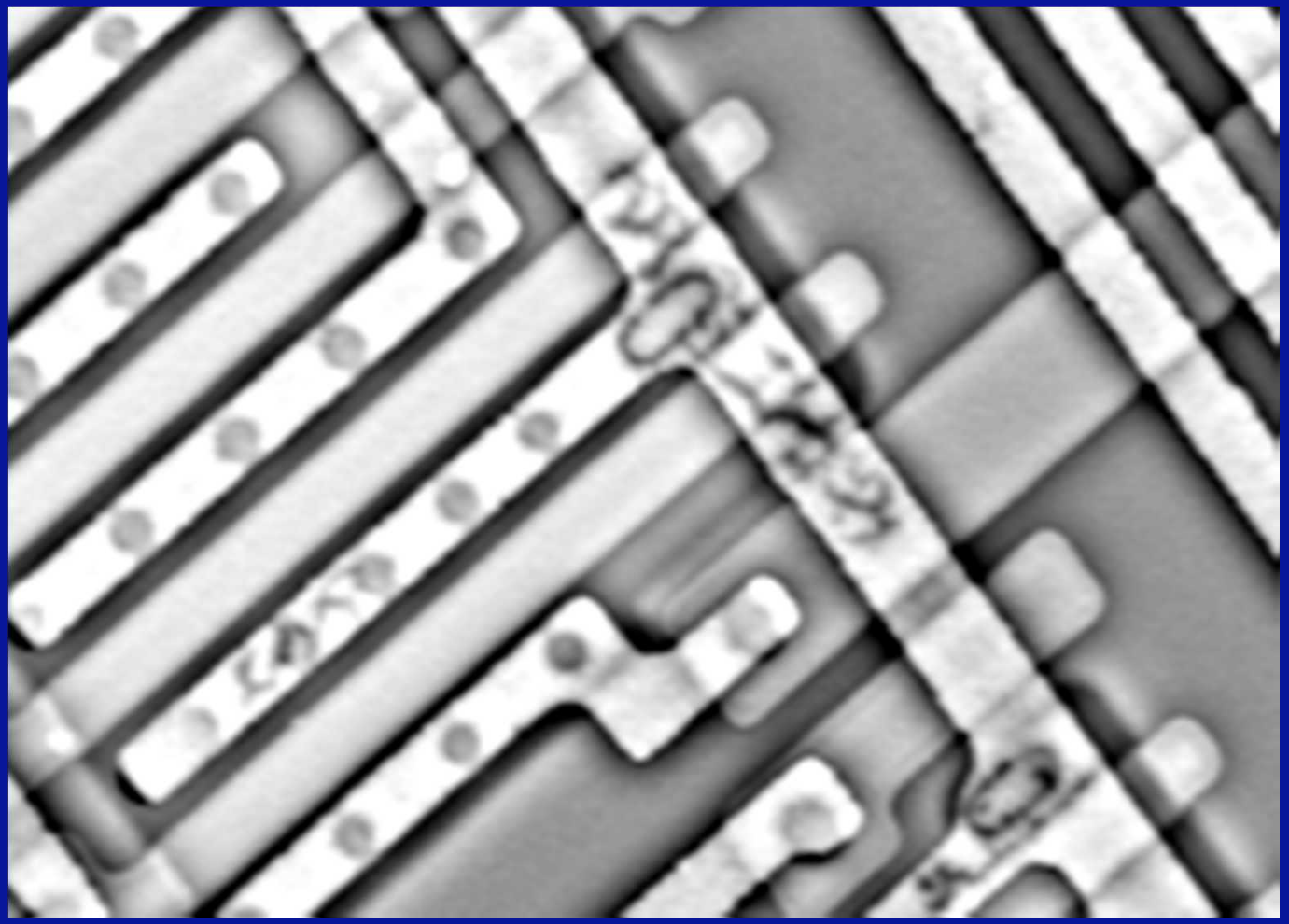
Backscattered Electron (BSE) Imaging

- Information yielded: BSE imaging detects difference in atomic number, used to find impurities and voids
- Physics behind use: image elastically scattered primaries from the sample, nuclear scattering the principle mechanism, limited spatial resolution, imaging greatly dependent on beam energy/penetration
- Implementation: only an SEM is needed with a BSE detector, lid/plastic removal required, choice of PBE will affect utility
- IC damage: no direct "physical" damage with e-beam testing, possible MOS damage and annealing, layer removal damage, ESD damage, conductive coating will alter IC performance

Electron Beam Interaction Products



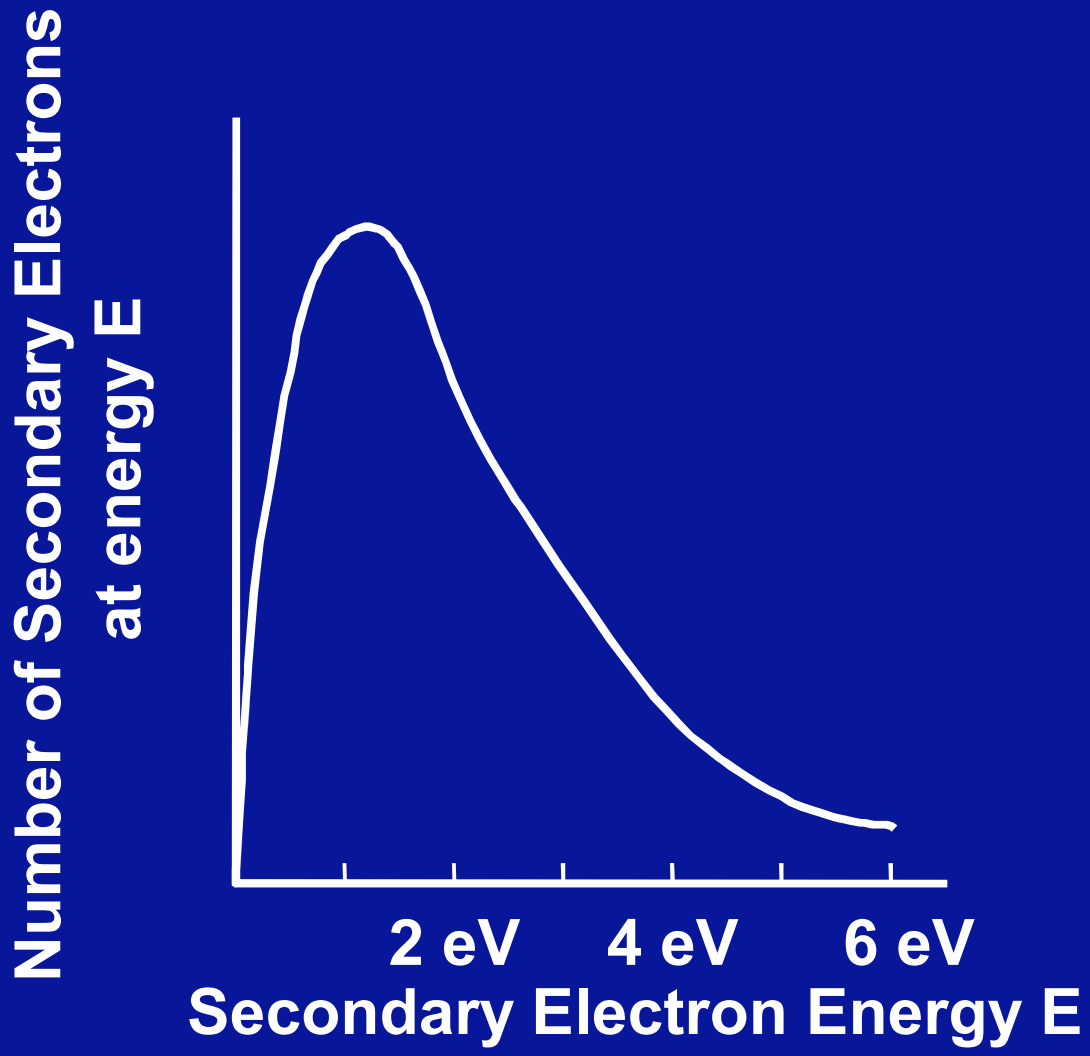
BSE Imaging Example



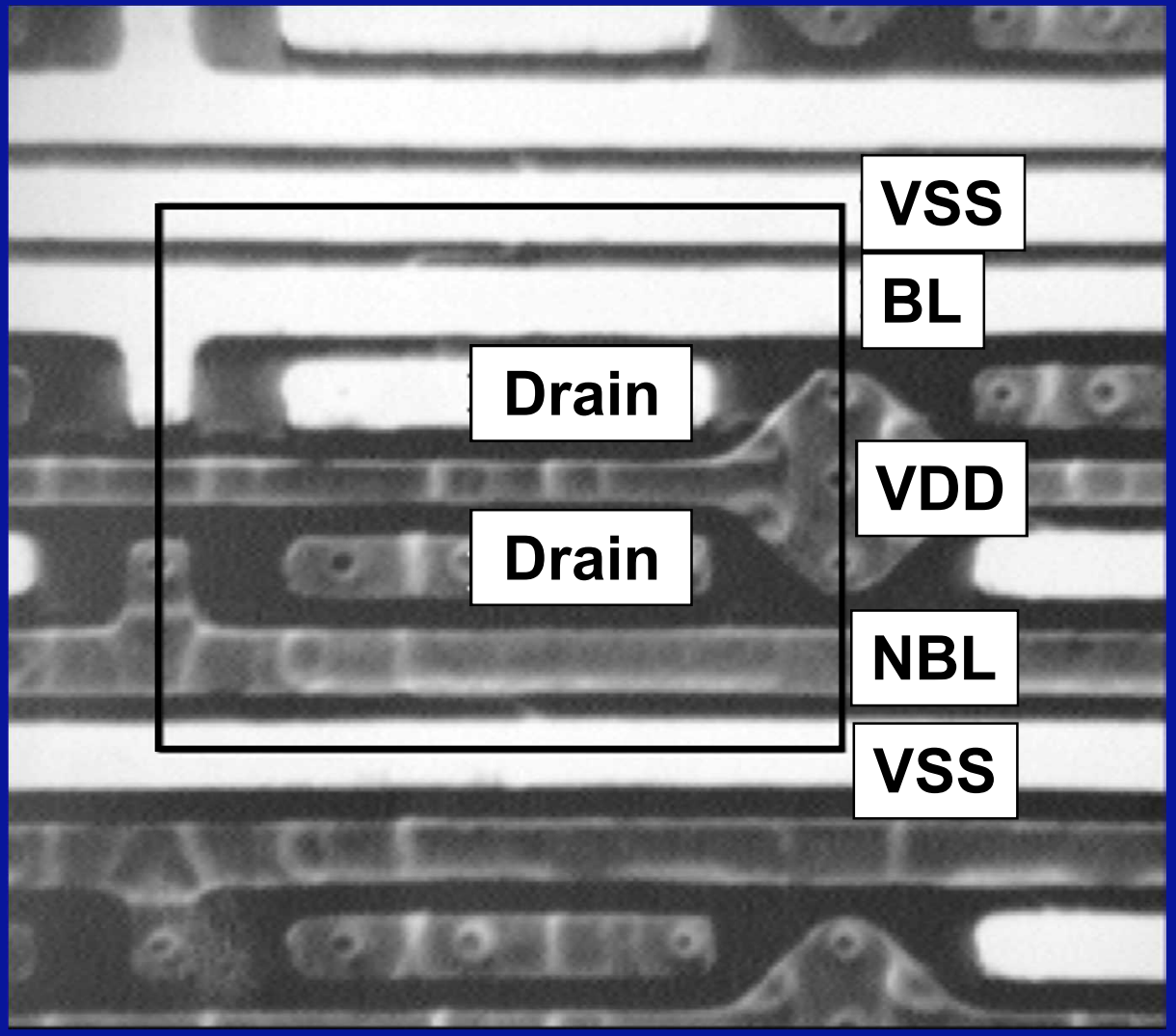
Voltage Contrast (VC) Imaging

- Information yielded: Produces a voltage map of an IC
- Physics behind use: VC takes advantage of differing SE emission efficiencies with surface potential, "see" difference in equilibrium and surface voltage, passivated devices can also be observed if proper PBE is used, quantitative resolution from image is ~ 0.5 V
- Implementation: need SEM, vacuum feedthrough, and voltage supply, local electric field concerns, charging and contaminants can obscure images
- IC damage: no direct "physical" damage with e-beam testing, possible MOS damage and annealing, layer removal damage, ESD damage, operation below 1 keV is non-destructive

Secondary Electron Energy Distribution



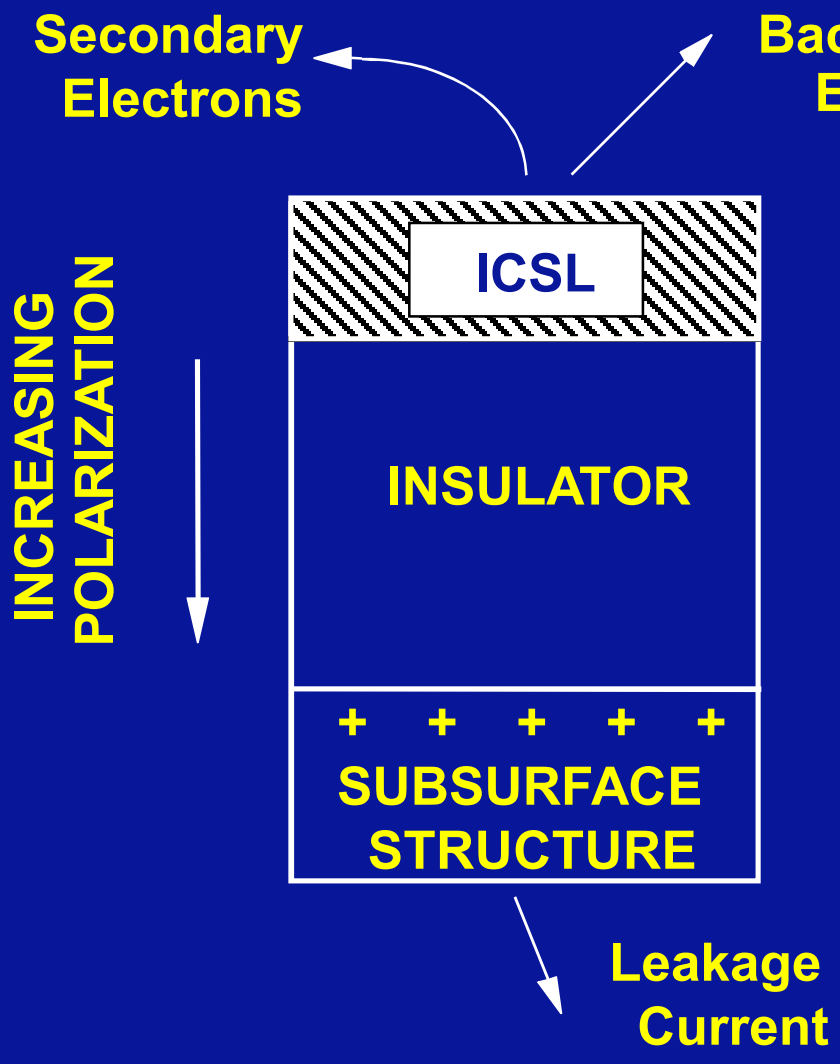
VC Imaging Example



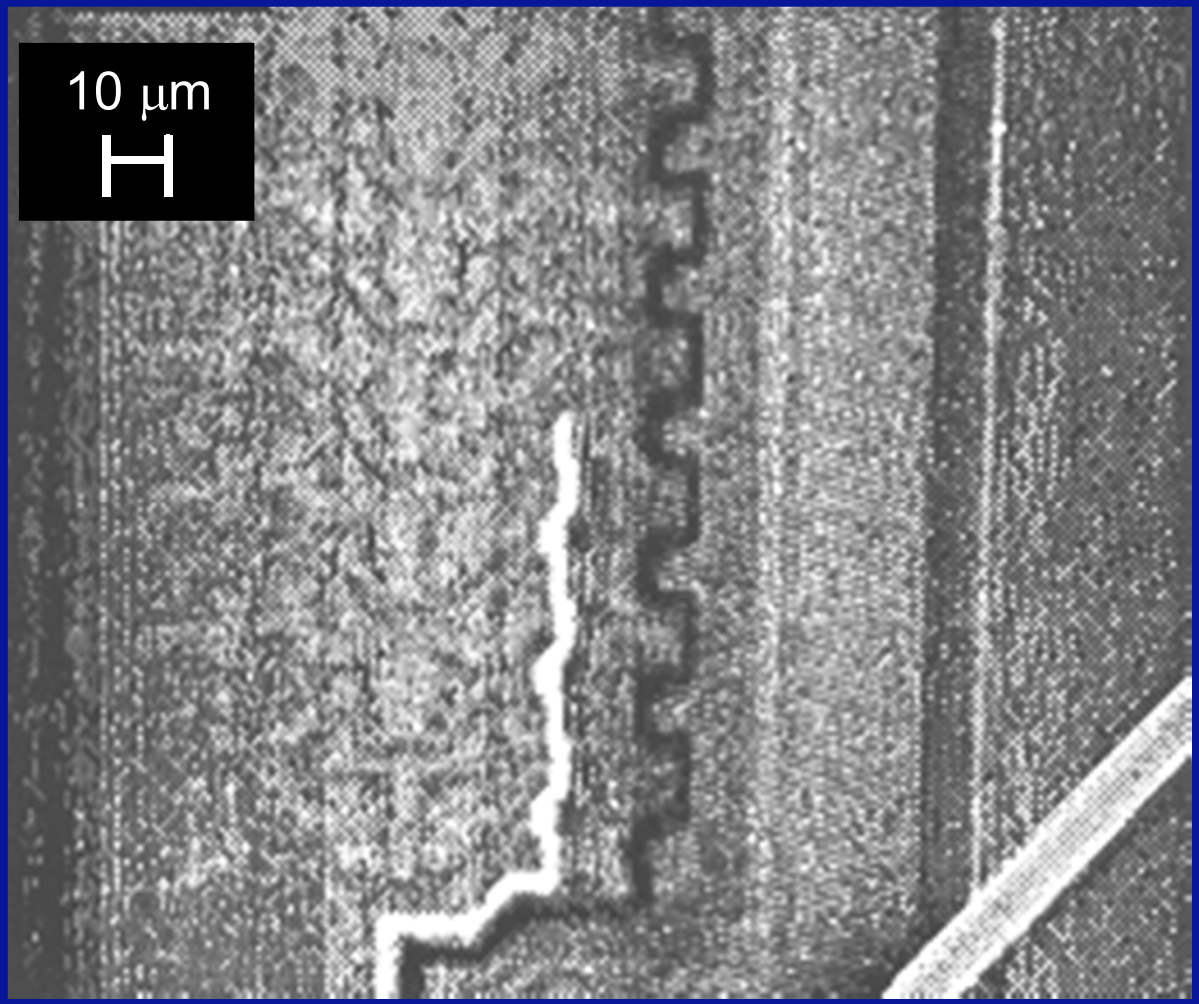
Capacitive Coupling Voltage Contrast (CCVC) Imaging

- Information yielded: Permits imaging and measurement of dynamic voltages on structures beneath the passivation, also depth measurement
- Physics behind use: CCVC uses passivation layer as a discharging capacitor, uses fast scan rates and low PBE, detector change from positive equilibrium potential, SNR vs. time resolution, depth measurement
- Implementation: need SEM, vacuum feedthrough, and voltage supply, local electric field concerns, charging and contaminants can obscure images, fast scan rate, digital image capture useful for averaging
- IC damage: operation below 1 keV is non-destructive other than lid/plastic removal

Physics of CCVC Generation



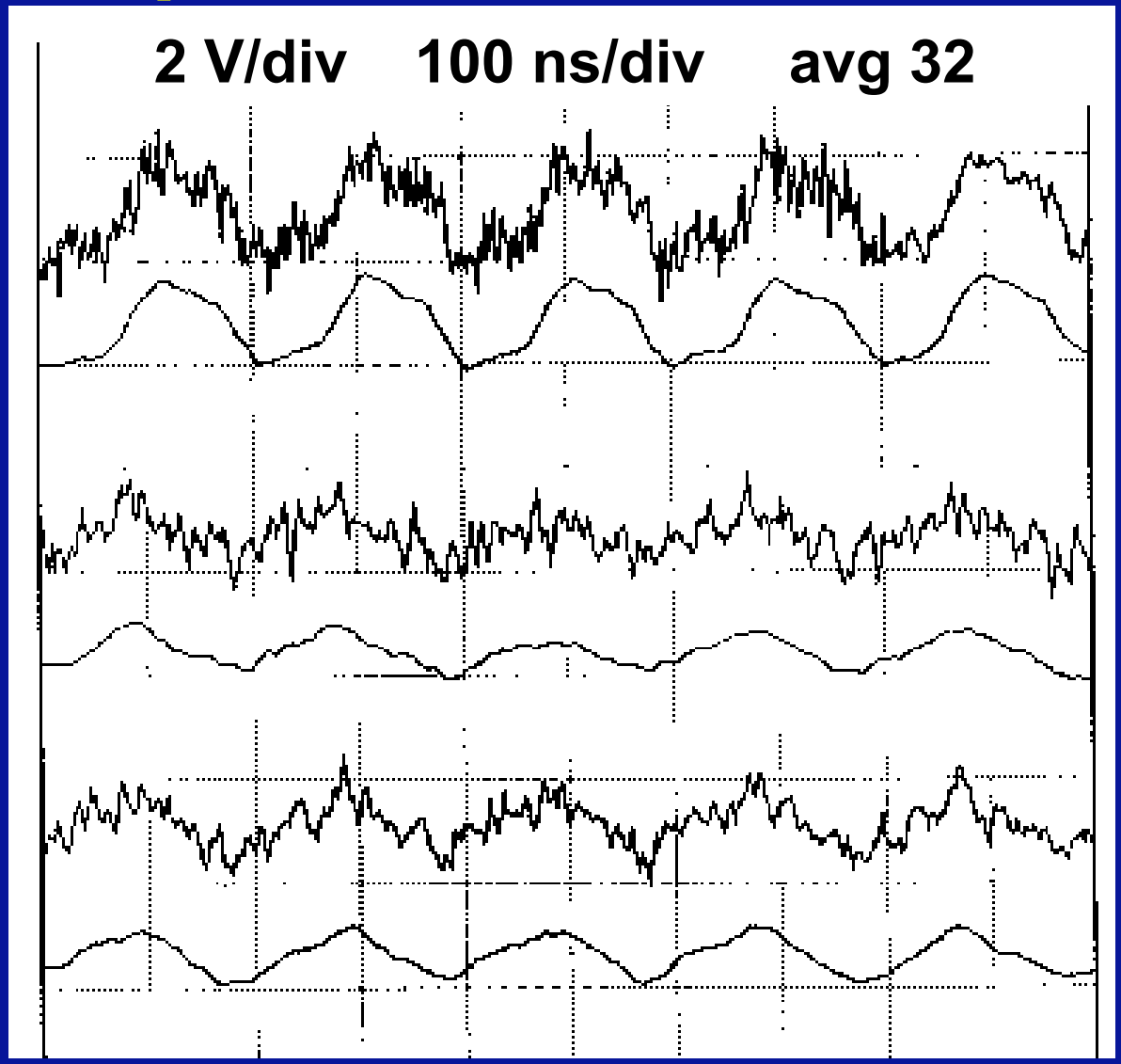
CCVC Imaging Example



Advanced Electron Beam Test (EBT) Systems

- Information yielded: EBT systems generate voltage waveforms of nodes and VC images of specific applied vectors, 10 mV and 10 ps resolutions
- Physics behind use: applied VC and CCVC, increased resolution from beam blanker and energy spectrometer, waveforms and images produced, CAD database incorporated
- Implementation: equipment available but cost is $500K to $1M, need to stimulate the IC, CAD compatibility, works only ~1 keV
- IC damage: operation below 1 keV is non-destructive other than lid/plastic removal

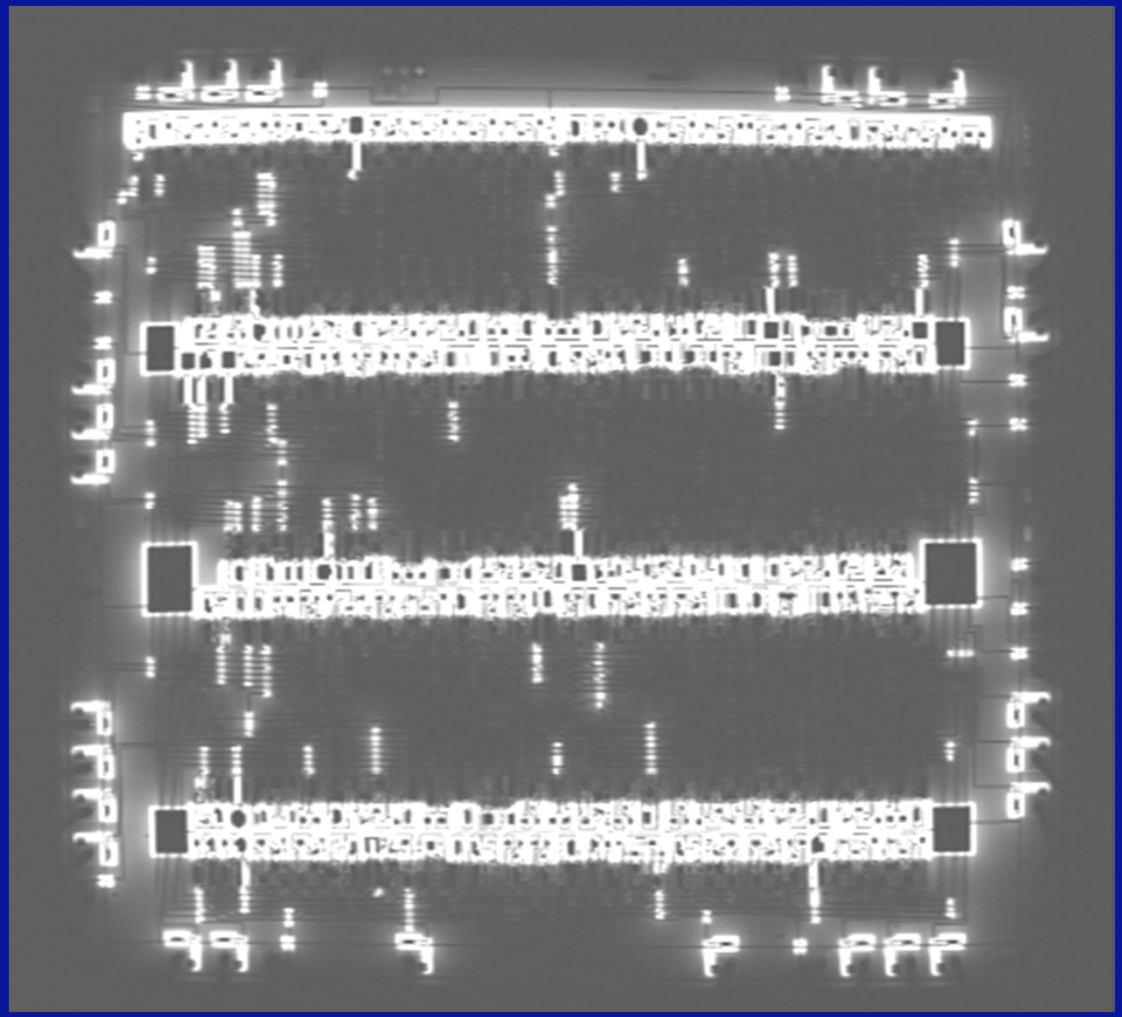
Example of an EBT Waveform



Electron Beam Induced Current (EBIC) Imaging

- Information yielded: EBIC imaging localizes regions of Fermi level transition, EBIC is primarily used to identify buried diffusions and semiconductor defects
- Physics behind use: uses non-random recombination of ehps (electron hole pairs) near space charge regions, IC is the detector, beam energy and IC pins observed greatly affect signal
- Implementation: need same equipment as VC, but replace voltage driver with current amplifier, passivation may remain intact, electrical testing can indicate which pin(s) to observe
- IC damage: same as for VC on passivated devices

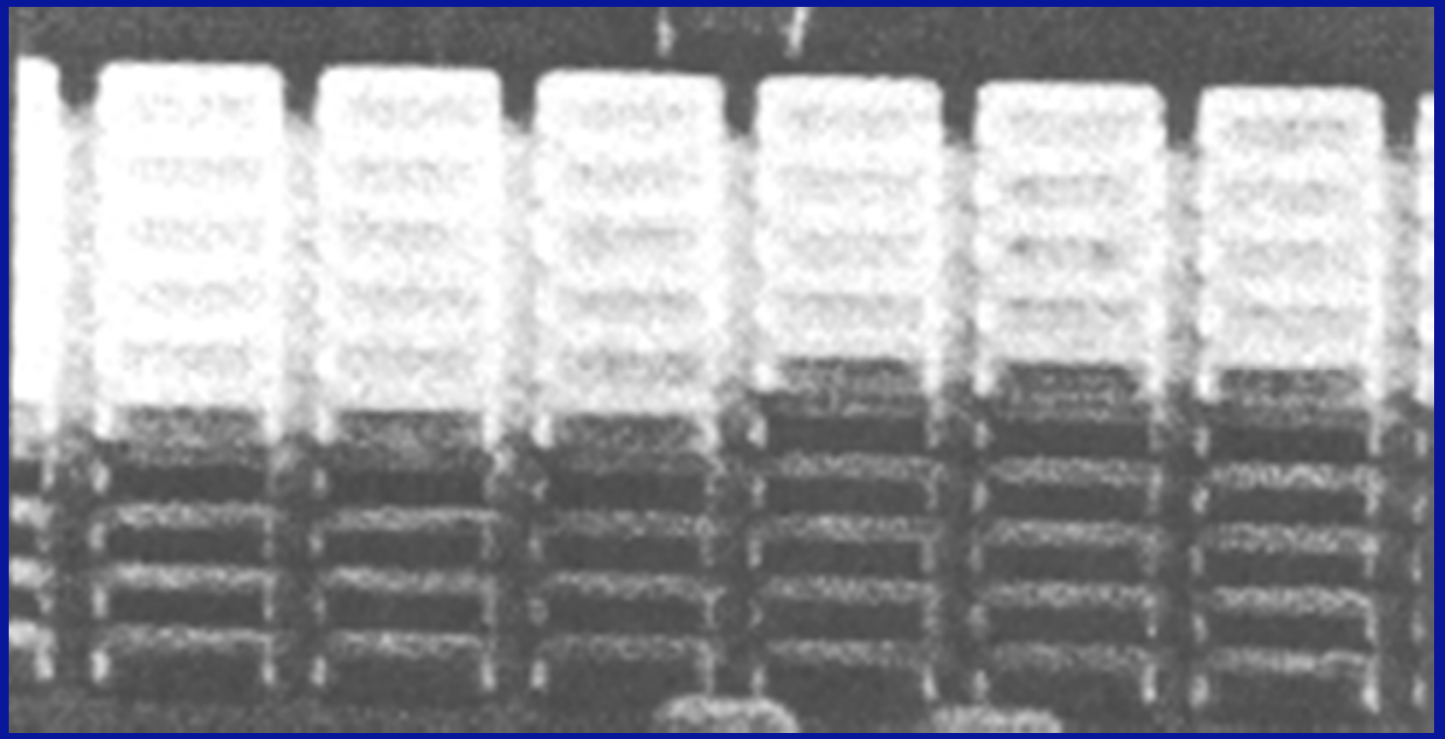
EBIC Imaging Example of an Entire Die



Passive Voltage Contrast

- Information yielded: conductor continuity and gate oxide ruptures can be located using the variation in VC with primary beam angle on depassivated devices
- Physics behind use: same as VC and SE emission using variation in equilibrium charging with tilt on floating structures, use low PBE (~1 keV) for best effect, SE emission varies as 1/cos, image locates difference in floating and grounded regions
- Implementation: SEM with low PBE (tilt desirable), sample prep and access to IC regions can be limited
- IC damage: same as for CCVC imaging

PVC Imaging Example

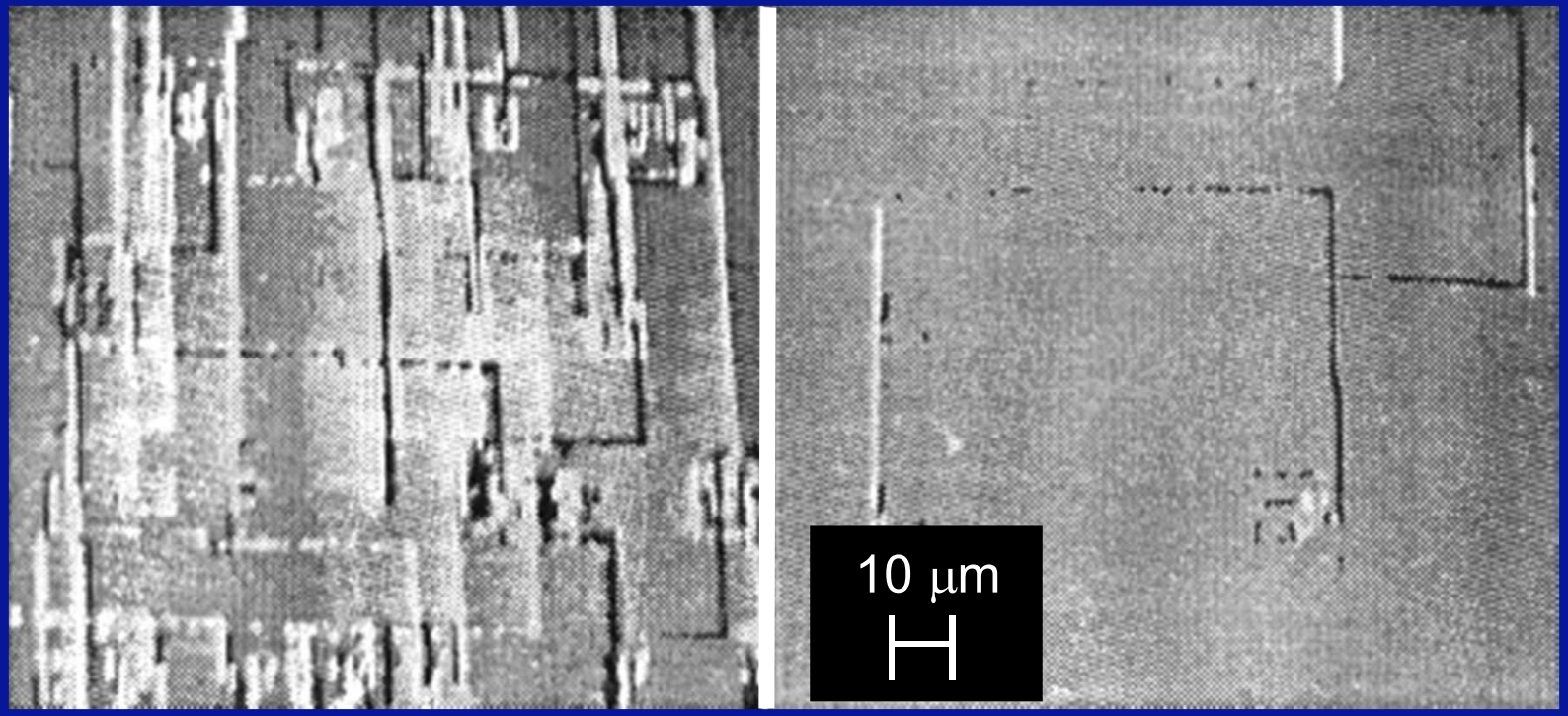


From S. Bothra et al., "A New Failure Mechanism by Corrosion of Tungsten in a Tungsten Plug Process", Proceedings of the IRPS, 1998, pp. 150-156.

CCVC Coupled with Quiescent Current (I_{DDQ}) Testing

- Information yielded: localizes high I_{DDQ} nodes
- Physics behind use: Use I_{DDQ} testing to determine vectors of high I_{DDQ}, then acquire CCVC images at those vectors, use image processing to keep only the common features, the failing node will be the only structure not lost in processing, assumes a failing node has about the same I_{DDQ} when activated
- Implementation: same hardware as CCVC imaging, need an IC tester for I_{DDQ} testing, image processing for image comparison, no alignment necessary, move of sample increases analysis time
- IC damage: same as for CCVC imaging

CCVC and I_{DDQ} Imaging Example



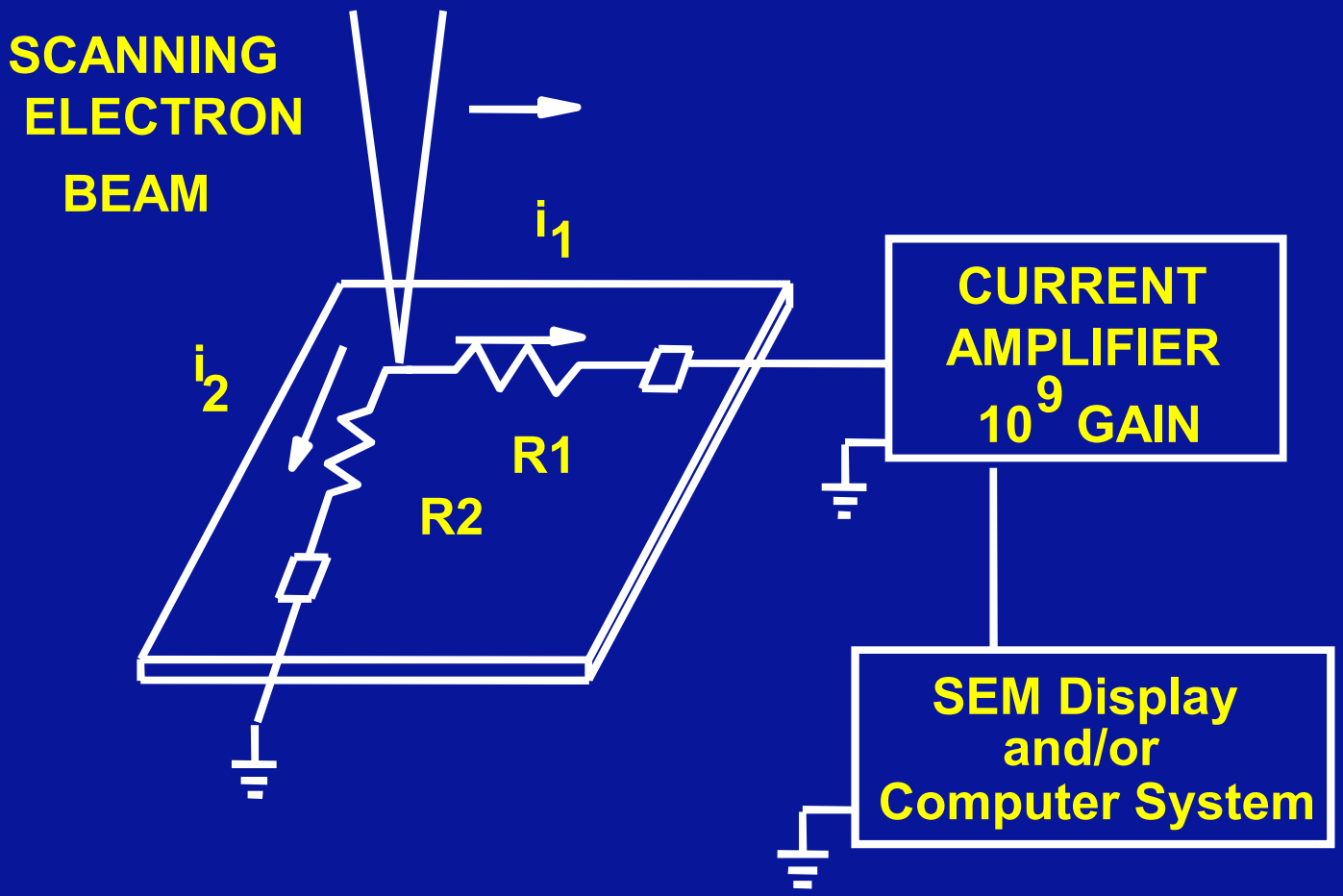
single image **16 processed images**

R. Bottini, et. al., "Failure Analysis of CMOS Devices with Anomalous IDD Currents", ISTFA, 1991, p. 381-388.

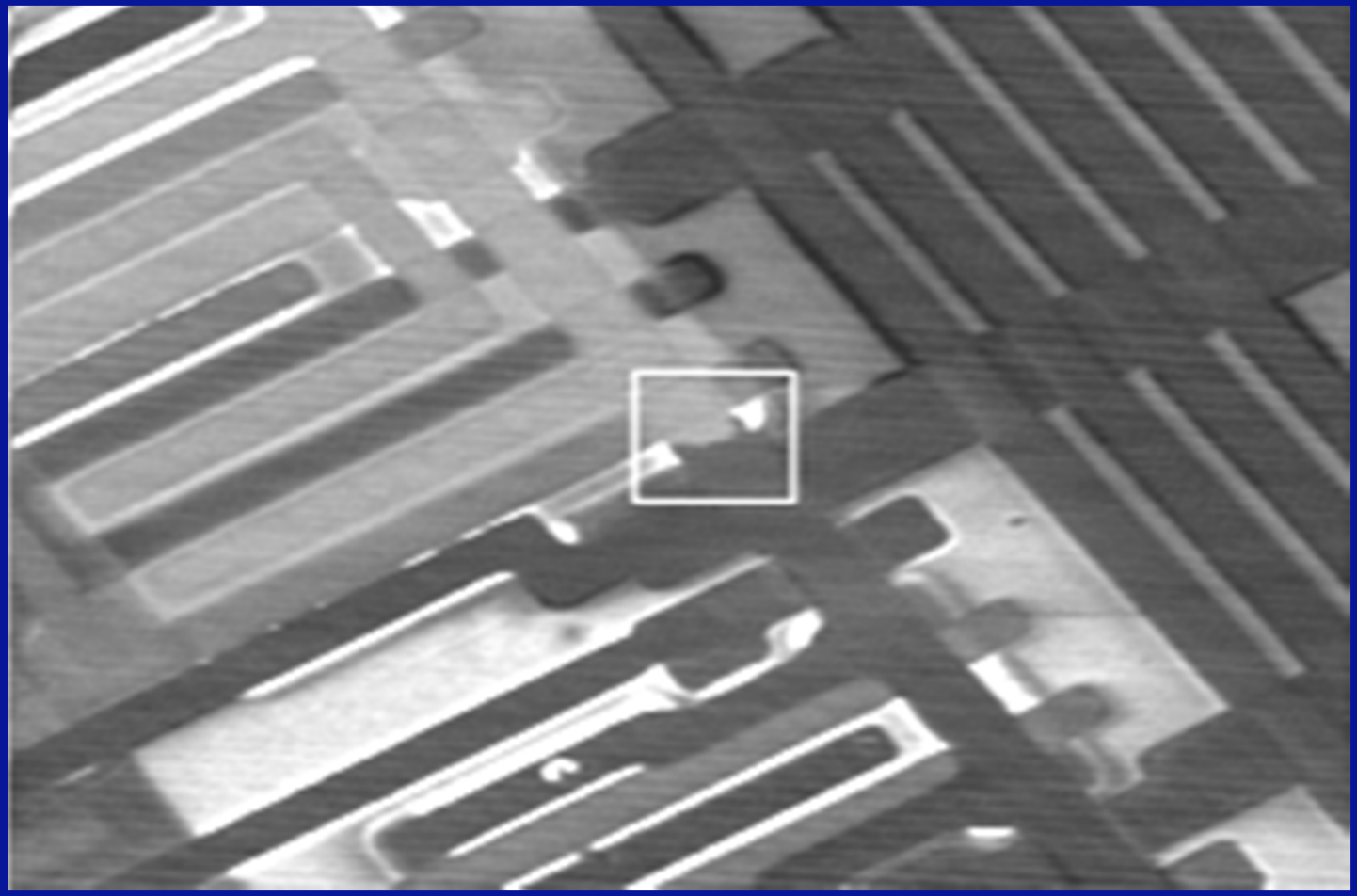
Resistive Contrast Imaging (RCI)

- Information yielded: generates a relative resistance map displaying buried conductors, locates opens
- Physics behind use: RCI uses the IC as a current divider, passivation may be intact, e-beam must reach buried conductors, portion of beam injected into conductors used to make RCI image, signals of 1 nA or less, test nodes selected by other testing, power and ground usually used, EBIC must be avoided, not all conductors "reachable" from I/O pins
- Implementation: same hardware as EBIC, choice of PBE and beam current crucial for RCI
- IC damage: performed properly no primary electrons reach MOS structures, slight x-ray dose, damage can be annealed

Resistive Contrast Imaging (RCI) System



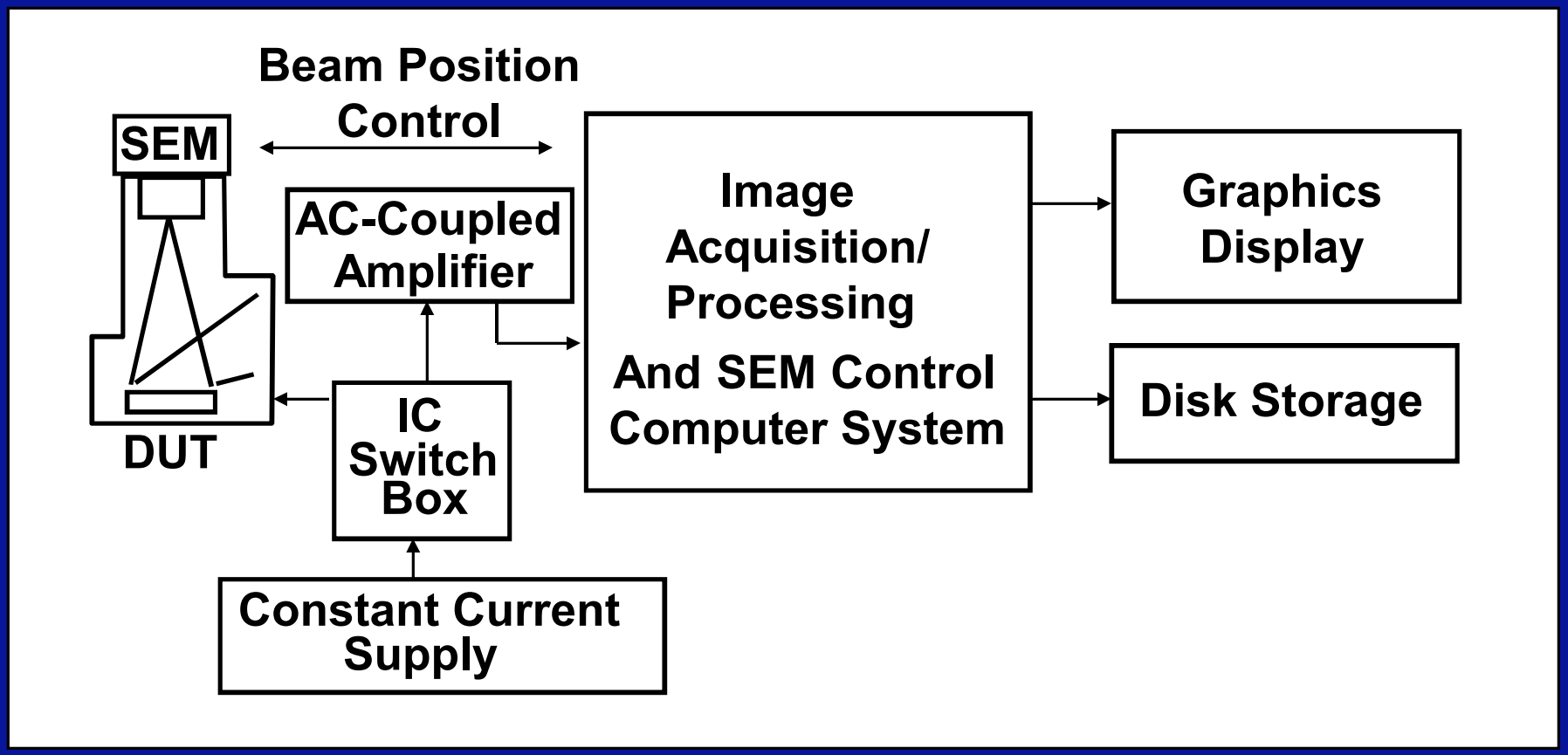
RCI Imaging Example



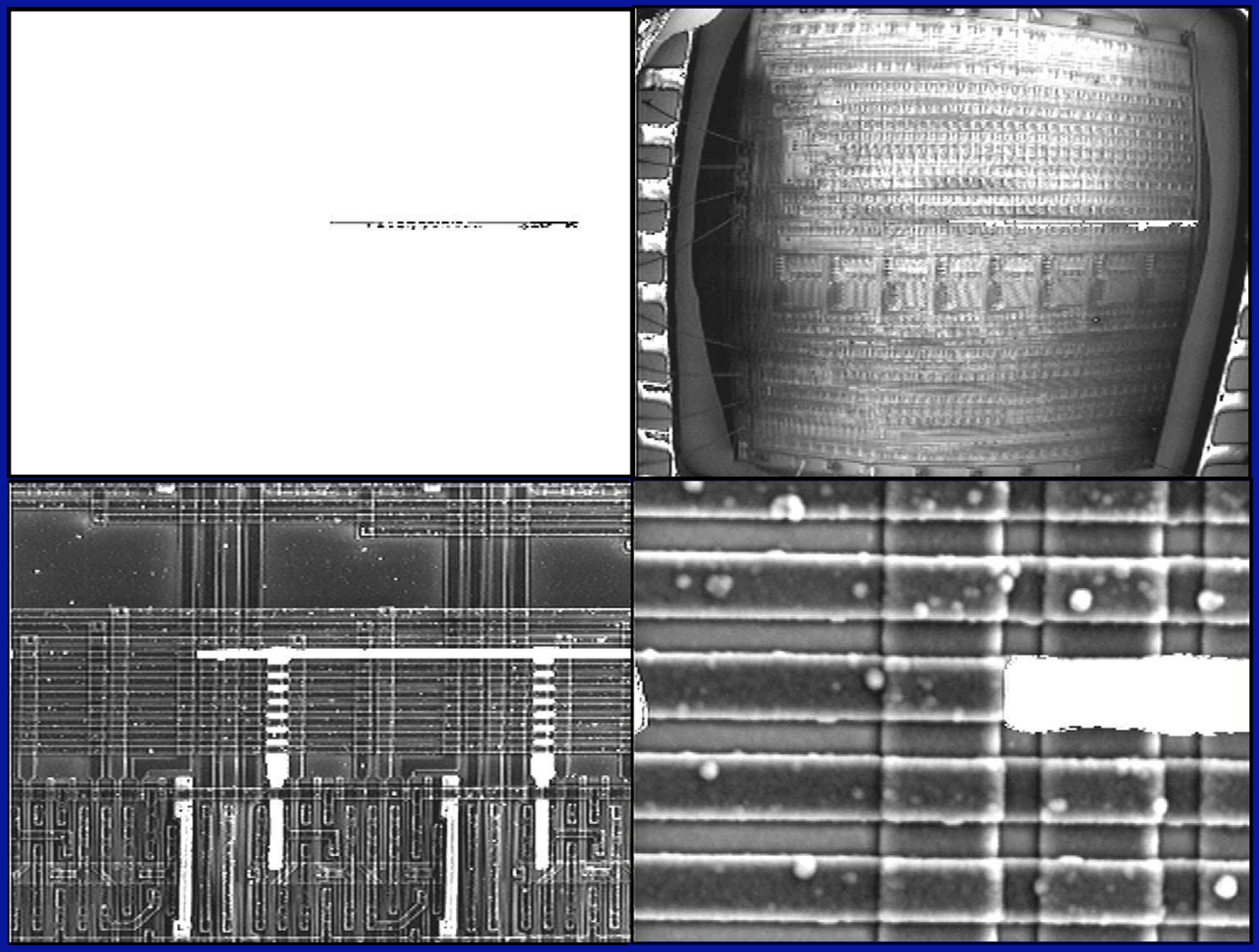
Charge-Induced Voltage Alteration (CIVA)

- Information yielded: localized open metal interconnections on passivated and depassivated ICs
- Physics behind use: supply IC with a constant current source and monitor voltage changes with e-beam scan, can locate both "complete" and QM opens, multi-layer structures may be observed by control of PBE
- Implementation: same hardware as VC except that a constant current source is used instead of a voltage supply, bias state must be non-contentive
- IC damage: same as for RCI

Charge-Induced Voltage Alteration (CIVA) Imaging System



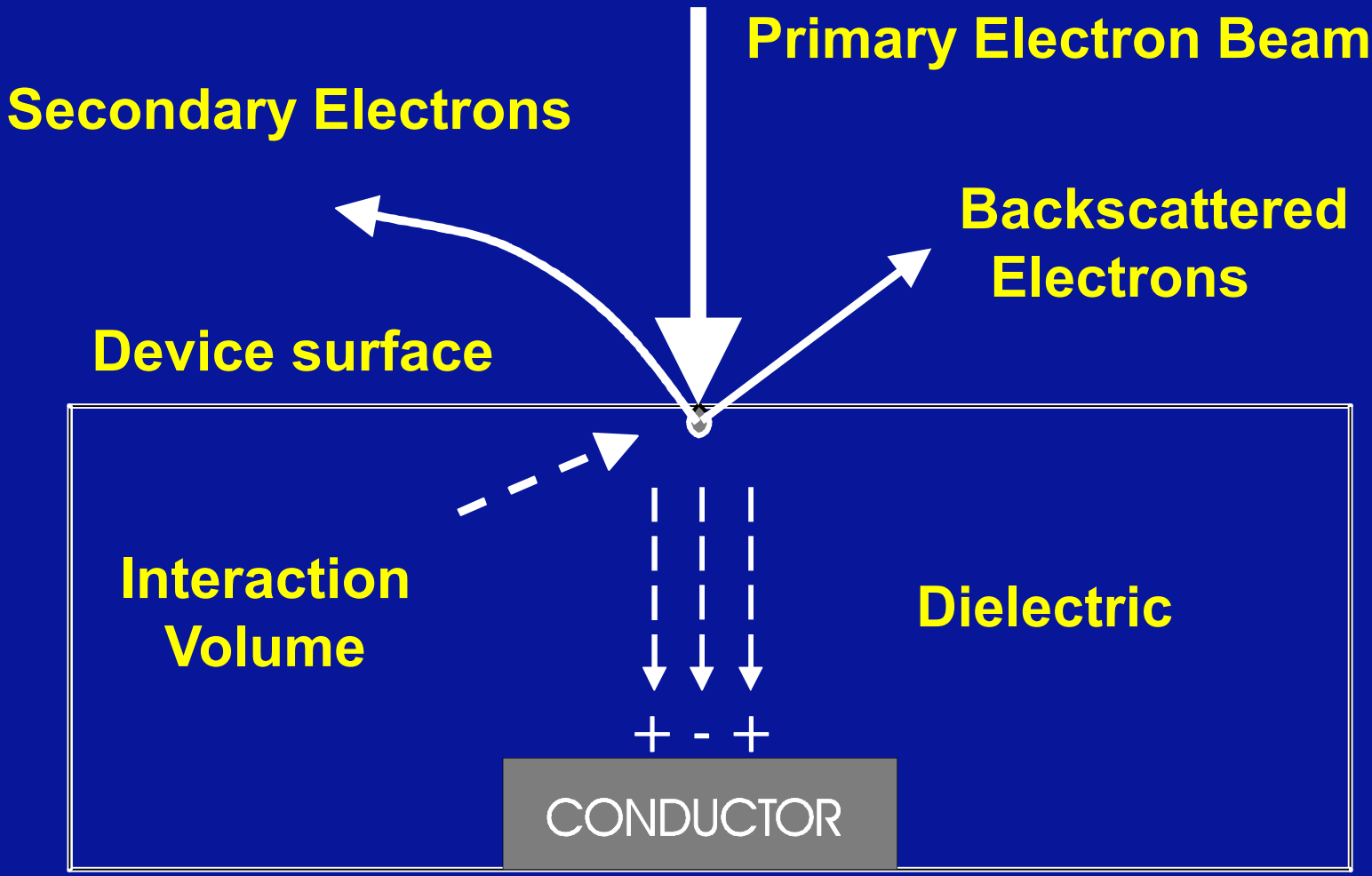
CIVA Imaging Example



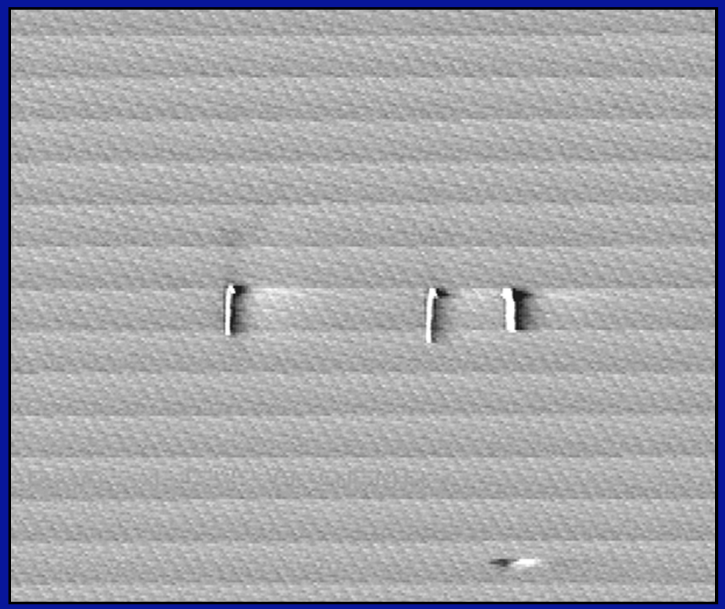
Low Energy Charge-Induced Voltage Alteration (LECIVA)

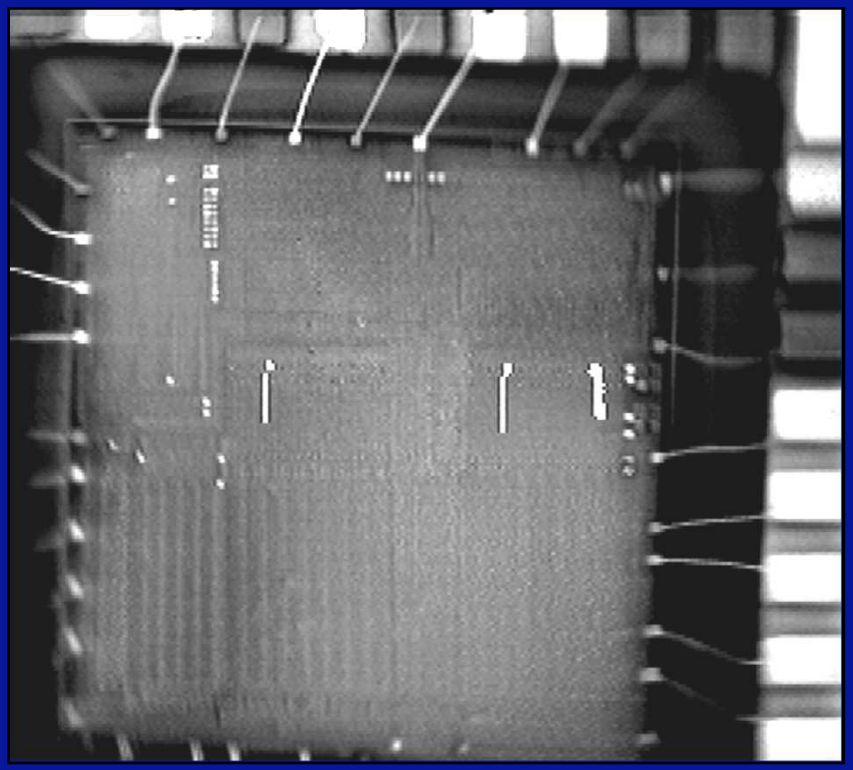
- Information yielded: localizes open interconnections on passivated ICs using low primary beam energies
- Physics behind use: LECIVA takes advantage of a change in surface equilibrium voltage (from positive to negative) with increasing beam current at low beam energy. The IC is biased similar to CIVA, using a constant current source and monitoring the changes in V_{DD} with the scan of the electron beam. Cannot probe through metal layers like CIVA.
- Implementation: same equipment as CIVA, electron beam test equipment which operates at low beam energies only can be used for LECIVA
- IC damage: same as for CCVC

LECIVA Signal Generation



LECIVA Imaging at 0.3 keV





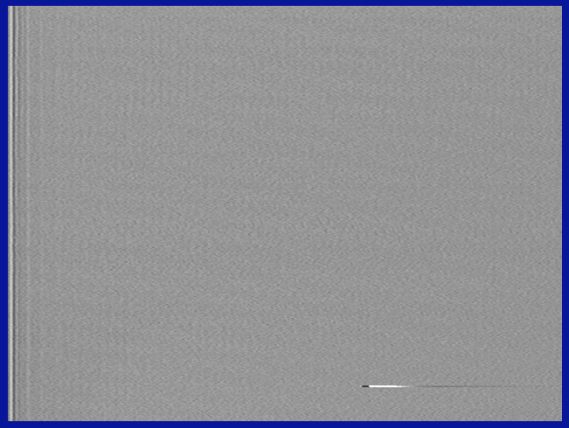
Light-Induced Voltage Alteration (LIVA)

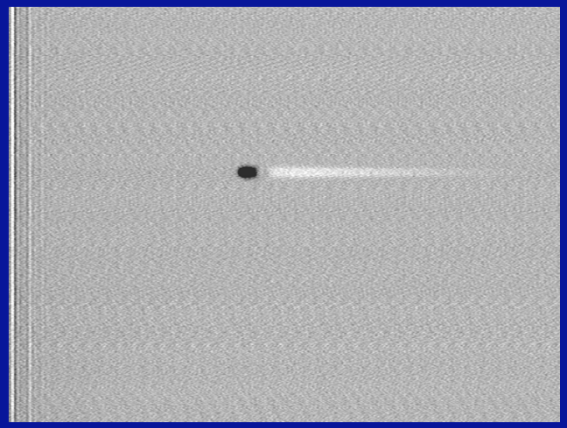
- Information yielded: SOM technique to localize diffusion related defects and transistor logic states from the IC front and backside
- Physics behind use: photons with energy greater than Si indirect bandgap make ehps (like EBIC), ehps affect IC operation, supply IC with a constant current source and monitor voltage changes with photon beam scan (like CIVA), diffusion defects and logic state voltage gradients alter IC power demands, proper IR laser makes backside analysis possible

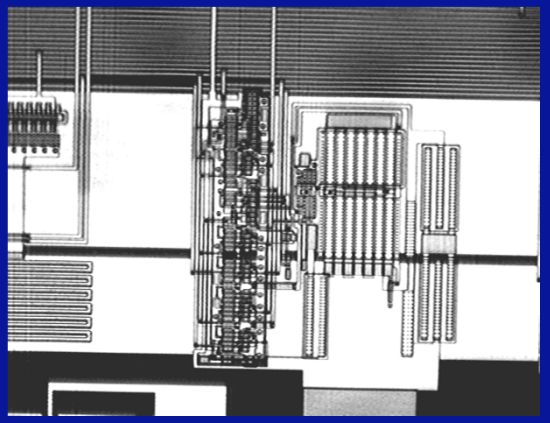
Light-Induced Voltage Alteration (LIVA) con't

- Implementation: need SOM with proper wavelength lasers, electrical connection, sample preparation for backside analysis, high power ICs and heavy doping decreases signal sensitivity
- IC damage: backside sample preparation must be done with care

Backside LIVA Defect Imaging



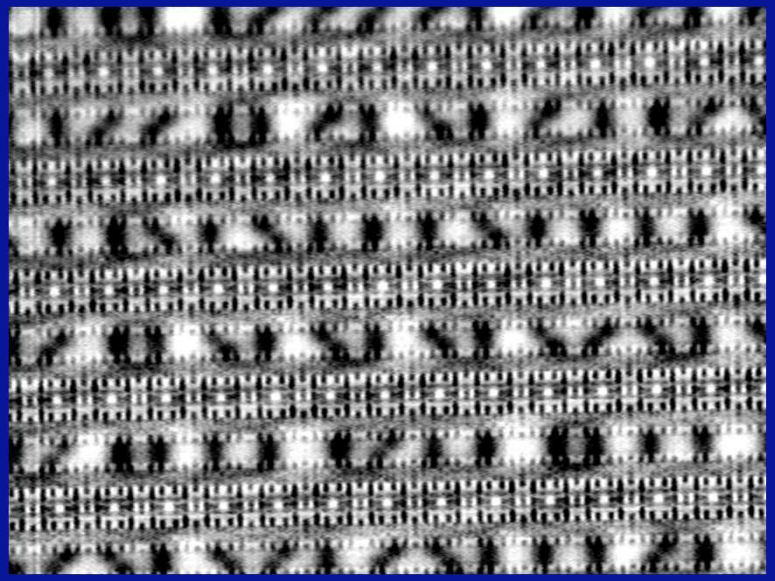




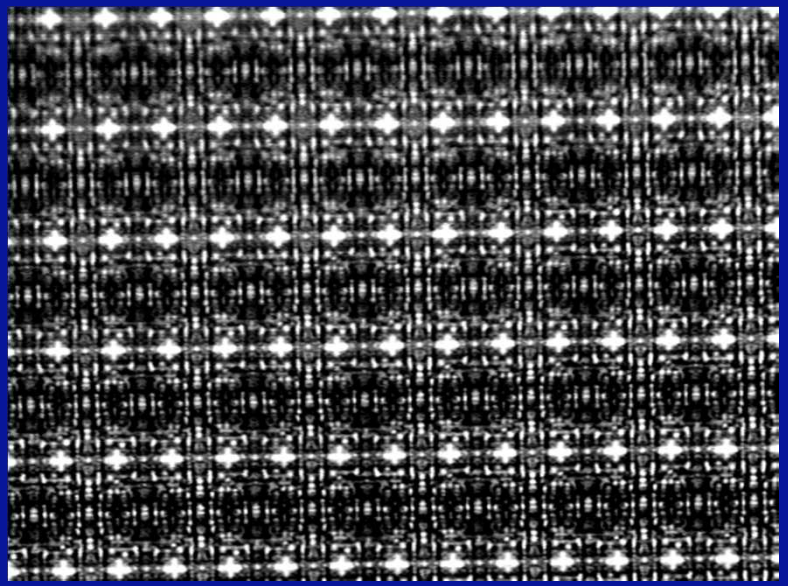
LIVA Images

Reflected Images

Backside LIVA Logic State Imaging



LIVA Image



Reflected Light Image

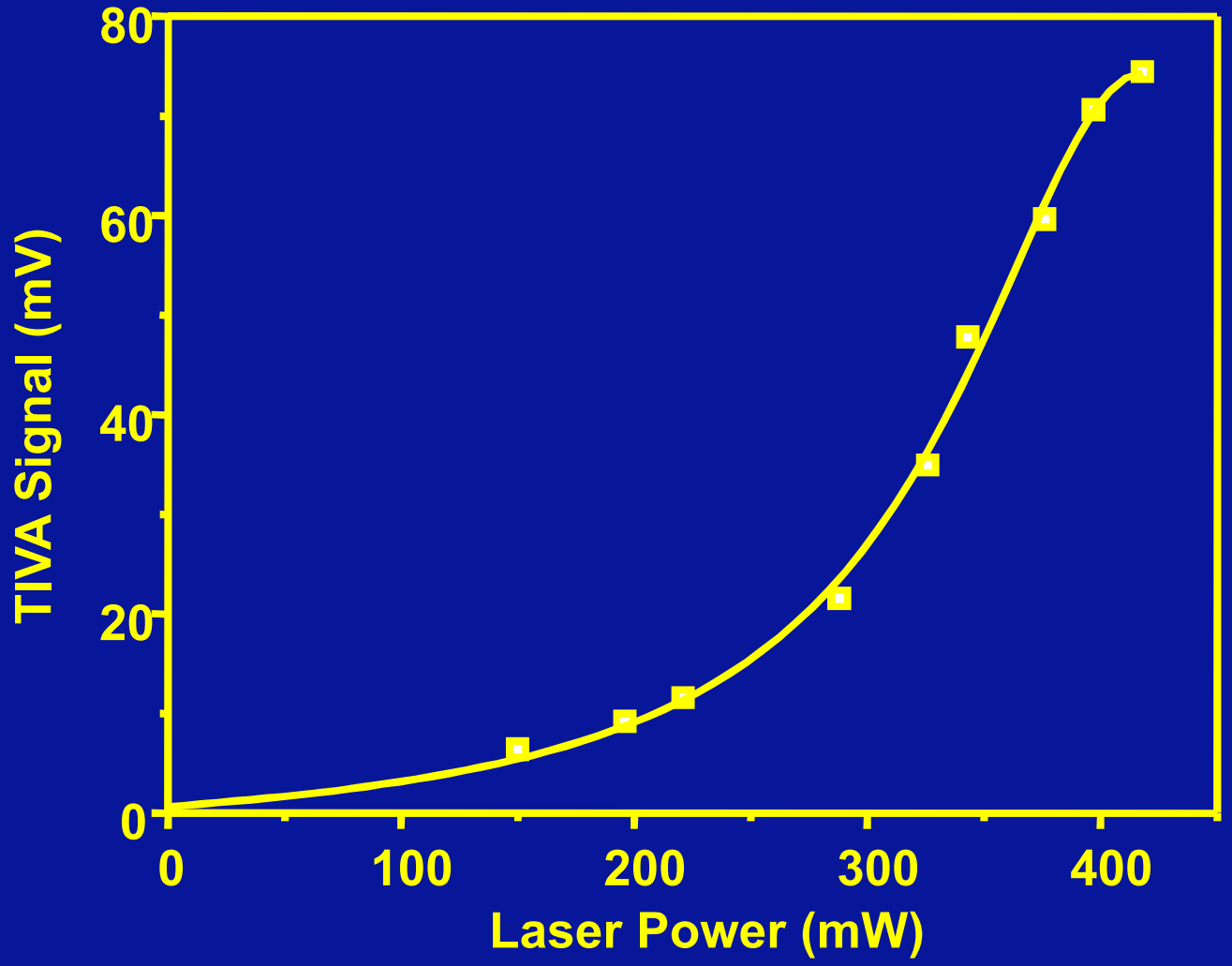
Thermally-Induced Voltage Alteration (TIVA) and Seebeck Effect Imaging (SEI)

- Information yielded: SOM technique to localize open interconnections and short sites from the IC front and backside
- Physics behind use: photons with energy less than Si indirect bandgap to generate heat, no ehps, shorts localized by resistance change (OBIRCH), opens located by Seebeck effect-thermal gradients produced voltage gradients, sensitivity increase using constant current biasing, (constant current OBIRCH proposed by Nikawa), non-linear signal gain with laser intensity

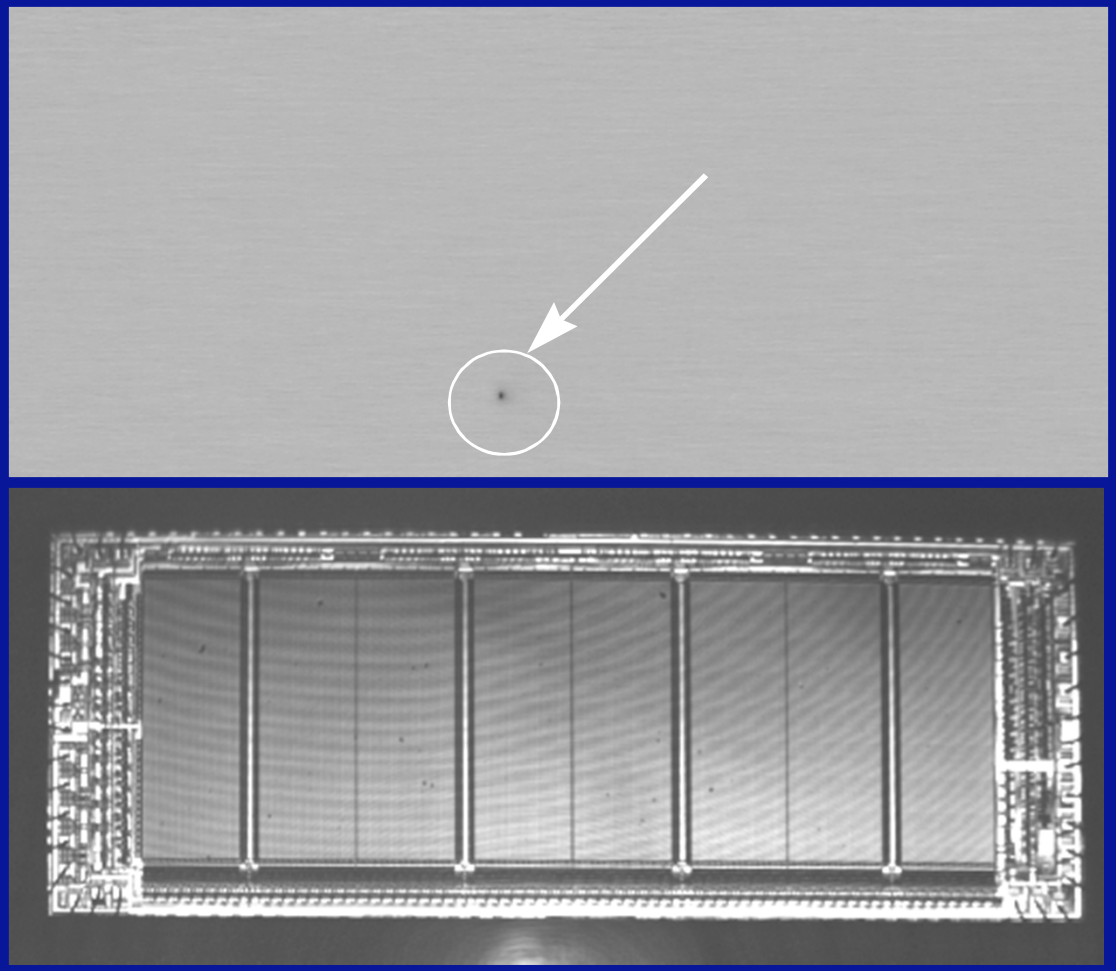
Thermally-Induced Voltage Alteration (TIVA) and Seebeck Effect Imaging (SEI)

- Implementation: same as LIVA, need proper laser λ, same limitations apply as with LIVA, SEI signals weaker than other "IVA's"
- IC damage: backside sample preparation must be done with care

Non-Linear Response with Laser Power



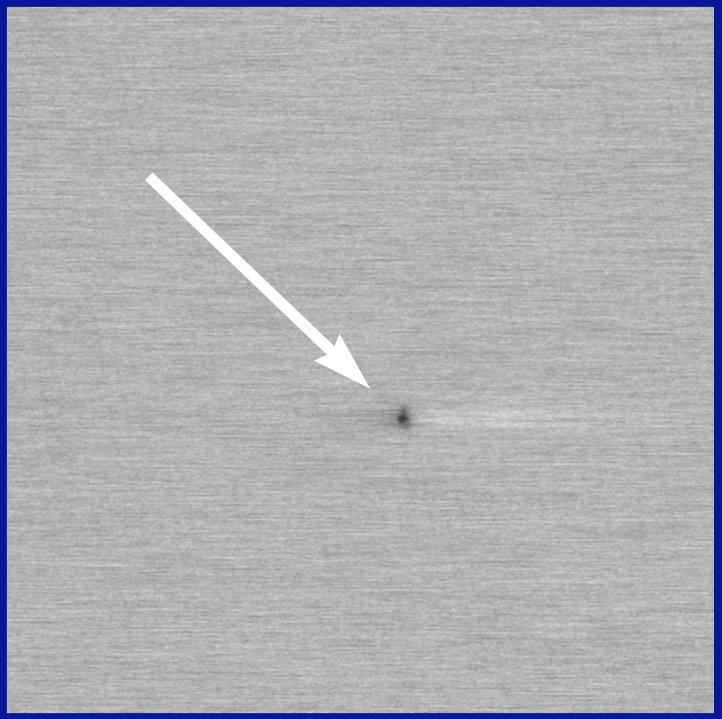
Front Side TIVA Imaging Example, 1 MB SRAM



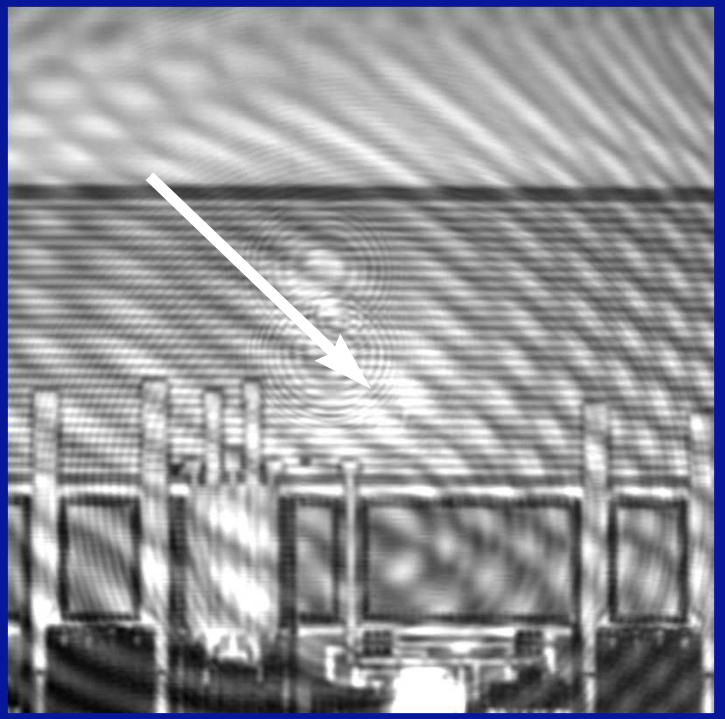
TIVA image

Reflected light image

Backside TIVA Example

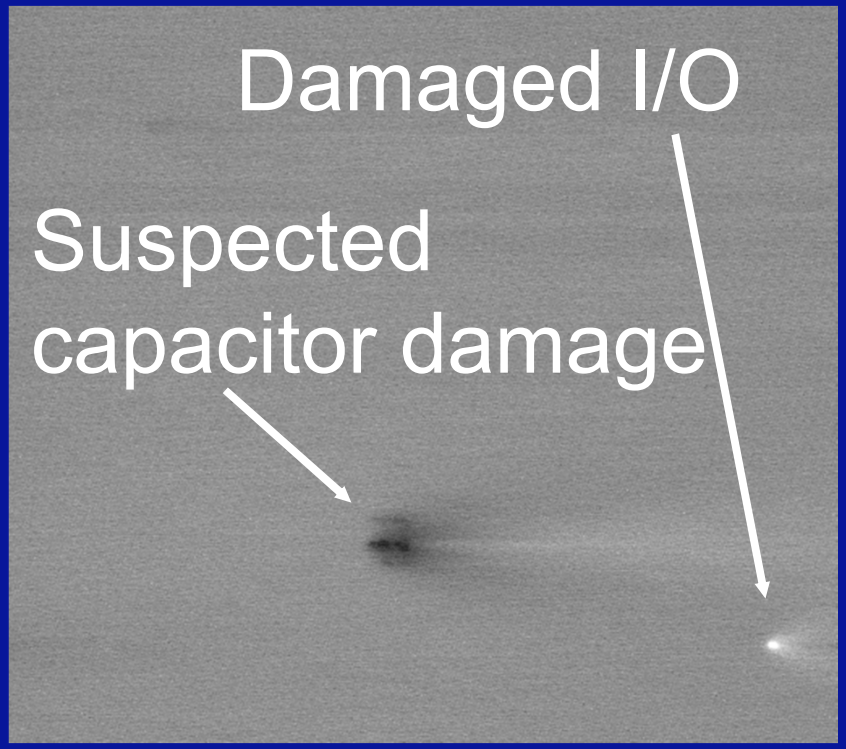


TIVA image

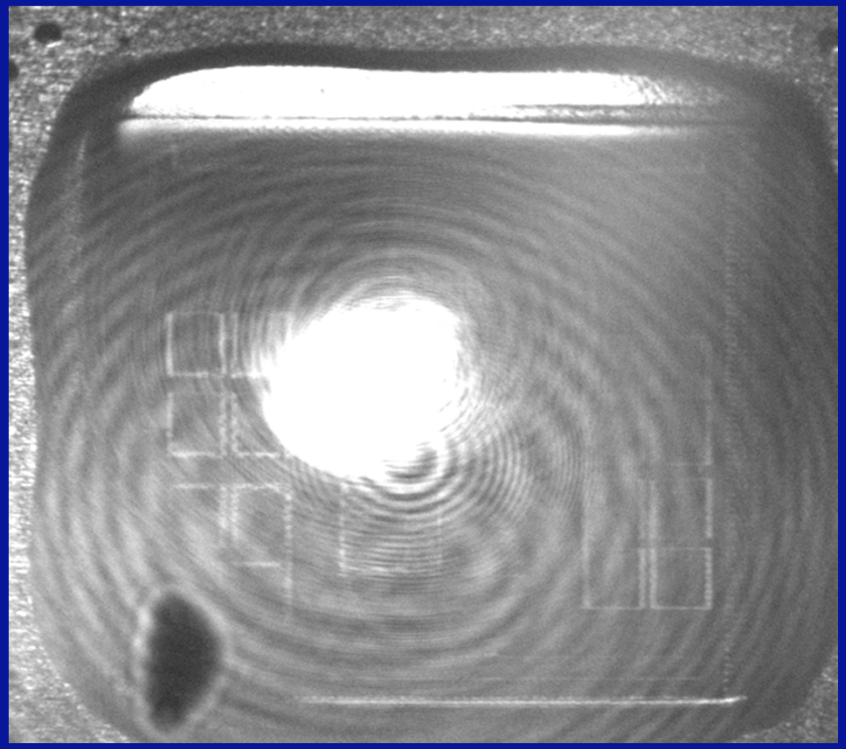


Reflected light image

TIVA Example - Microprocessor

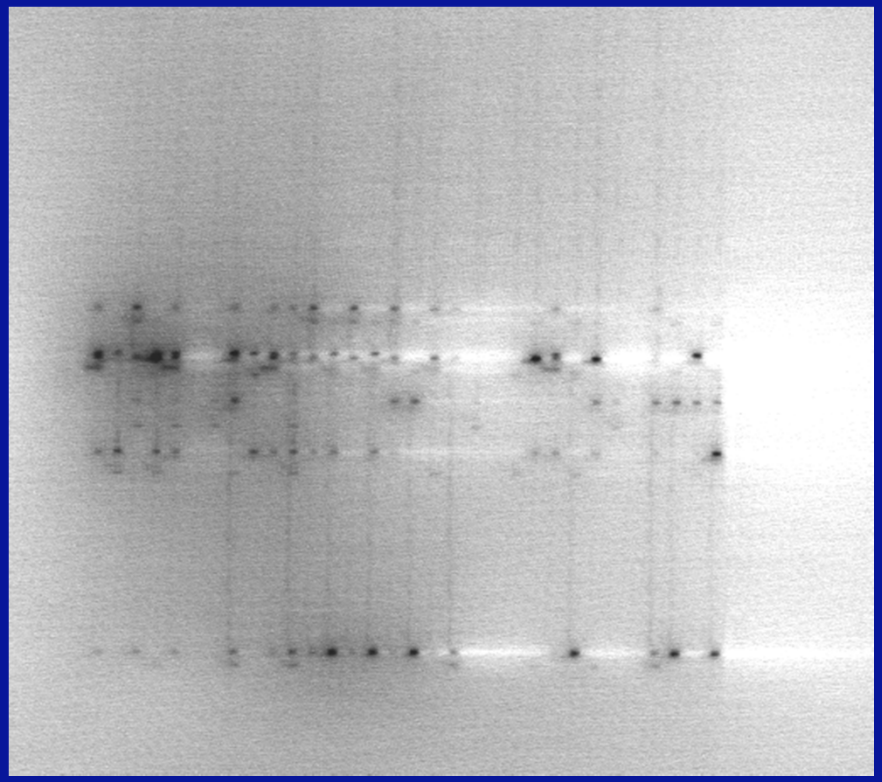


TIVA Image
(6LM 0.3 μm technology)

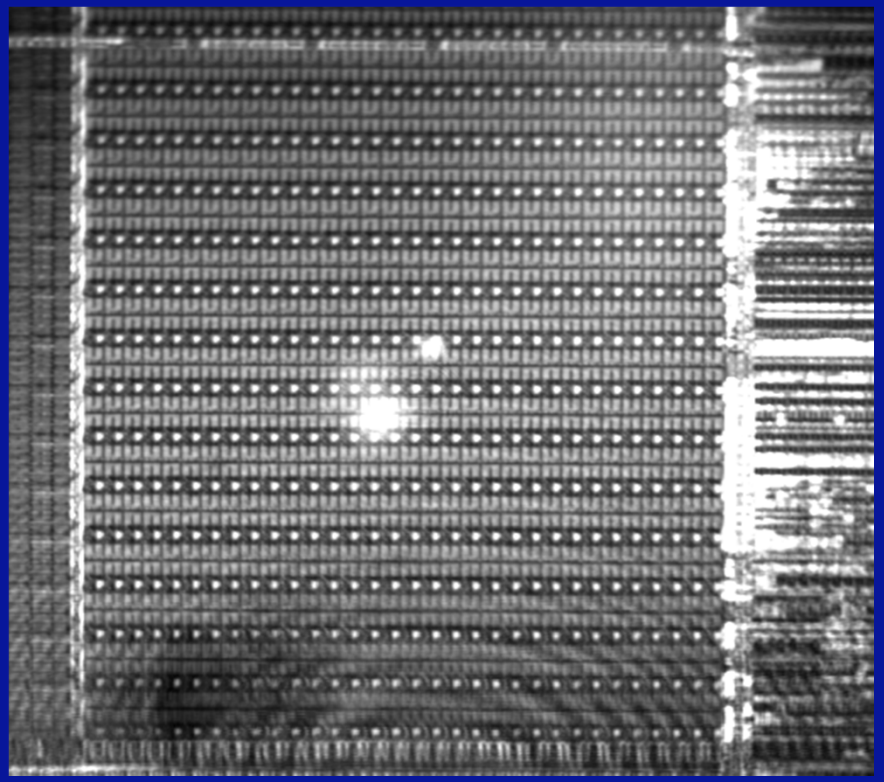


Reflected Image

TIVA Microprocessor Failure: Suspected Capacitor Damage

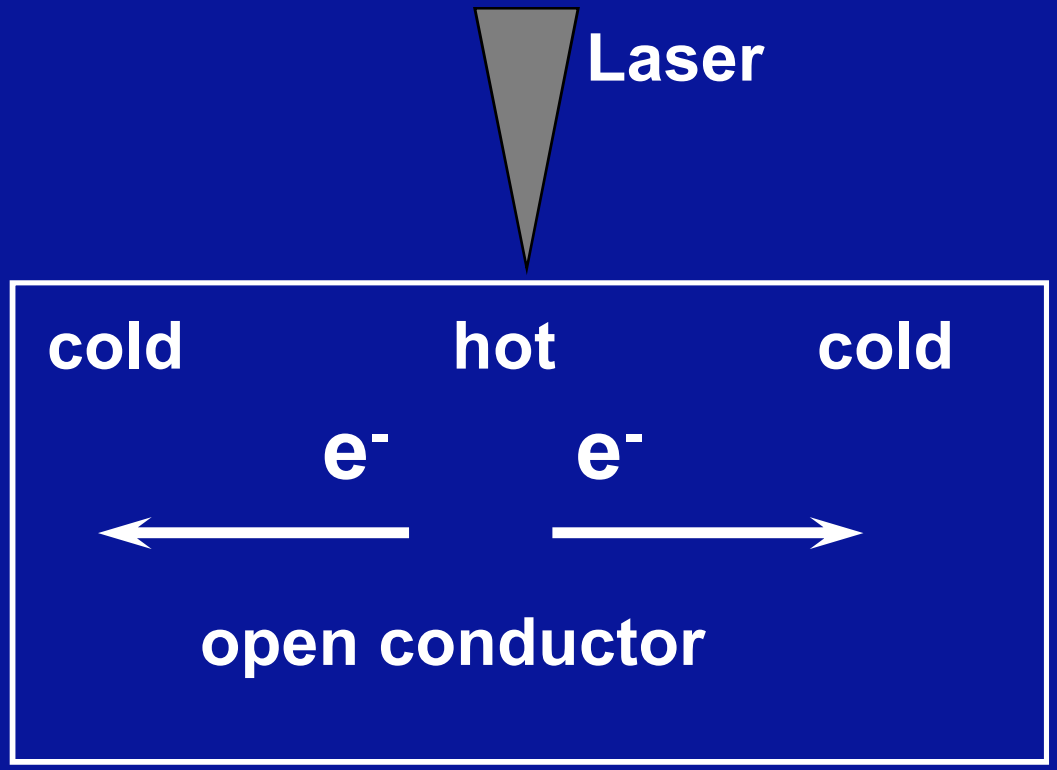


TIVA Image
(6LM 0.3 μm technology)

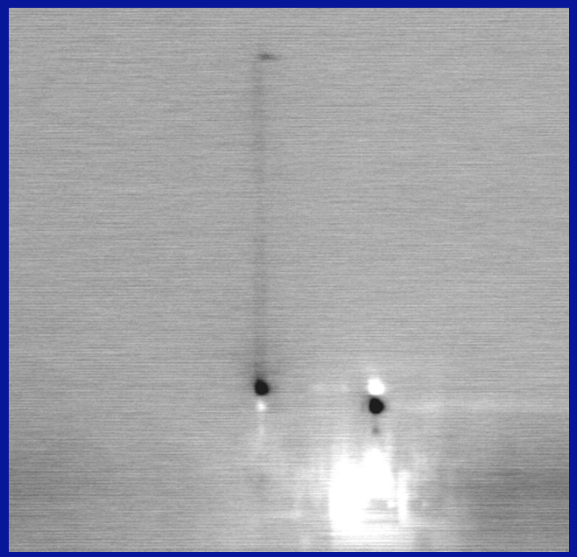


Reflected image

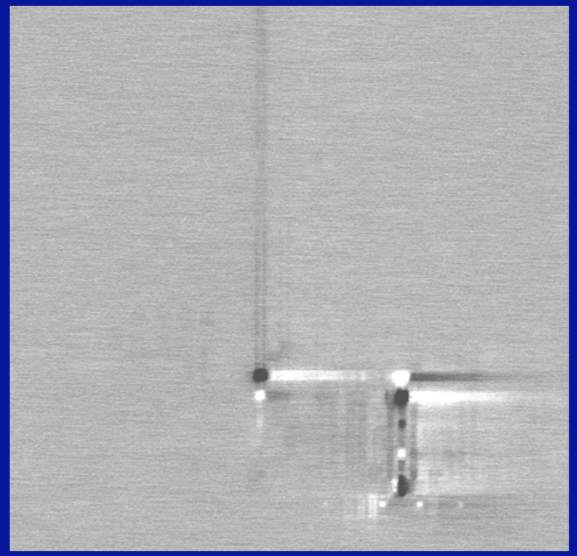
Seebeck Effect Voltage Generation



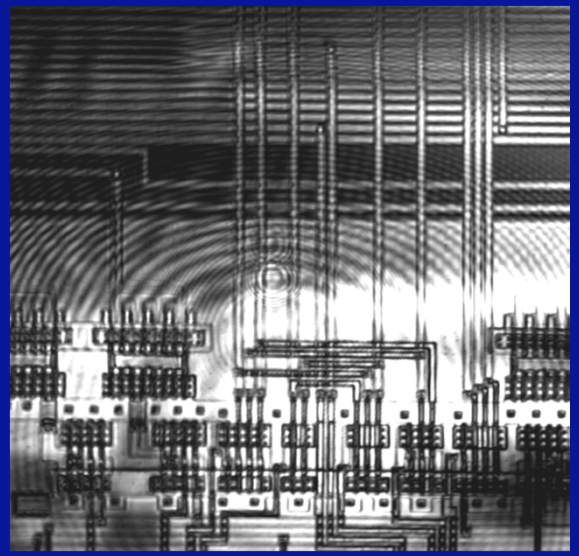
SEI Signal Improvement, 80C51 FIB Cut (Backside)



Before
45 min acquisition



After
2 min acquisition

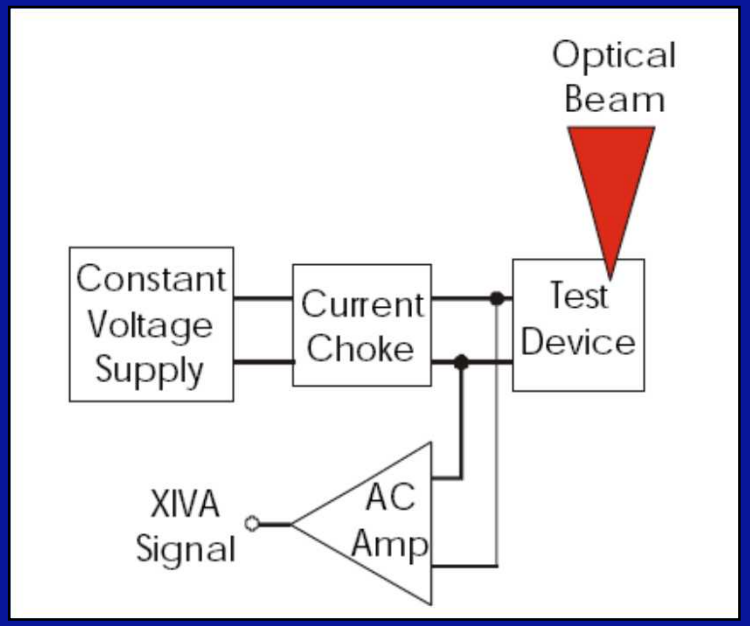


SEI Images

Reflected image

Externally Induced Voltage Alteration (XIVA)

- An ac current choke and a constant voltage supply
- Measures voltage changes in choke



From R.A. Falk,"Advanced LIVA/TIVA Techniques", ISTFA, 2001, p. 59.

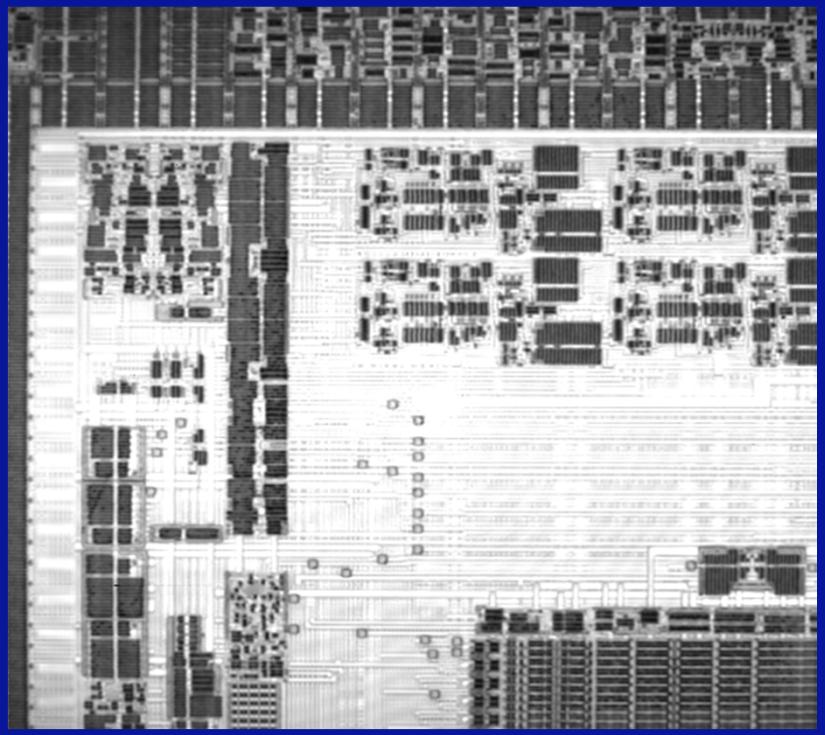
Soft Defect Localization (SDL)

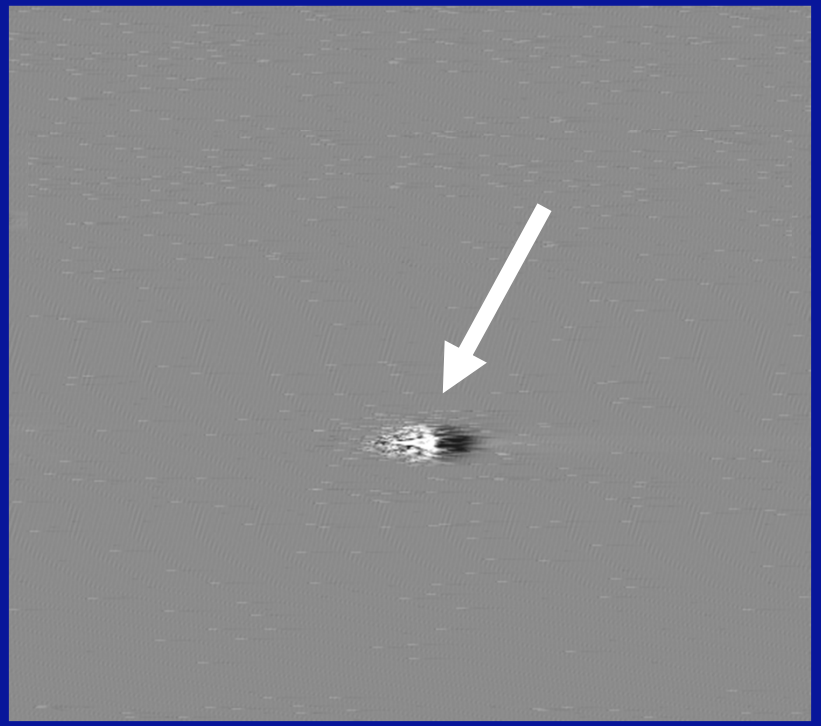
- Information yielded: localizes soft defects (resistive vias, leaky gate oxides, ILD, process variation, timing marginality) from the front and backside of an IC
- Physics behind use: A scanned 1.3 μm laser locally heats the sample IC similar to SEI/TIVA/OBIRCH. Soft defects will change their properties with heating. Detected by operating the device and monitoring the pass/fail status as the laser is scanned. The resulting SDL image yields the location of the soft defect.

Soft Defect Localization (SDL)

- Implementation: same equipment as SEI/TIVA/OBIRCH with the addition of IC stimulus/monitoring equipment
- IC damage: same as for TIVA/SEI
- LADA (Laser-Assisted Device Alteration) uses similar detection hardware with a photocurrent producing laser source
  - Depending on laser power and transistor geometry can slow down or speed up switching devices
  - Useful for critical timing investigations

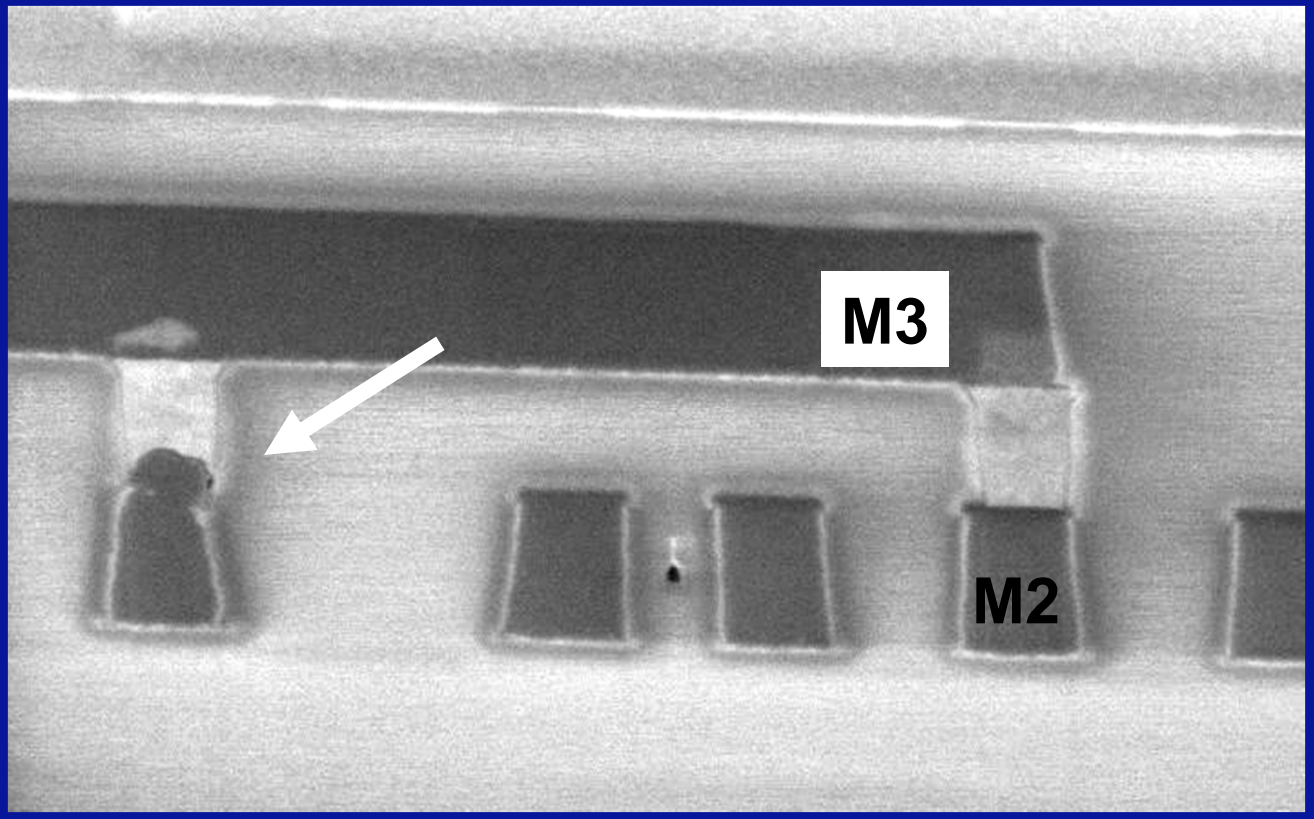
SDL Example-Resistive Interconnection





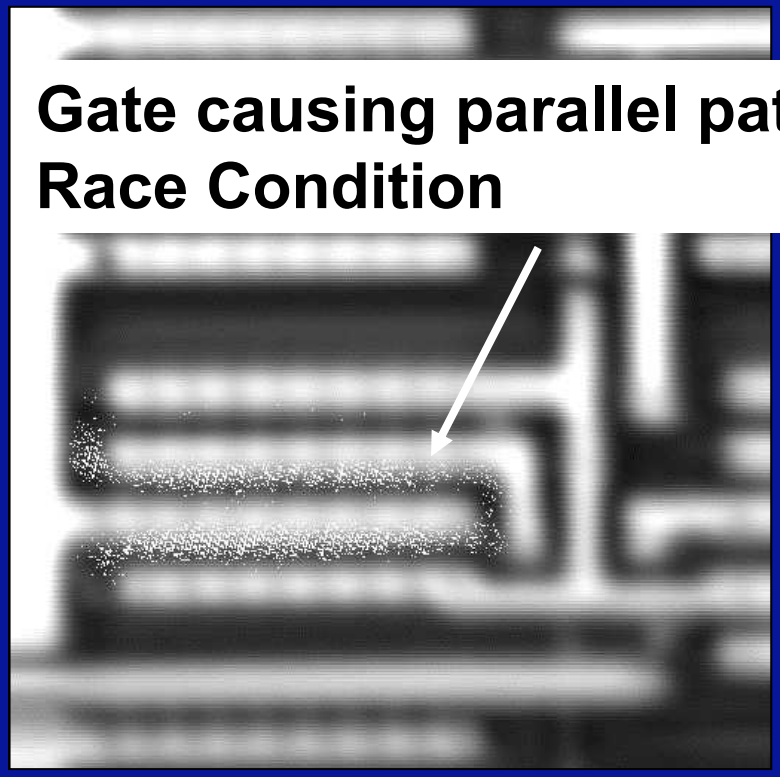
Fails at low temperature, high speed

SDL Example-Resistive Interconnection



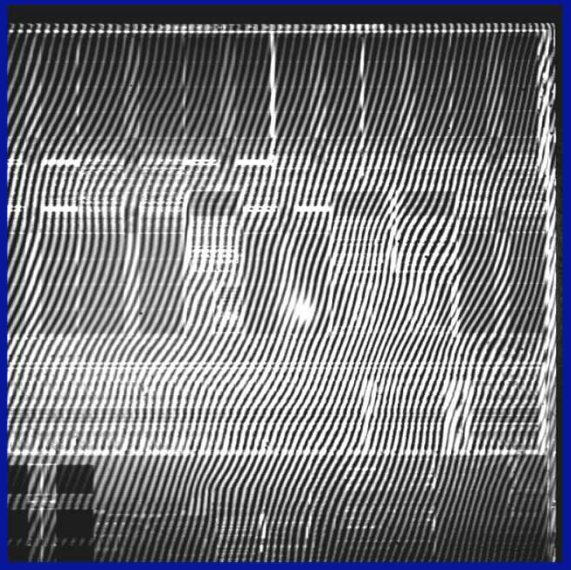
Al extrusions clearly seen on left via

SDL Example – Parallel Path Race Site

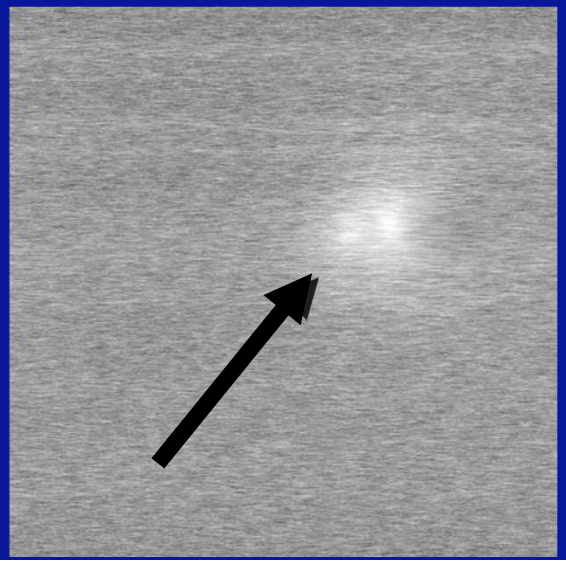


SDL Timing Analysis

- Examination of a microprocessor from the backside
- Intermittently failing in control circuitry of instruction cache
- SDL site identified as a weak link in a serial path
- Improvements made the site less susceptible to process variations



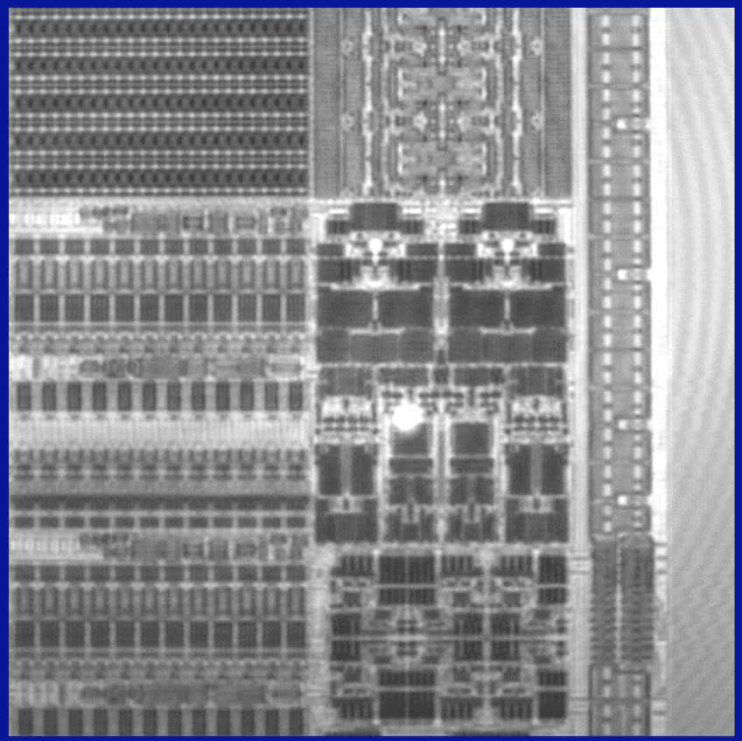
Backside reflected image



SDL Image

SDL Timing Analysis

Higher Magnification Images



Reflected light image

SDL image

Conclusions

- Electron and optical beam probing are powerful tools for failure analysis
- Capabilities and flexibility should insure their place in failure analysis for the foreseeable future