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Flip-Chip and Backside Techniques Seminar ISTFA '07

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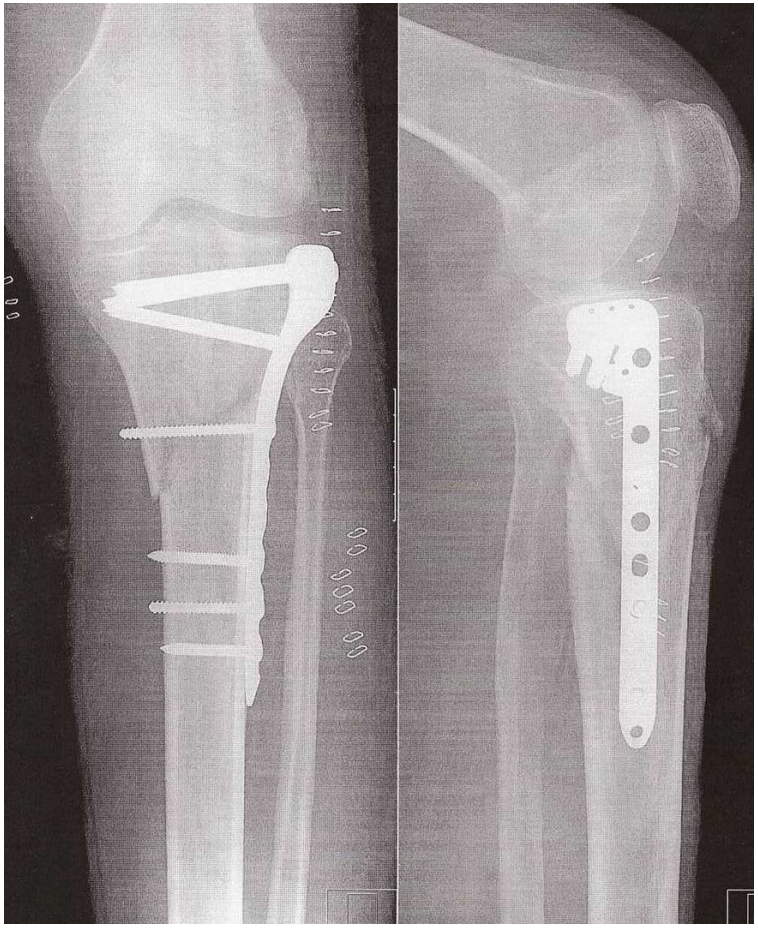
Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Important Parts of Failure Analysis

Failure Localization

Corrective Action



Purpose

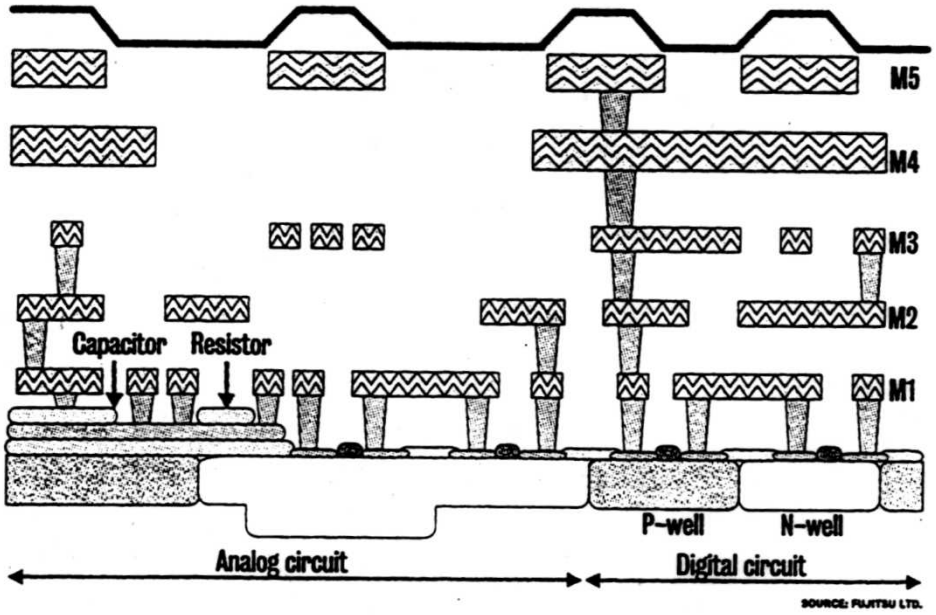
To describe the basic physics needed to understand backside technique application and physical preparation of samples for backside IC analysis.

Outline

- Introduction
- Basics
  - Light transmission through silicon
  - Optical image formation through silicon
- Backside preparation techniques
  - Global Si thinning
  - Local Si thinning/Precision probe hole milling
- Addendum Material: Backside FA techniques
  - Passive (emission-based) techniques
  - Active techniques
- Conclusions

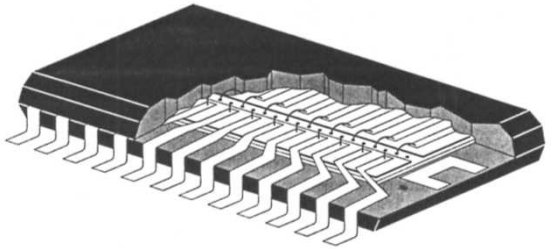
Why FA from the Backside of the Die?

Multi-layer metallization

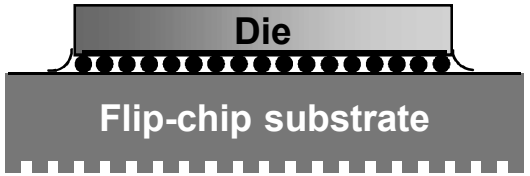


new packaging techniques e.g.

LOC (Lead On Chip)

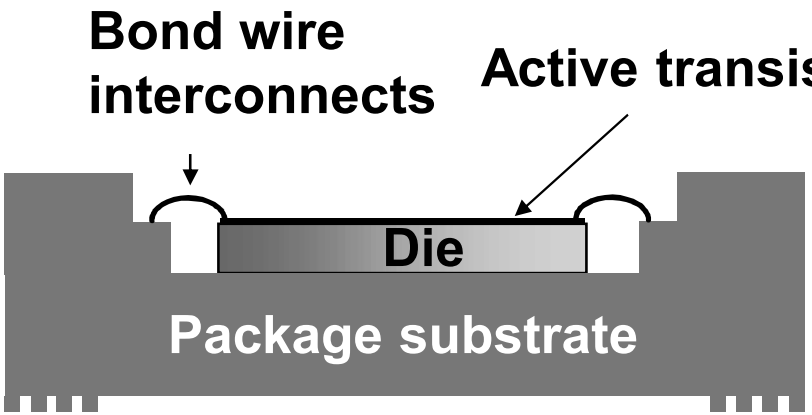


Flip-Chip

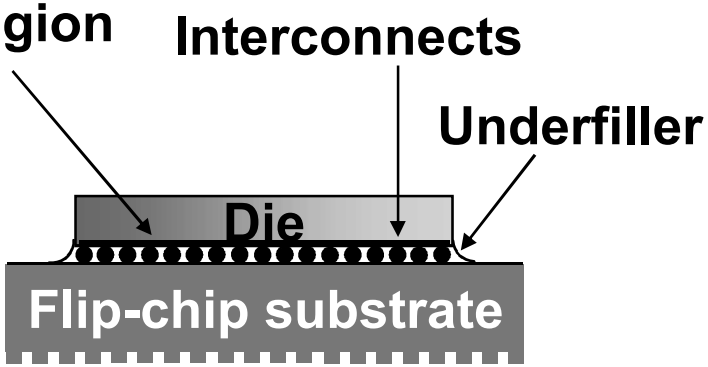


Data taken from Fujitsu

Wirebond vs. Flip-chip Packaging

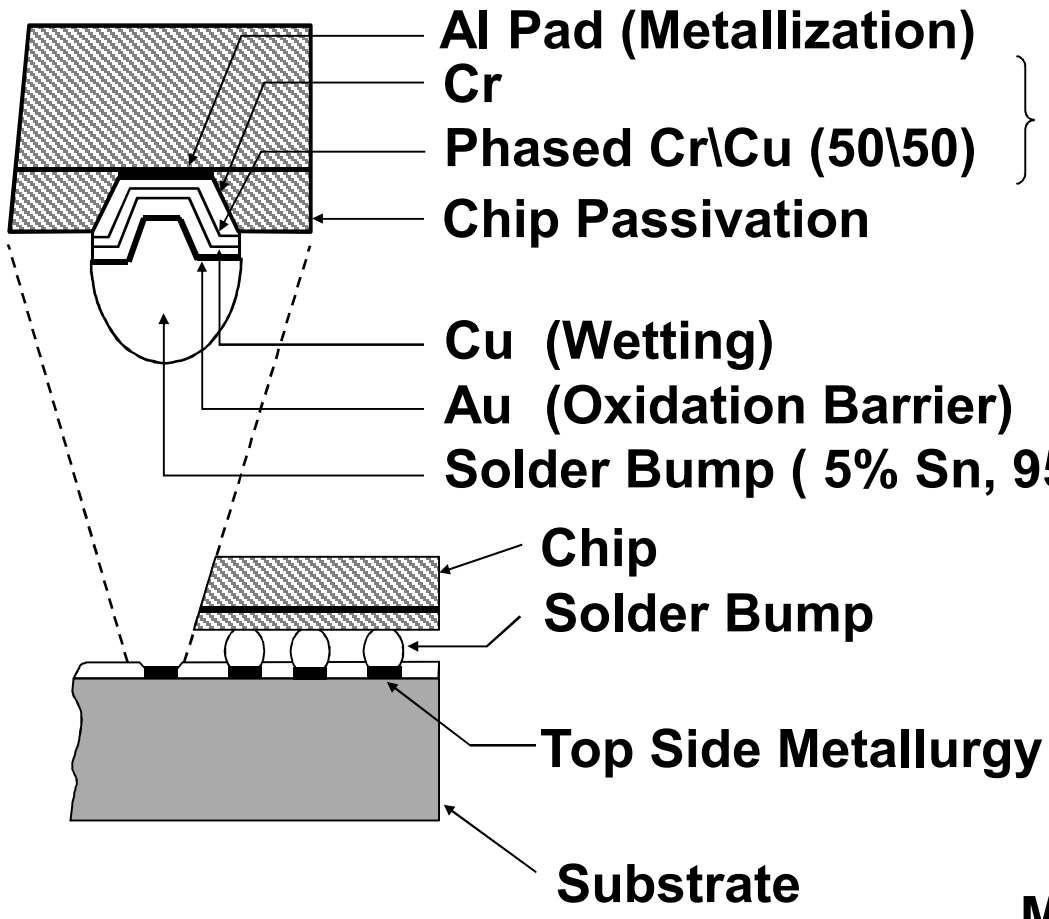


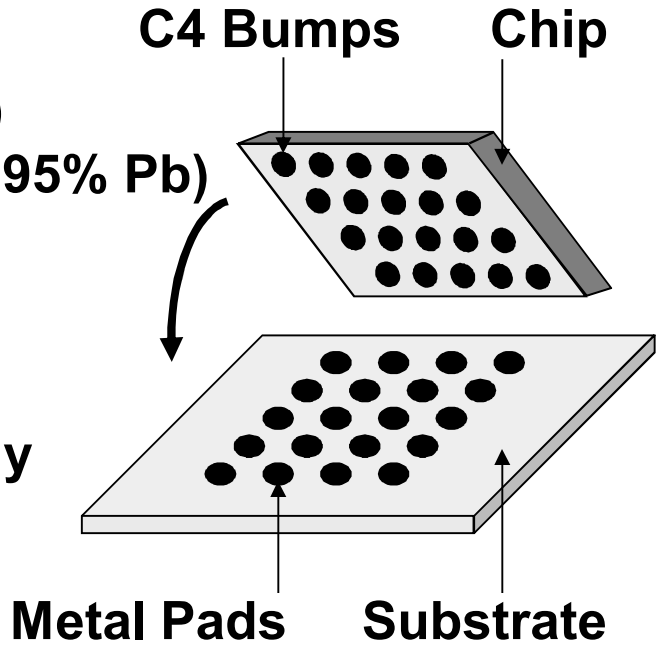
Wirebond package die



Flip-chip packaged die

C4 (Controlled Collapse Chip Connection) Technology



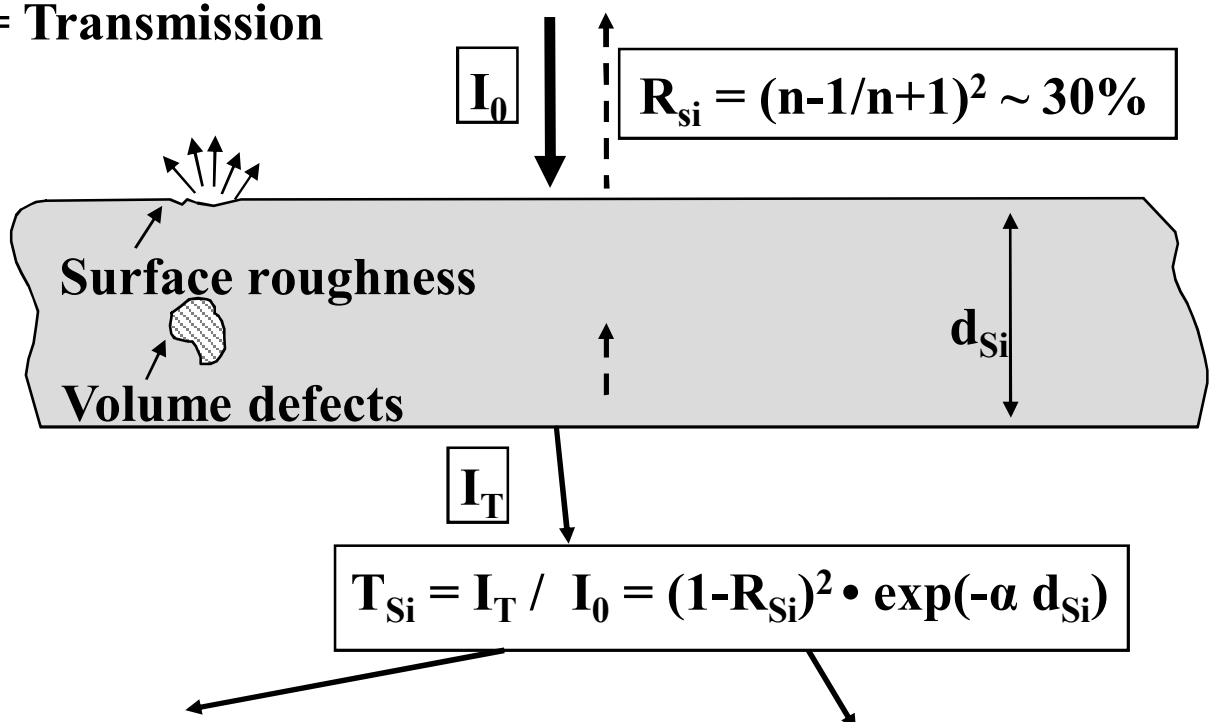


Major Benefits of Flip Chips

- Flip chips are more slim and compact ---> lighter weight products
- Flip chips permit higher speeds and enhanced electrical performance (electrical parasitics and paths are reduced
- Flip chips permit a higher I/O density at smaller chip size
- Flip chips permit a higher power dissipation/ enhance thermal dissipation
  ----> flip chips are used in multimedia products, portable electronic products, audiovisual products, (notebook) PC‘s, workstations (microprocessors), etc.

Transmission Through Bulk Si

R = Reflection
T = Transmission

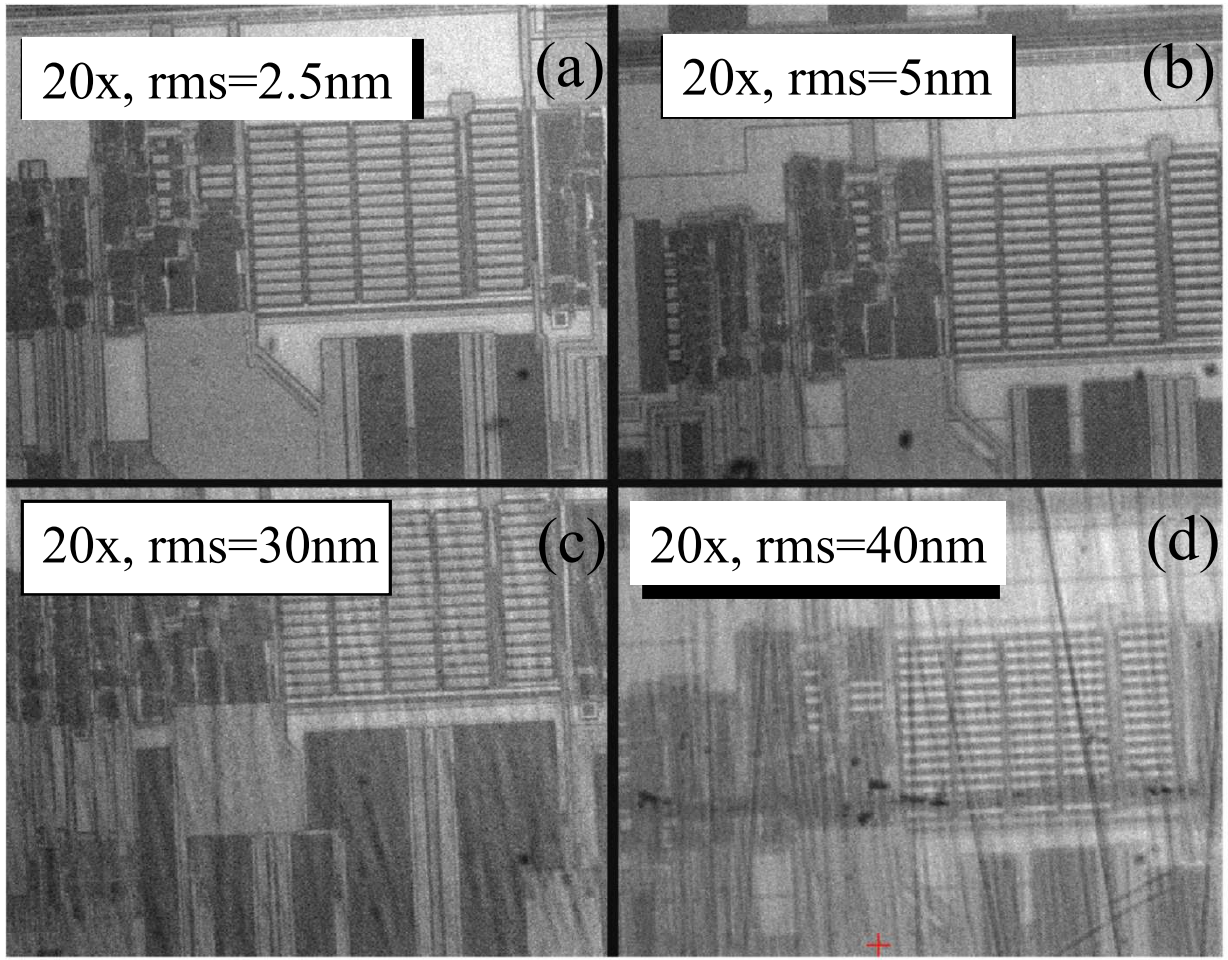


scattering due to surface roughness

$\alpha_{Si}(\lambda)$ = bandgap related absorption
$\alpha_{n,p}(\lambda)$ = free carrier absorption
α_{volume} = scattering due to volume defects (to neglect)

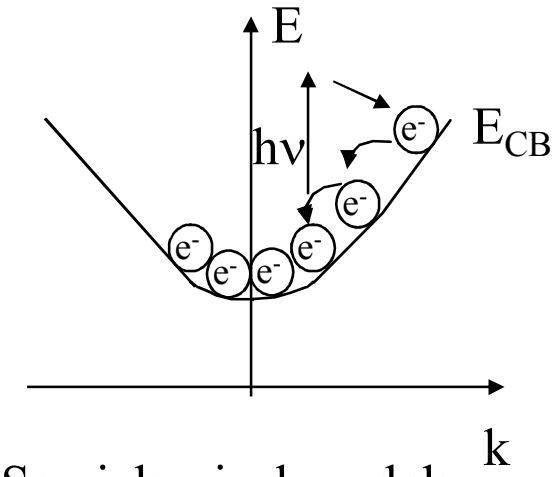
Scattering due to surface roughness

Images (a) - (d): substrate doping 1 x 10^{15} cm^{-3}; d_{Si}= 150µm



⇒ rms (root mean square) < 5nm

Free carrier absorption
(intraband absorption, α)

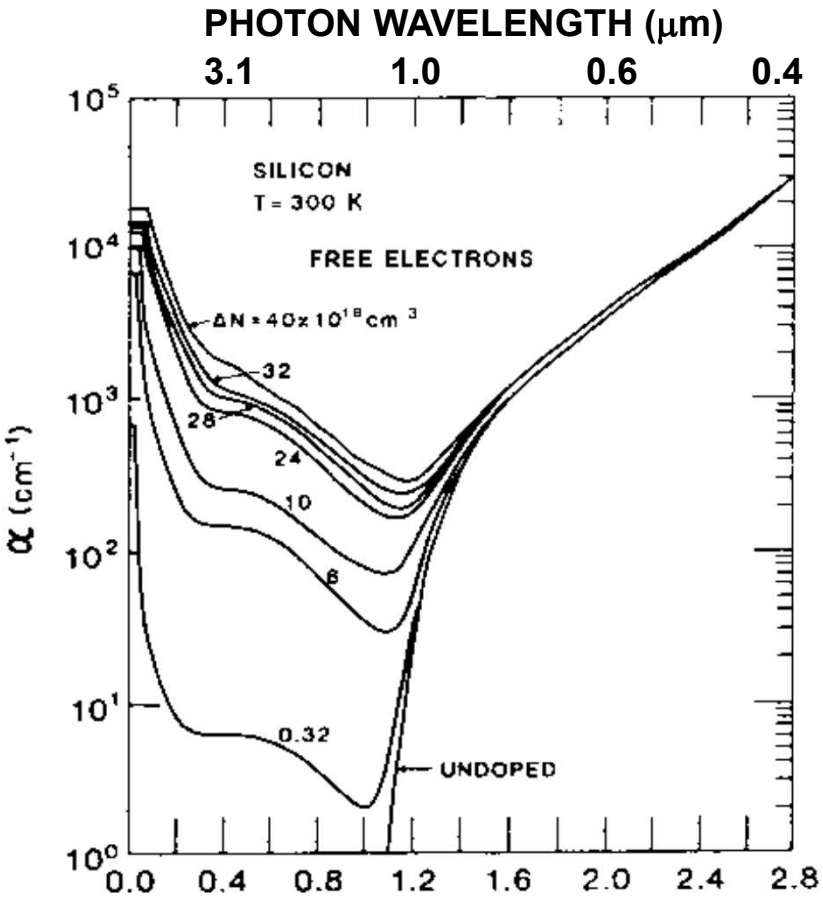


Semiclassical model:

wavelength doping concentration

α prop. to $\frac{\lambda 2n}{(m^*)2\mu}$

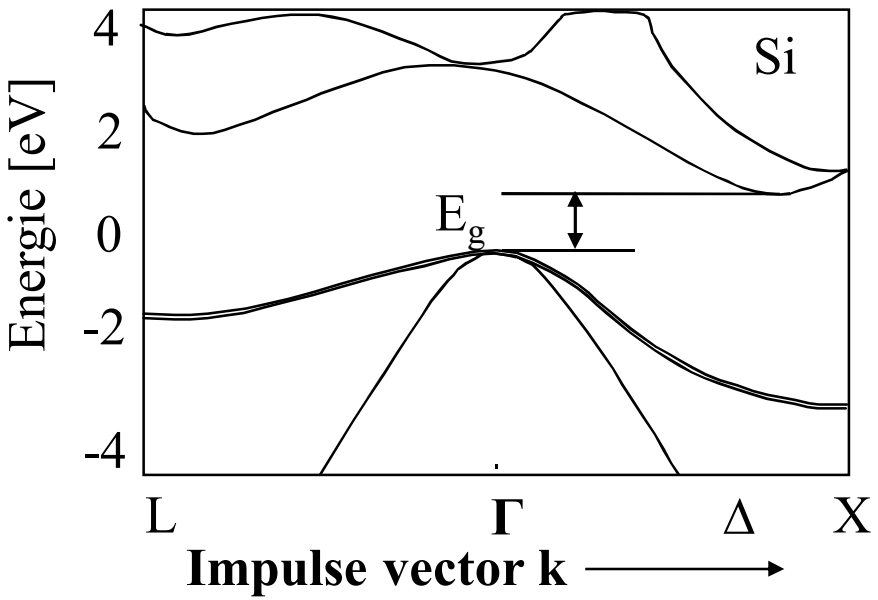
effective mass mobility



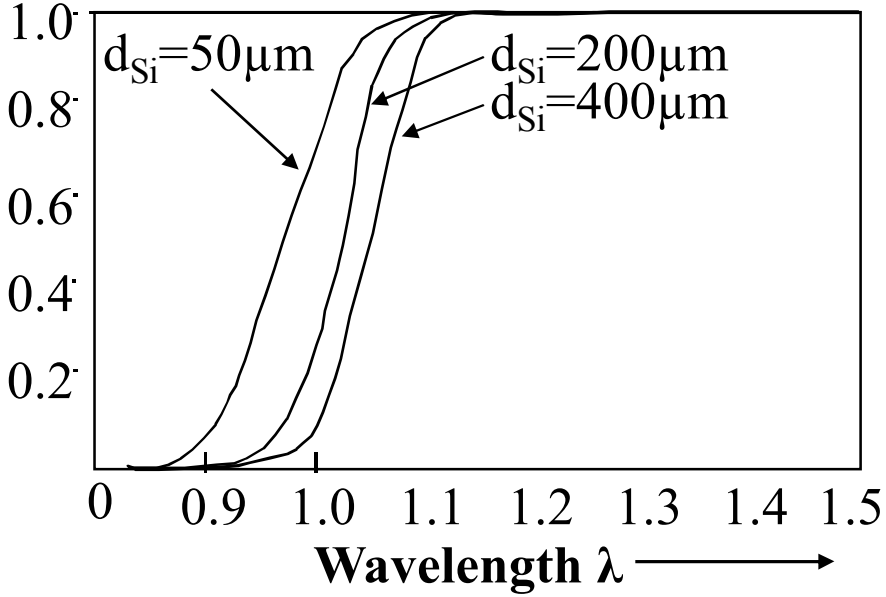
$N_e = 5 \times 10^{18}$ cm^{-3} ⇒ ID = ≈ 4% (d = 400 μm, 1.3 μ

Band-gap related absorption
(interband absorption)

Band diagram of Si



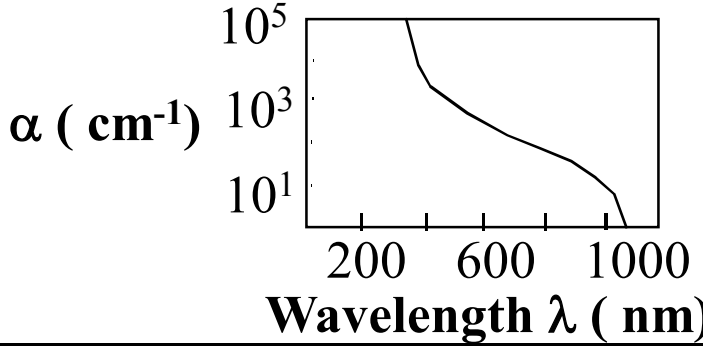
Transmission of undoped Si



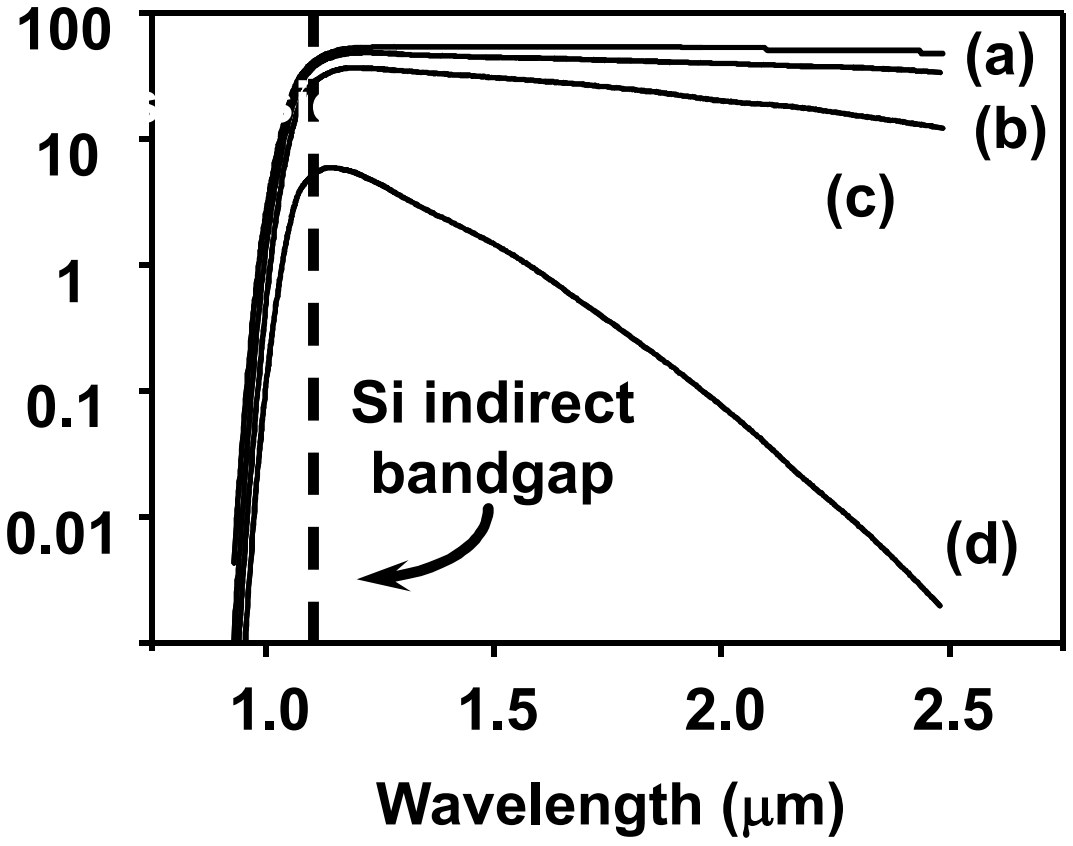
E_g=1.12 eV (300 K)

Si (E_g=1.12eV or 1107nm)

T proportional to $e^{-\alpha d_{Si}}$



IR Transmission
625 μm of p-Doped Silicon

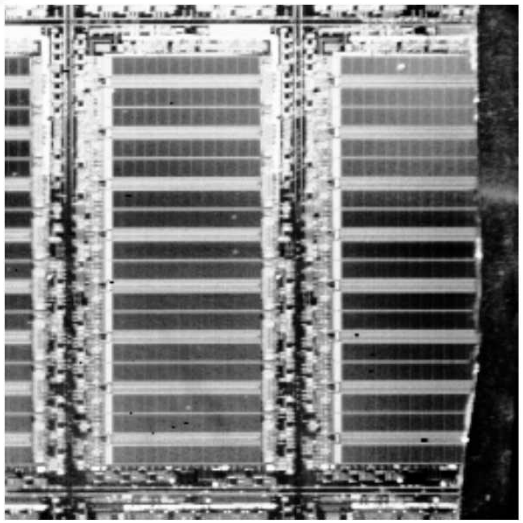


Dopant Conc.
x 10^{16} cm^{-3}
(a) 1.5
(b) 33
(c) 120
(d) 730

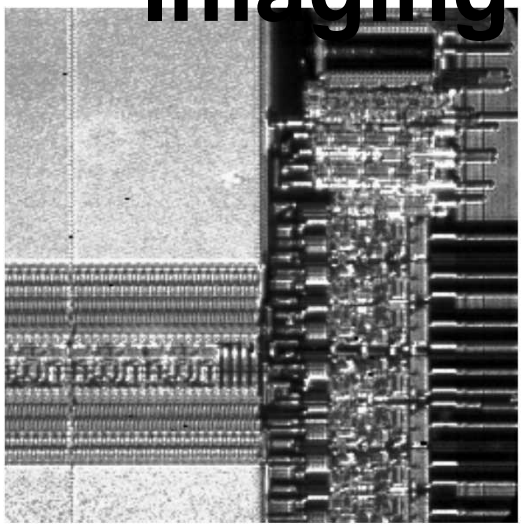
IR Backside Imaging

Illuminated images: $p_{substrate}$=1*10^{15}cm^{-3}; HgCdTe detector (IR Labs)

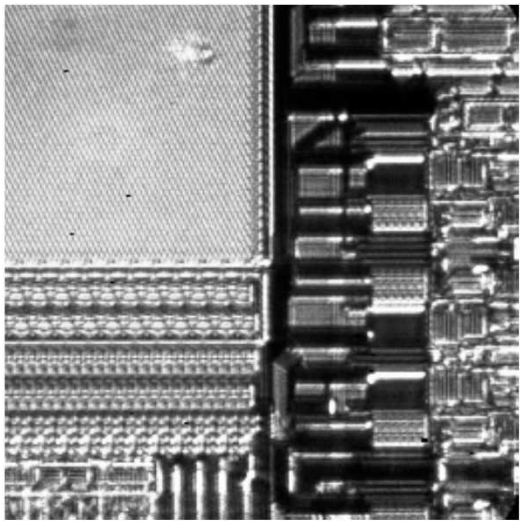
70µm



X1

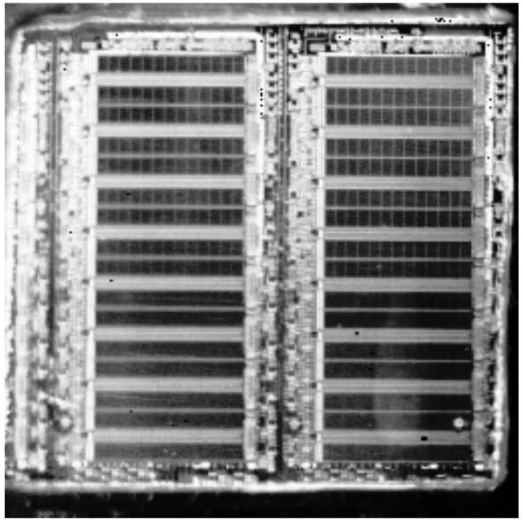


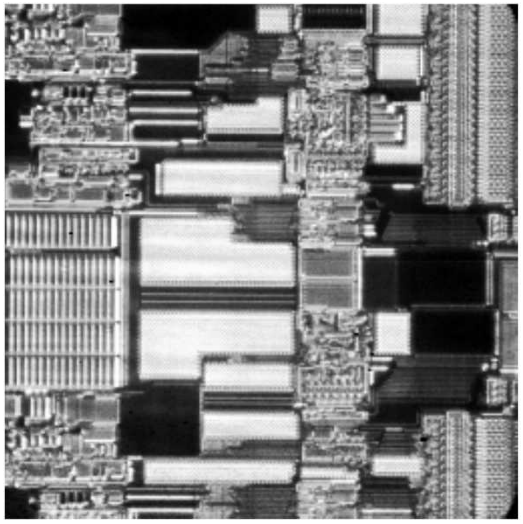
X20

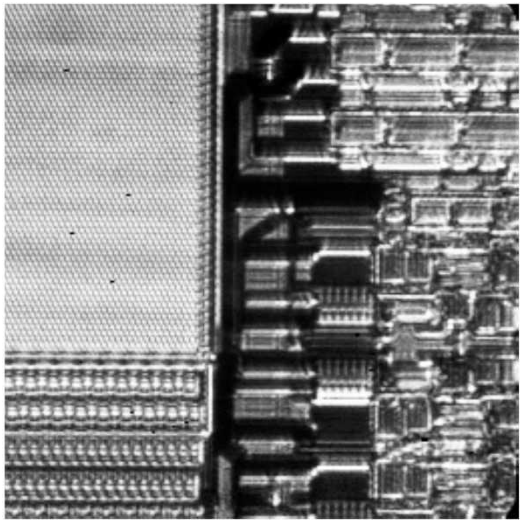


X50

670µm

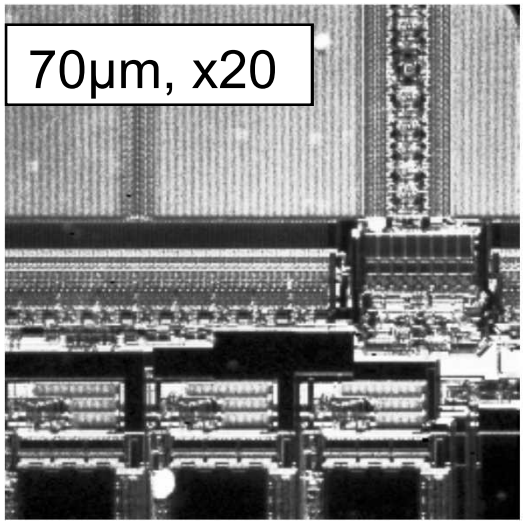


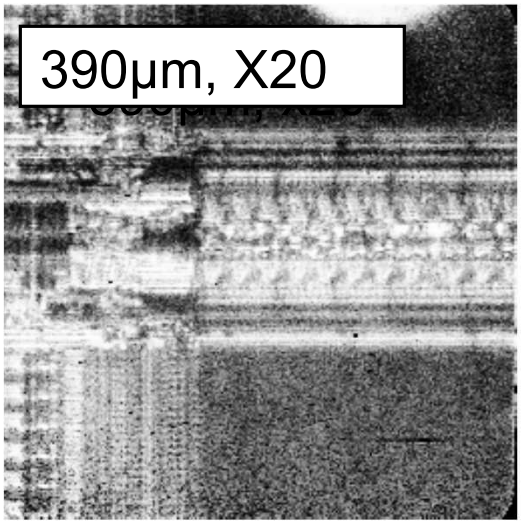


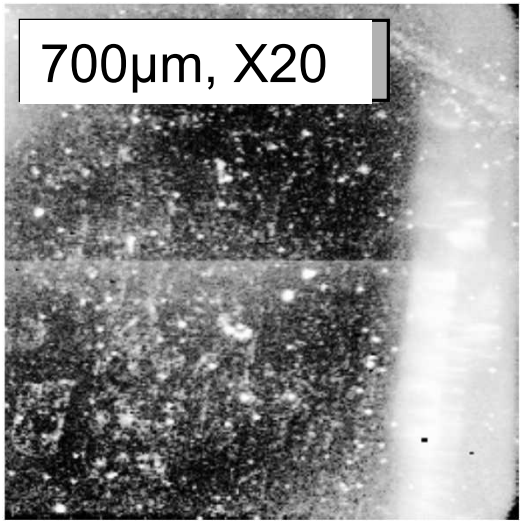


IR Backside Imaging

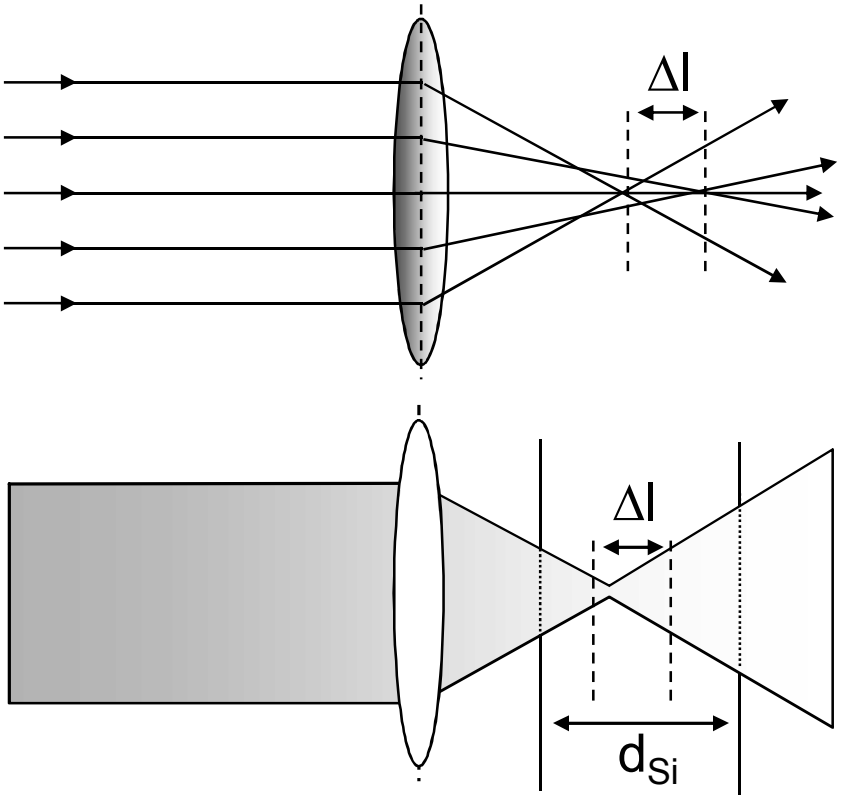
Illuminated images: $p_{substrate}=1*10^{19}cm^{-3}$; HgCdTe detector (IR Labs)







Spherical Aberration



geometrical optics:

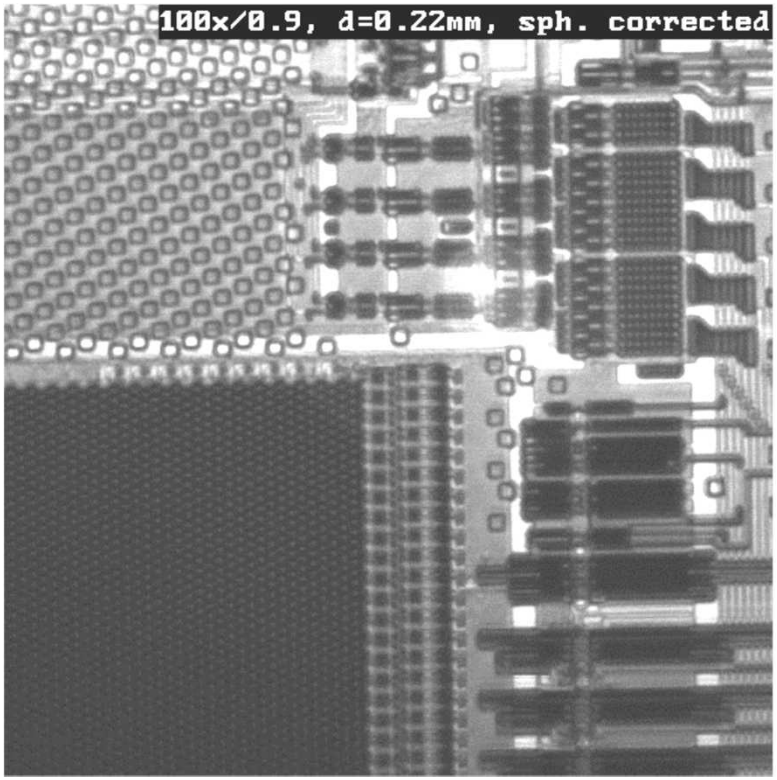
thin biconvex lens

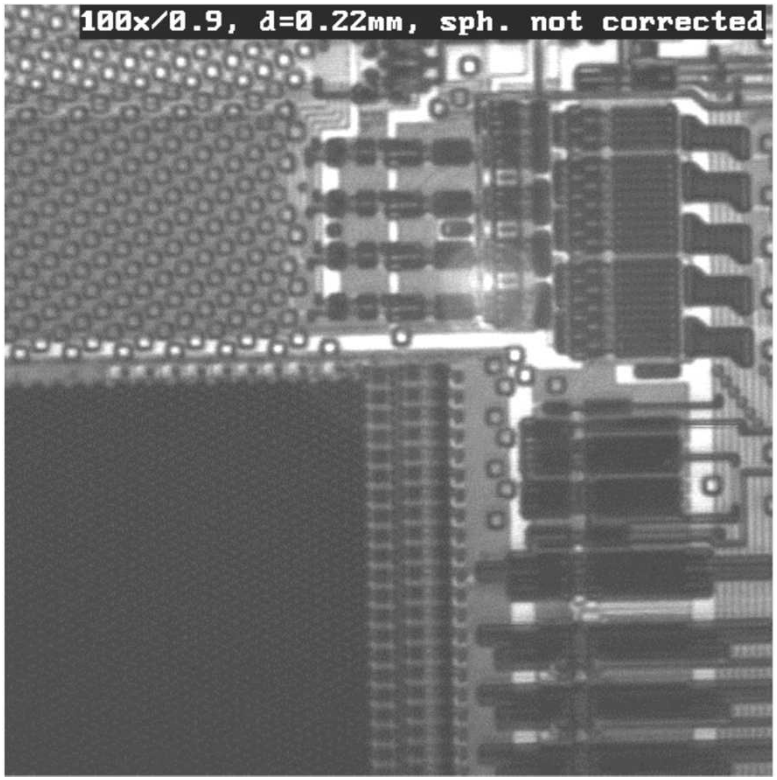
Planparallel Si of thickness d_{Si}

$$\Delta l = \Delta l\,(\,d_{Si}, n_{Si}, NA)$$

$\Rightarrow$ **sperical aberration increases with d_{Si}**

Zeiss IR confocal LSM (1152 nm)





$p_{substrate}$ = 1x$10^{19}$$cm^{-3}$; d=220µm; 100x objective NA=0.9

Optical Image Formation from the Backside of the Die: Key Issues

- **Surface roughness: rms < 5nm**

$$res = \frac{0.61 \cdot \lambda}{NA}$$

- **reduced lateral resolution:**
  → **best image formation: confocal laser scanning microscope**

- **lens failure for large NA: sperical aberration**
  → **use of a corrected microscope objective (100X) or thinning the die**

Backside preparation techniques

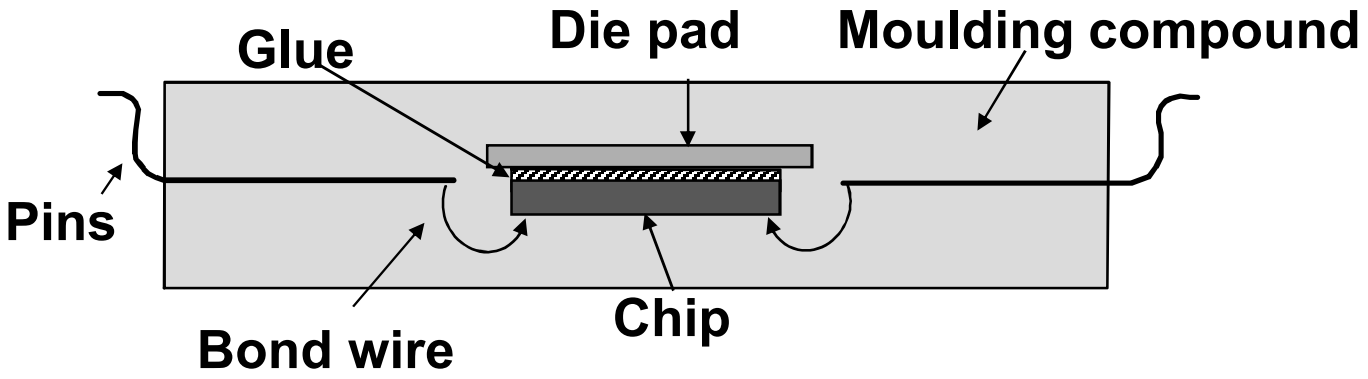
Global Si thinning

- CNC milling
- mechanical grinding/ polishing
- RIE

Local Si thinning / Precision probe hole milling

- FIB
- LMC technique

Cross-section : plastic package

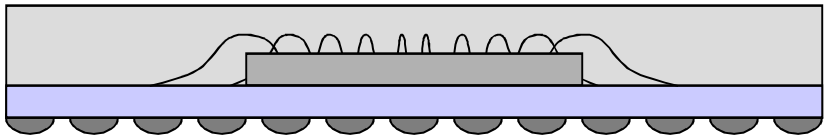


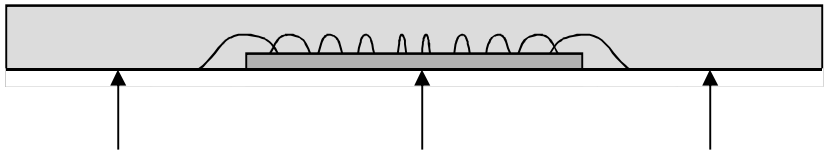
Maintaining Electrical Continuity

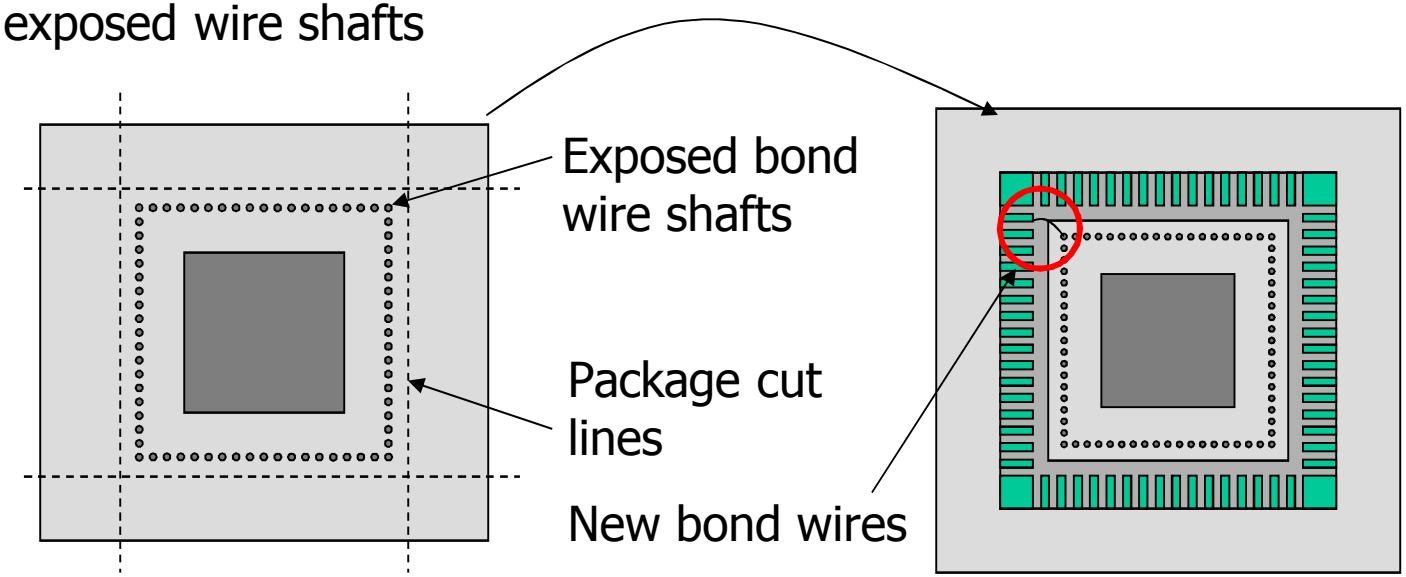
Step 1: Grind/polish through bumps and circuit board

Step 2: Cut excess material away from BGA package

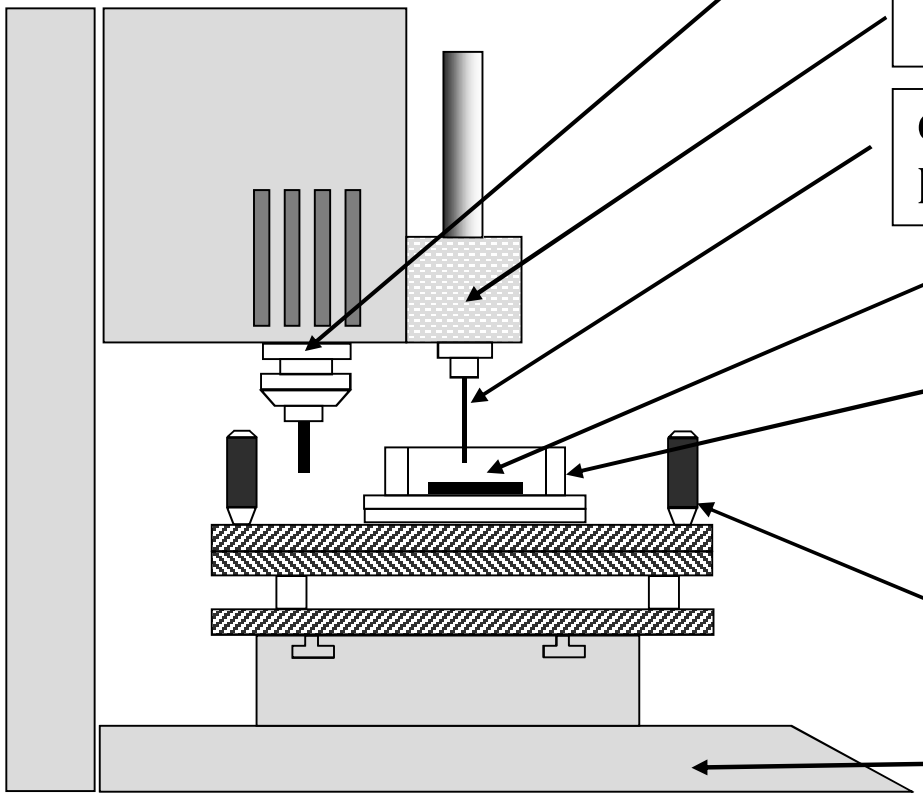
Step 3: Place remaining BGA package in PGA package and rebond to exposed wire shafts







Schematic view of the CNC milling machine



Motor spindle CNC with a milling head of hard metal

High-frequency spindle (45000 - 60000 rpm)

diamond milling head diameter 2 - 3mm

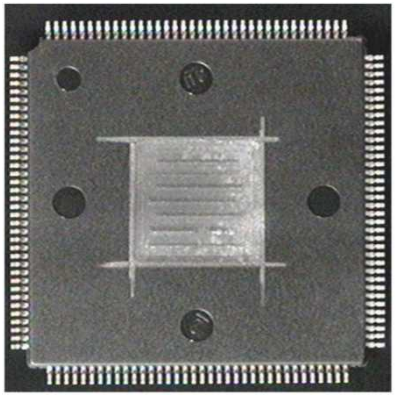
device

Container for water-cooling

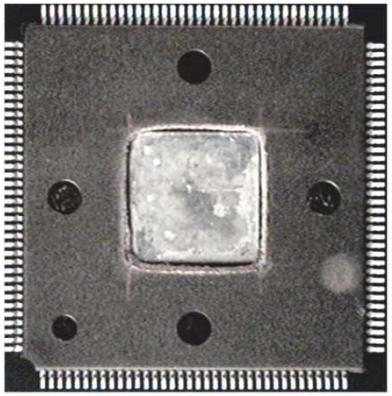
Micrometer screw for adjustment

CNC-machine

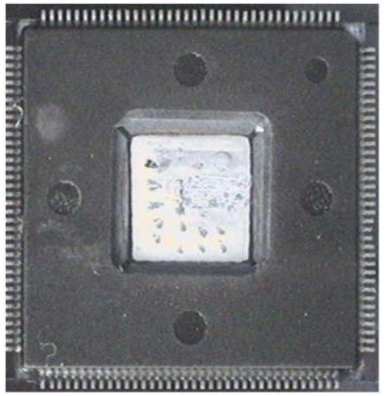
CNC milling: Process steps



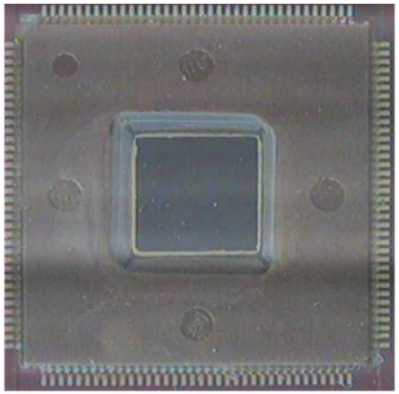
Chip size marked, plastic milled



Plastic removed down to the leadframe



Lead frame removed down to the glue



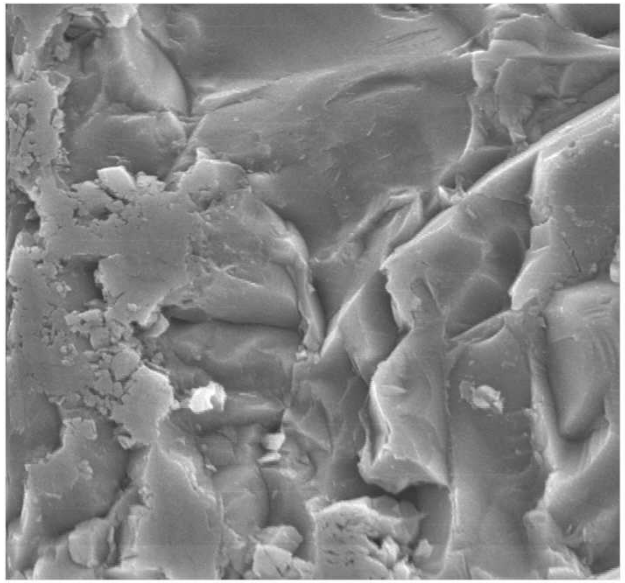
Glue removed

Milling of the Si substrate

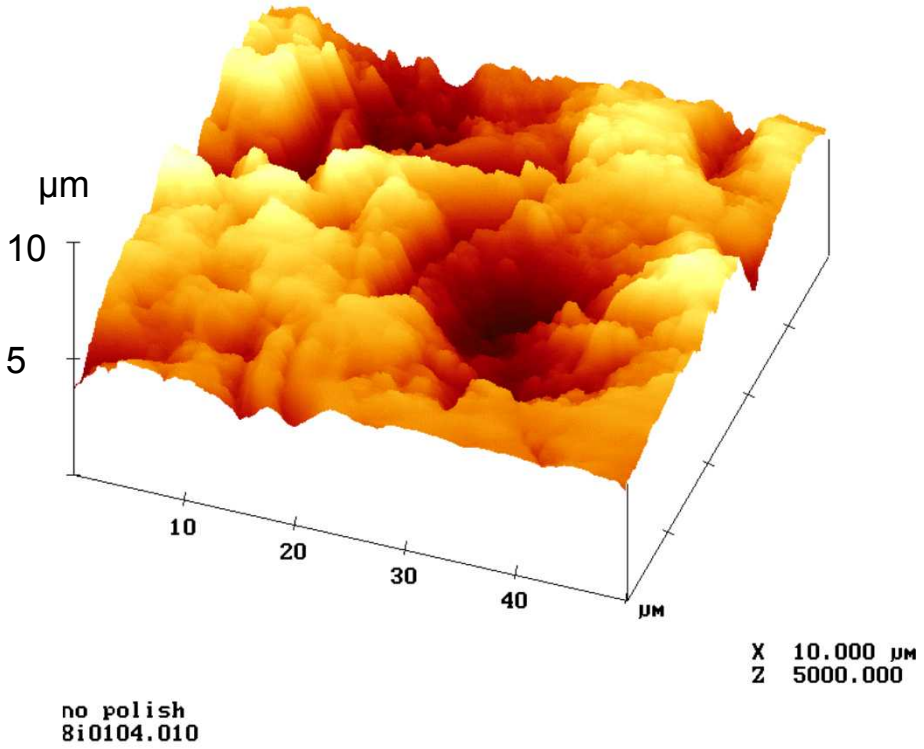
Si substrate polished

Si Substrate Surface after CNC Milling

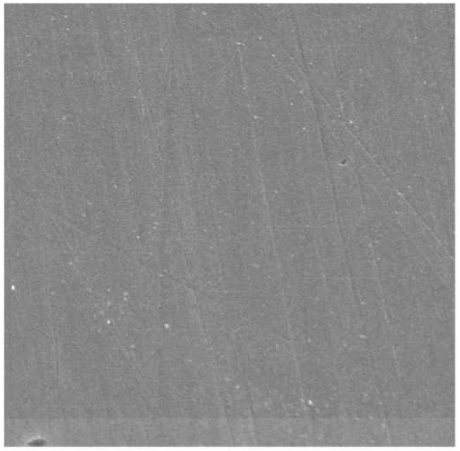
SEM image (1500 x)



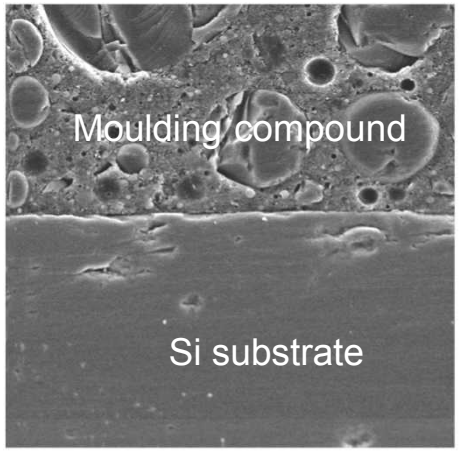
Surface topography (AFM)



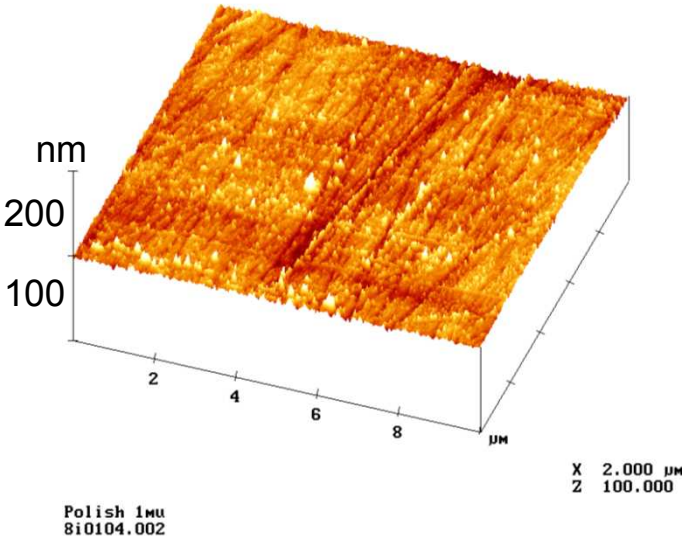
Si Substrate Surface after Mechanical Polishing



SEM image (700 x)

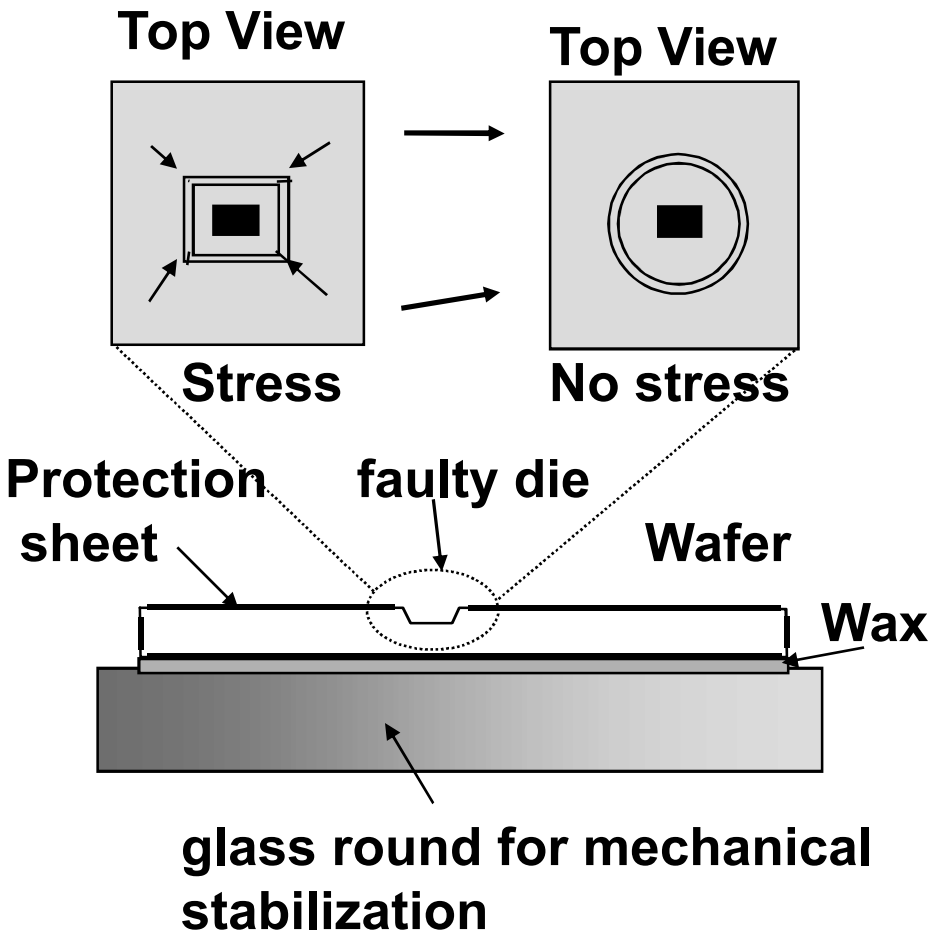


SEM image (1500 x)



Surface topography (AFM)

CNC Milling on Wafer Level



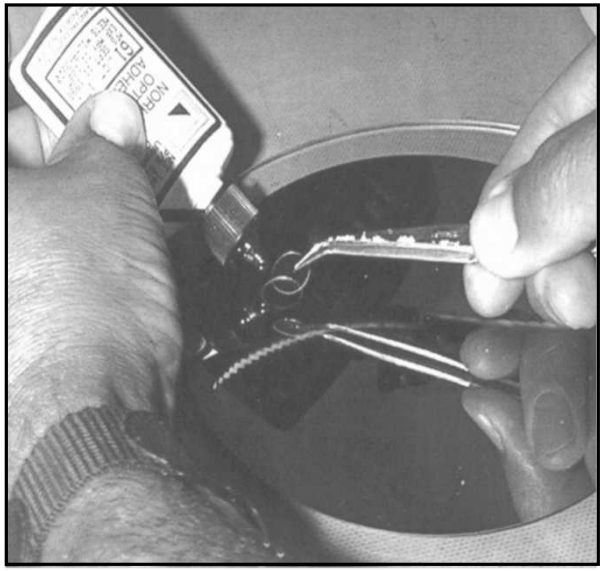


Image courtesy of Hypervision

CNC Milling

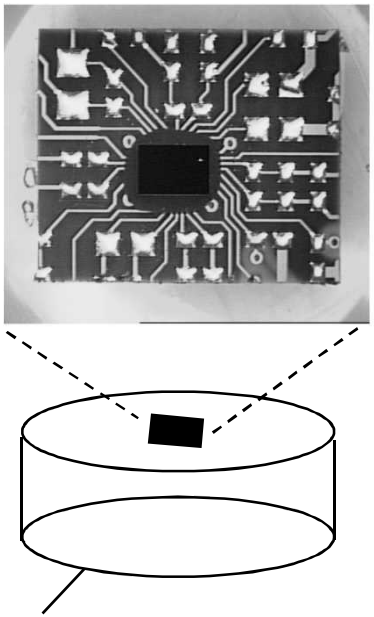
- Global thinning of Si
- min. remaining Si thickness: ca. 100 µm
- large areas >= 1 cm^2
- planarity/ surface homogeneity preserved

(ca. 20 µm at 1 cm^2)

- surface roughness: rms <= 3-5 nm
- suited for packaged devices, flip-chips, wafer level

Mechanical Grinding/ Polishing

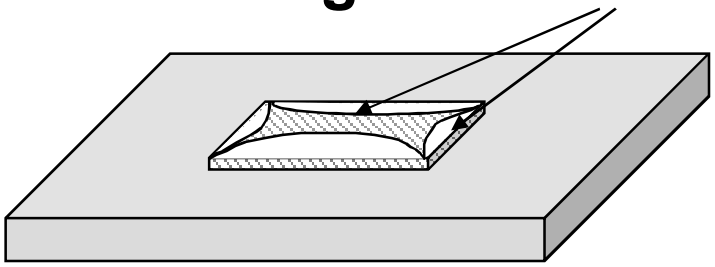
Encapsulated grinding



Grinding/ Polishing

- Global thinning of Si
- min. remaining Si thickness: ca. 100 µm
- surface roughness: rms < 3-5 nm
- use for packaged devices limited
- major challenge: even surface

Outer edges thinned more than the center



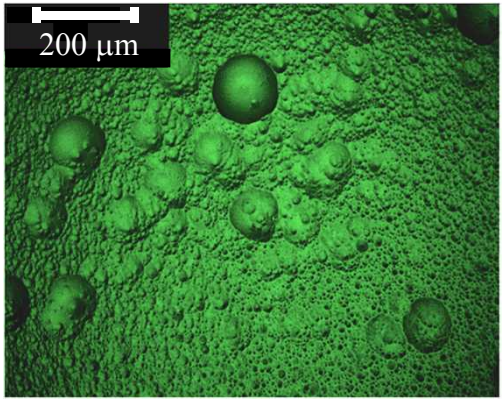
Silicon Removal by Dry Etching

Requirements:- high etch rates > 10 µm/ min
- highly reflective shiny surface after etching
- uniformity
- remaining Si thickness after etching ca. 100 µm
- functionality of the chip preserved

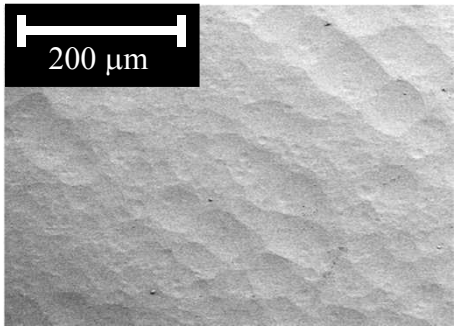
→ High etching rates due to high plasma density e.g.:
- Microwave plasma + RIE
- ICP (Inductive Coupled Plasma) + RIE
- ECR (Electron Cyclotron Resonance) + RIE

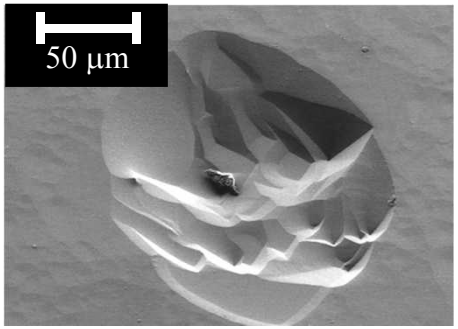
RIE - Backside Etching

Die thinned to 50µm
Nextral NE860 high density SF_6Plasma

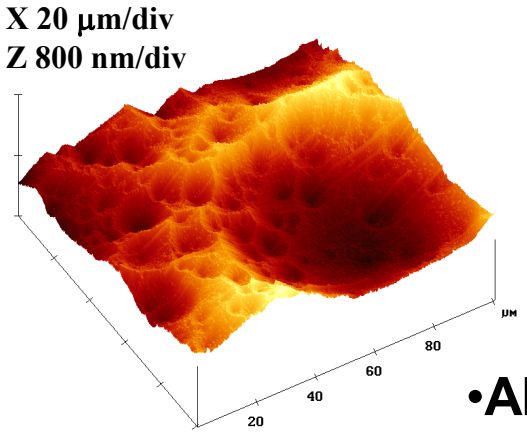


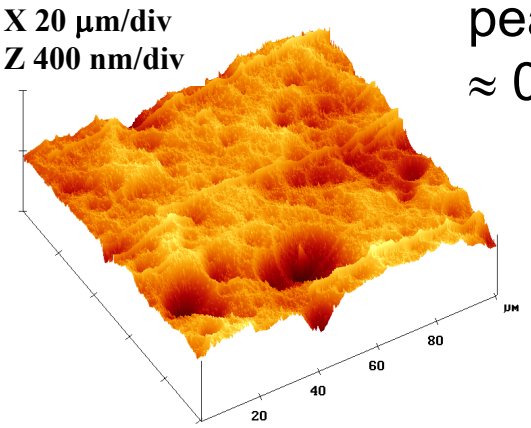
Surface in optical microscope





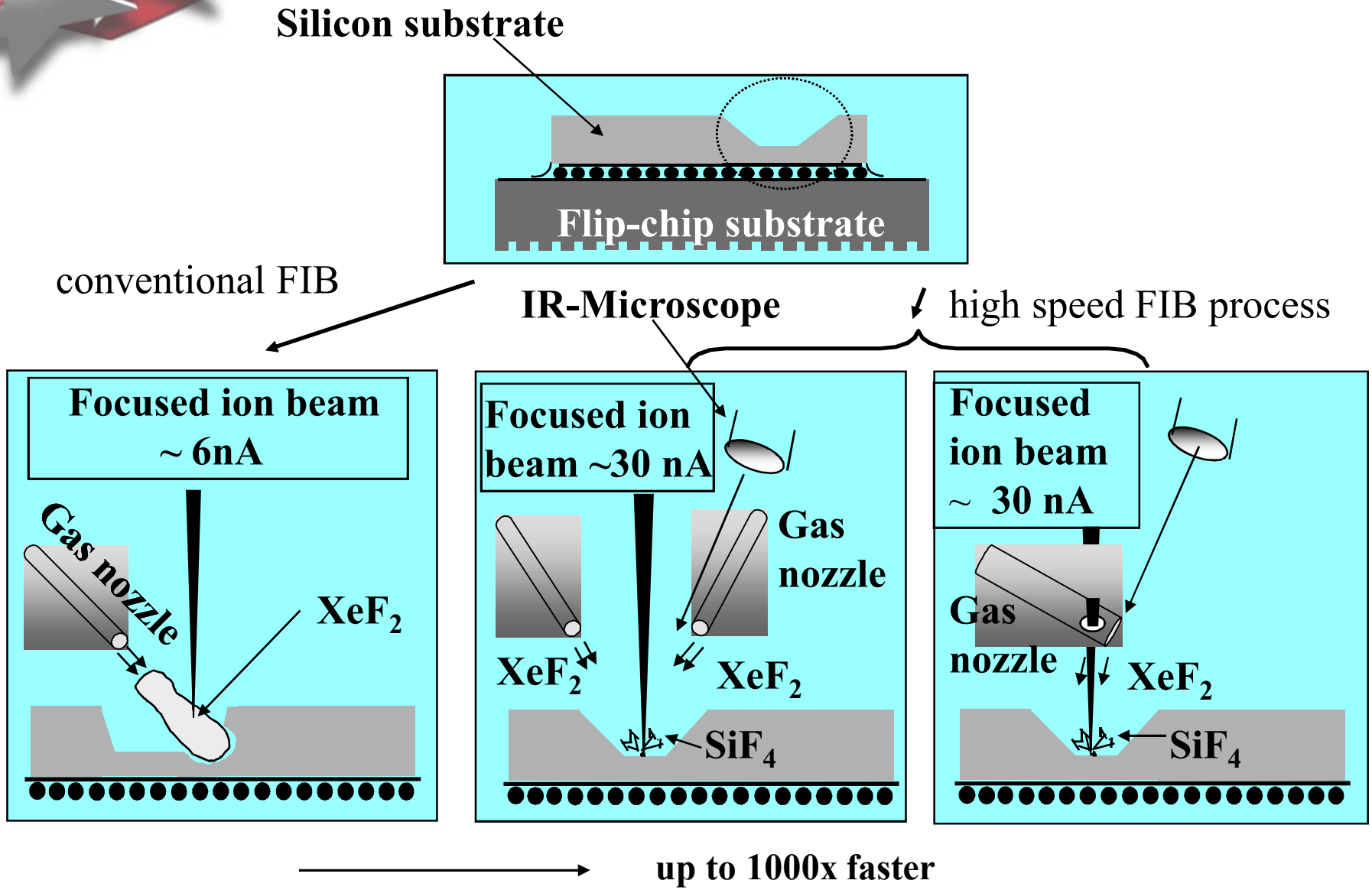
Surface viewed in SEM



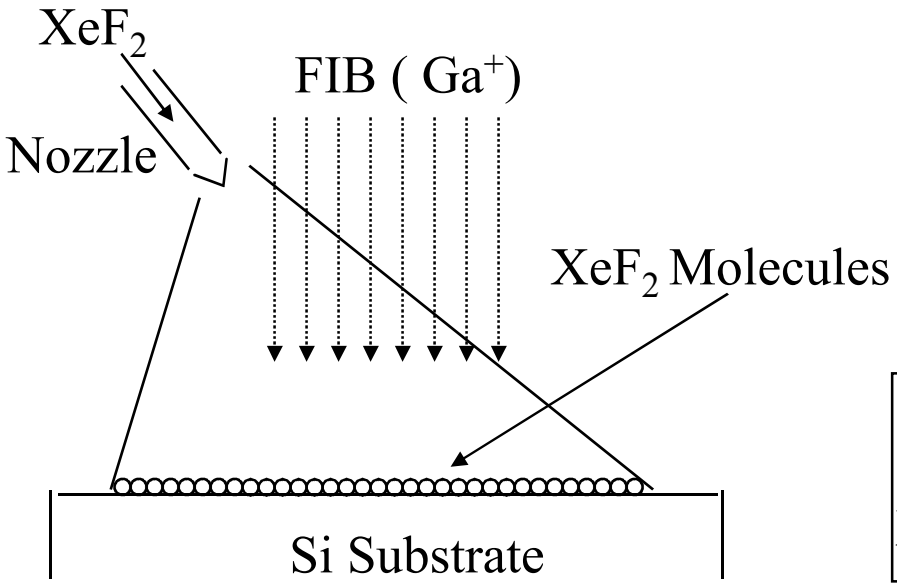


•AFM
Topology peak to peak ≈ 0.5µm

FIB


Silicon substrate
Flip-chip substrate
conventional FIB
IR-Microscope
high speed FIB process
Focused ion beam
~ 6nA
Gas nozzle
XeF2
Focused ion
beam ~30 nA
Gas
nozzle
XeF2
XeF2
SiF4
Focused
ion beam
~ 30 nA
Gas
nozzle
XeF2
SiF4
up to 1000x faster

Gas-Assisted Etching of Si with FIB



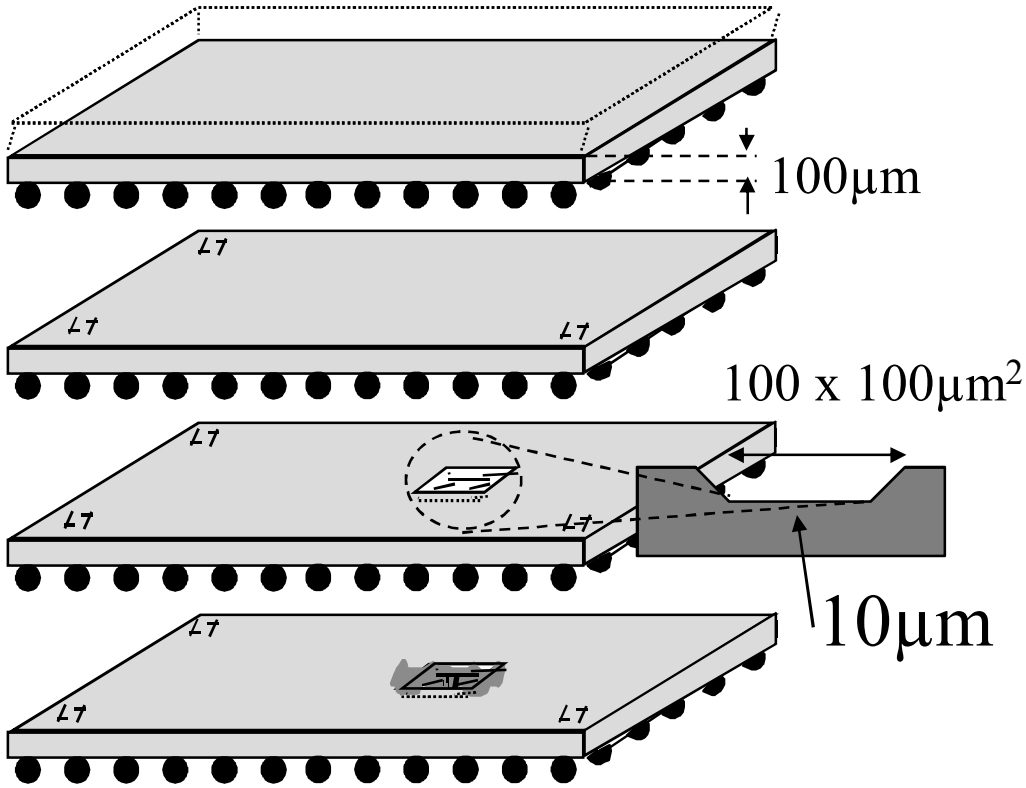
- Enhanced material removal
- no redeposition
- selectivity

	Al	W	Si	SiO_2/ Si_3N_4
XeF_2	0	>10	>10	>10

(FIB assisted) surface reaction:

$$Si + 2\,XeF_2 \xrightarrow{(Ga^+)} SiF_4\uparrow + 2\,Xe\uparrow$$

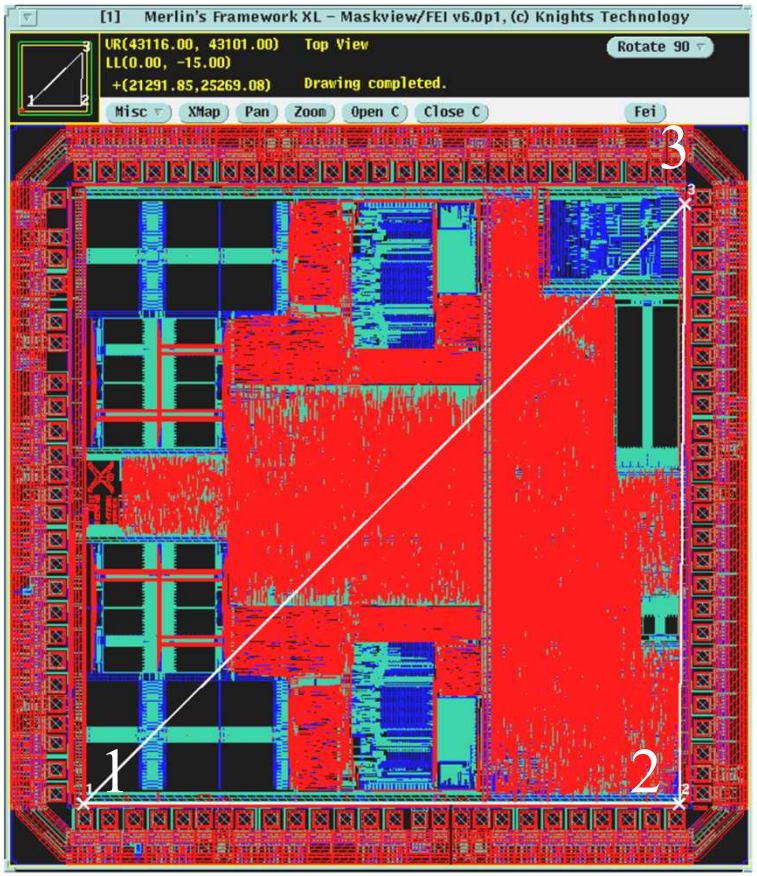
Backside FIB preparation

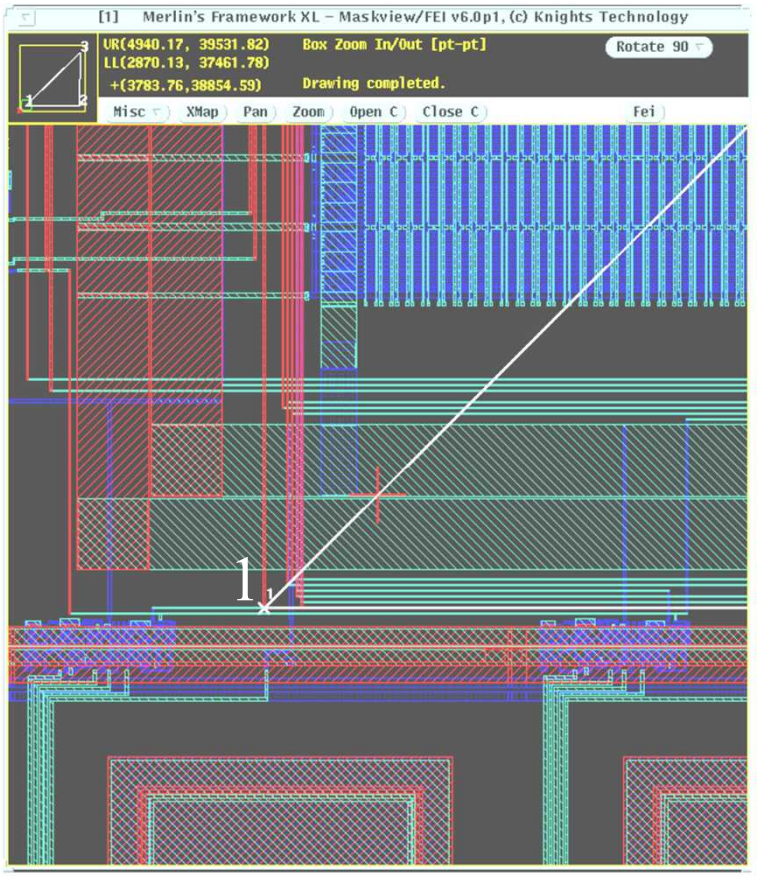


1. Global Si thinning
2. Identification of alignment points for CAD navigation
3. Local Si thinning with high-speed FIB etching process (time required: ca. 10 min)
4. Precision Probe hole milling with FIB

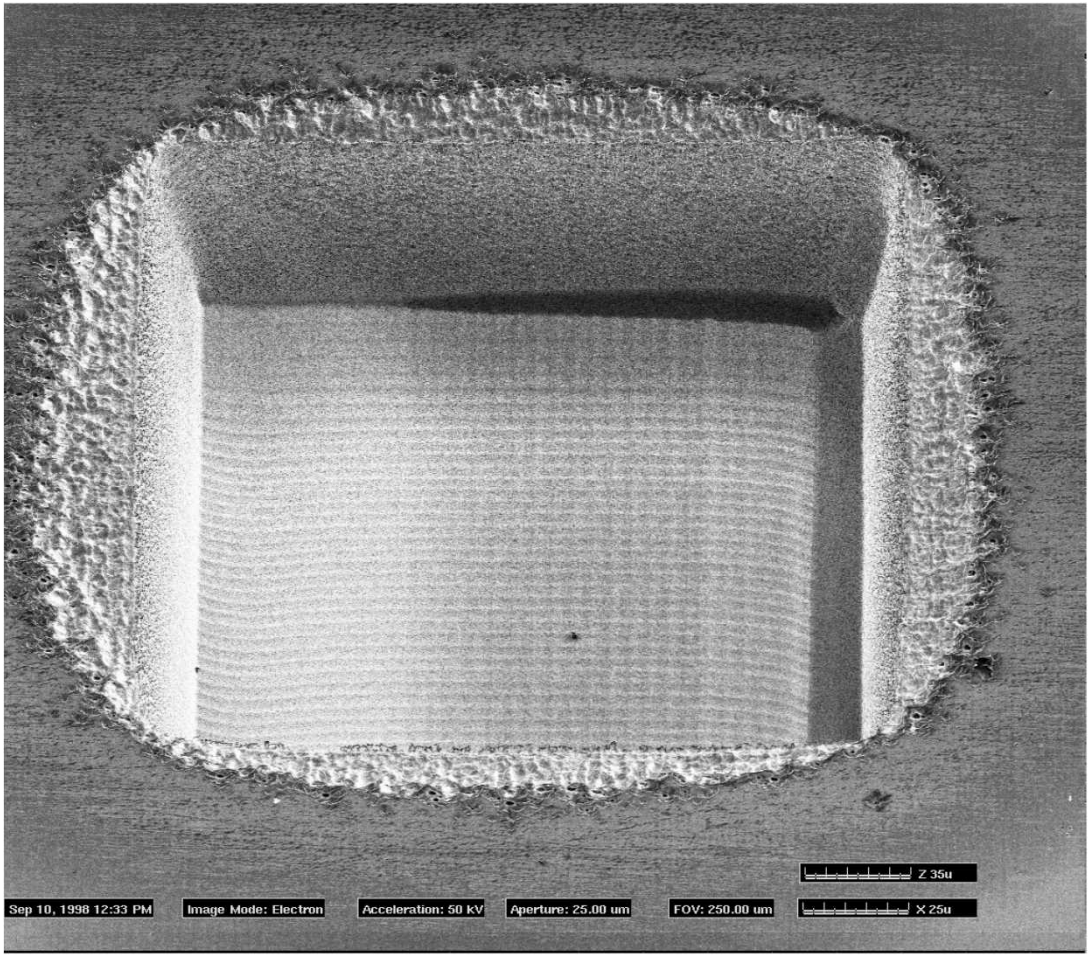
Supporting Navigation by Correlating to CAD-Data

3 Point Alignment of Layout to x-y-table of FIB using CAD-Navigation



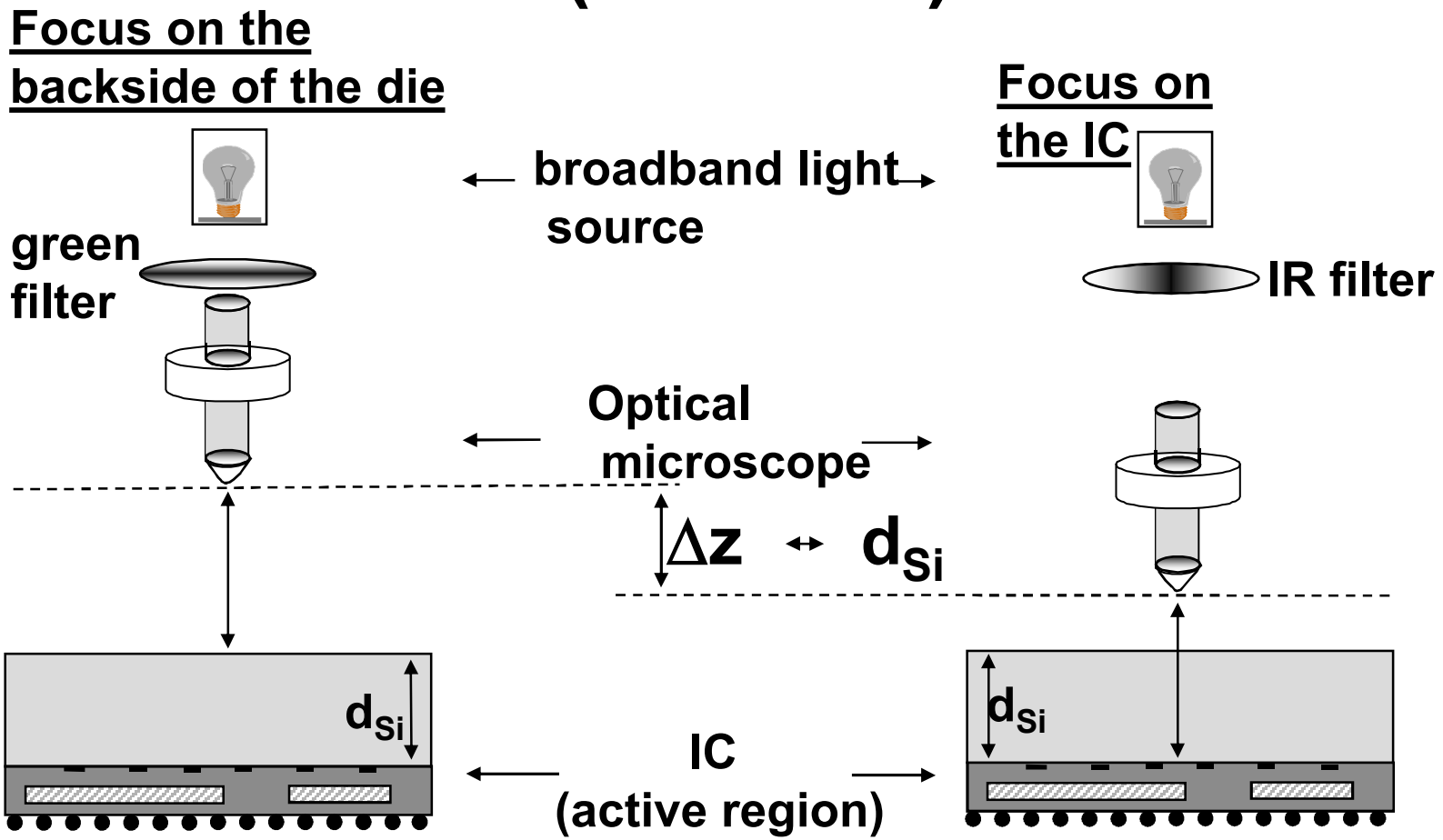


FIB etched trench (Micrion)

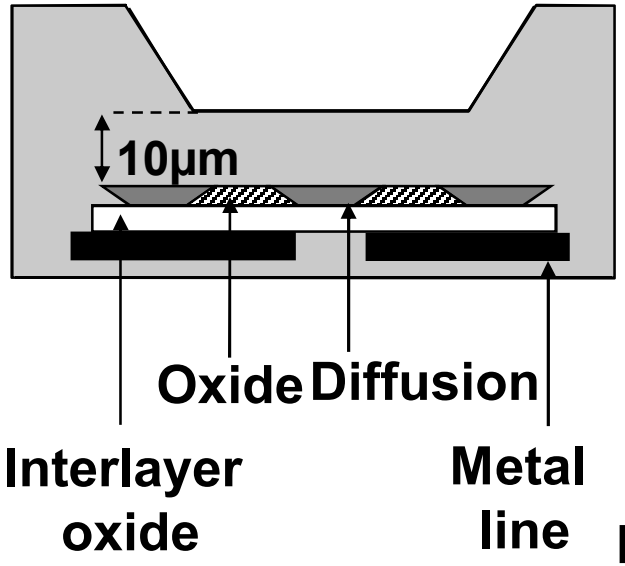


$p_{substrate} = 1x10^{19}cm^{-3}$;

Endpoint detection with FIB (Micrion)



Precision probe hole milling

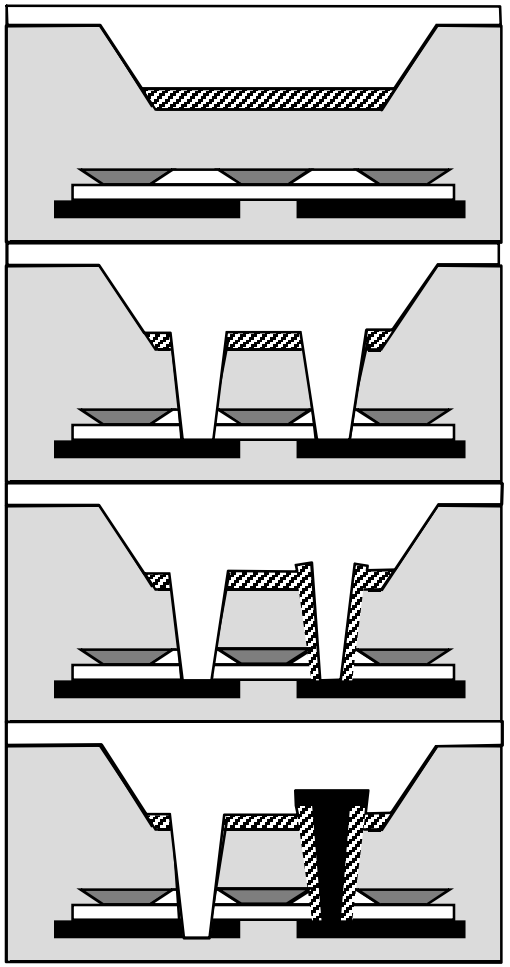


SiO_2 deposition

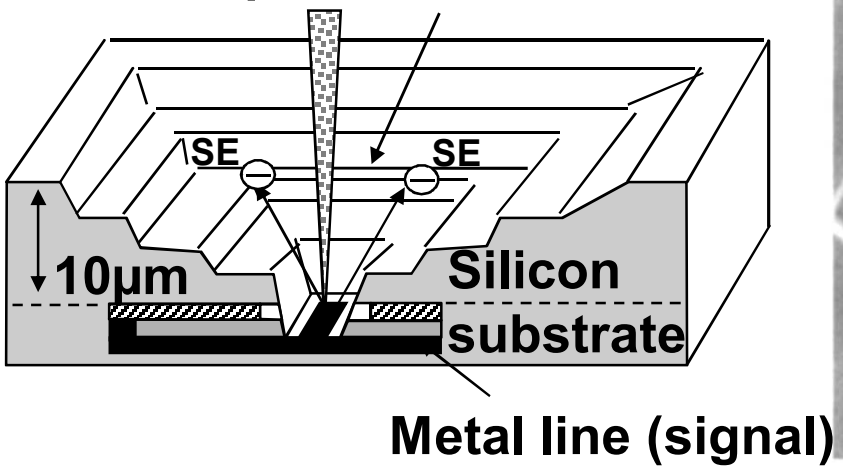
XeF_2 assisted milling

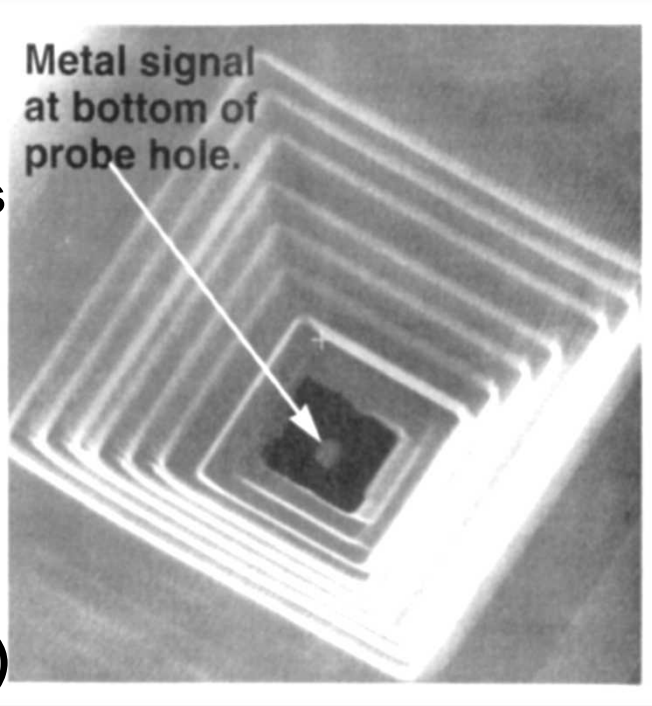
SiO_2 deposition and reopening of the holes

Metal deposition and cutting the old signal lines



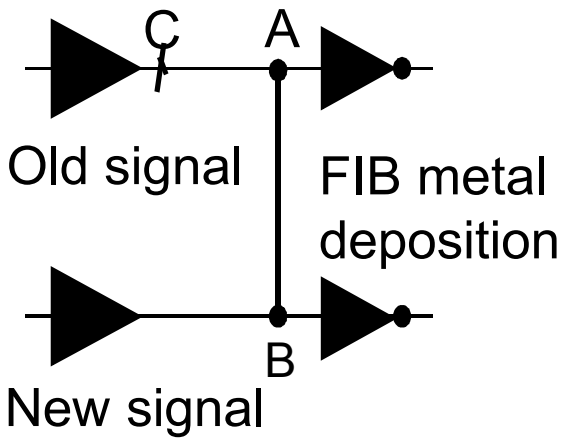
FIB precision probe hole

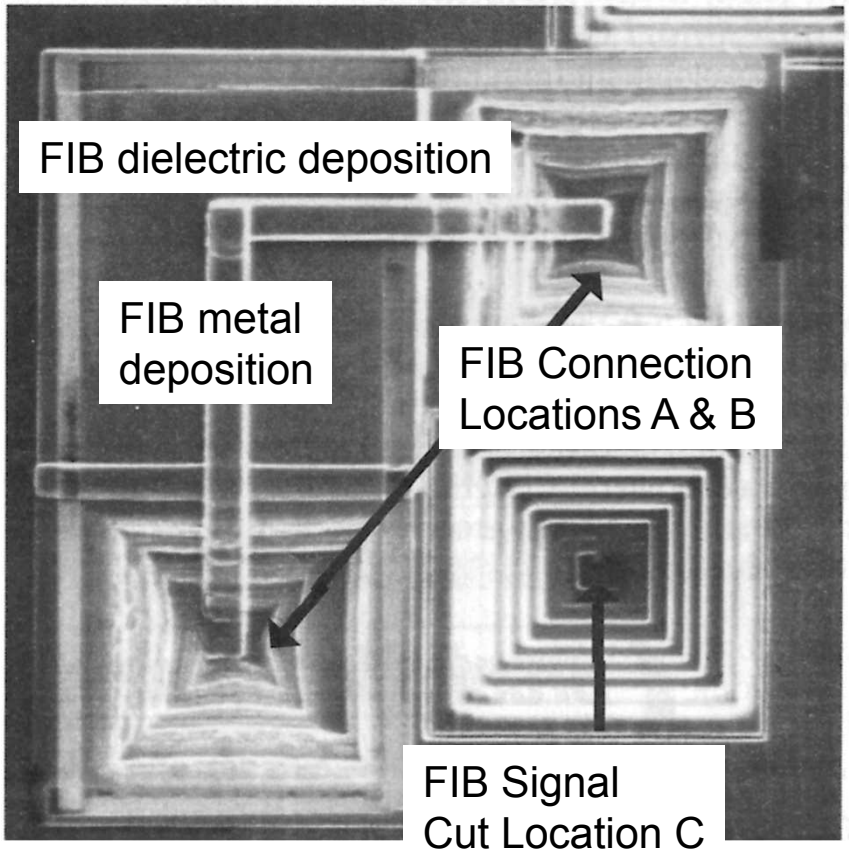




Device modification from the backside of the die

Circuit Edit Schematic





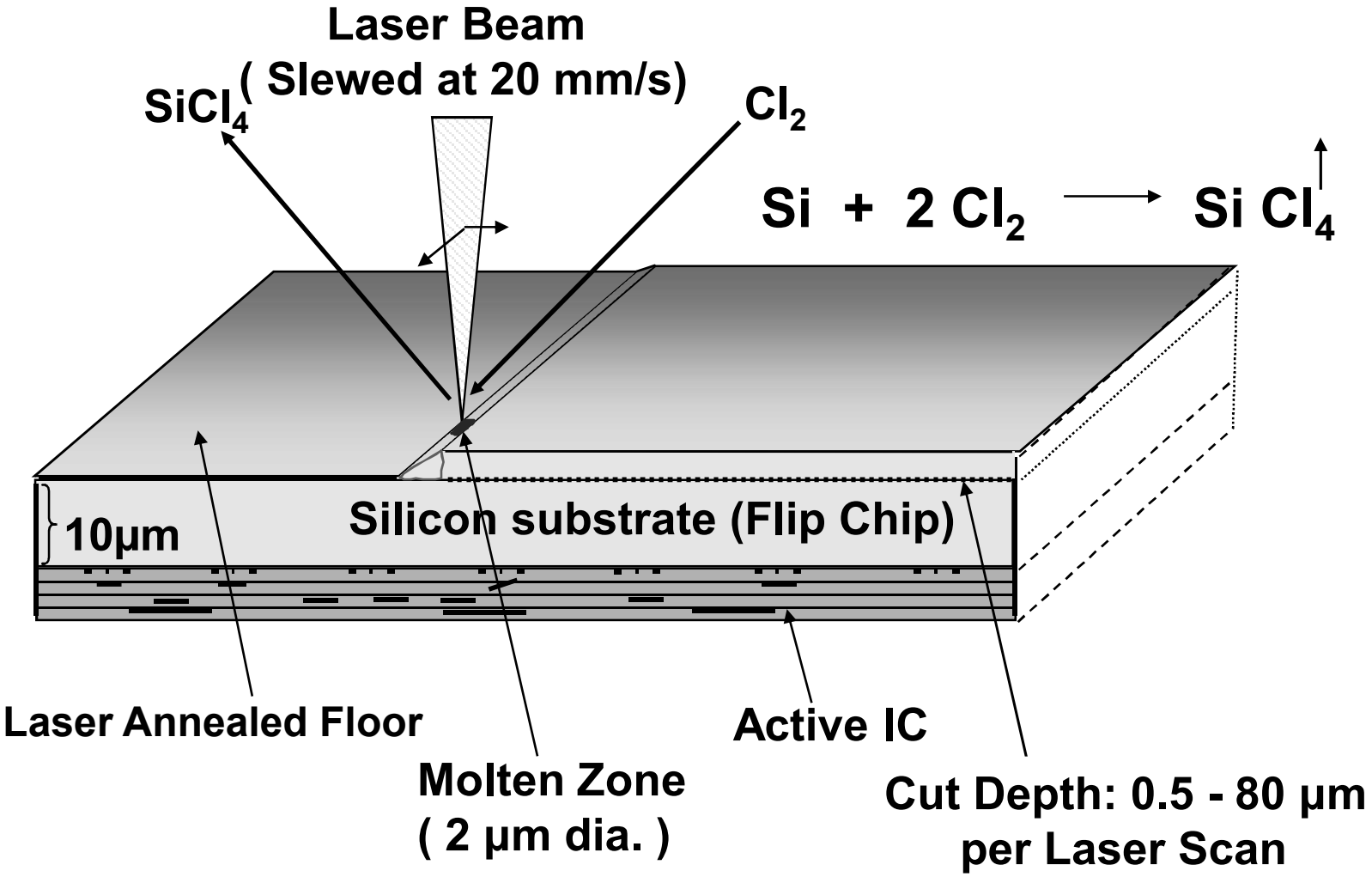
FIB for backside preparation

- Applications of FIB for backside FA: device modification
  mechanical or e-beam probing

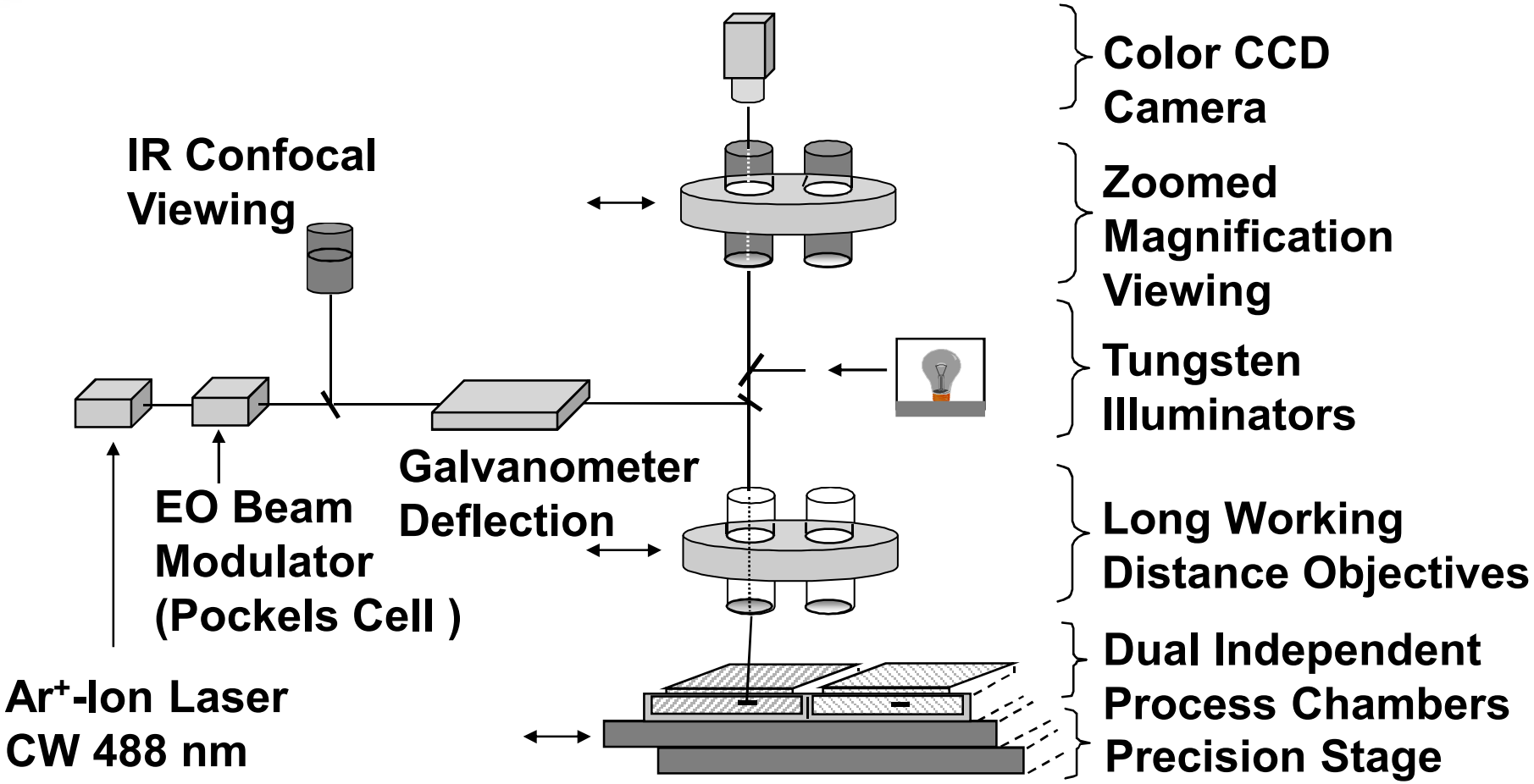
- High speed FIB etching process: local thinning of Si
  (typically 100 x 100 μm^2)

- Precision probe hole milling similar to standard FIB frontside process with spatial resolution < 0.1µm → FIB is the **most precise** tool for backside preparation

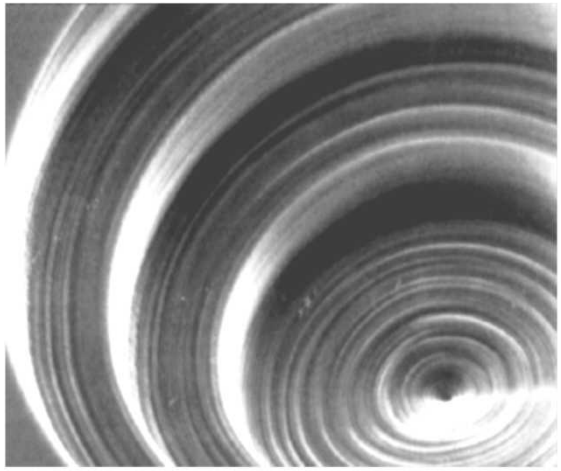
Laser MicroChemical (LMC) Etching



Schematics of setup for LMC Si-etching

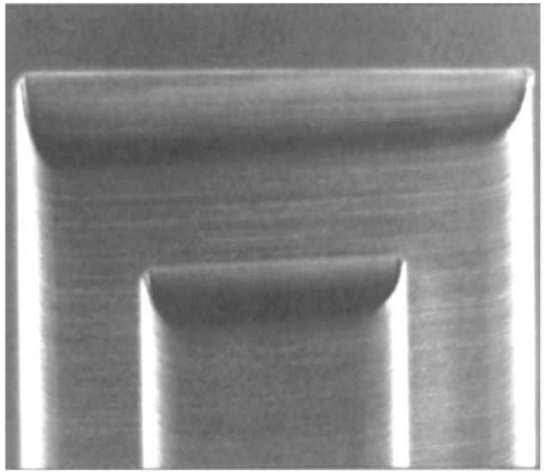


LMC etching and deposition



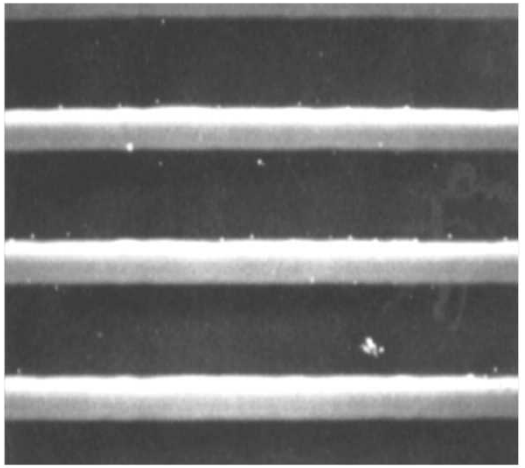
10µm

Silicon etch at
100000 µm^3/ s



10µm

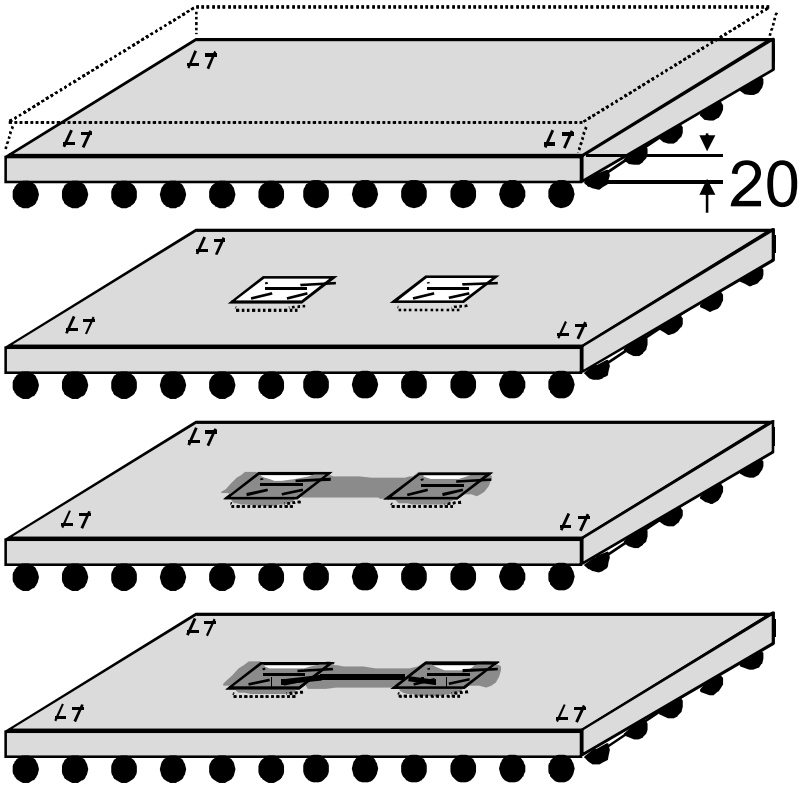
Silicon etch at
100000 µm^3/ s



10µm

Platinum deposition at
100 µm/ s

LMC Process for Backside FA Applications



1. Global thinning of Si (e.g. CNC milling); LMC reveals alignment fiducials;

2. LMC etching of trenches over the regions of interest (typical area 500 x 500 µm^2)

3. Deposition of a dielectric isolation e.g. laser deposited oxide

4. Local repairs at the base of the isolated trenches typically using a FIB. For longer interconnects (interconnects between trenches), laser deposition is used.

Benefits of LMC technique

- Speed enhancement of several orders of magnitude (microchemical reaction) compared to FIB

- process spatial resolution $\Delta x, \Delta y <= 0.5\mu m$
  $\Delta z <= 0.1\mu m$: endpoint detection via OBIC

- surface roughness achieved:rms typically 30nm

applications for backside FA: in combination with FIB sample preparation for e-beam/ mech. probing and device modification;

- outlook for backside FA: optimization of the illuminated image / signal strength for various backside localization techniques

Backside preparation techniques

Global Si thinning

- CNC milling
- mechanical grinding/ polishing
- RIE

large areas >=1 cm^2
min. remaining Si thickness: ca. 100µm

Local Si thinning

- LMC technique
- FIB (high speed process)

areas up to 500 x 500 μm^2
min. remaining Si thickness: ca. 10µm
spatial resolution limited (ca. 1 µm)

Precision probe hole milling

- FIB

high spatial resolution (ca. 0.1 µm)

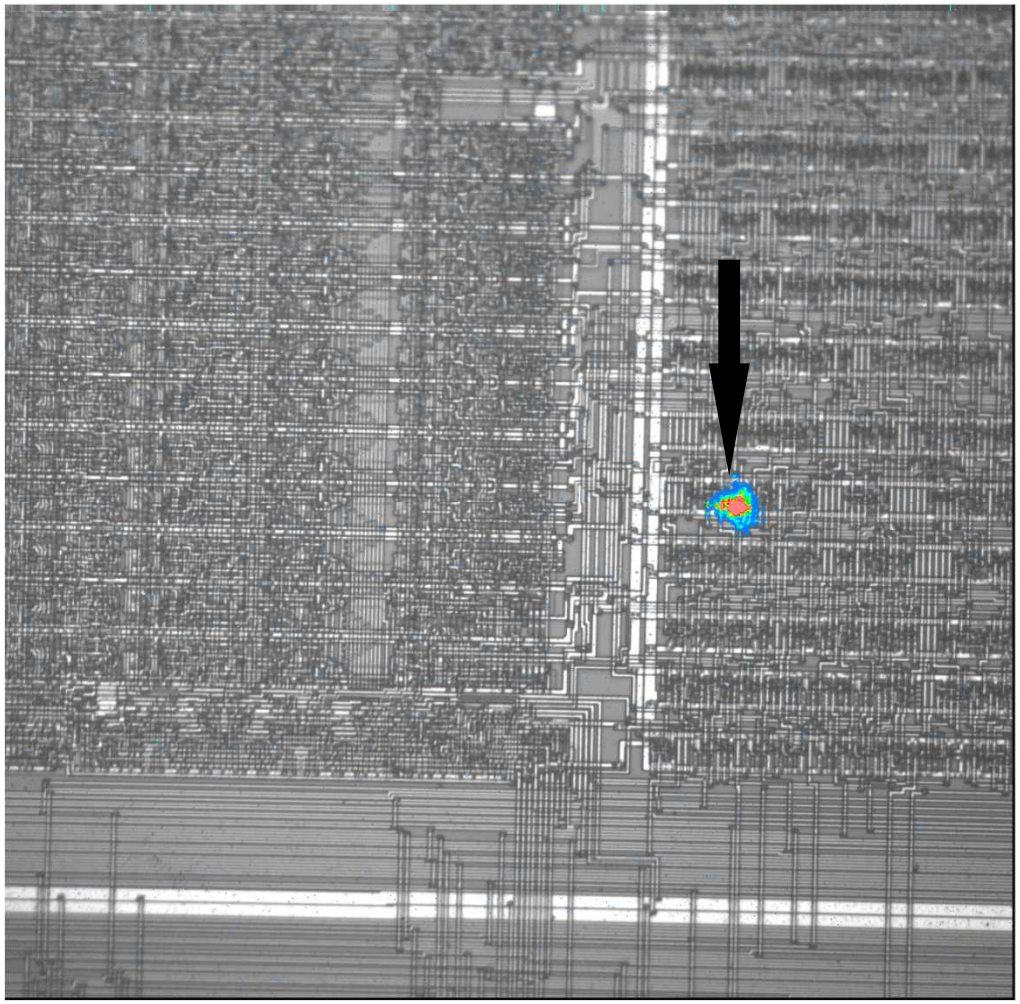
Defect Localization Techniques

- **Backside analysis techniques fall into two categories:**
  - Passive (Measure light emissions)
  - Active (use light, e.g., to influence circuit operation)
- **Sample preparation and pitfalls are similar**

Backside Techniques

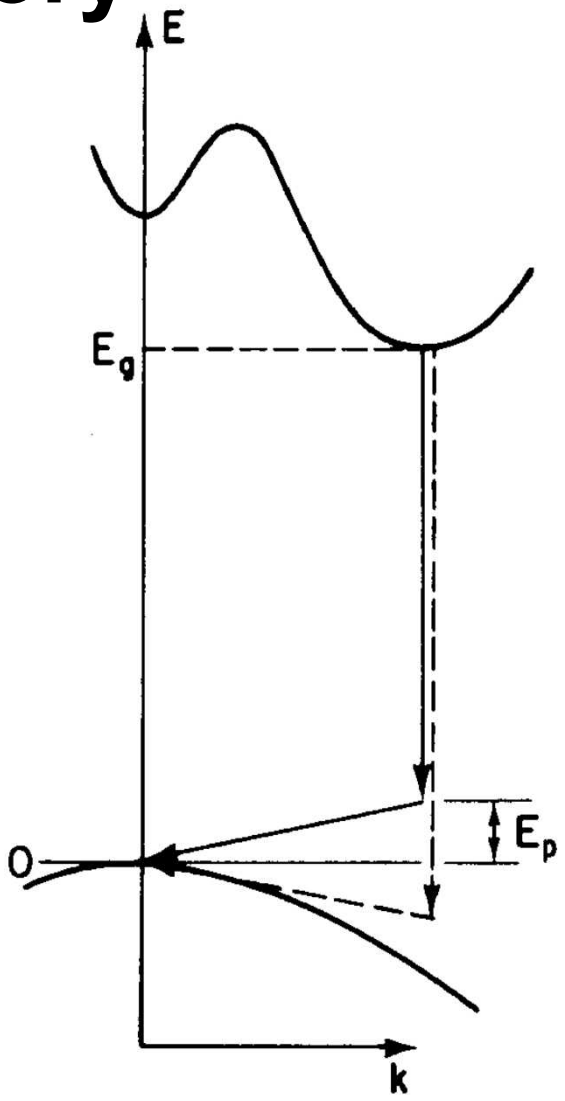
- **Emission based**
  - NIR light emission
  - PICA - IBM
- **FIB/E-beam**
- **Optical probe based**
  - electrooptic based
  - Laser voltage probe (LVP)
  - LIVA
  - IR-OBIRCH/TIVA/SEI
  - SDL/LADA

Photoemission Microscopy (PEM)



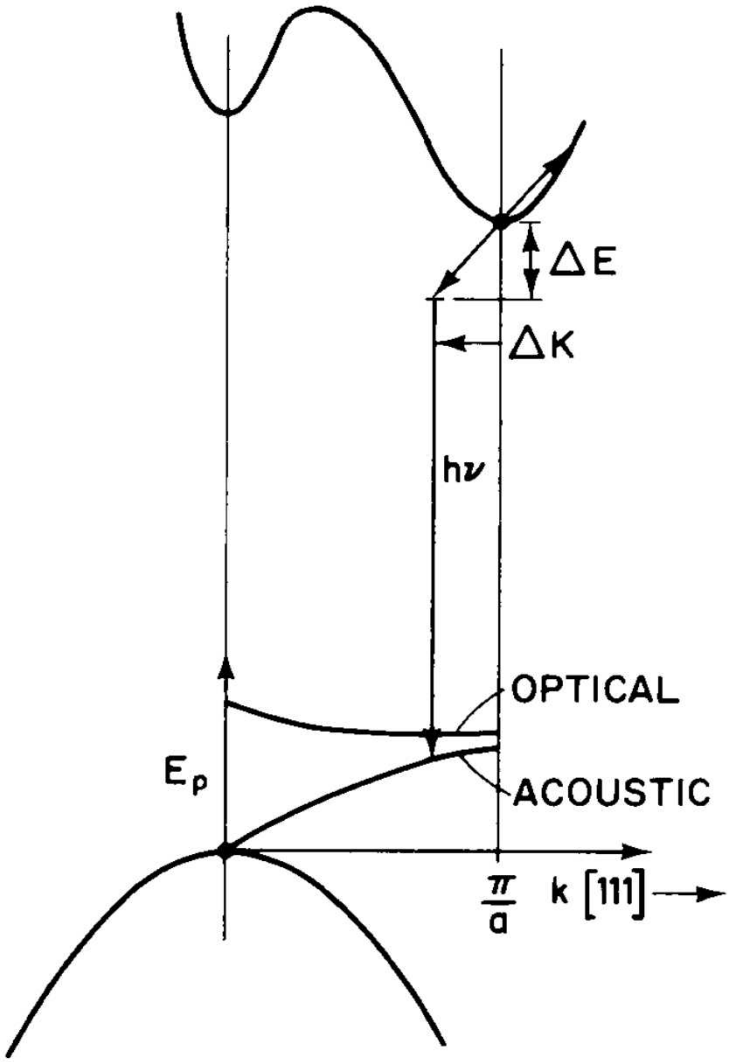
Emission Theory

- Recombination can be intraband or interband
- Momentum must be conserved - phonon emission likely
- E_G = 1.11 eV or (1.12 μm) at 300 K



Emission Theory

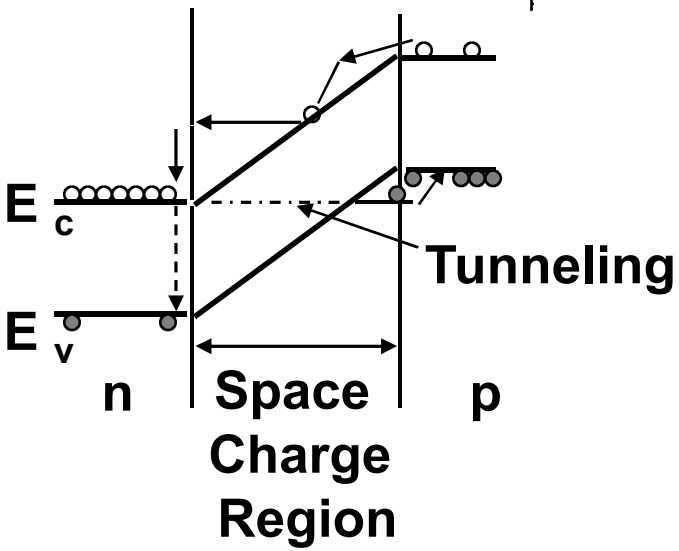
- Only chance for short wavelength emission is from hot carriers
- $dE = k_B T_e$
- Possible under high field situations
- Visible: 390 - 770 nm
- NIR: 770 - 1500 nm

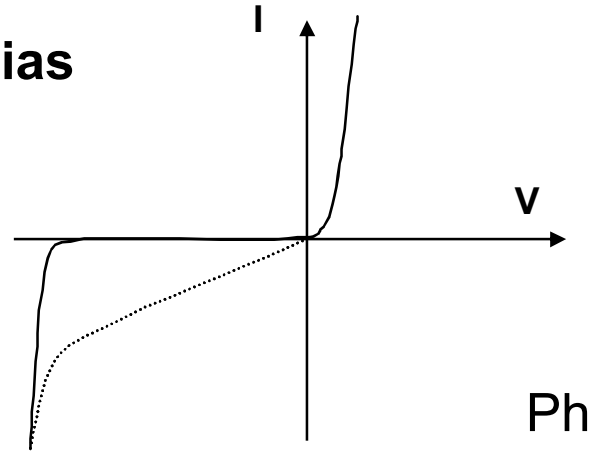


The 2 Basic Mechanisms of Photoemission in IC

Junction: Reverse Bias

Scattering of Field Accelerated Carriers (+ Recombination)

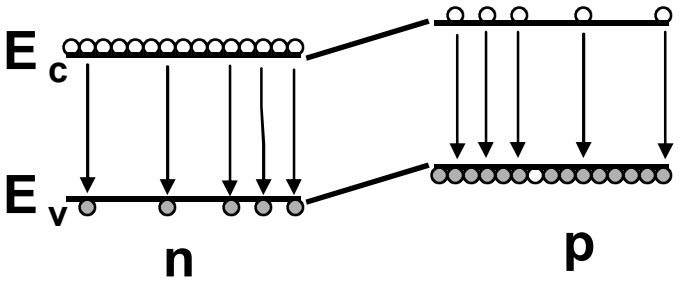




Forward Bias

Minority Carrier Injection

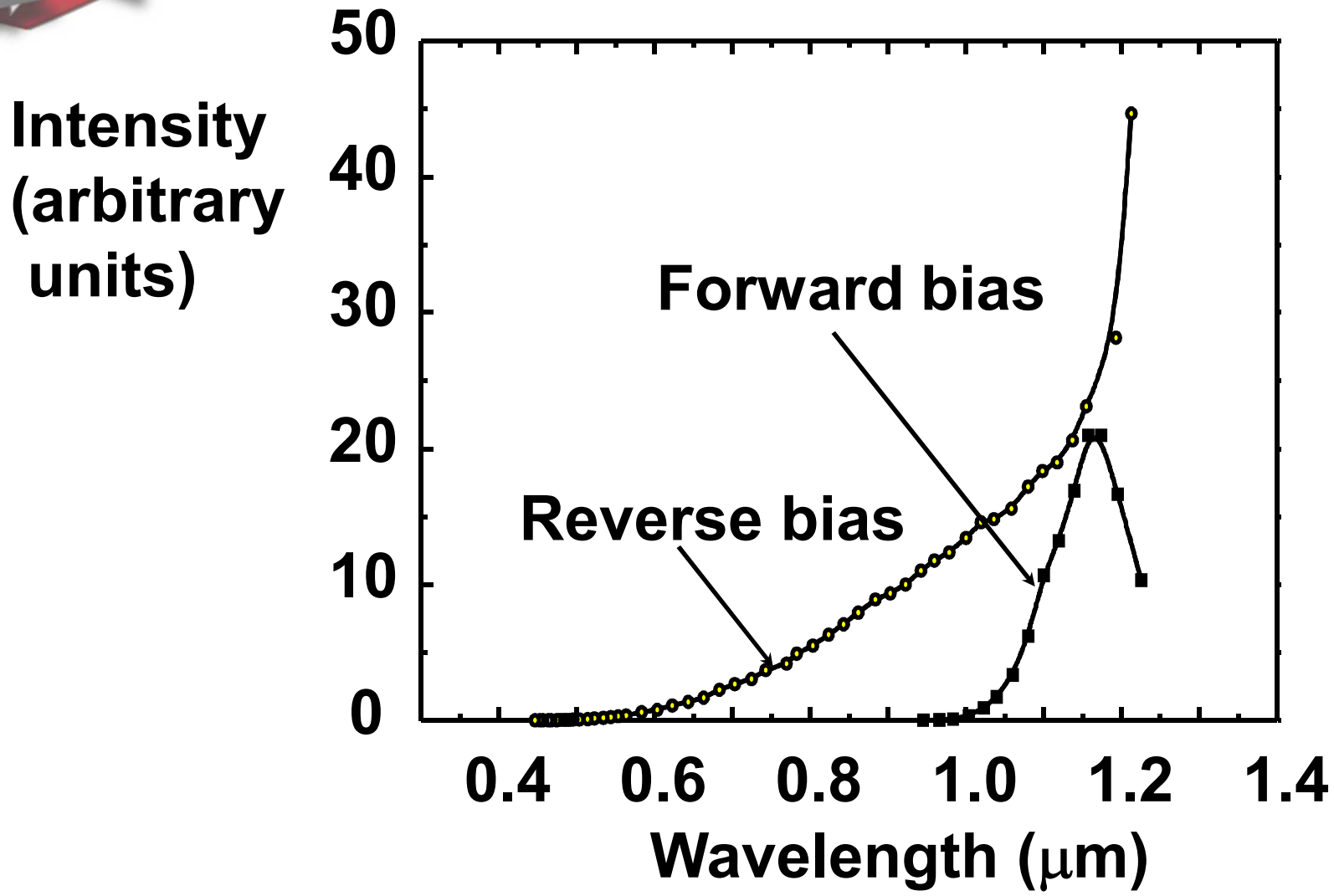
Photoemission via Band-Band Recombination



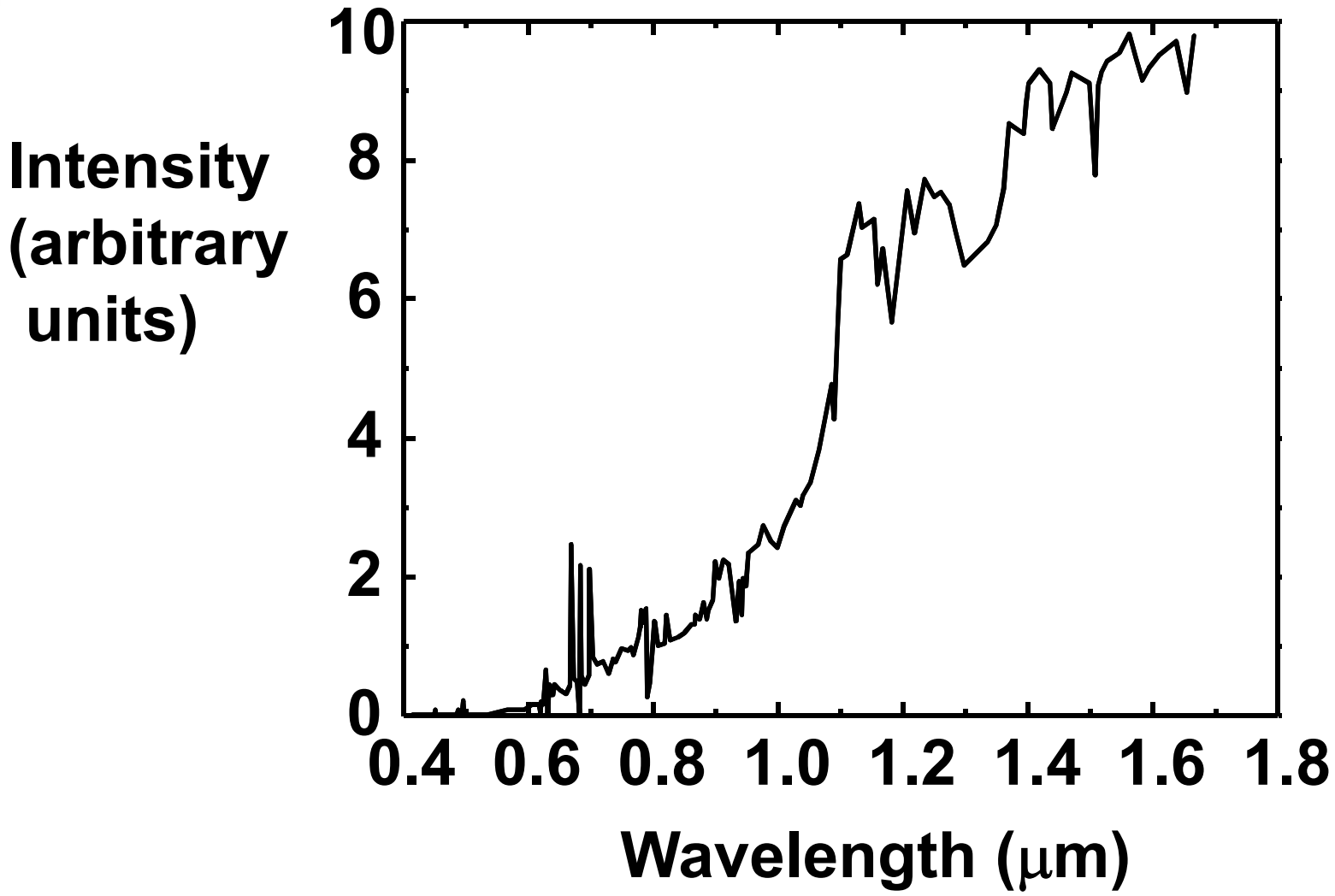
Si Integrated Circuit Emission

Light Emitting Process	E-Field
Forward biased junctions	Low
Reverse biased junctions	High
Latchup	Low
Transistor saturation	High
Gate shorts	Mixed

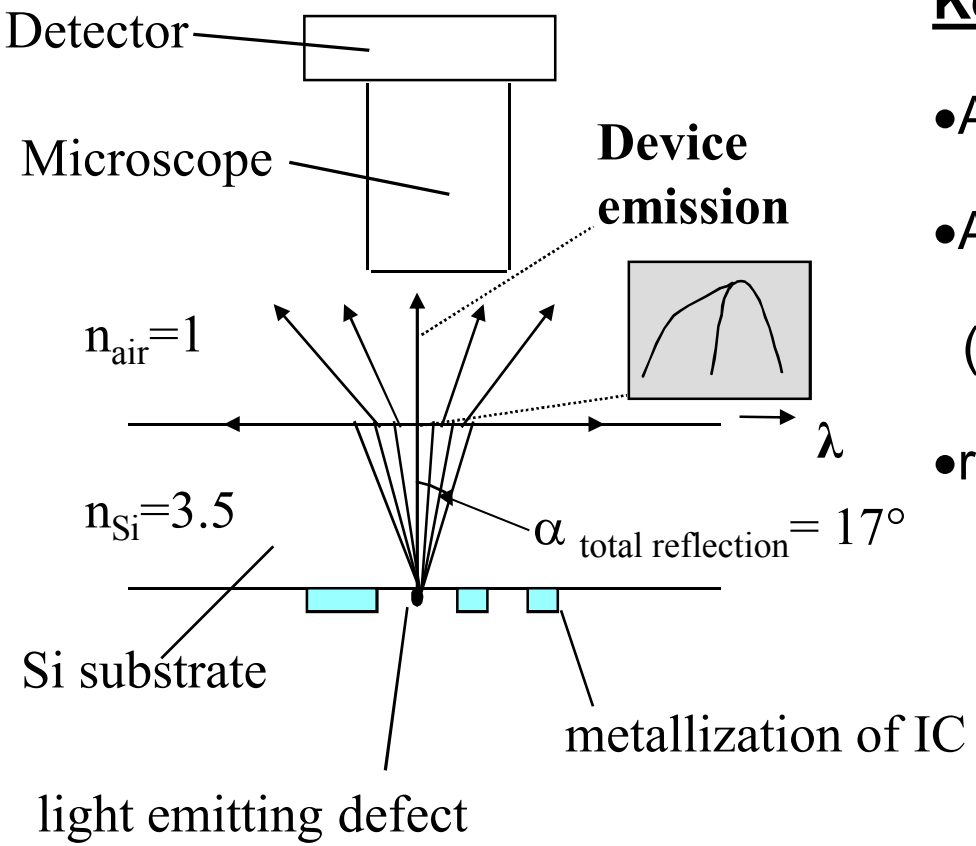
p-n Junction Emission



n-MOSFET Saturation



PEM Inspection from Backside: Key Issues



Key issues:

- Absorption of the Si substrate
- Absorption by free carriers

  (doping density of the Si substrate)
- reflection micrograph:

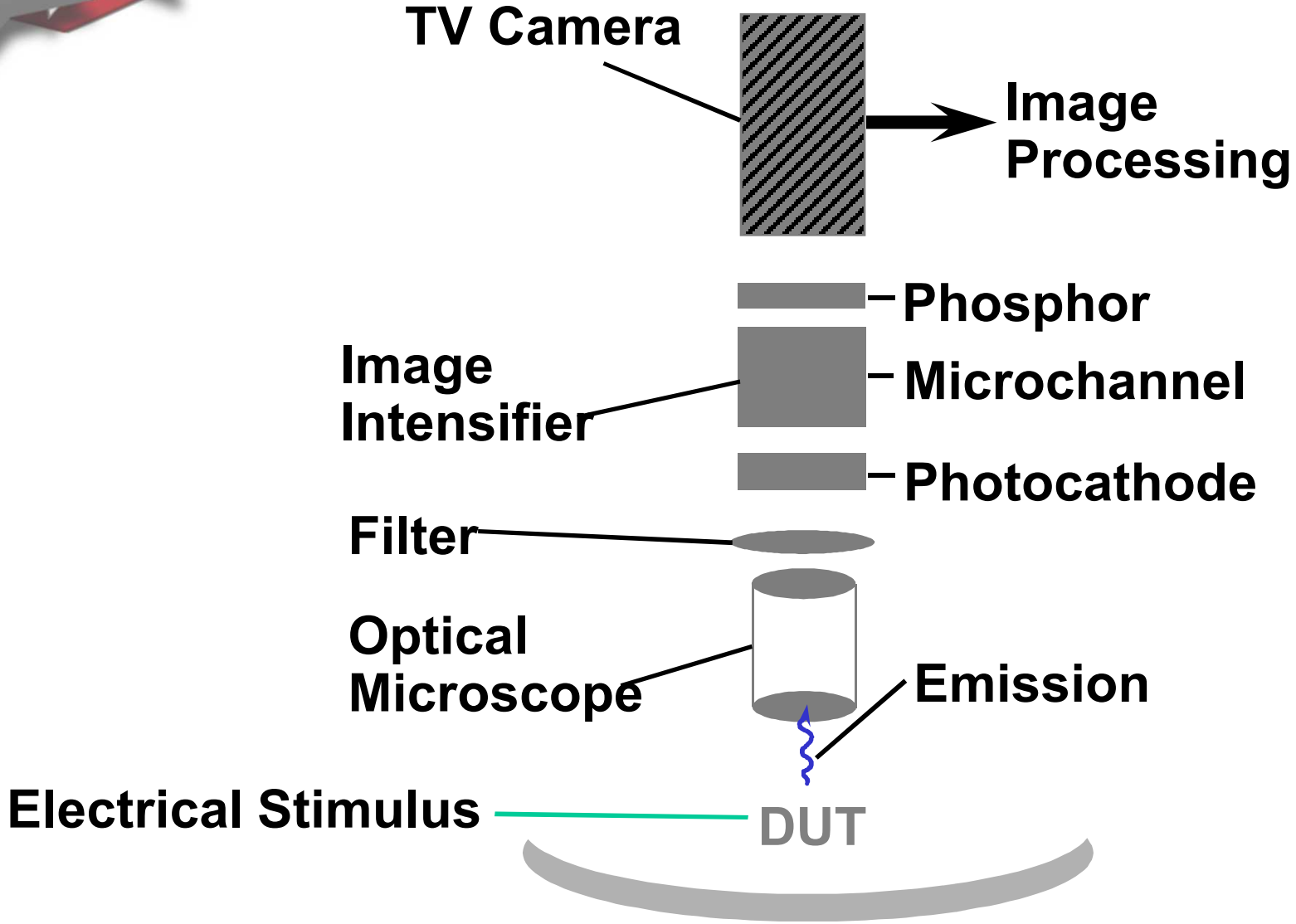
  ⇒hard to get +

  reduced lateral resolution

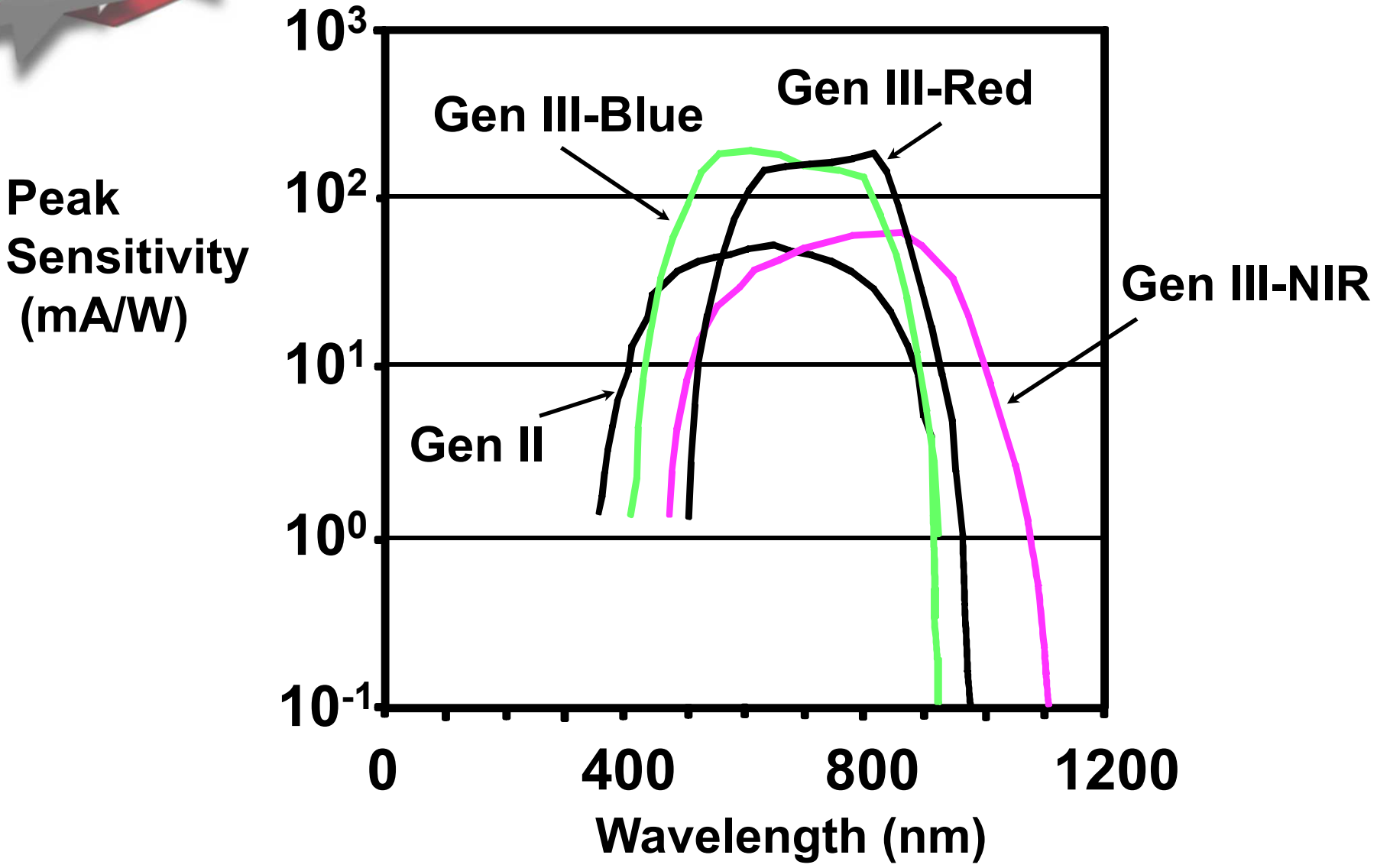
Cameras

- **Intensified cameras**
  - Developed for military night vision use
  - Spectral response centered in visible range
- **Cooled Array Cameras**
  - Developed for high performance imaging applications (Astronomy)
  - Many detector materials and formats available
  - External cooling usually required

Intensified Cameras



Intensifier Response

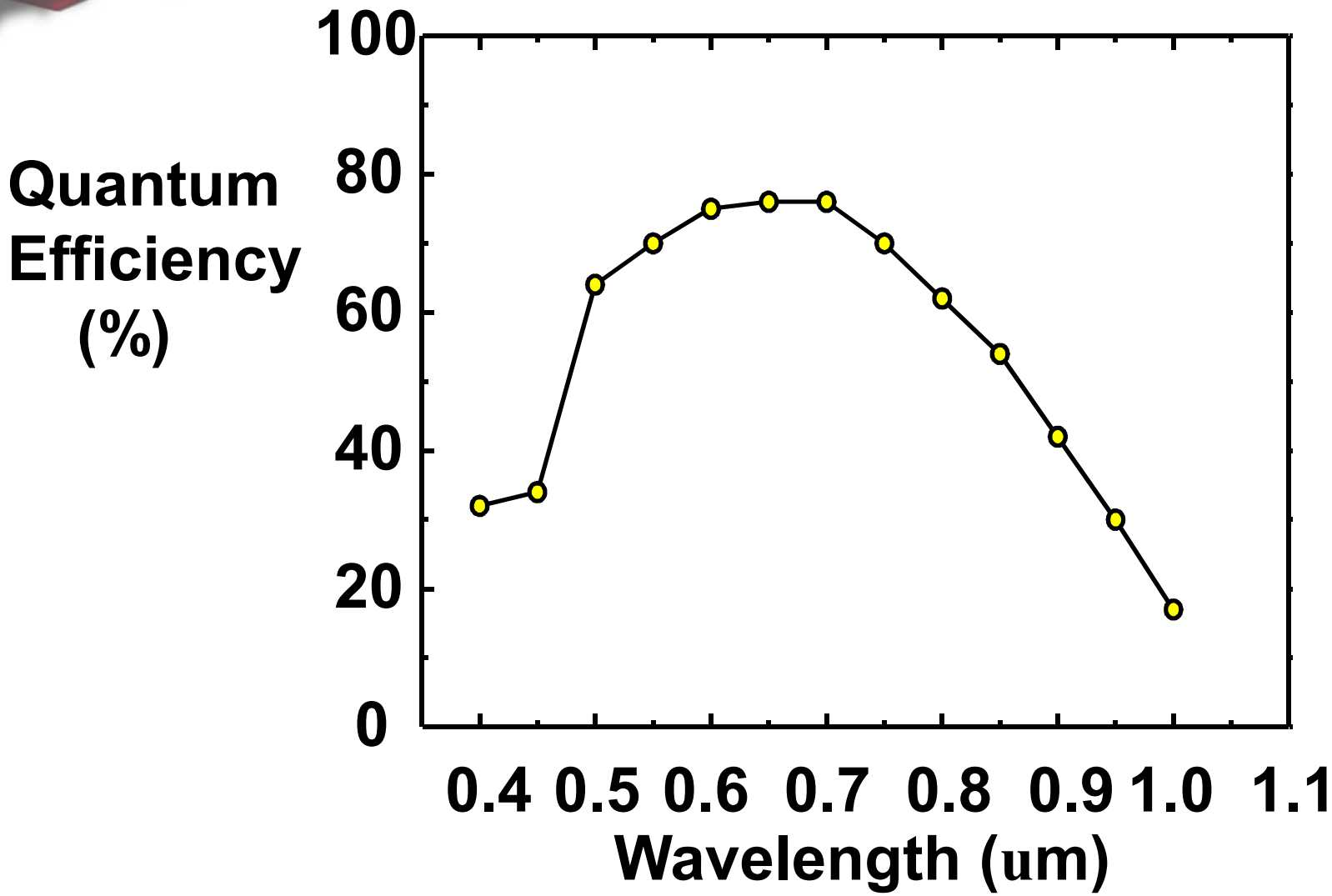


Silicon CCD Cameras

- Cameras commercially available from several sources
- Arrays made by many companies (e.g. Tektronix, Kodak, Thompson, etc.)
- Mature manufacturing technology
- Cooling can be Peltier, liquid/Peltier, or LN_2

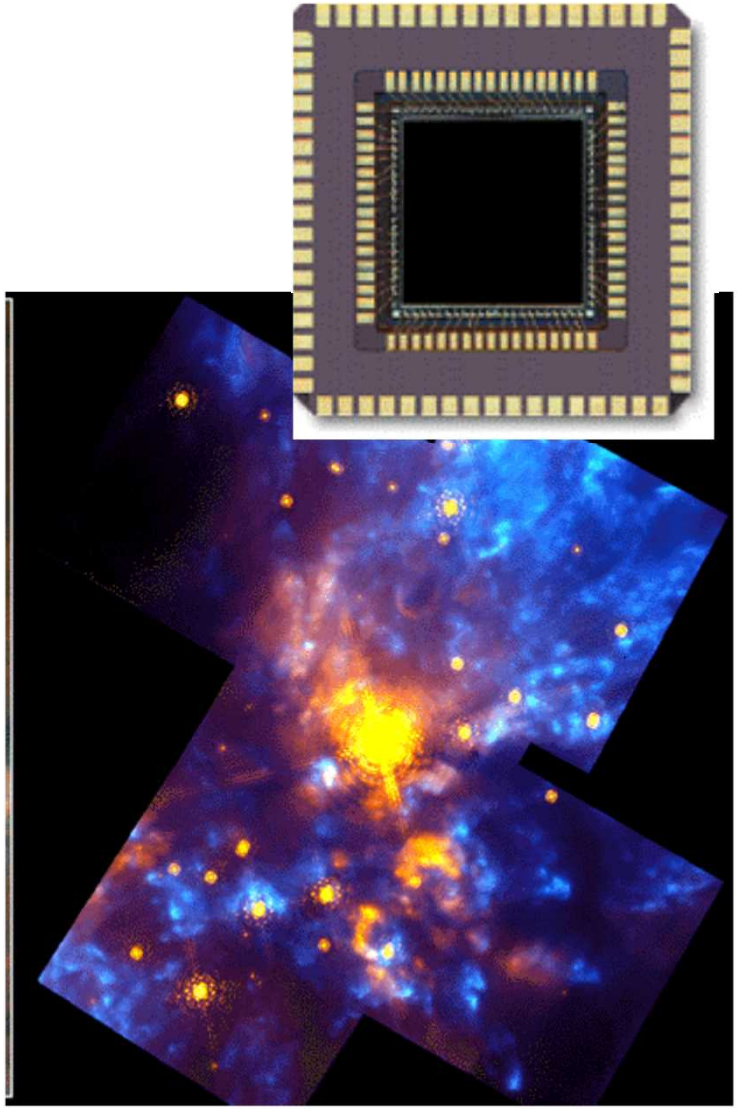
http://www.photomet.com/

Si - CCD Array QE

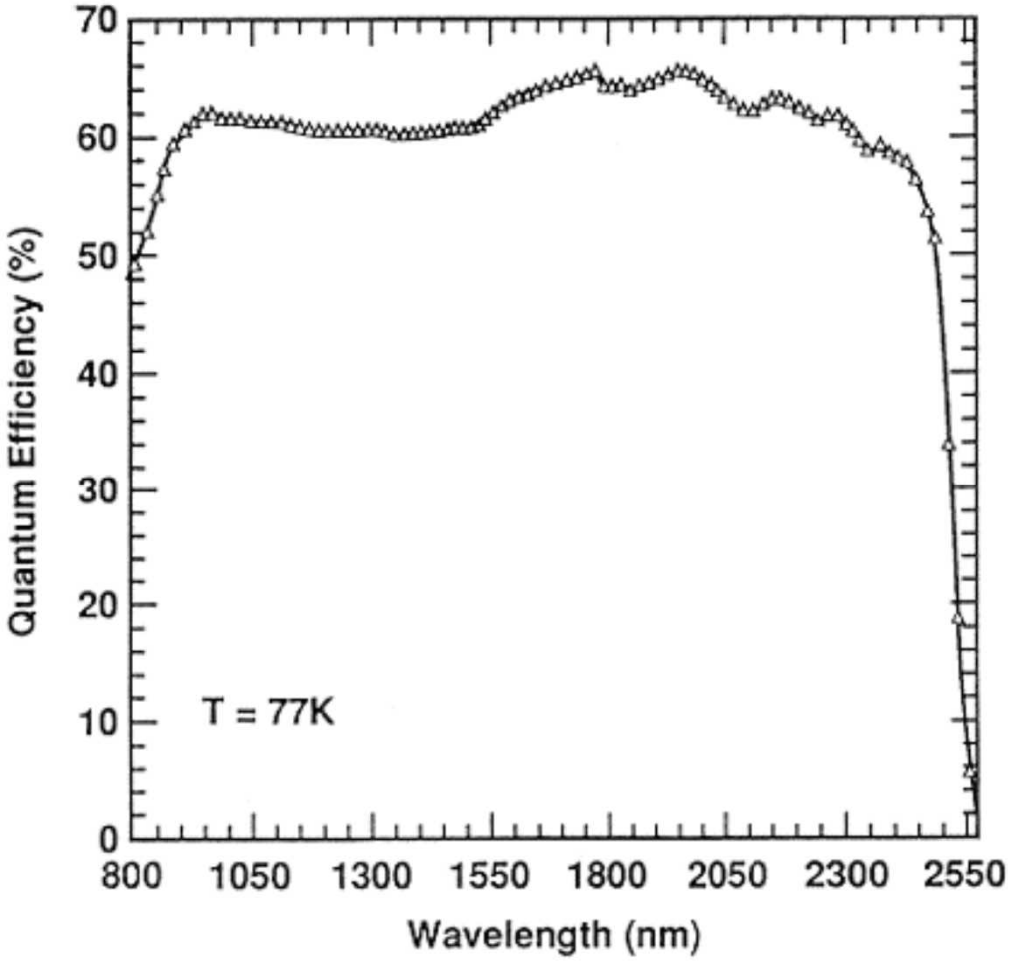


NICMOS Array

- NICMOS - Near Infrared Camera Multi-Object Spectrograph
- 256 by 256 pixel HgCdTe array
- Optimized for use between 800 & 2500 nm
- First Array with Si-CCD level performance in NIR
- Flown on Hubble Space Telescope - February 1997



NICMOS Array Response

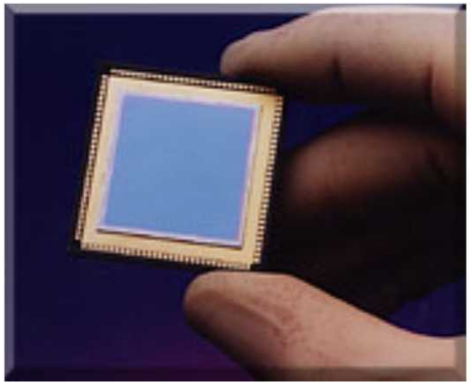


Read Noise (77 K) : **<40 e^-**

Dark Current (77 K): **<1 e^-/s**

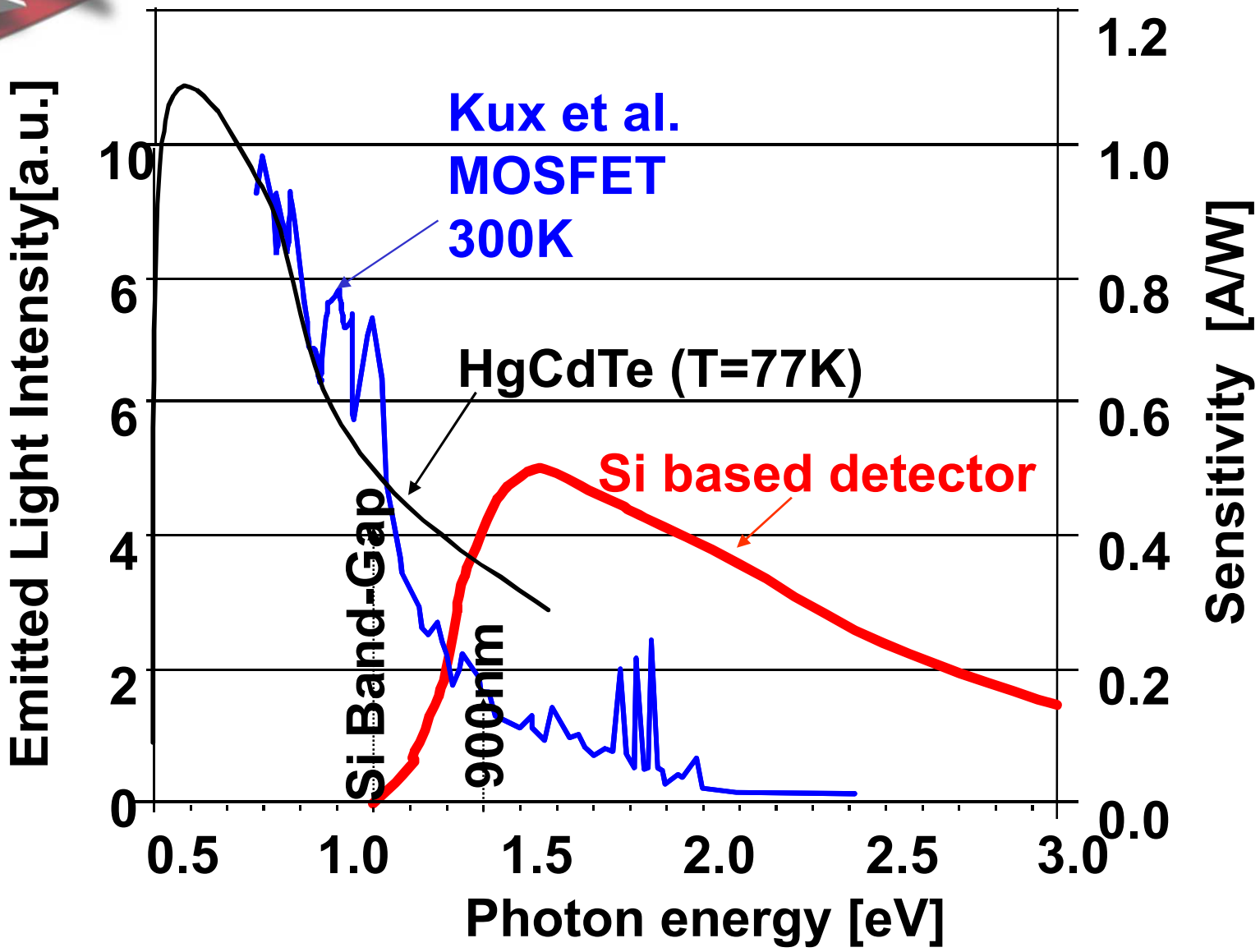
Other NIR Arrays

- Other arrays are available with low noise NIR response:
  - **InSb (Indium Antimonide)**
    - 64x64 to 1024x1024 pixel formats
    - Spectral response ~0.6 to 5 μm
    - Operating temperature 35 K
    - Infrared blocking more difficult
  - **PtSi (Platinum Silicide)**
    - 256x256 pixel array format
    - Spectral range 1 to 5.7 μm
    - Operating temperature 79 K



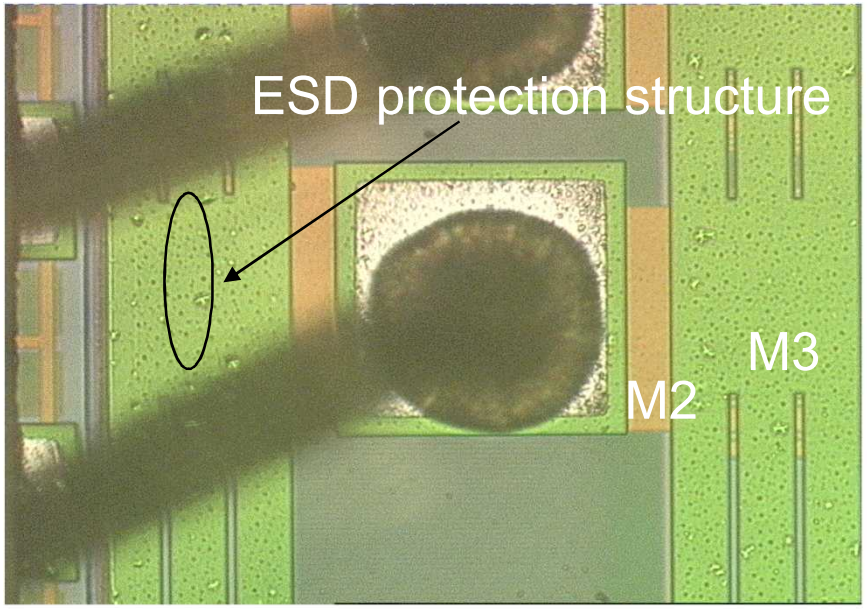
http://www.sbrc.com/

PEM

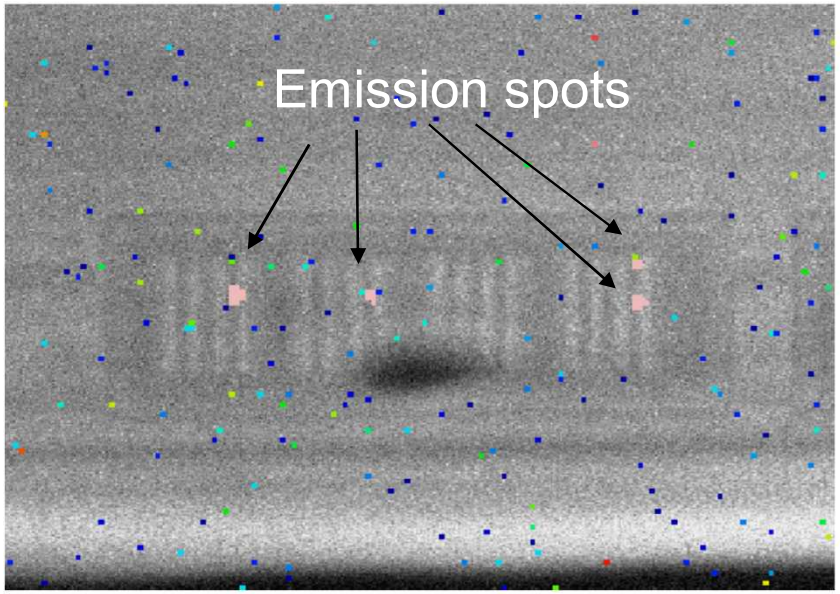

Kux et al.
MOSFET
300K
HgCdTe (T=77K)
Si based detector
Si Band-Gap
900nm
Emitted Light Intensity[a.u.]
Sensitivity [A/W]
Photon energy [eV]
0
2
4
6
6
10
0.0
0.2
0.4
0.6
0.8
1.0
1.2
0.5
1.0
1.5
2.0
2.5
3.0

PEM

Frontside illuminated image



Backside PEM (Si CCD detector)

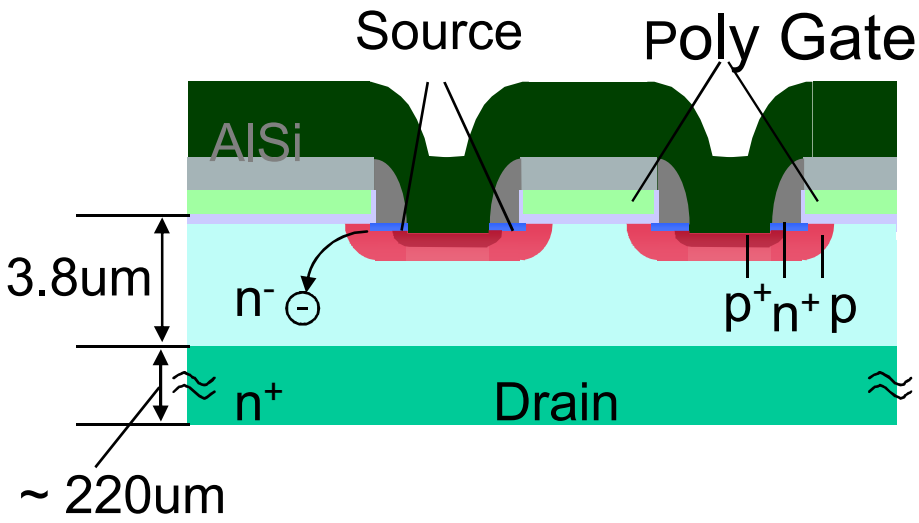


d_{Si}=150µm, $n_{substrate}$=1x$10^{19}$$cm^{-3}$

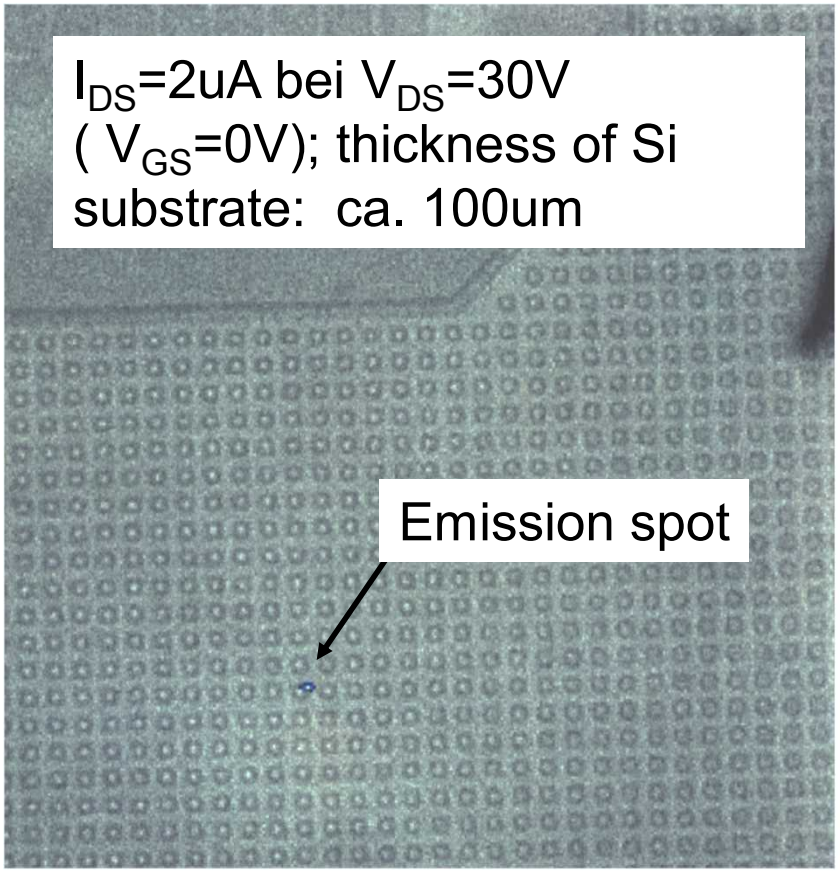
$I_{leakage}$=2µA, V=3.5V after electrical overstresss

30V S-FET: vertical Power MOSFET

Schematics of device



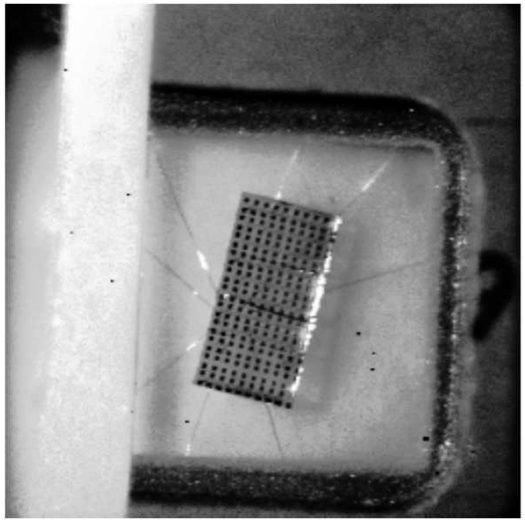
Backside emission microscopy
(Si CCD detector)



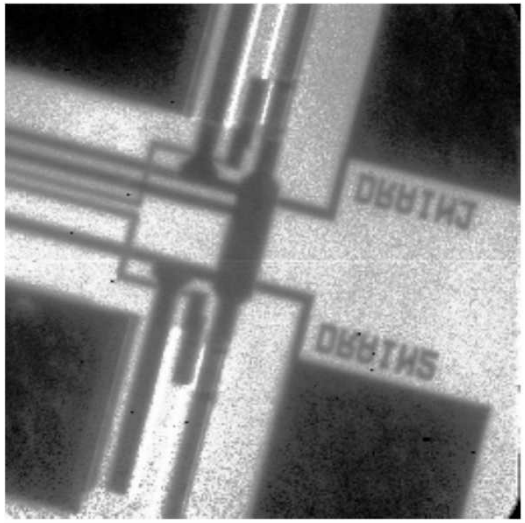
PEM

Backside illuminated images

X1

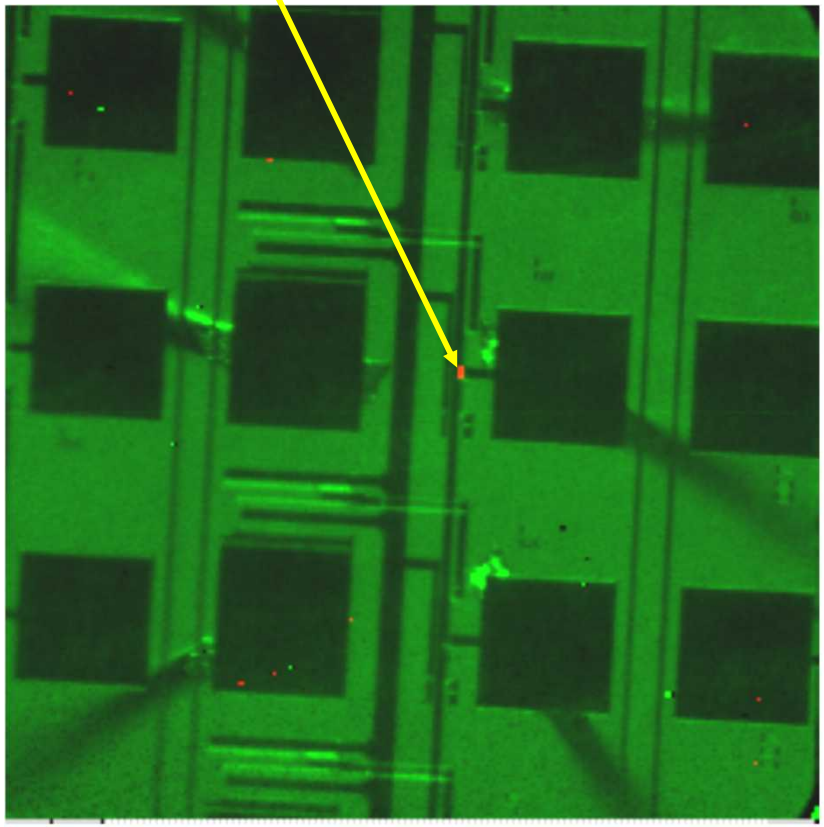


X50



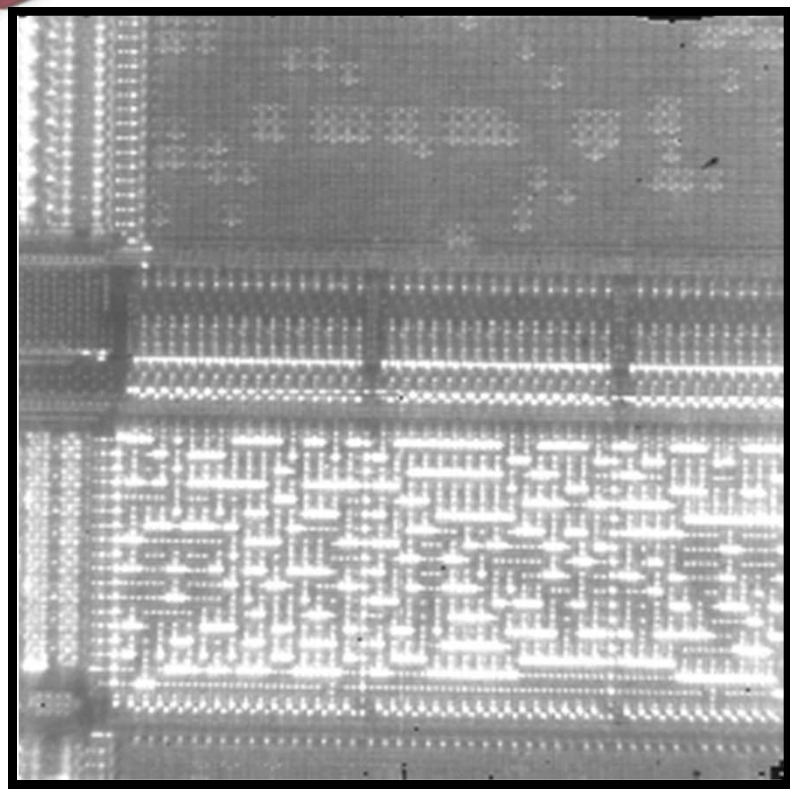
Backside emission signal: n-channel MOSFET

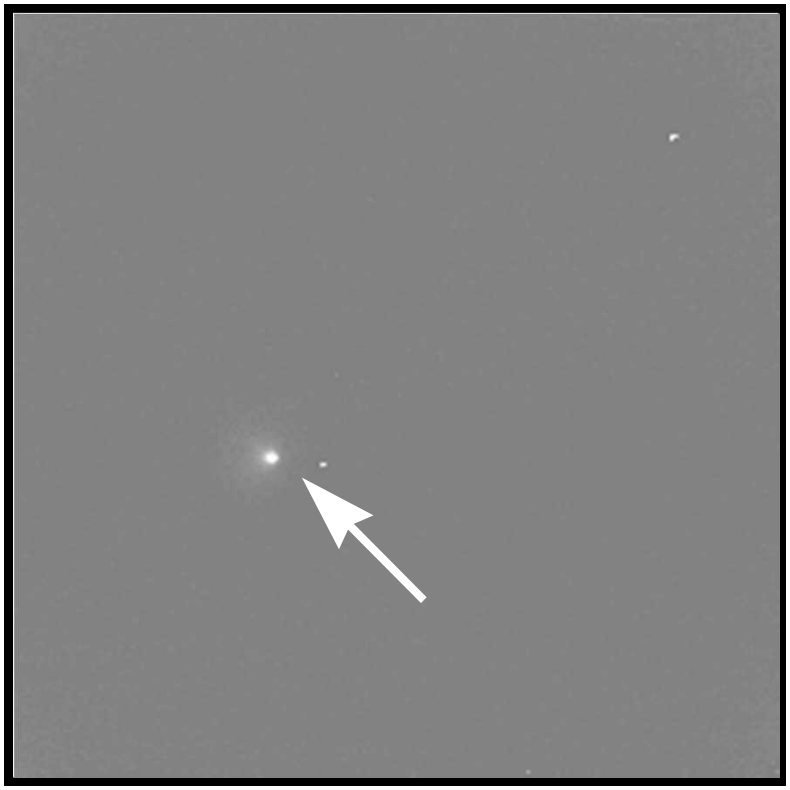
V_g=5V, V_{SD}=3.5V, I_{DS}=1.5mA, 10 sec integration time



Backside emission microscopy with HgCdTe camera; Measurements performed by A. Zaplatin **IR Labs**

Gate Oxide Breakdown

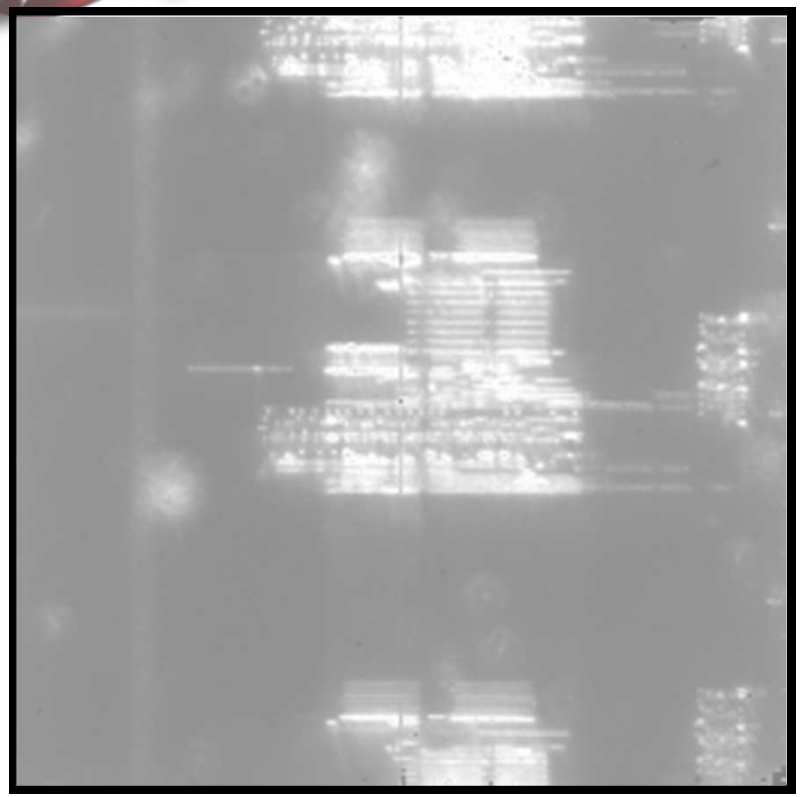




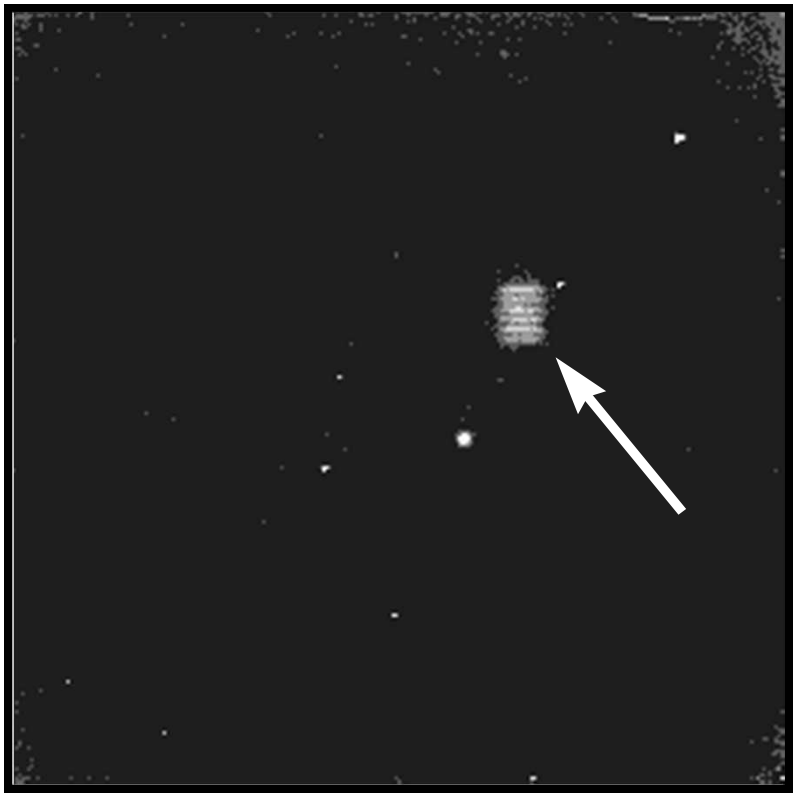
Reflected Image **Emission Image**

1.5 sec. exposure, I_{DD} = 1.47 mA

Saturation Emission



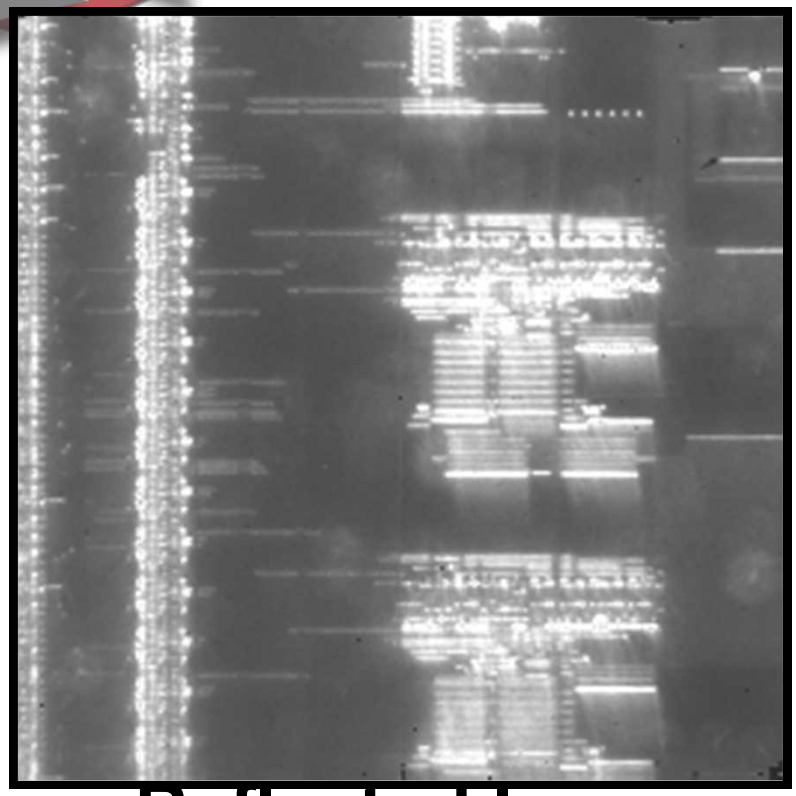
Reflected Image



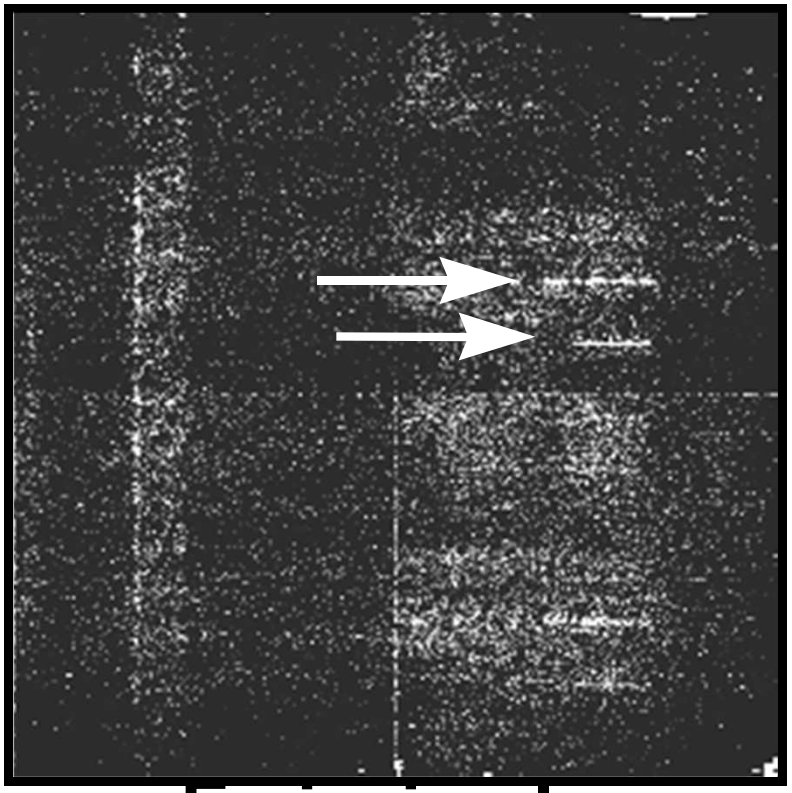
Emission Image

Full thickness die, 10 sec. exposure,
I_{DD} = 225 μA

Backside Defect Detection



Reflected Image



Emission Image

Full thickness die, 200 sec. exposure

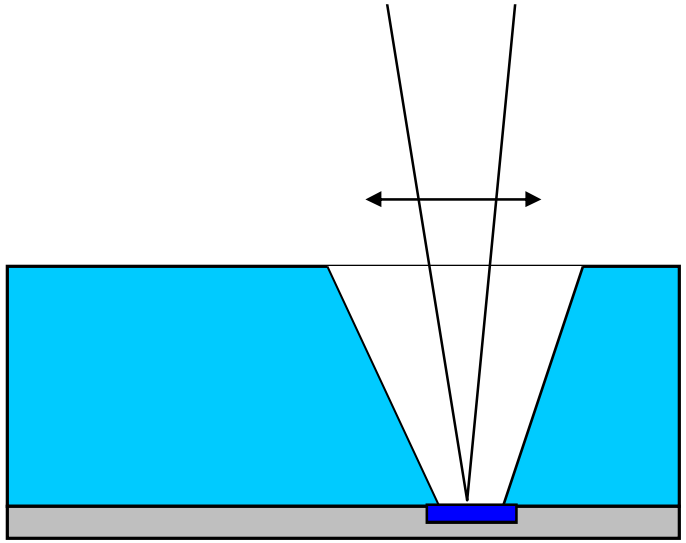
I_{DD} = 200 μA

PEM Conclusions

- Physics suggests stronger light emission in NIR than at visible wavelengths
- Technology to detect NIR emission relatively new
- Head to head comparison of visible and NIR cameras proved NIR emission is stronger
- Similar signal to noise images can be acquired with up to 1000 times shorter exposures

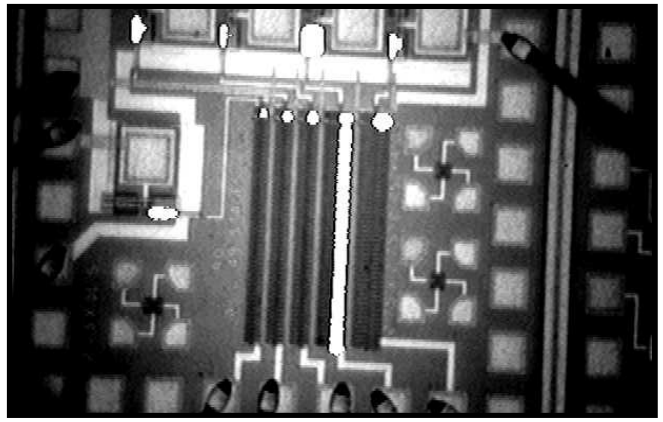
FIB/e-beam Analysis

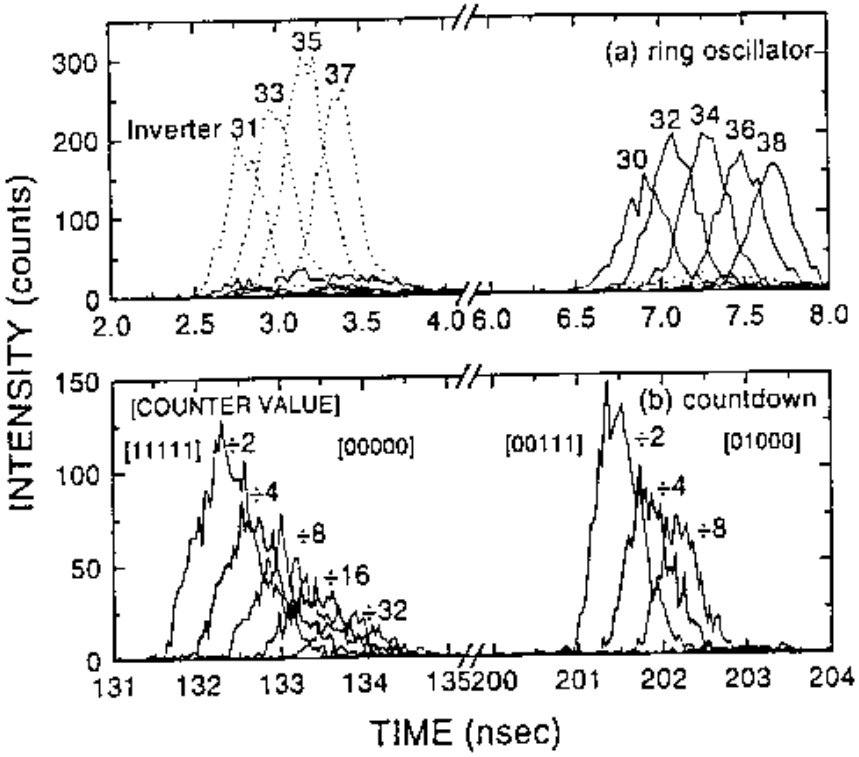
- Adaptation of e-beam probing to flip-chip analysis has proven to be tedious but doable
- Method used FIB with gas assisted etching to expose conductors for probing
- Inverted CAD database used for automated navigation
- Optical methods are preferable as little preparation is needed



PICA

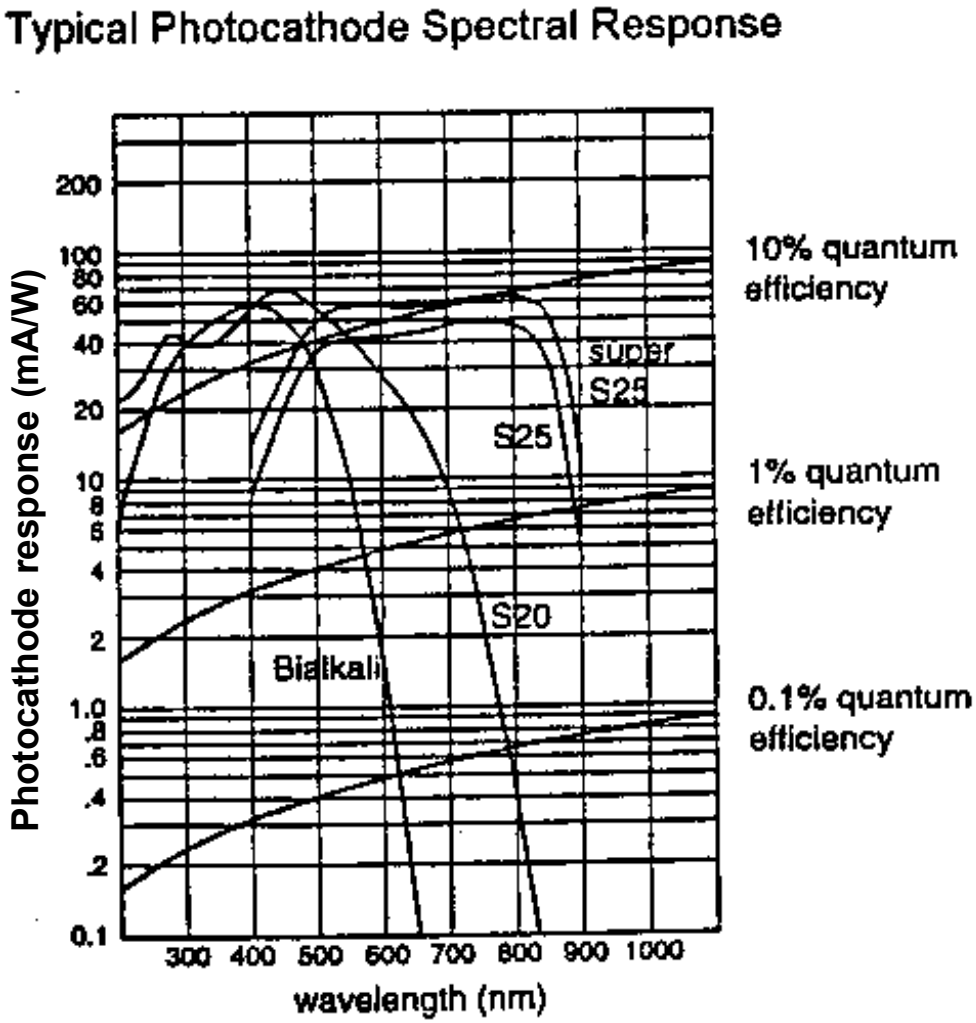
- Picosecond Imaging Circuit Analyzer (PICA)
  - Kash & Tsang, IBM
- Well known that well working gates emit light during switching
- Emission is strongest when gate voltage is half of the drain voltage - the midpoint of the logic transition
- PICA uses a strobed, intensified detector to gather spatial information and time information
- The use of optical information emitted from IC makes PICA non-invasive and fast





PICA

- Gated detector used to stroboscopically acquire timing information
- Thermoelectrically cooled microchannelplate photomultiplier (MCP) with a position sensitive anode used to collect light
- Dark count per pixel ~0.001/s
- Photon timing with 100 ps accuracy possible
- Detector response excellent for frontside, marginal for backside applications

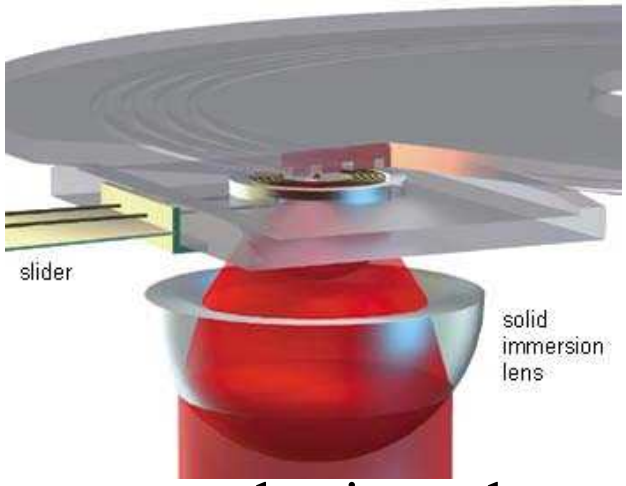


Single Point PICA

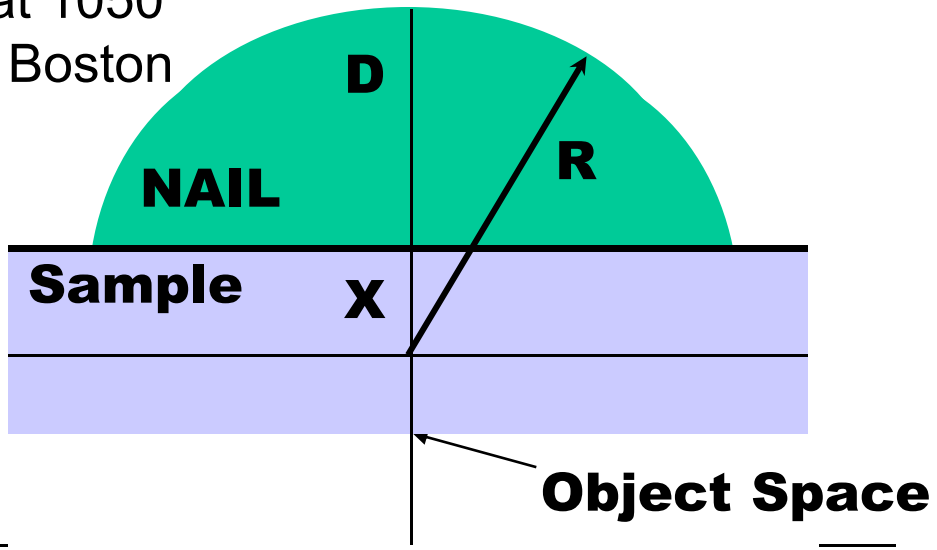
- **Traditional PICA technique**
  - Collect all data from field of view (parallel acquisition)
  - Requires 2-D intensified array camera
  - Collection efficiency and photon flux yield long data acquisition times
    - But you get timing information from every transistor in the field of view
- **Single point PICA**
  - Position single photodetector over transistor of interest
  - Photodetector can be extremely fast and sensitive to IR light
    - More detector choices than in traditional PICA
    - IR-sensitive detectors better for backside applications
  - Issues
    - Positioning detector
    - High NA lenses for resolution and collection efficiency
      - Need solid immersion lenses

Solid Immersion Lenses

- Lateral resolution limit in optical microscopy determined by
  - Wavelength of light
  - Numerical aperture of optical system
  - Index of refraction in object space
- NAIL
  - Numerical Aperture Increasing Lens
  - Resolution of 243 nm reported at 1050 nm wavelength (M. Selim Unlu, Boston University, March 2002)
- SILs for backside FA made of Si
  - same material imaging through

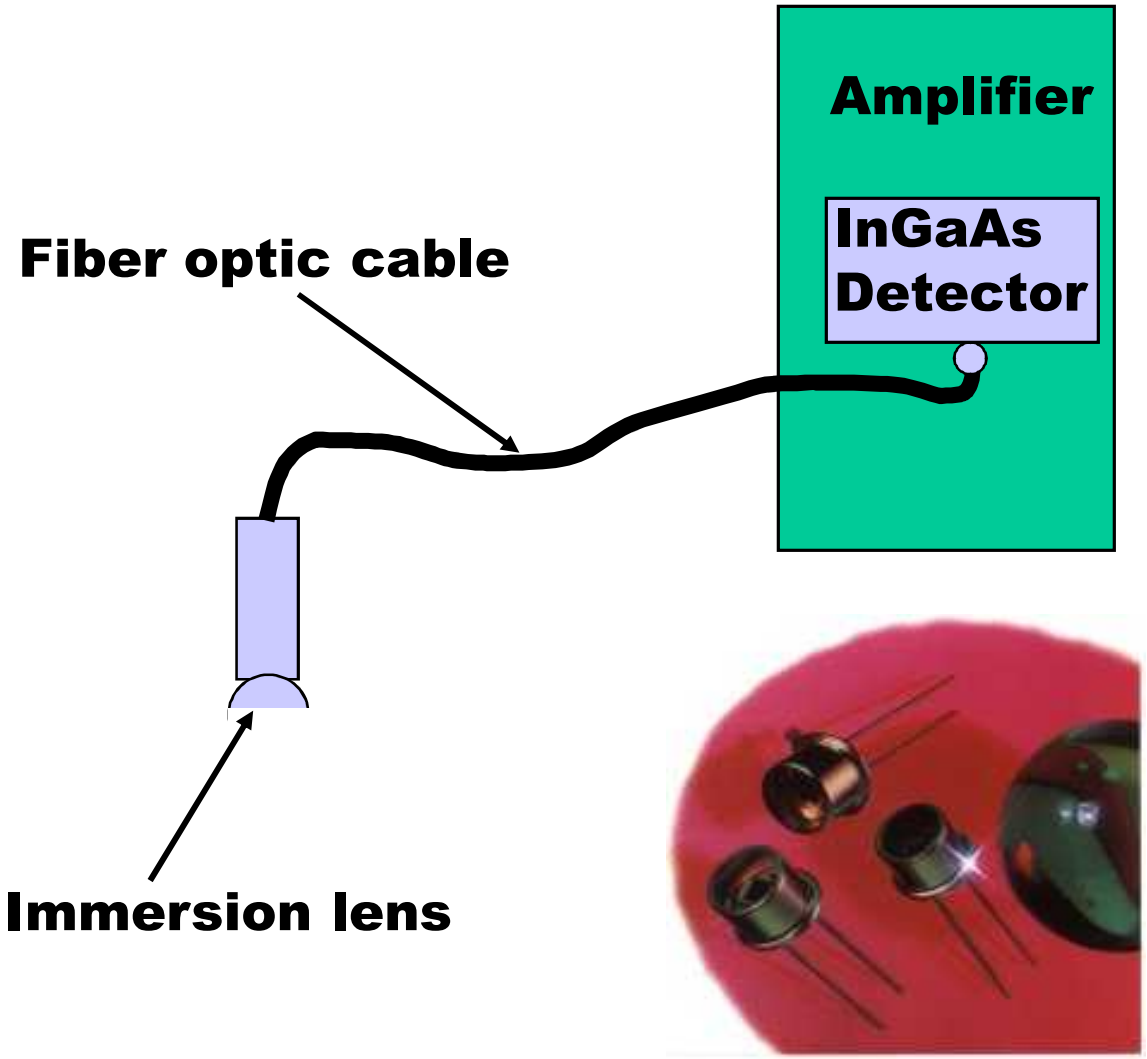


www.physicsweb.org



Single Point PICA

- Method is greatly simplified compared to traditional PICA
  - High NA lens
  - InGaAs photodiode
  - Fiber optic cable
- InGaAs detectors have good sensitivity in IR and are fast (t_r~100 ps)
- Method assumes that you know which transistor to look at
  - Serial data acquisition

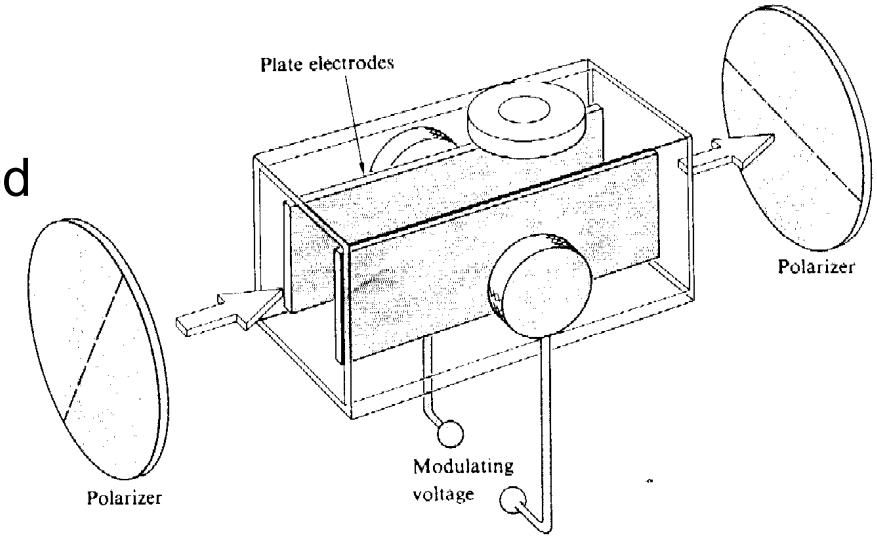


Electrooptic Effects

- First effects observed in 1875 by Scottish physicist John Kerr
- Isotropic, transparent substance becomes birefringent when placed in an electric field
- Optic axis corresponds to the direction of the applied field

$$\Delta n = \lambda_0 K E^2$$

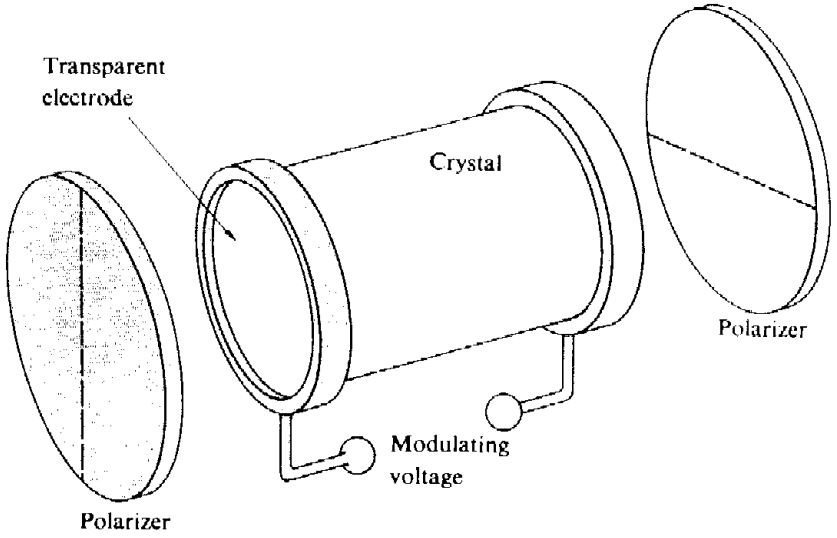
- K is the Kerr constant, E is the applied field, l_0 is the vacuum wavelength in meters



$$\Delta\varphi = \frac{2\pi K \ell V^2}{d^2}$$

Pockels Effect

- German physicist, Fredrich Carl Alwin Pockels
- Studied electrooptic effects in 1893
- Pockels effect has birefringence proportional to electric field to the first power and thus the applied voltage
- Exists only in crystals which lack center symmetry
- KD*P and lithium niobate are common examples
- r_{63} is the electrooptic constant



$$\Delta\varphi = \frac{2\pi n_0^3 r_{63} V}{\lambda_0}$$

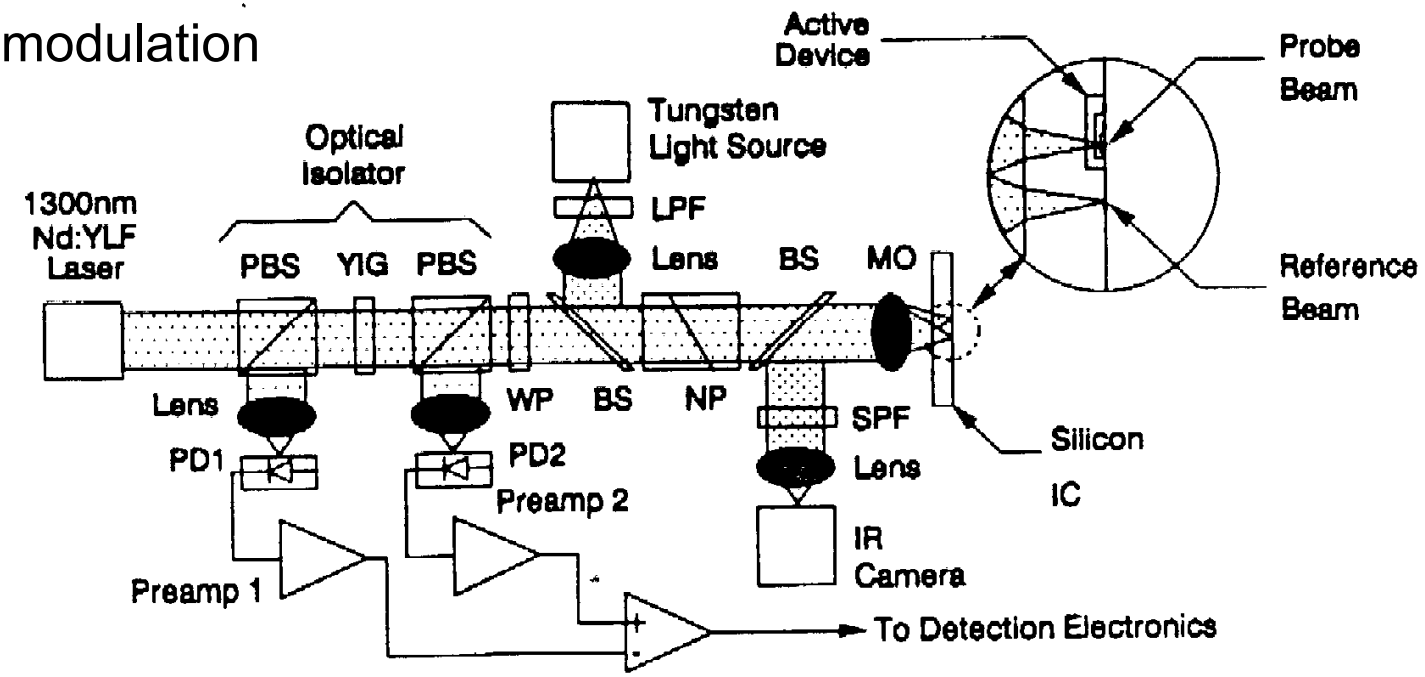
Electrooptic techniques

- Refractive index related to electron and hole concentrations
- N_e, N_h are electron and hole concentrations
- Idea is to sense changes in index of refraction through device backside
- Effects are very fast, allowing GHz frequency measurements

$$\Delta n = \frac{n_0 q^2}{2\omega^2 \varepsilon}\left[\frac{b_e N_e^{1.05}}{m_{ce}^*} + \frac{b_h N_h^{0.80}}{m_{ch}^*}\right]$$

E-O

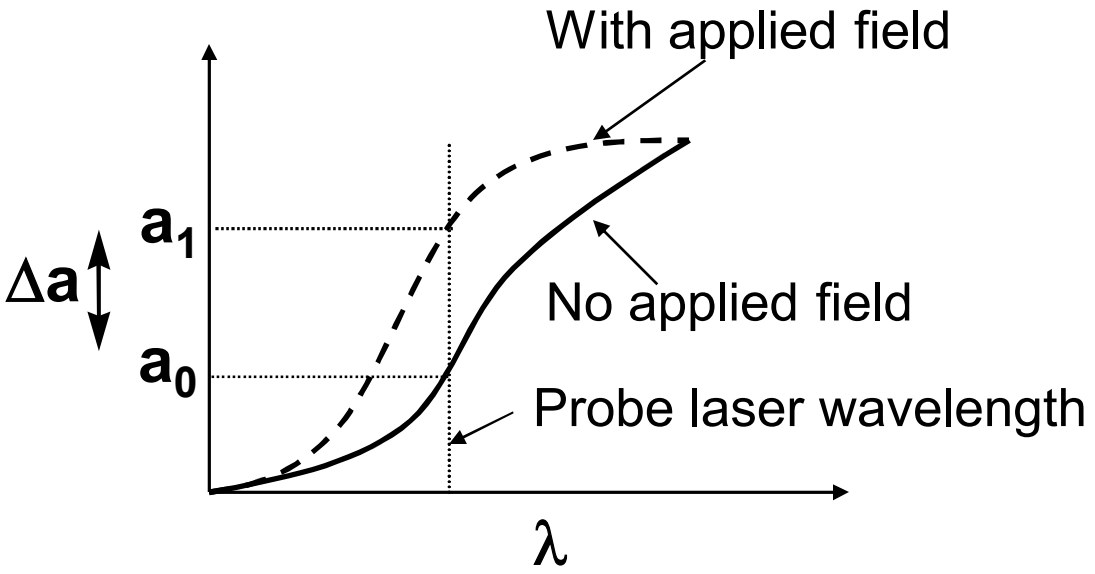
- Pulsed Nd:YLF (1.3 mm) laser (50 ps)
- Light split into two beams with custom Nomarski prism
- Compare phase of reference beam with probe beam
- Phase difference translates to a polarization change when beams are combined
- Polarization modulation converted to amplitude modulation



Laser Voltage Probe (LVP)

- Work first done in early 1980's
- Early work in Silicon done at Stanford University by Bloom, and Heinrich
- Franz-Keldysh effect - electro-absorption
  - Electric fields > 10^4 V/cm
  - Tunneling states created
  - Tunneling states effectively reduce the bandgap
  - Photons near bandgap wavelength now absorbed

Absorption Characteristics at High Electric Field



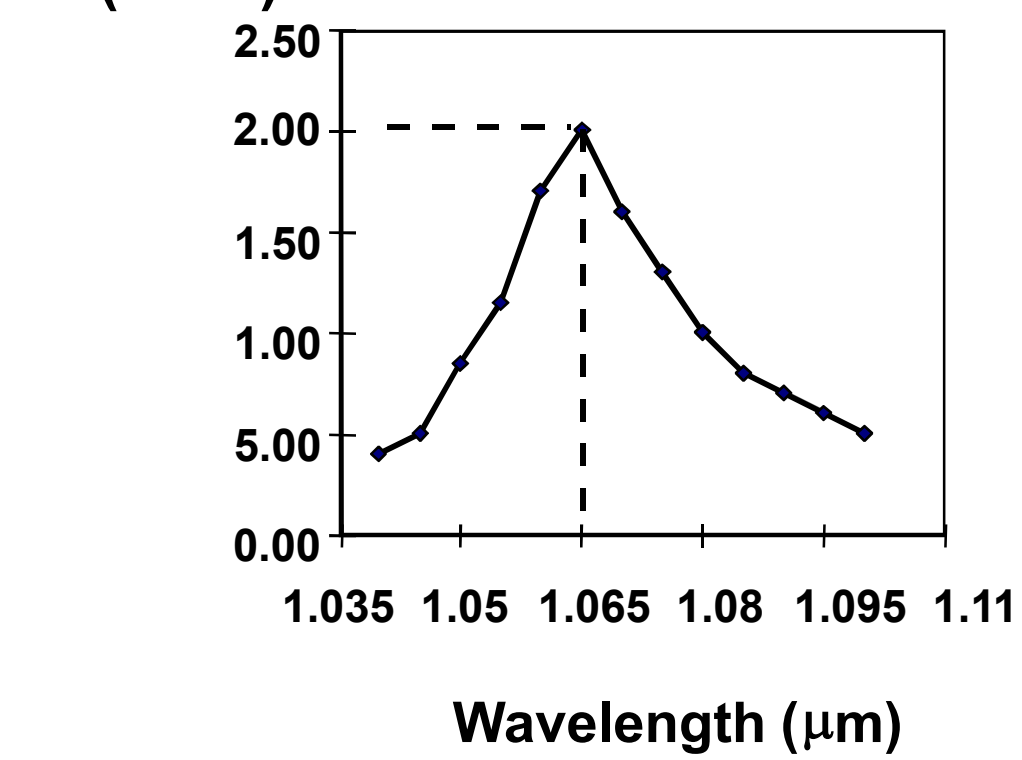
- Change in absorption with applied electric field
- Probe beam wavelength is fixed
- absorption at probe wavelength changes

Normalized Electro-Absorption

$$\Delta a = (a_1 - a_0) / a_0$$

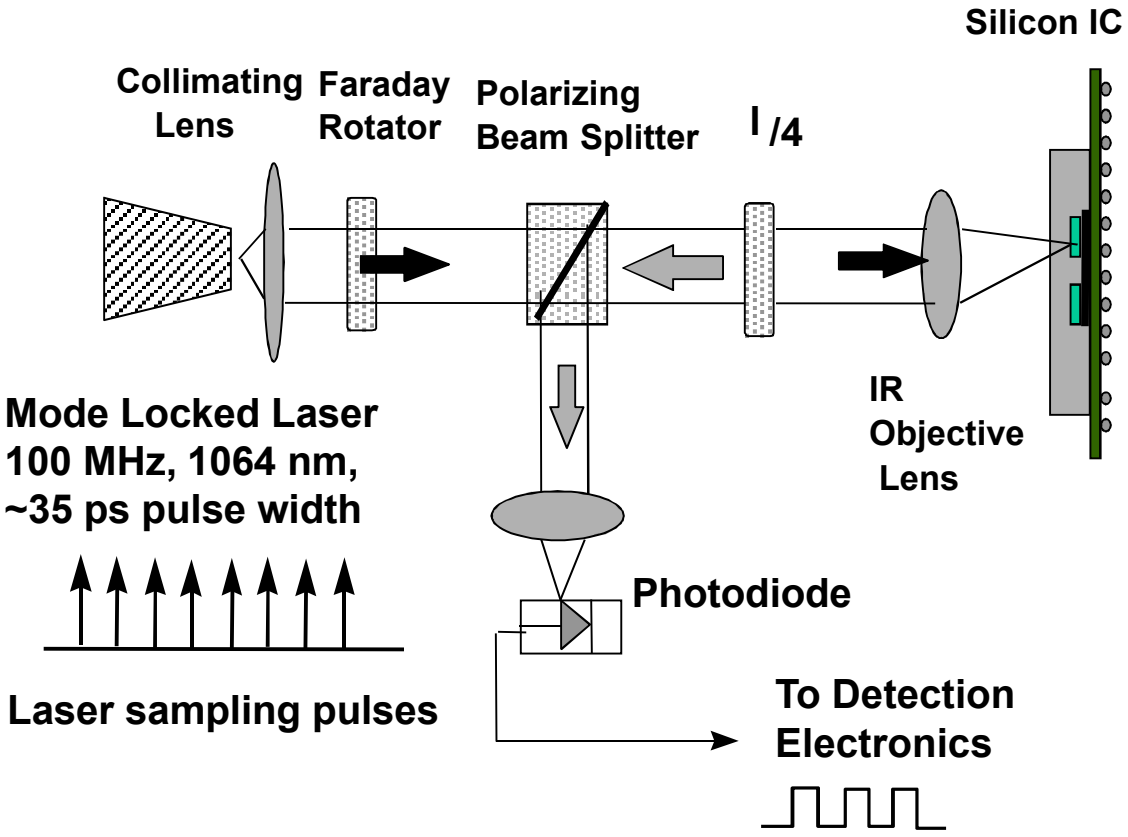
LVP

- Measured F-K absorption change with wavelength
- Maximum effect at 1065 nm
- 1064 nm is convenient Nd:YAG line
- Magnitude of effect is ppm level



LVP

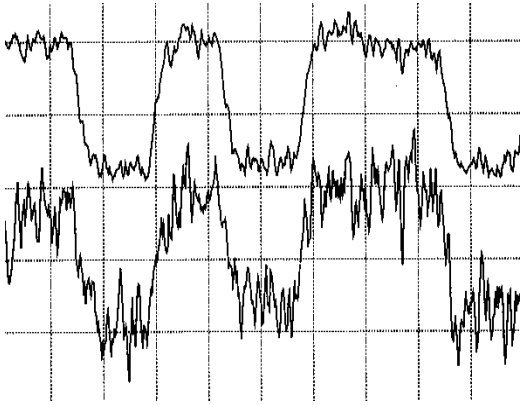
- Equipment setup similar to other e-o based methods
- Mode locked laser allows ~12 GHz bandwidth
- IR laser limits spot size to ~0.7 mm



LVP example

- Comparison of e-beam to LVP
- Both waveforms use stroboscopic technique
- e-beam pulse width can be changed
- Laser pulse width cannot
- Cannot reduce BW of LVP to improve signal

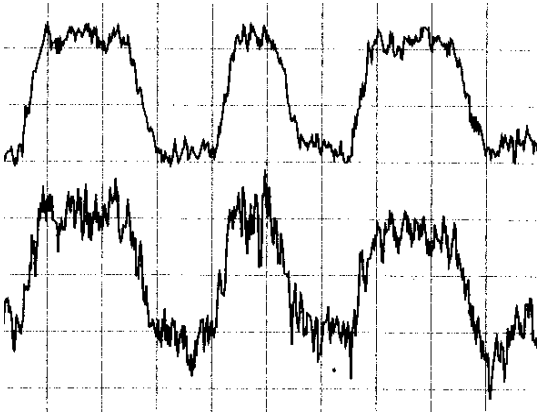
E-Beam (50ps sampling pulse)



5 min. avg.

30 s avg.

LVP (35ps sampling pulse)



5 min. avg.

30 s avg.

20 ns

LVP Summary

- LVP systems commercially available
- Improvements in IR laser technology will improve BW (Ti:Sapphire lasers have fs pulse widths but not in IR)
- Interaction of IR laser with circuit operation needs research - LIVA and related techniques rely on this interaction

SLM Techniques

- **Scanning Laser Microscope (SLM) based analysis techniques**
  - LIVA (Light-induced voltage alteration)
  - TIVA (Thermally-induced voltage alteration)
  - SEI (Seebeck effect imaging)
  - OBIRCH (Optical beam-induced resistance change)
- **Useful for localizing open and shorted interconnections simultaneously**
- **Demonstrate front and backside IC examples**

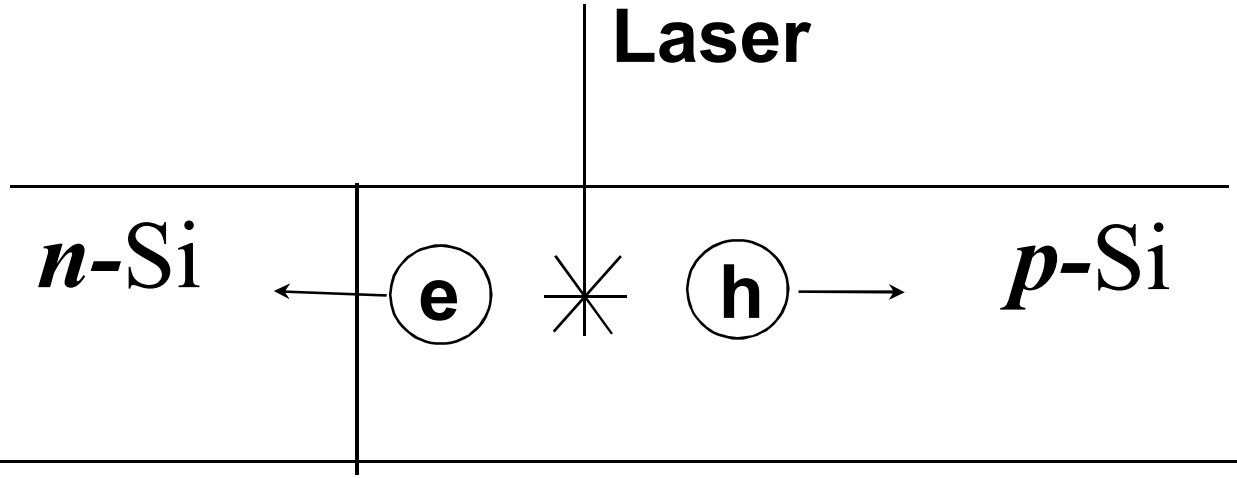
Light-Induced Voltage Alteration (LIVA)

- Enables:
  -quick localization of defective junctions and junctions connected to defects
  -imaging of transistor logic states (off or on)

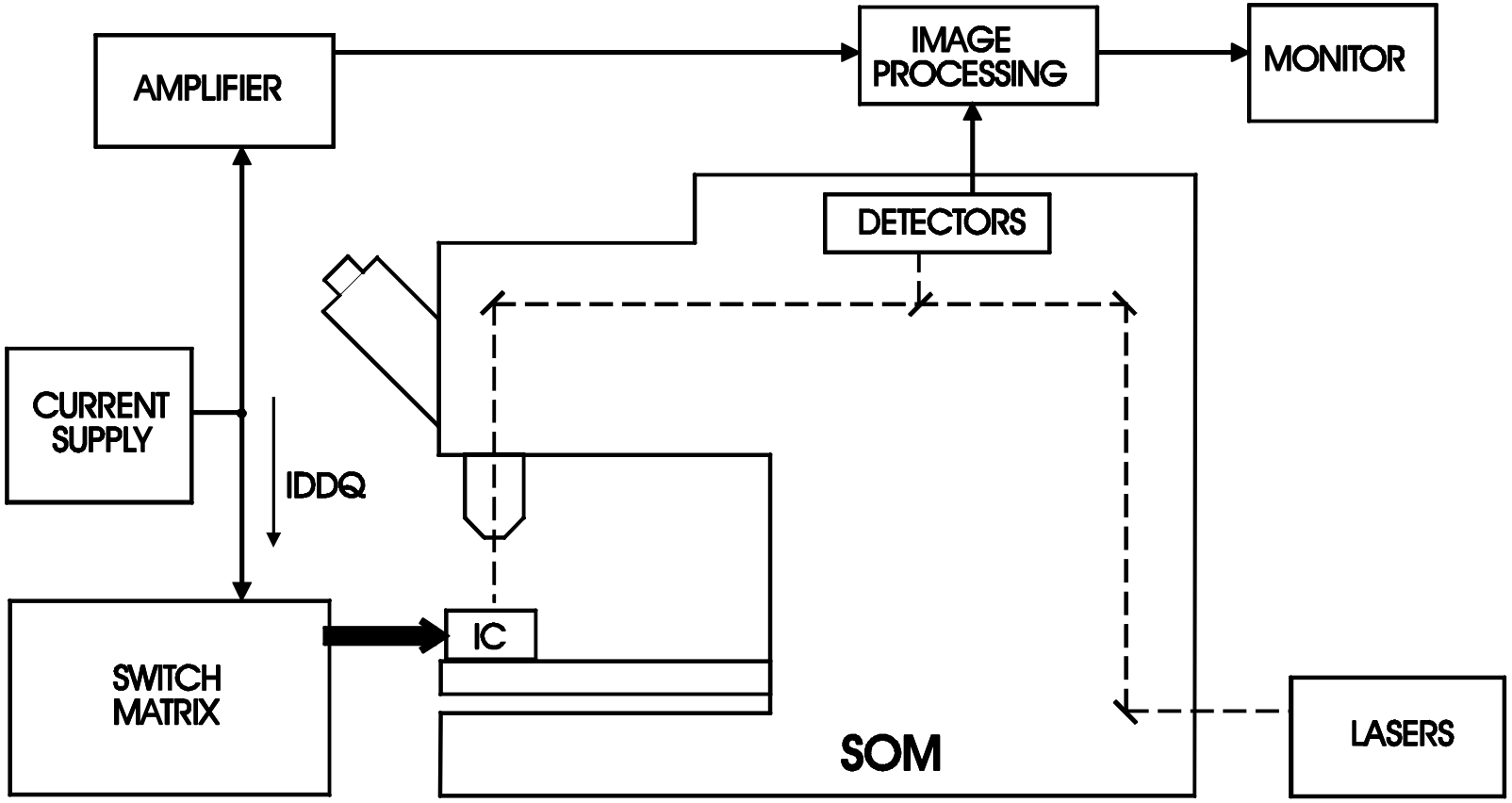
- Easily implemented on existing scanning optical microscopy (SOM) equipment

Electron-hole pair (ehp) Generation from Photons

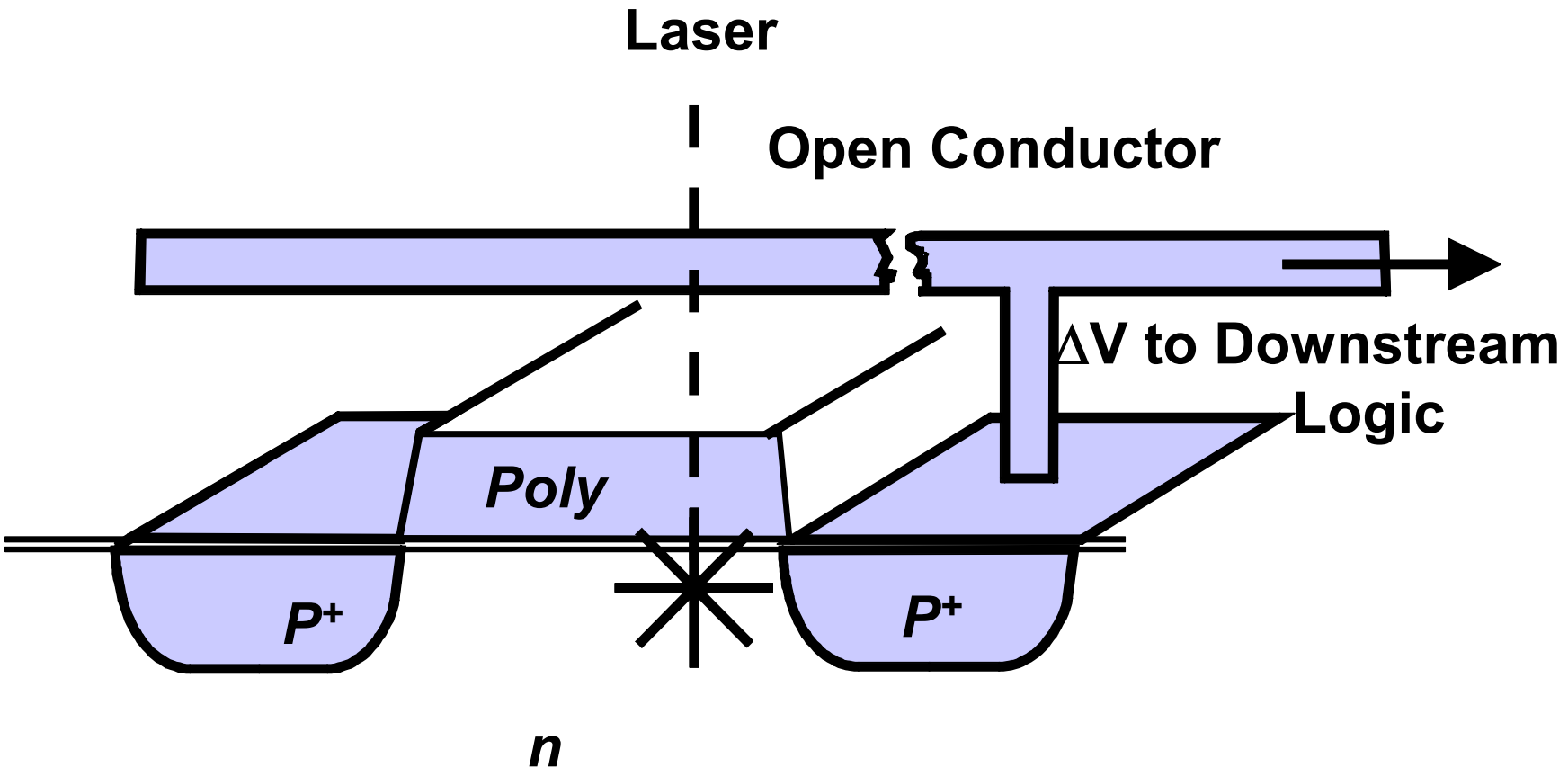
- Photons injected into Si with energies greater than the indirect Si bandgap (~1.1 eV) will produce ehps
- Nonrandom recombination of ehps will produce a "photocurrent" that affects IC operation



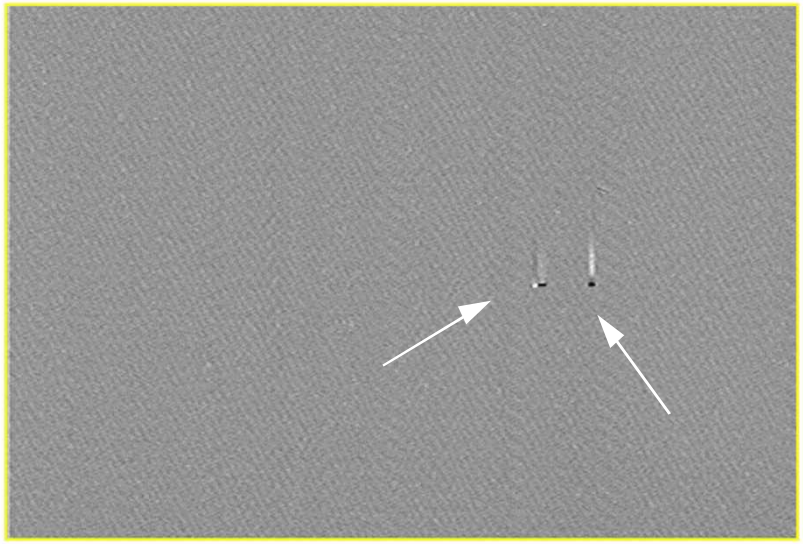
LIVA System


AMPLIFIER
IMAGE PROCESSING
MONITOR
DETECTORS
CURRENT SUPPLY
IDDQ
IC
SWITCH MATRIX
SOM
LASERS

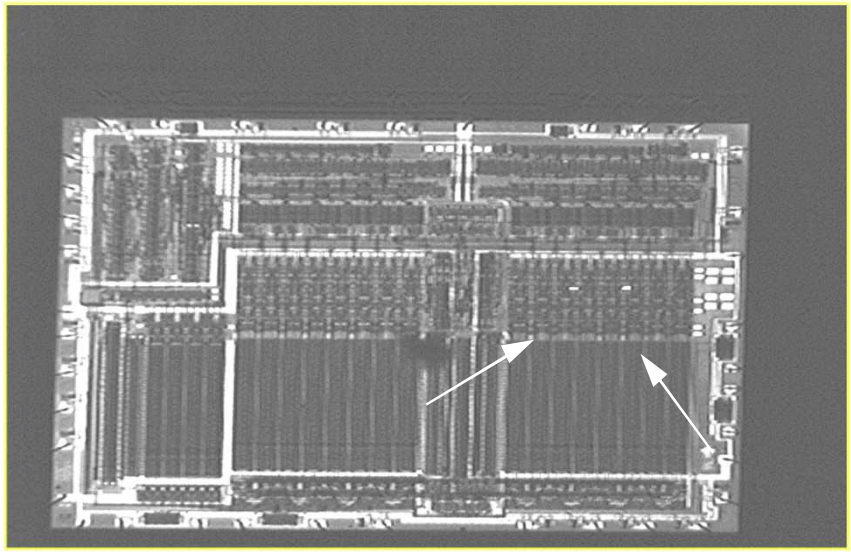
LIVA Signal From Open Conductors



LIVA Example: Open Conductors

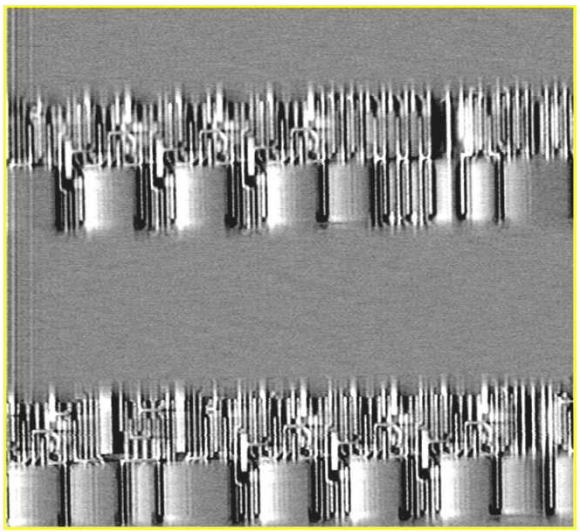


LIVA image

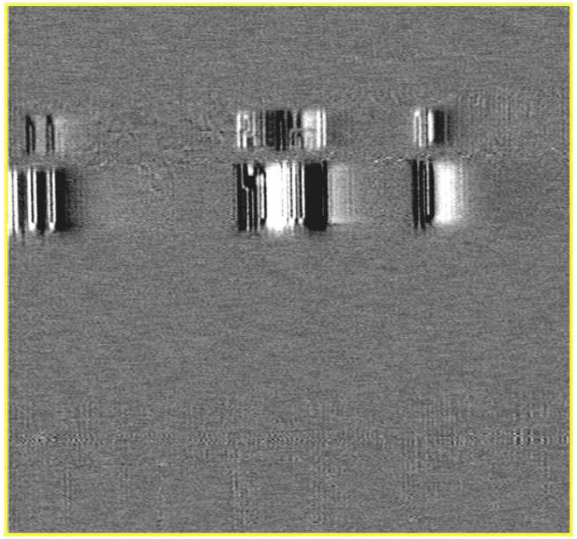


LIVA/Reflected image of the same field of view

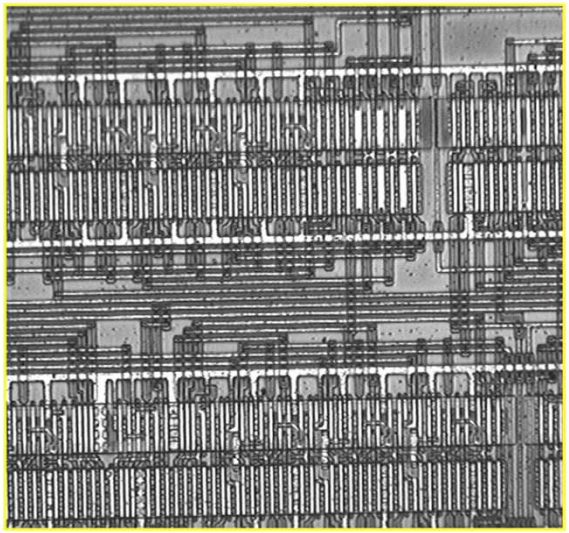
LIVA Example: Logic State Imaging



Transistors generate a LIVA signal from nonrandom ehp recombination

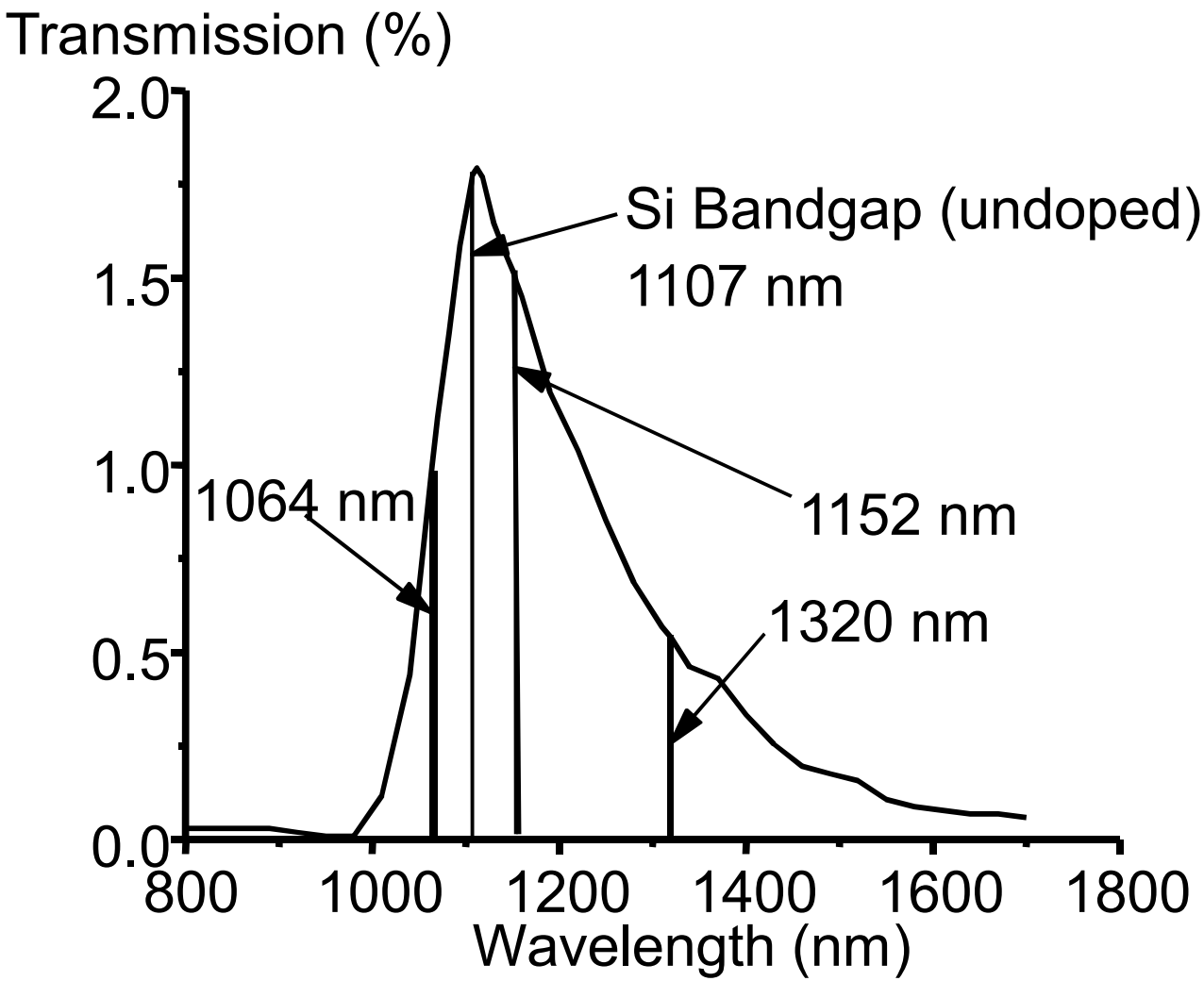


LIVA difference between two logic states

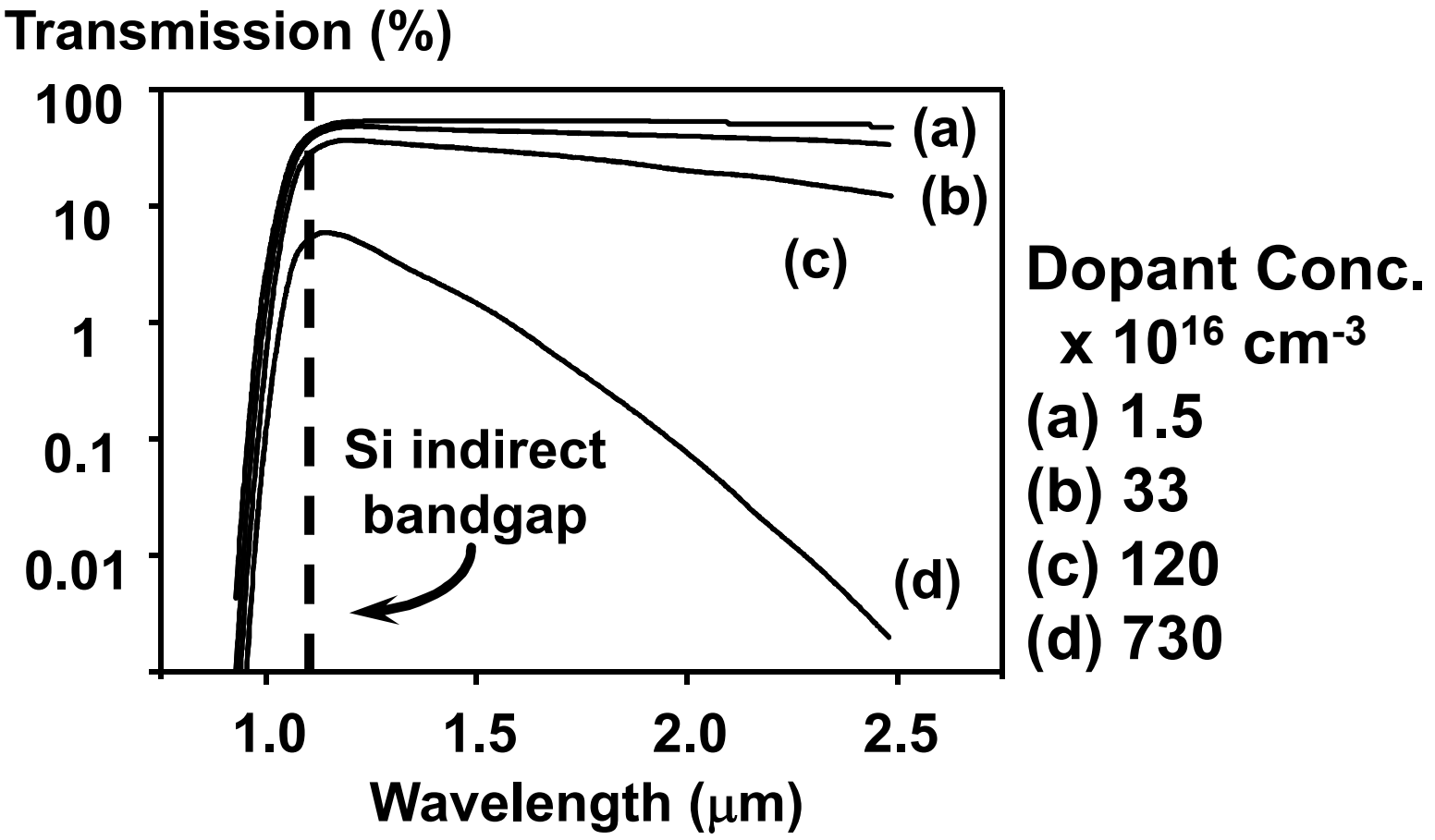


Reflected light image

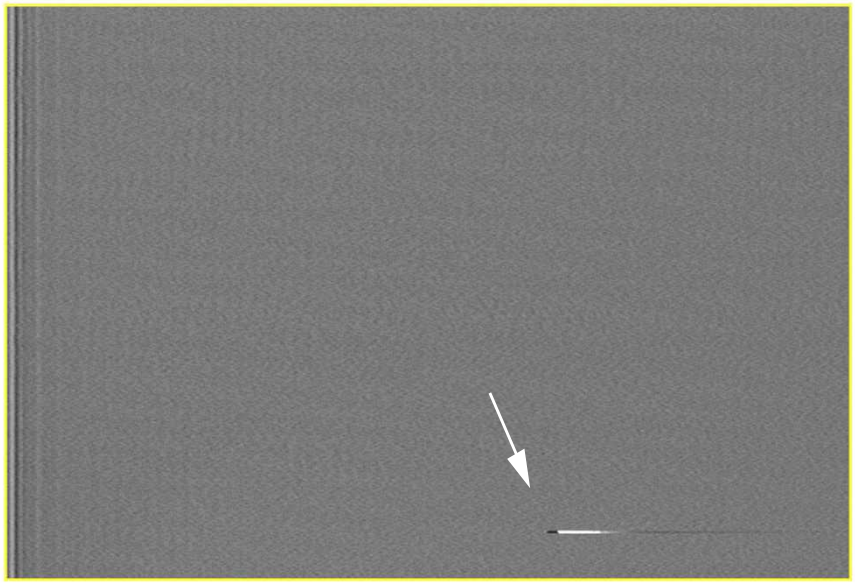
IR Transmission in Silicon



IR Transmission Through 625 μm of *p*-Doped Silicon



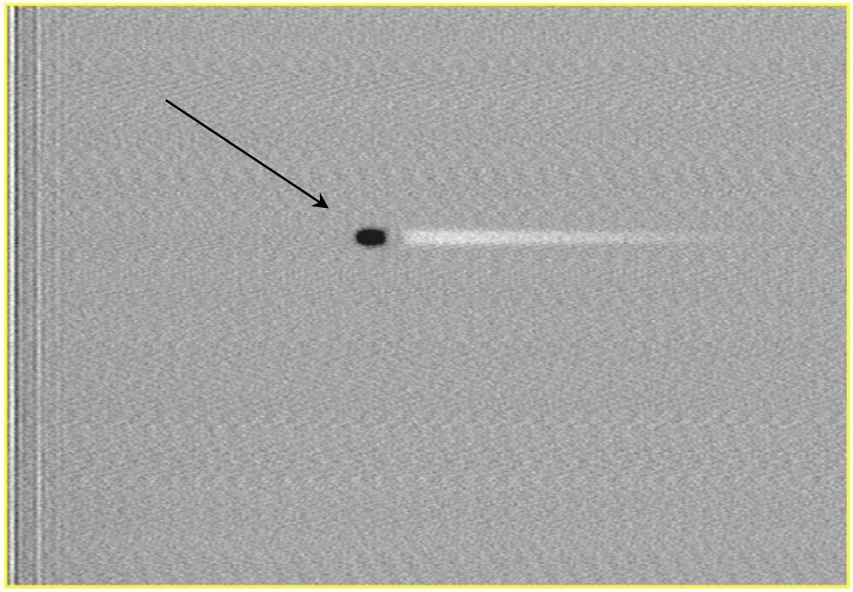
IR LIVA Backside Example: Open Metal to Silicon Contact



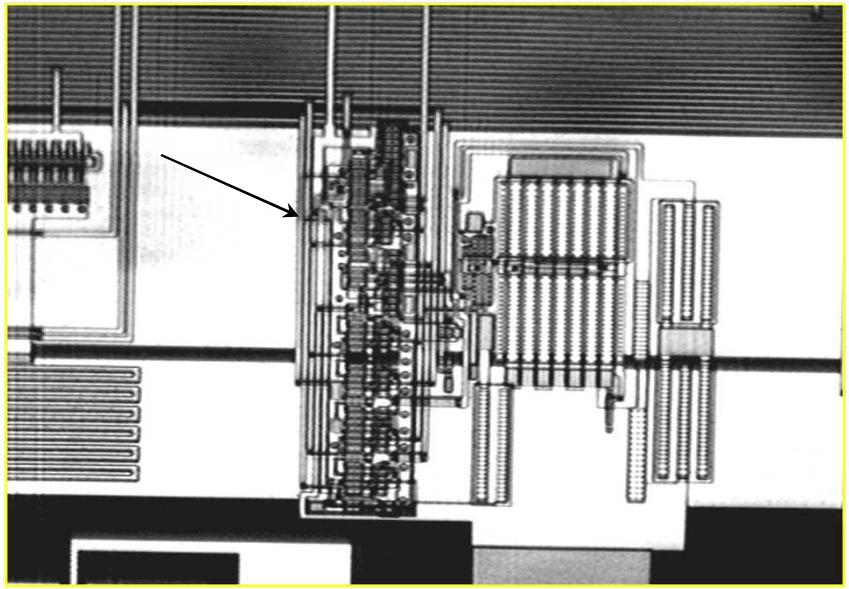
Backside IR LIVA of defect

Reflected IR image

IR LIVA Backside Example: Open Metal to Silicon Contact



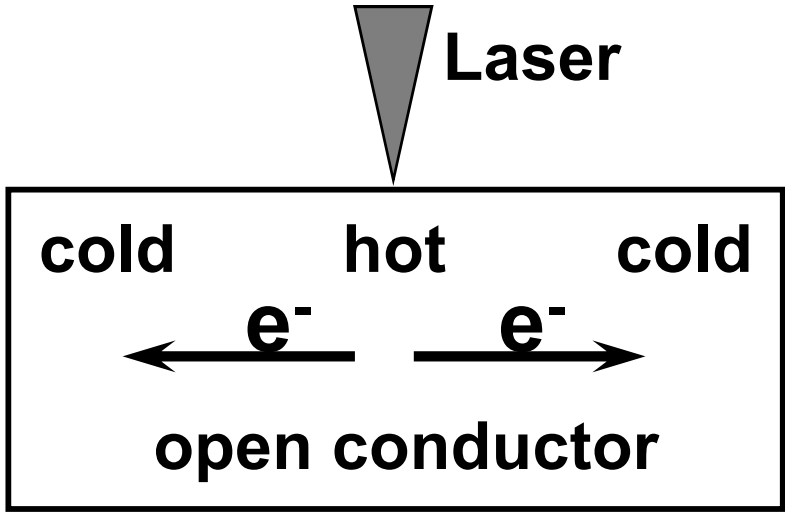
Backside IR LIVA image of defect



Reflected IR image

Seebeck Effect

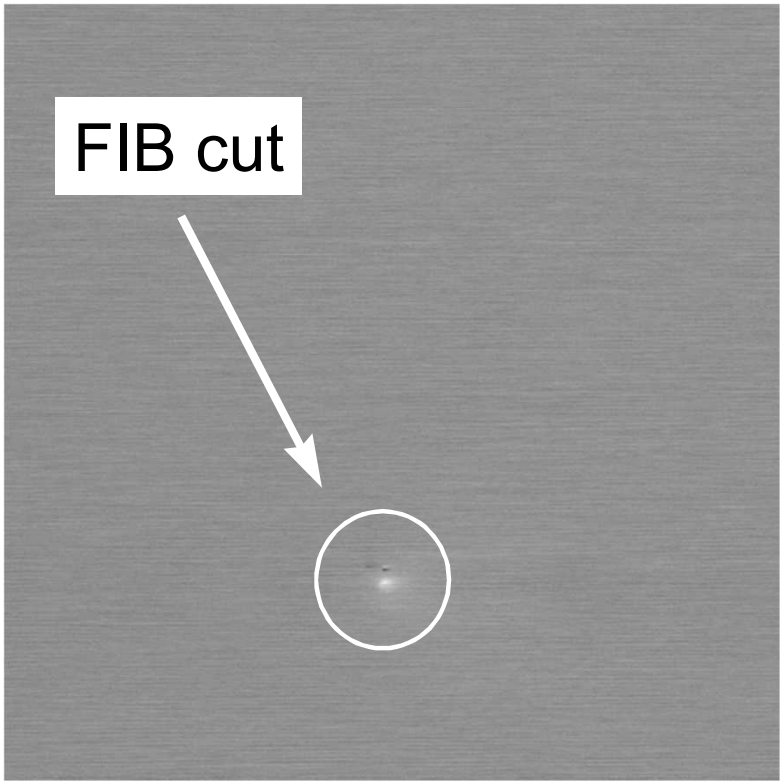
- Thermal Gradients Produce Voltage Gradients on Open Interconnections
  - typically μV/K for metals
- Localized Heating Using Focused Laser
  - already used to detect voids in conductors
  - changes voltage of open conductors
  - alters IC power demands

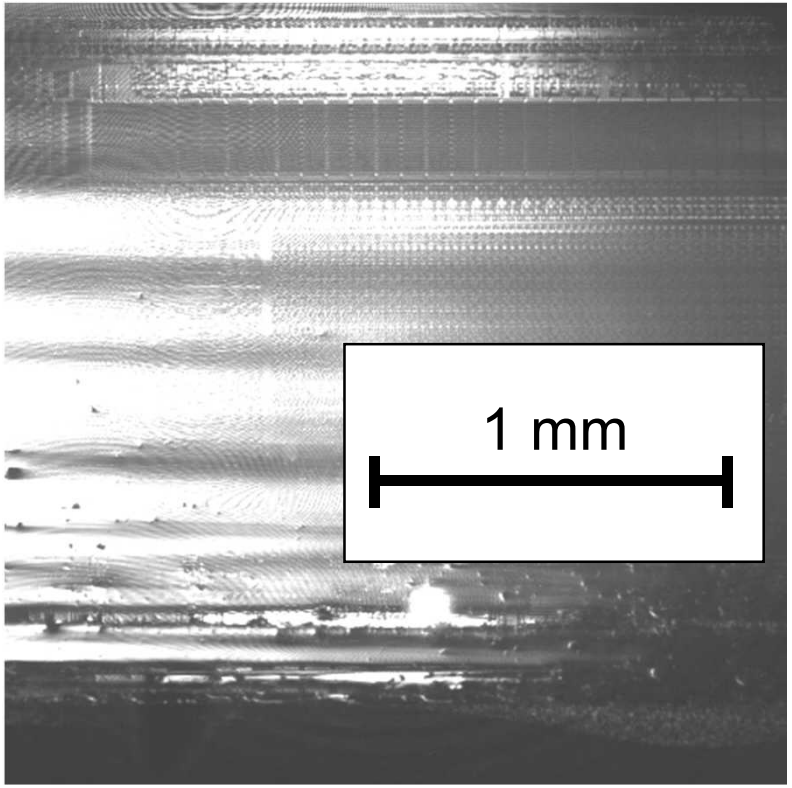


Localized Heating

- **1320 nm Laser**
  - 120 mW Nd:YAG laser
  - yields localized temperature variations of about 120 ^{o}C max
  - photon energy will not produce electron-hole pairs
    - avoids photocurrent effects
- **Reasonable Spatial Resolution**
  - about 1.3 μm

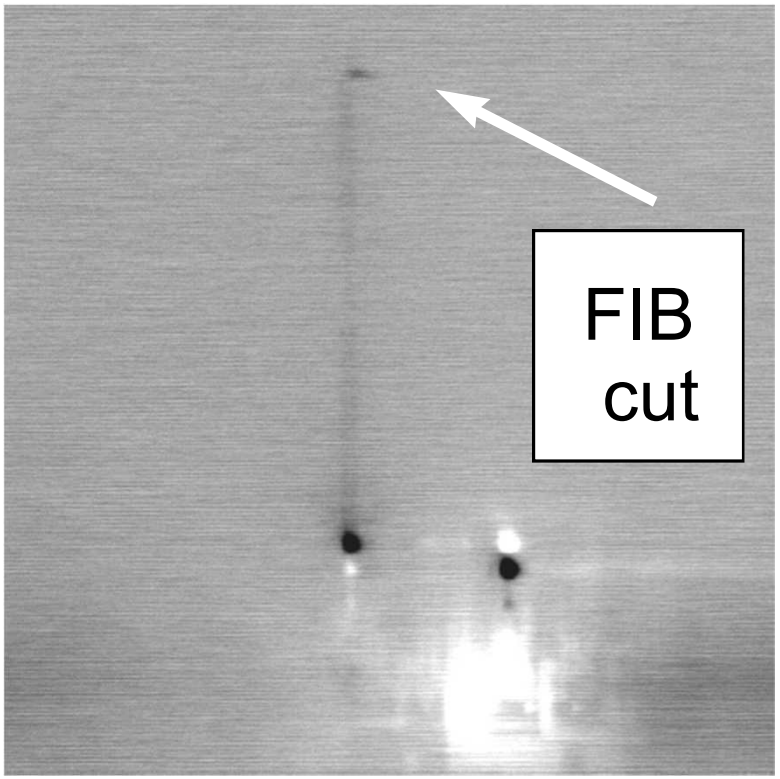
Backside SEI Example - 80C51

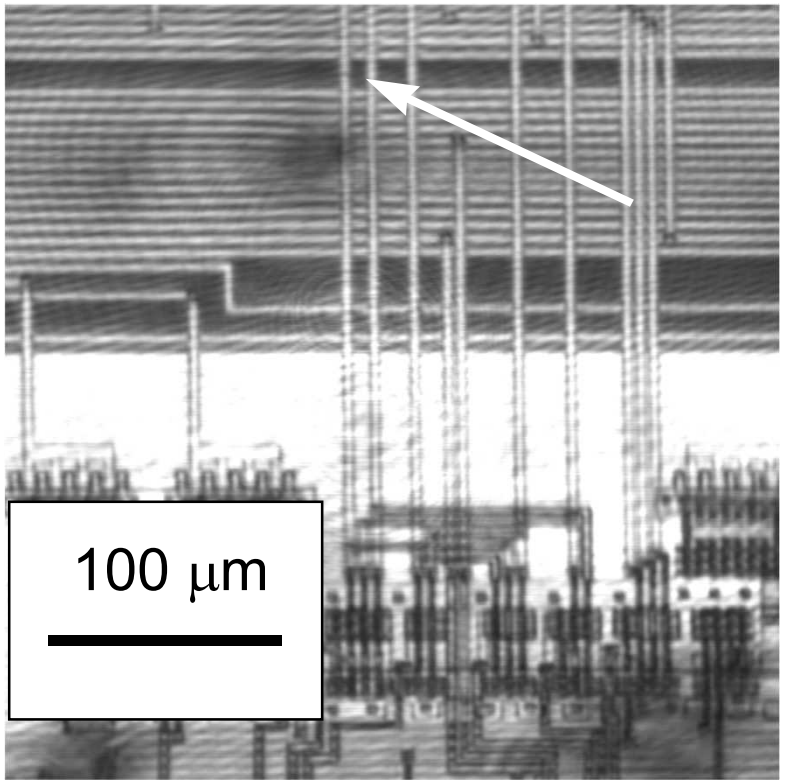




SEI Image (low mag) Reflected Image

Backside SEI Example - 80C51





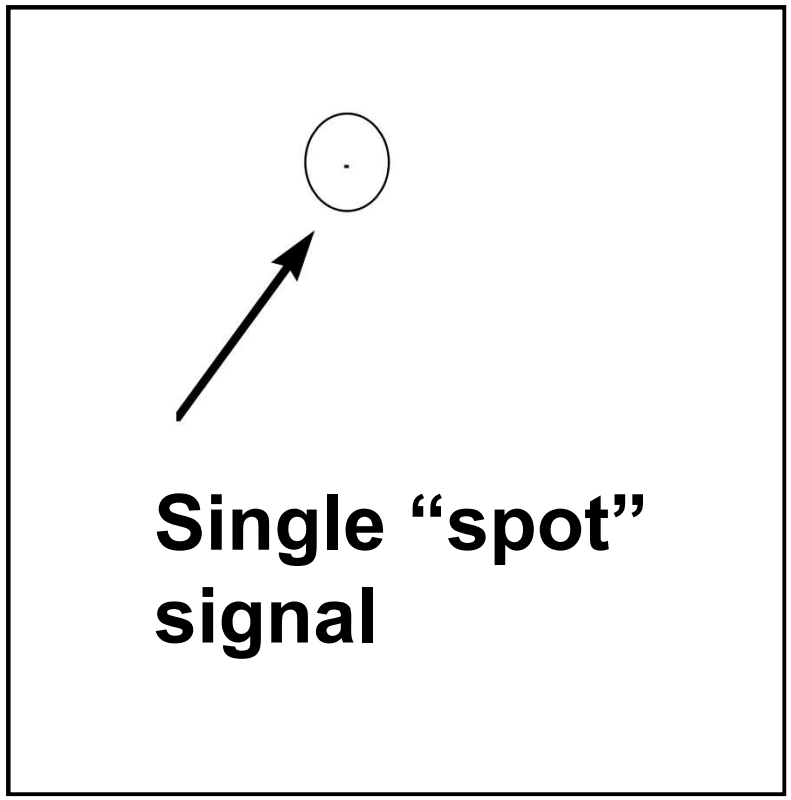
-metal-poly interconnect contrast

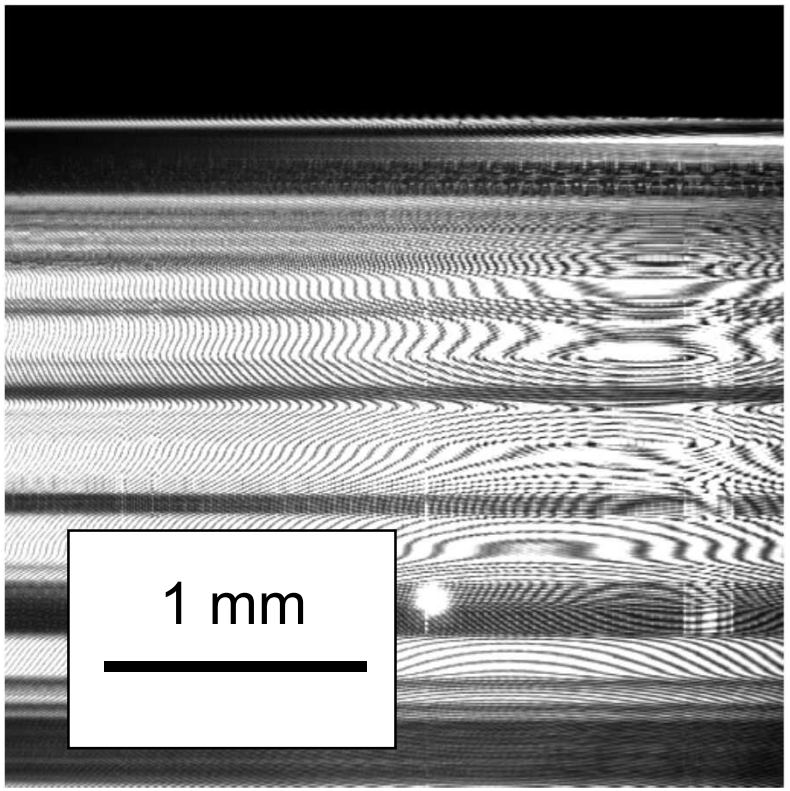
thermocouple or Schottky barrier effect

Thermally-Induced Voltage Alteration (TIVA)

- Local Heating Changes Resistance of Short
  - produces a change in IC power demand
- Effect Previously Demonstrated as OBIRCH (Optical Beam Induced Resistance Change)
- Increased Sensitivity Using Constant Current Biasing - TIVA

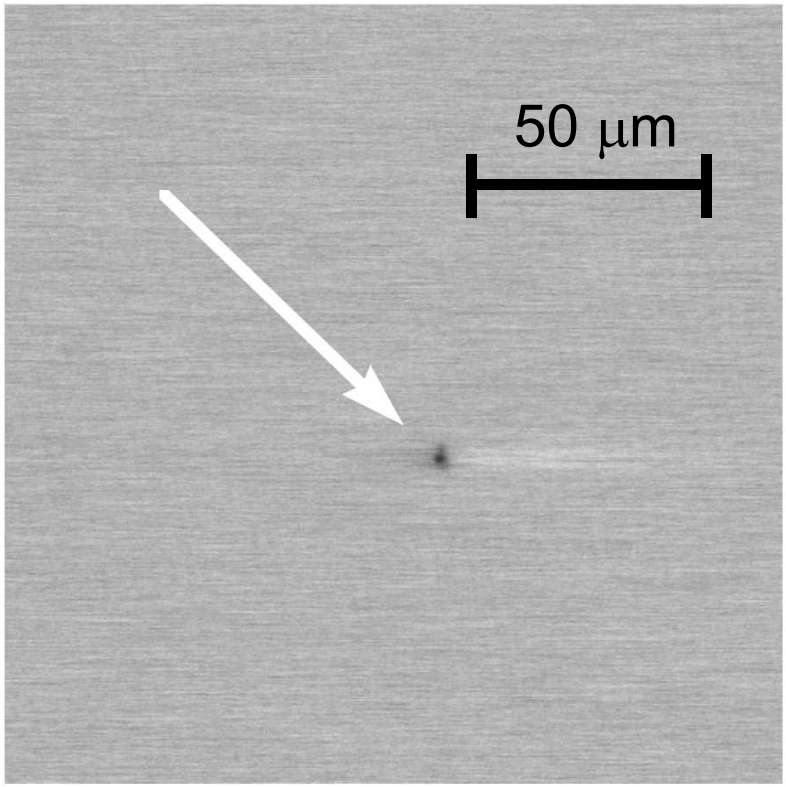
Backside TIVA Example - SRAM Particle Short

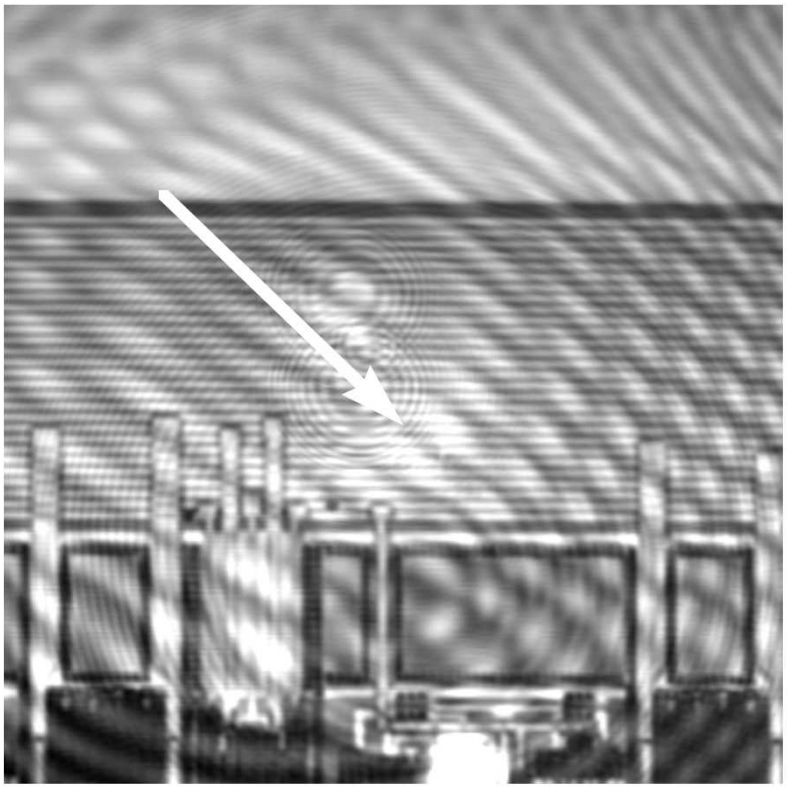




TIVA Image (low mag) Reflected Image

Backside TIVA Example - SRAM





-particle under metal, not visible

TIVA/SEI Summary

- Demonstrated New Thermal Probing Technique for Front and Backside FA
  - SEI for open interconnections
  - TIVA for IC shorts
- Excellent Spatial and Signal Sensitivity for Failure Localization
  - thermal conduction through metal
- Easily Implemented on Existing SOMs

Conclusions

- Continued growth in use of flip-chip packaging and multi-level metallization processes is driving development of backside analysis techniques
- Backside preparation techniques and their effects on device analysis reviewed
- Primary tools rely on light
  - Light emitted by the circuit
  - Changes in circuit operation because of the presence of light beam
  - Changes in optical properties of materials caused by electrical operation of the circuit
- Non-optical tools are destructive and require extensive preparation, but are effective