

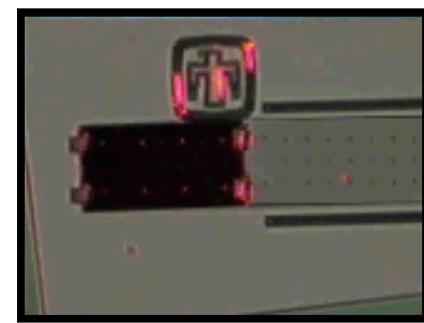
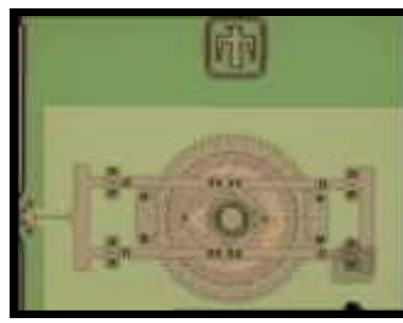
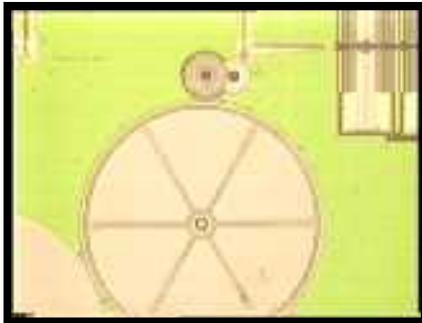
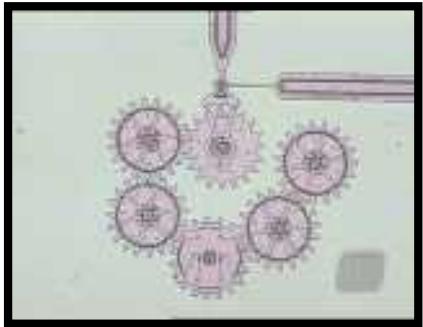


# Etch-Induced Defects Govern the Strength of Microfabricated Silicon

SAND2008-0570C

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University of Colorado at Boulder



Source: [mems.sandia.gov](http://mems.sandia.gov)

32nd International Conference & Exposition on Advanced Ceramics and Composites  
January 29<sup>th</sup>, 2008

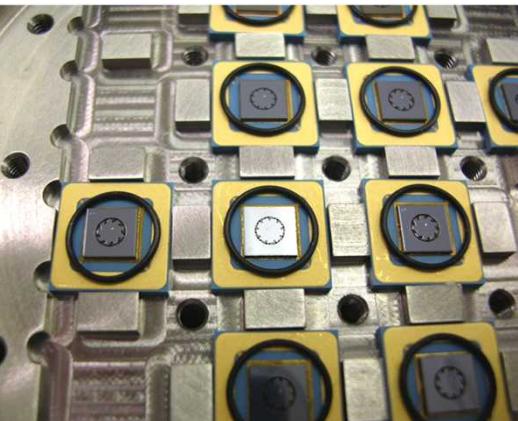
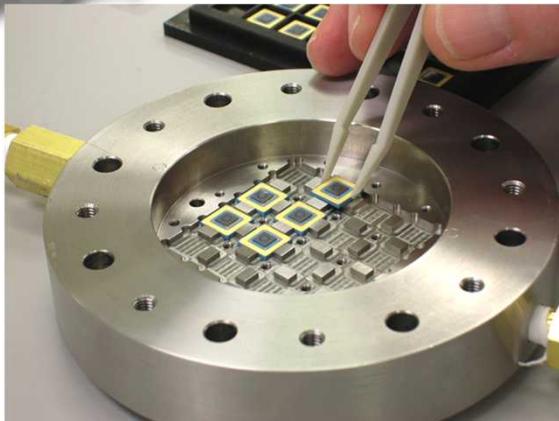


Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

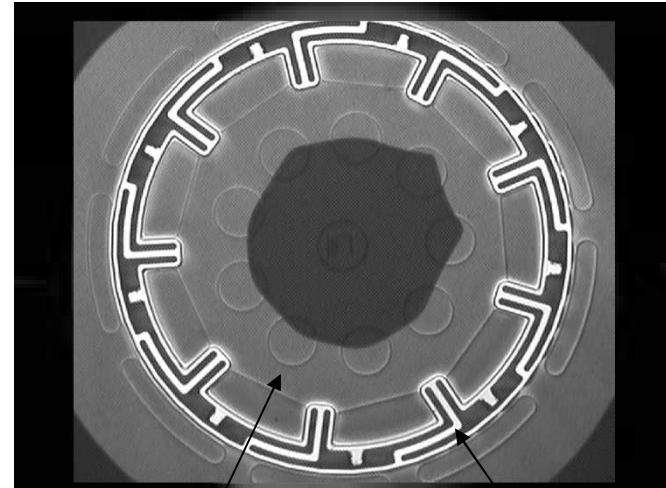


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# Motivation: A Silicon-On-Insulator (SOI) Accelerometer Switch

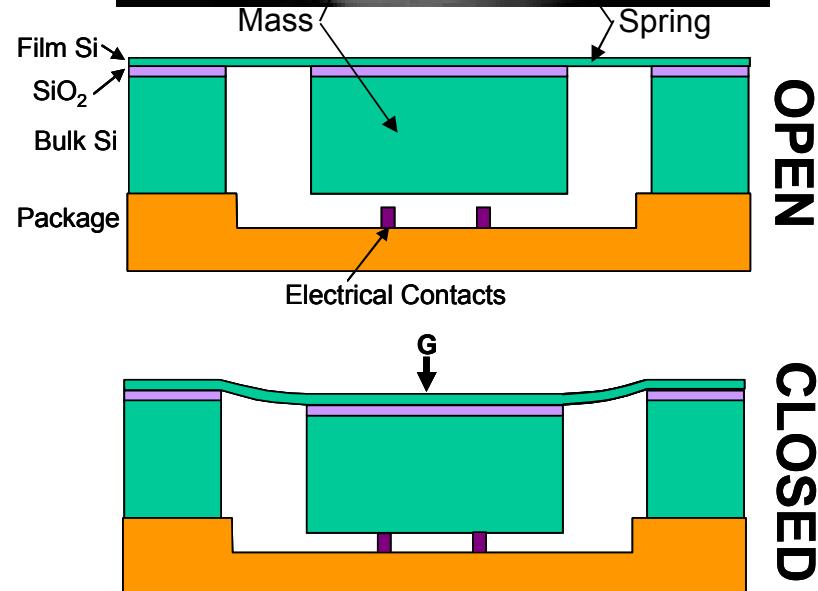


D. Tanner

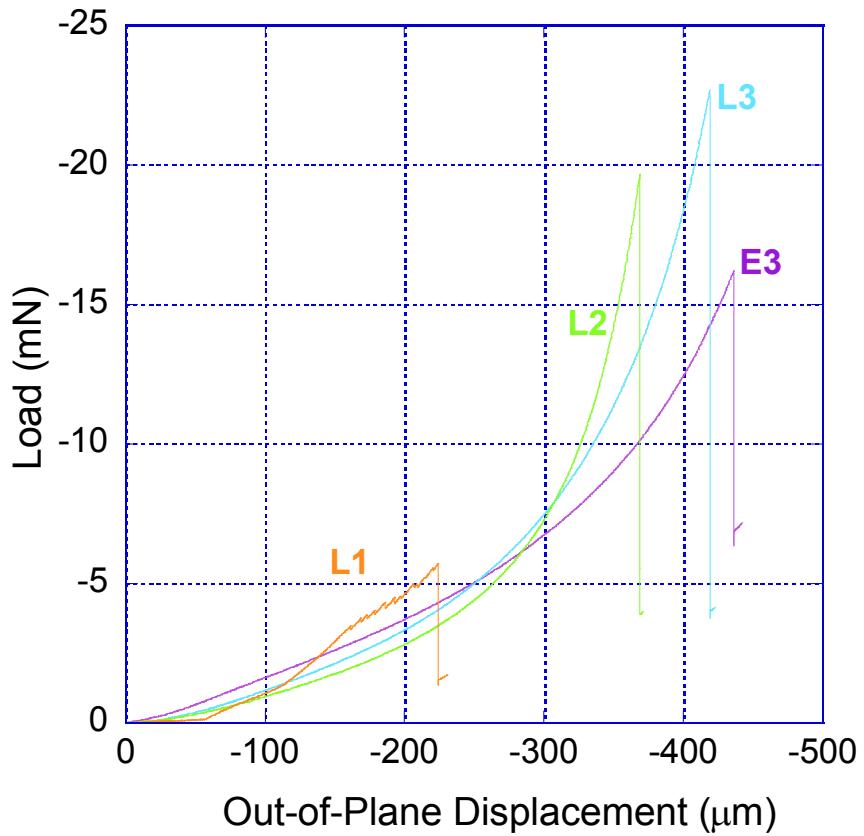
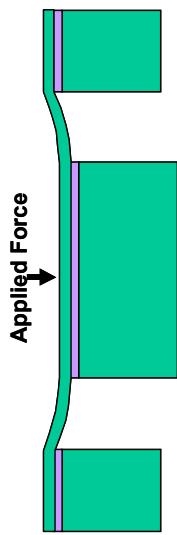


## DESIGN REQUIREMENTS:

- Acceleration level requirements: activate at a specific G-band,  $G < 25$
- 3.3 V on switch, nominal 3 mA
- Stable, known contact resistance
- Lifetime of 30 years
- **Reliability of 0.95**
- Temperature requirements
  - (MIL SPEC -55C to 125)
- **Random Vibration, 20 to 2000 Hz**
- Flight Loading
- Shock requirements



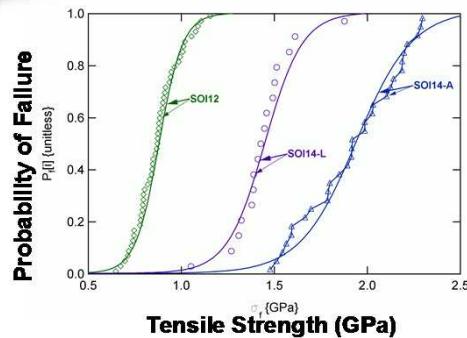
# Performance of Accelerometer Devices



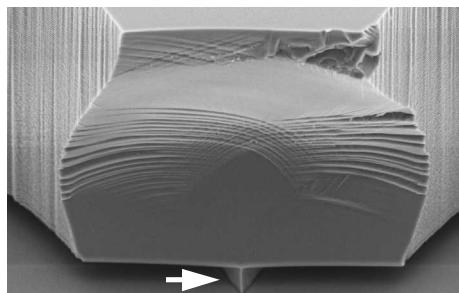
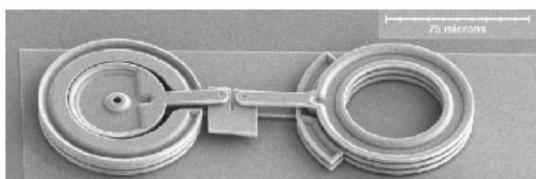
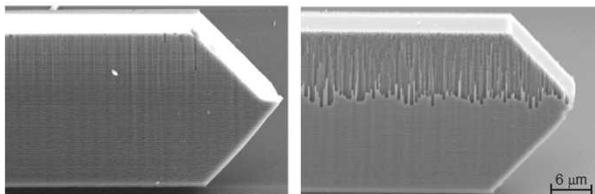
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# The Brittle Nature of Silicon Makes Its Structural Reliability Challenging



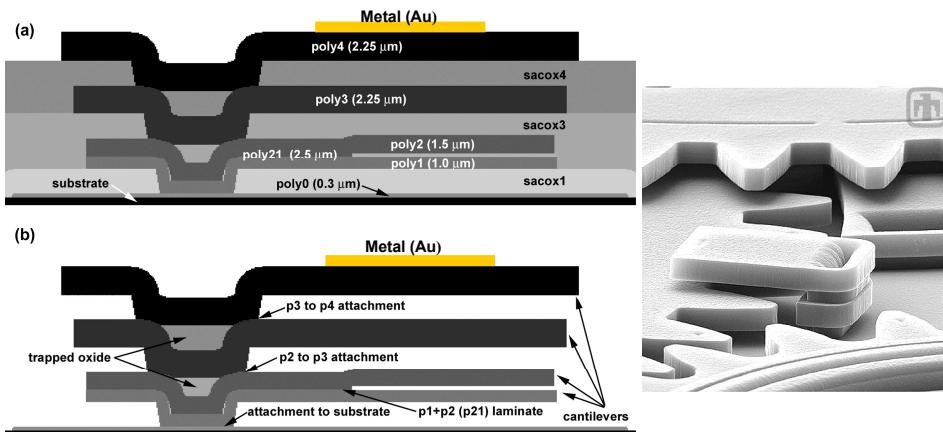
1. **Statistically Unreliable.** While Silicon has a “typical” or characteristic strength of  $>>1$  GPa, there is a lot of scatter in the distribution of strengths.
2. **Process Sensitive.** Strength is strongly dependent on process conditions.
3. **Low Toughness.** Fracture toughness  $\sim 1.0$  MPa $\sqrt{m}$  is like window-pane glass! Very small flaws cause fracture.
4. **Sensitive to Flaws and Stress-Concentrations.** No ability to accommodate unexpected flaws or stress-concentrations.



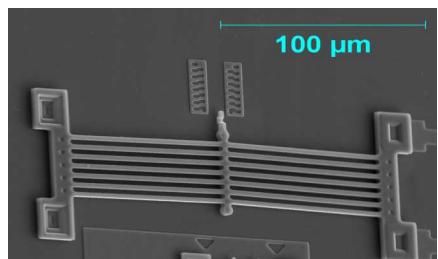
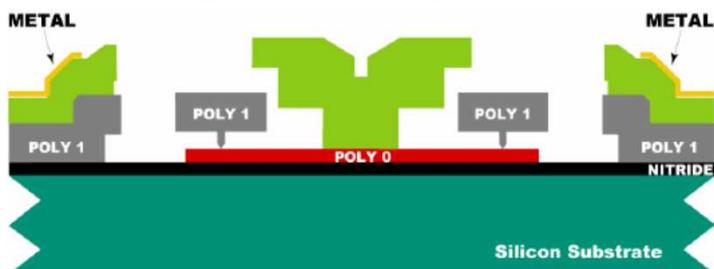
# Common Silicon Microfab Technologies

## Surface Micromachining (SMM)

### A Sandia's SUMMiT V Polysilicon:

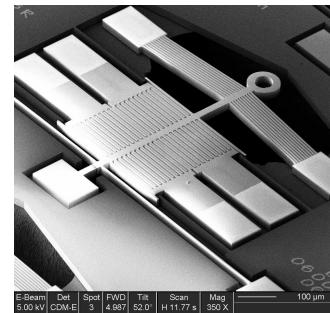
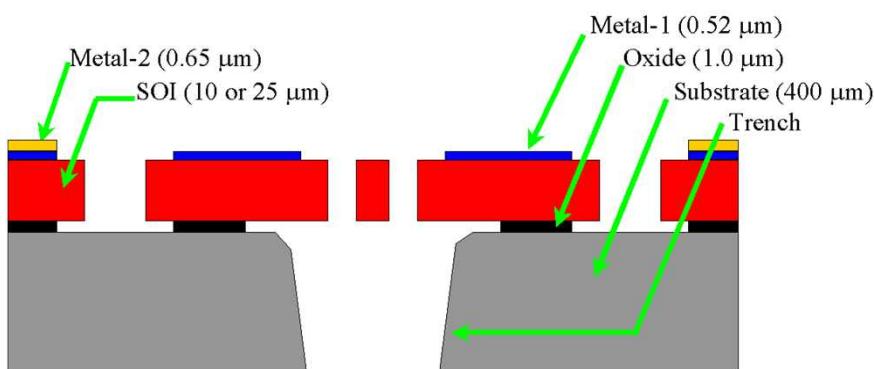


### B MEMSCAP's polyMUMPs polysilicon:



## Bulk Micromachining (BMM)

### C MEMSCAP's SOIMUMPs silicon-on-insulator:

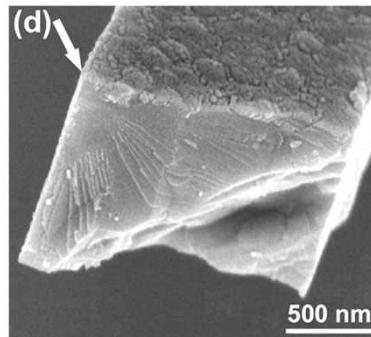


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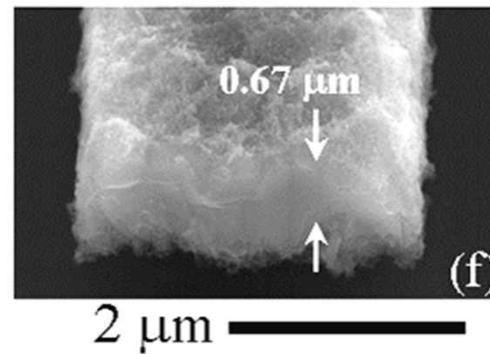
# Outline:

## *Etch-induced Nanoscale flaws affect the strength of all Si microfab technologies*

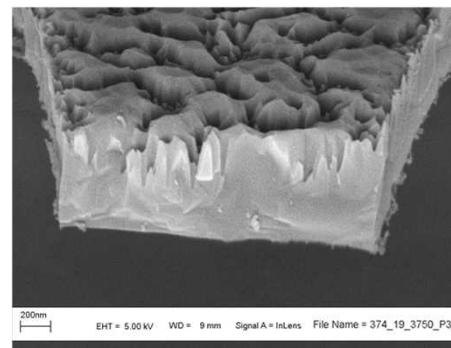
1. As-fabricated surface roughness (etch-induced nanoscale flaws)



2. Galvanic corrosion as a pathway to degraded properties.



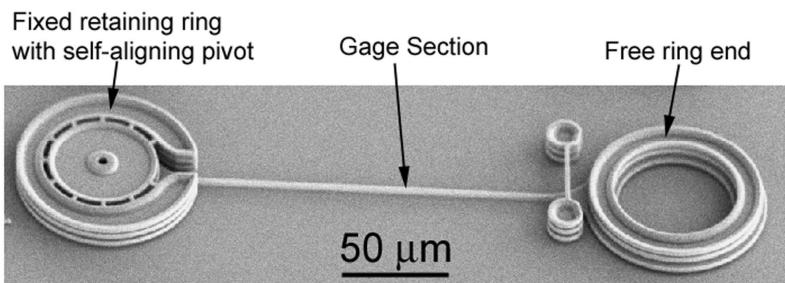
3. Best-case and worst-case scenarios in silicon fabrication processes



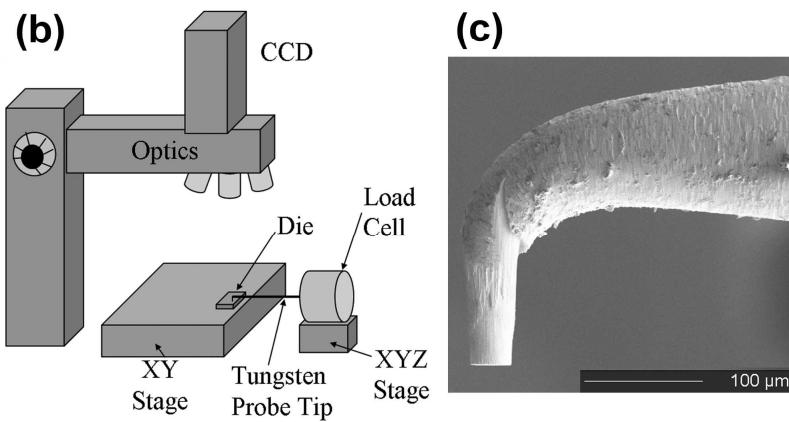
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# Fundamental Strength Measurements On Microfabricated Silicon

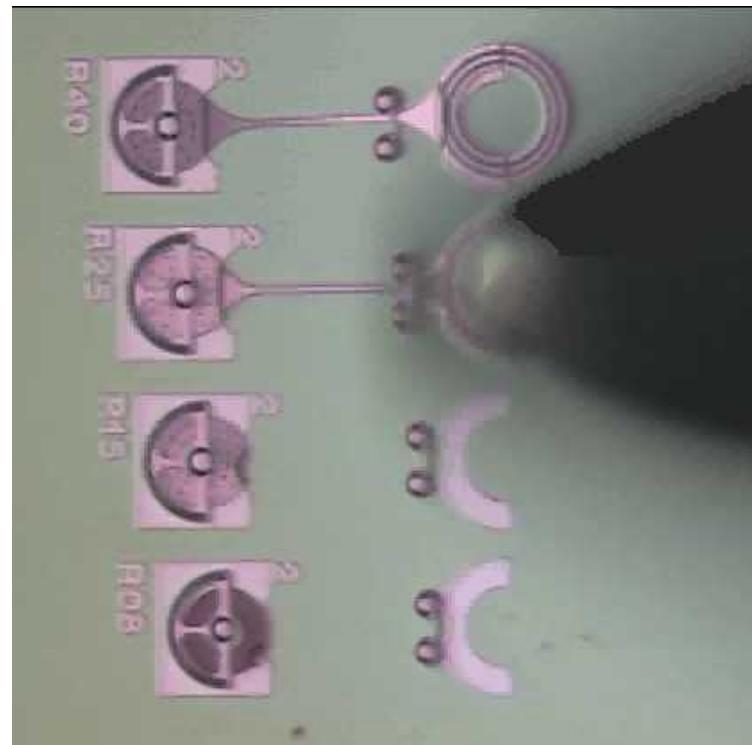
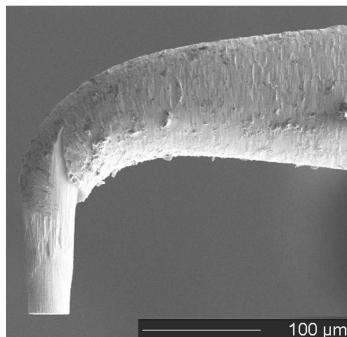
(a)



(b)

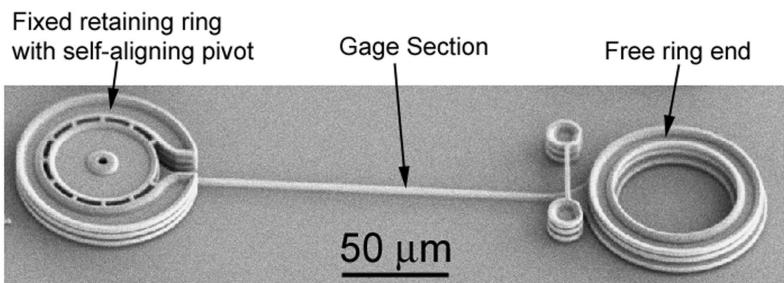


(c)

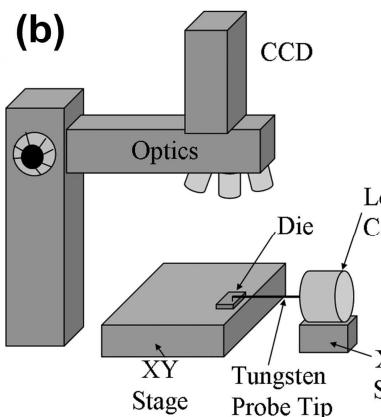


# Fundamental Strength Measurements On Microfabricated Silicon

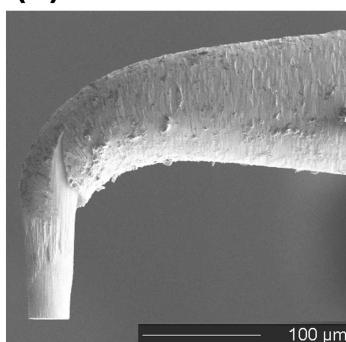
(a)



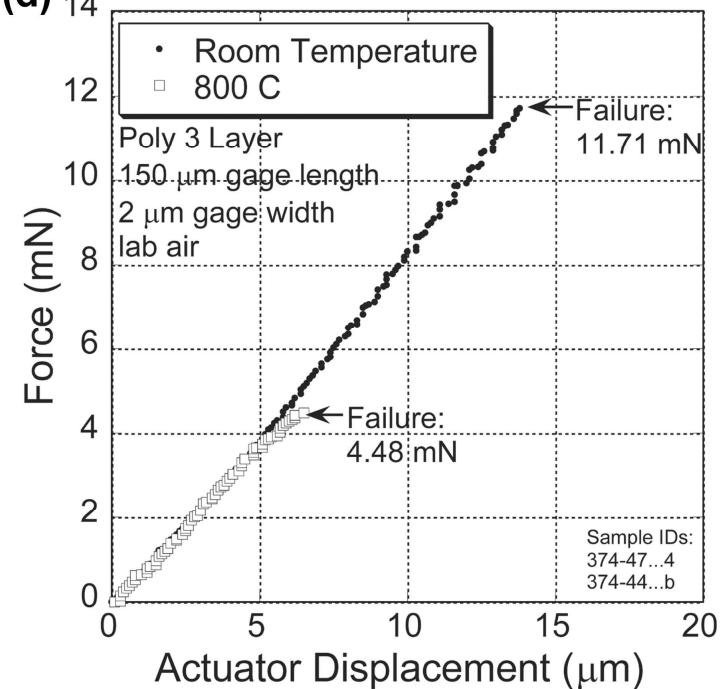
(b)



(c)

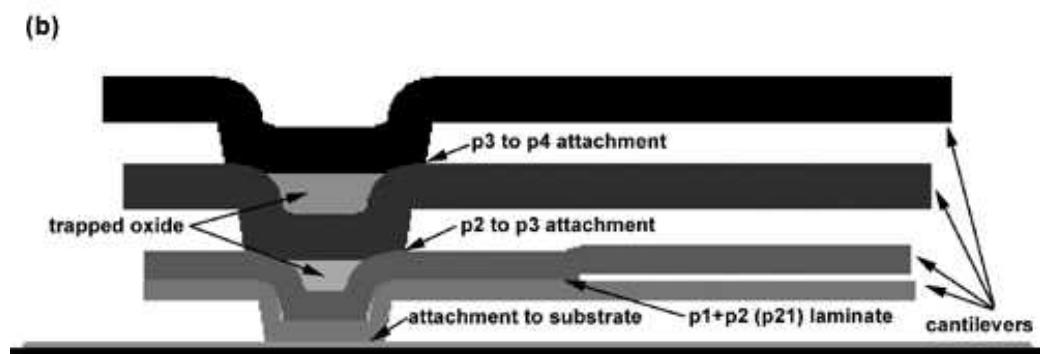
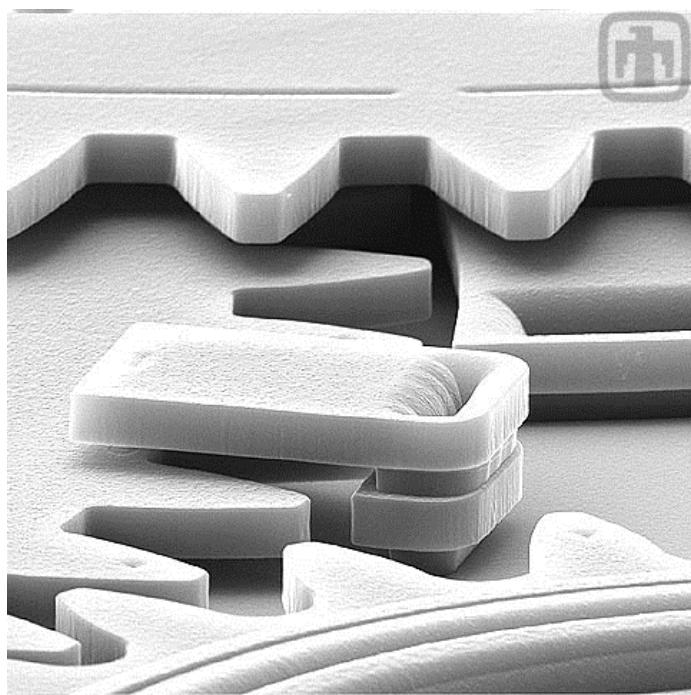
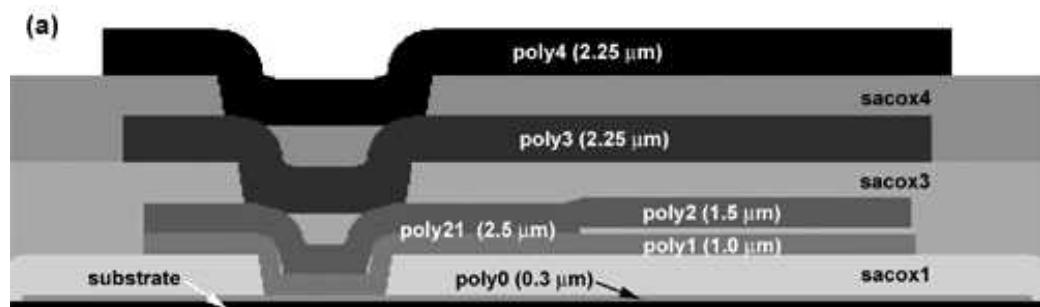
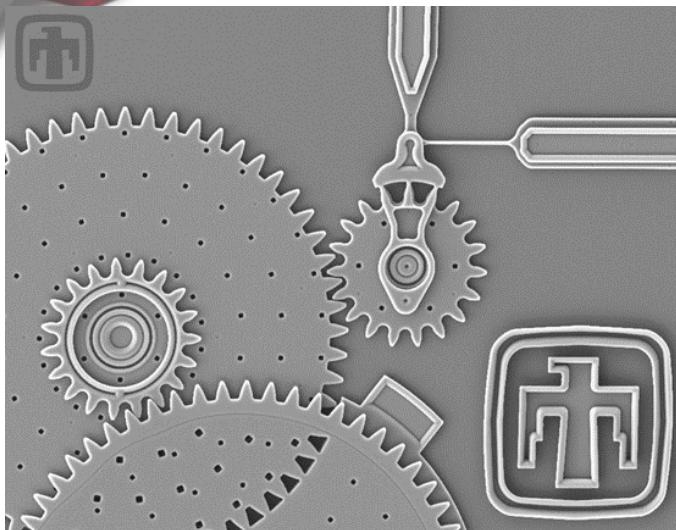


(d)





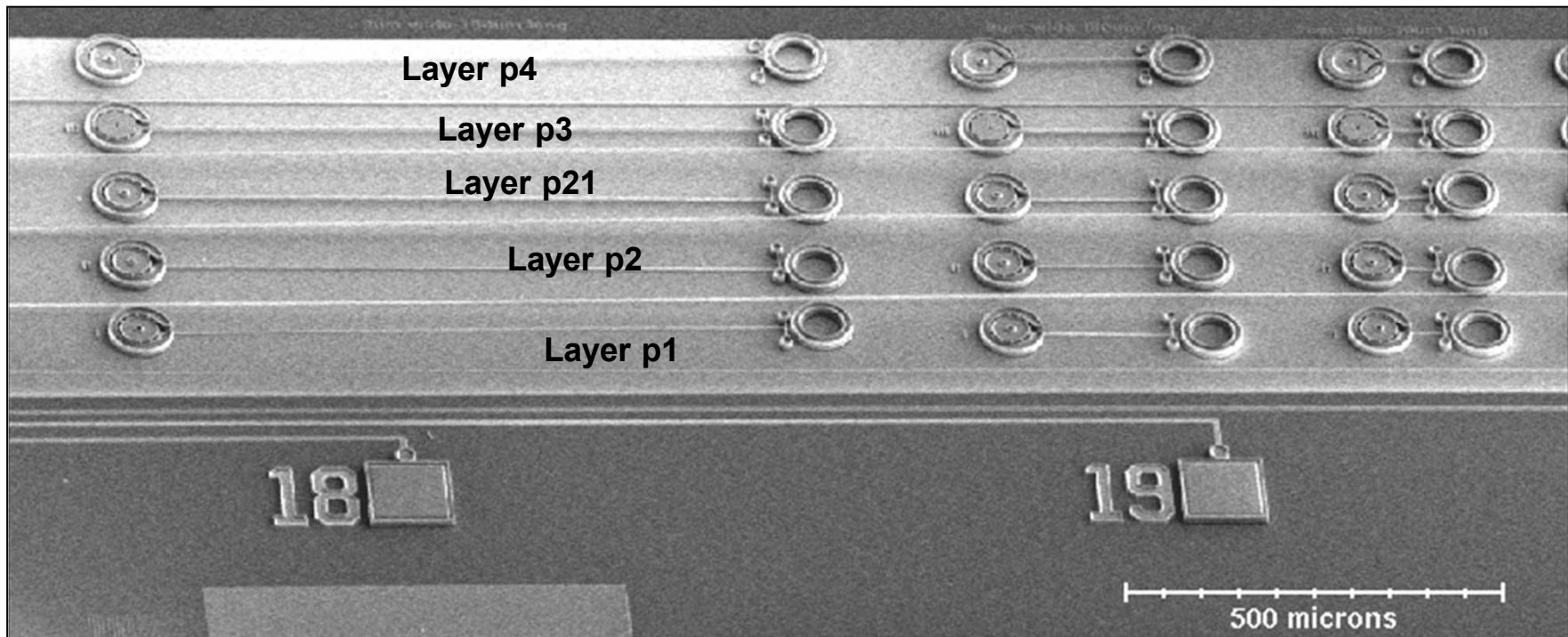
# Sandia's SUMMiT Multilayer Polycrystalline Silicon MEMS Fabrication Technology



Sandia National Laboratories



# *Microtensile bars made from Each layer of SUMMiT V polysilicon*



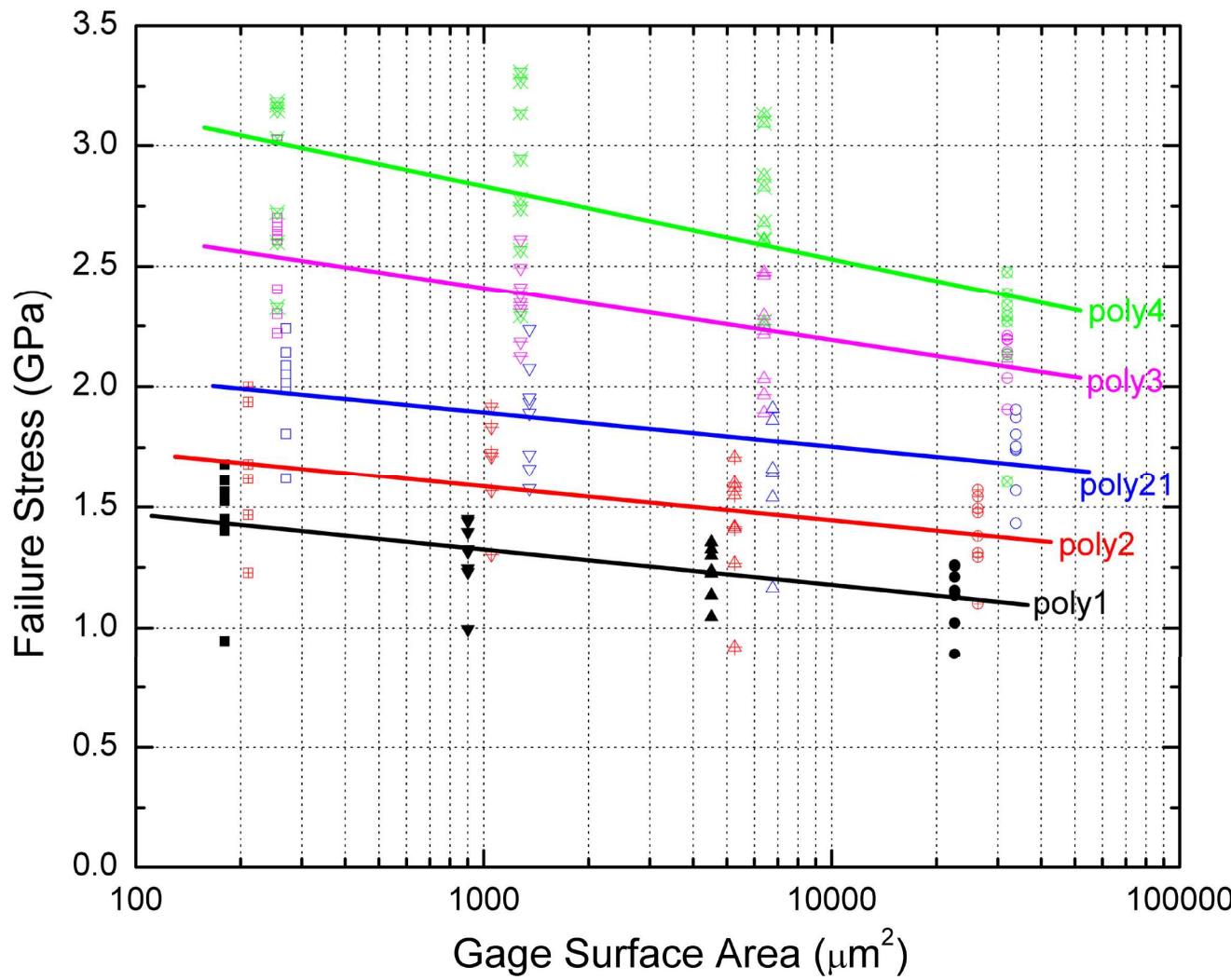
*SEM image of test structures*

**Tensile bars are 2  $\mu\text{m}$  wide with gage lengths  
of 30, 150, 750, or 3750 microns.**



**Sandia National Laboratories**

# Strength varies as a function of specimen size (Weibull size effect)



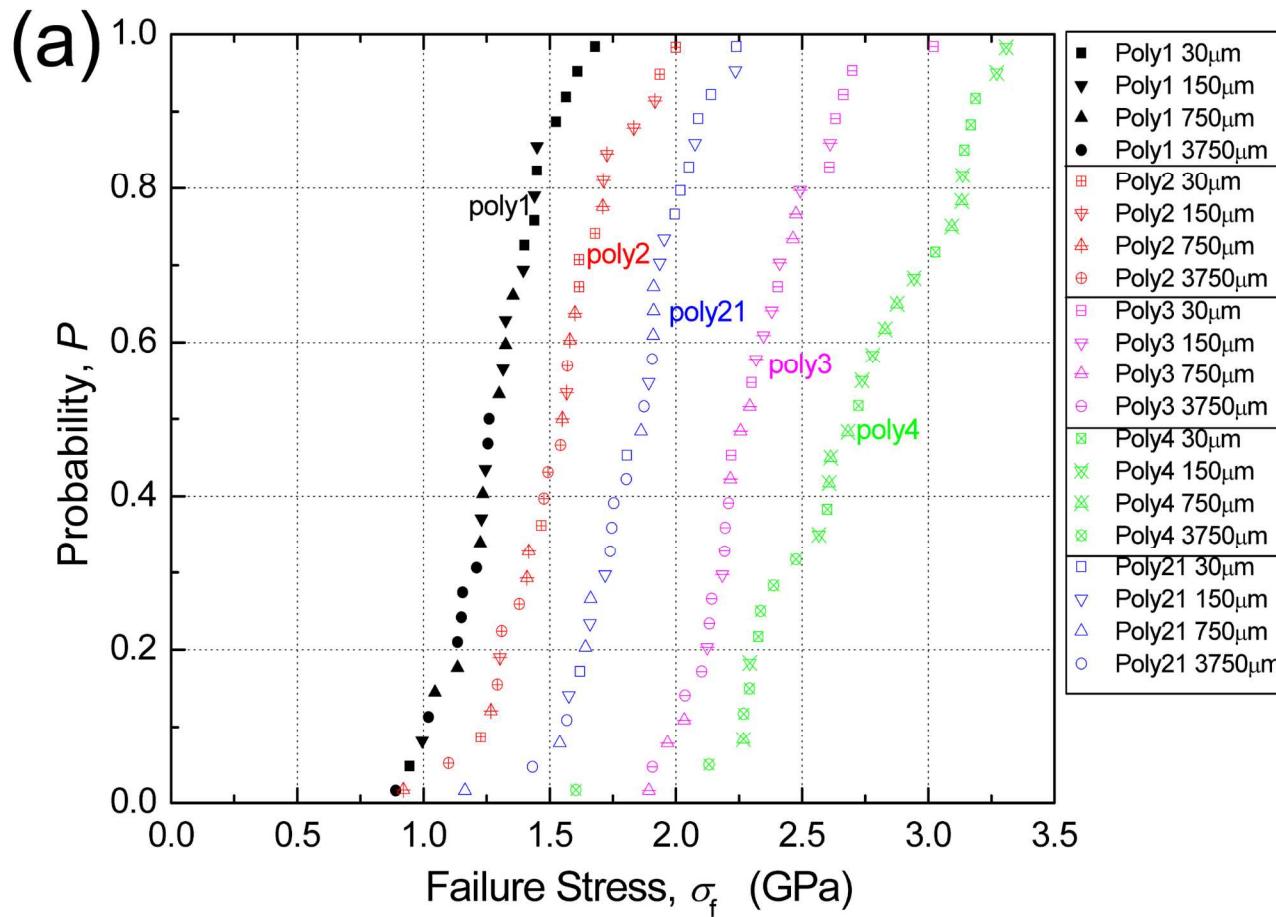
$$\left( \frac{\sigma_1}{\sigma_2} \right) = \left( \frac{A_2}{A_1} \right)^{1/m}$$

B.L. Boyce et al., J. MEMS 16:179-90, 2007



Sandia National Laboratories

# Each layer of SUMMiT V polysilicon has a different strength distribution

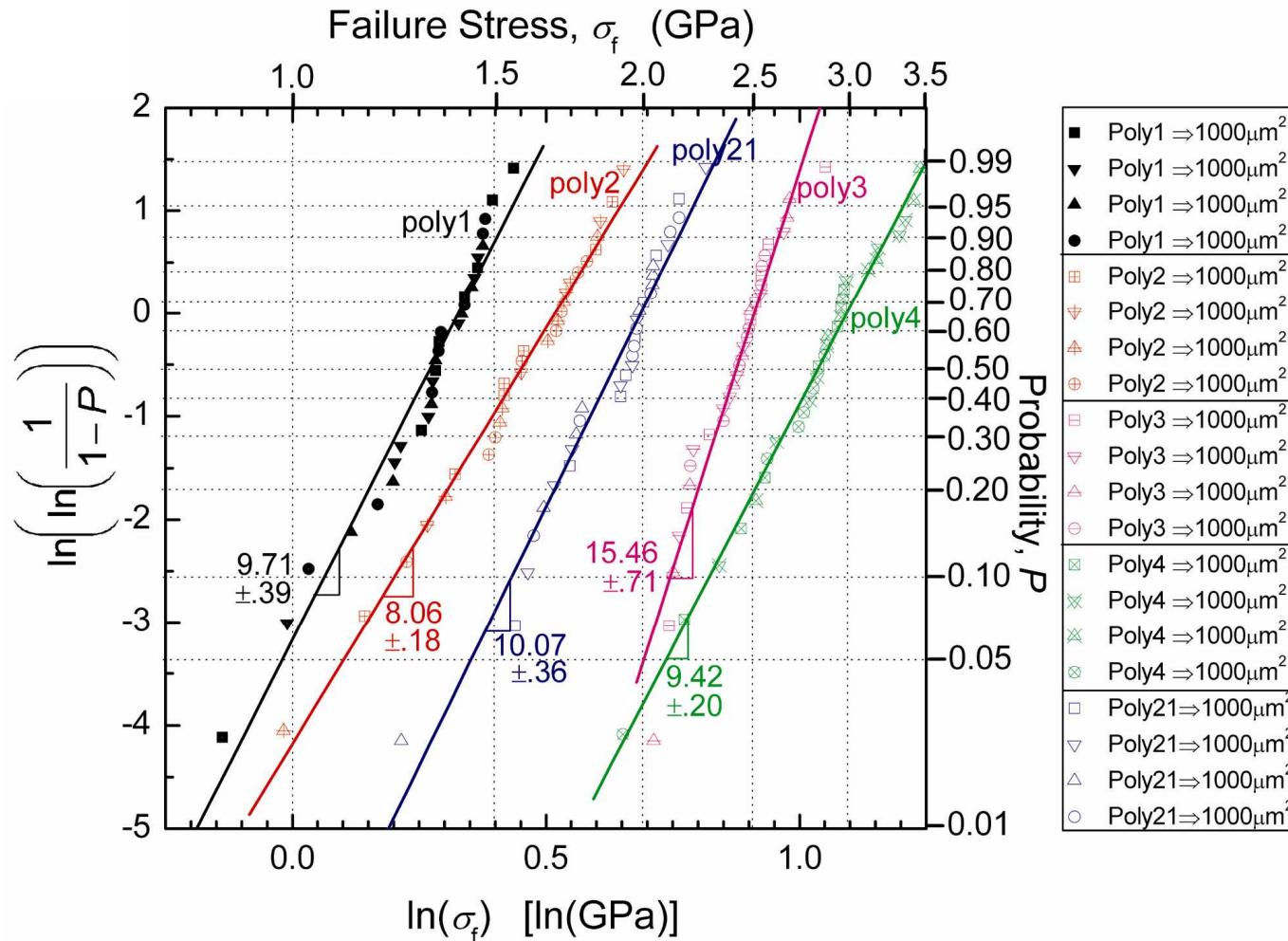


Sandia's SUMMIT V MEMS process utilizes a stack of 5 layers of polysilicon. Each layer has a different strength.



Sandia National Laboratories

# Each layer of SUMMiT V polysilicon has a different strength distribution



$$P = 1 - \exp\left[-\left(\frac{\sigma}{\sigma_\theta}\right)^m\right]$$

$$\ln\left(\ln\left(\frac{1}{1-P}\right)\right) = m \ln \sigma - m \ln \sigma_\theta$$

B.L. Boyce et al., J. MEMS 16:179-90, 2007



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# **Possible Causes For Layer-Dependent Strength Differences**

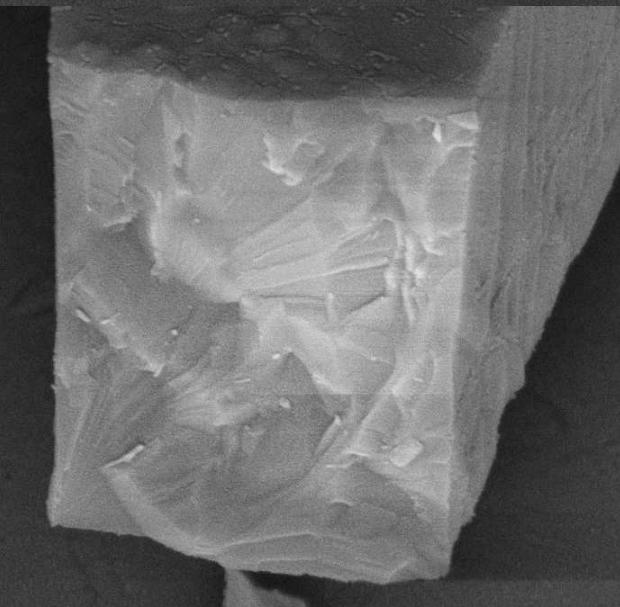
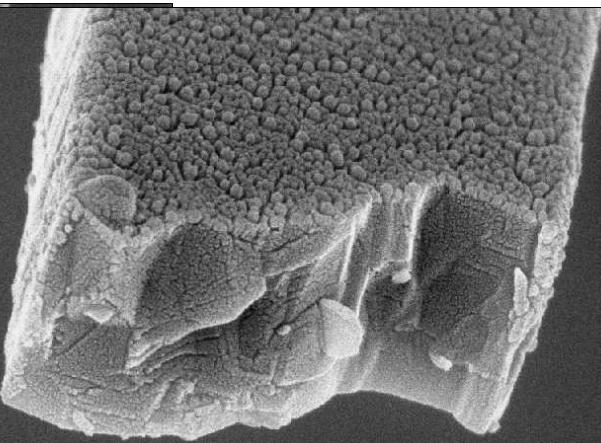
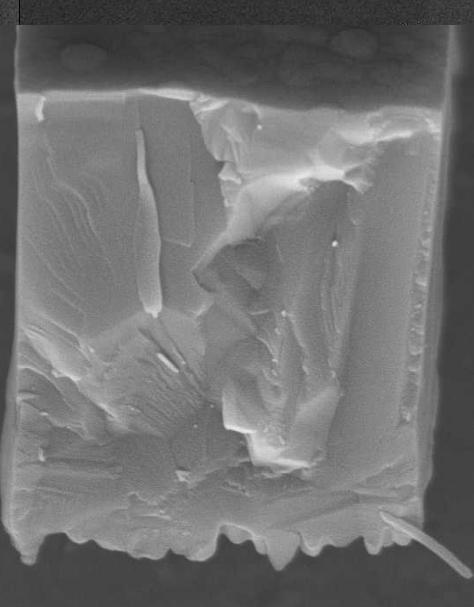
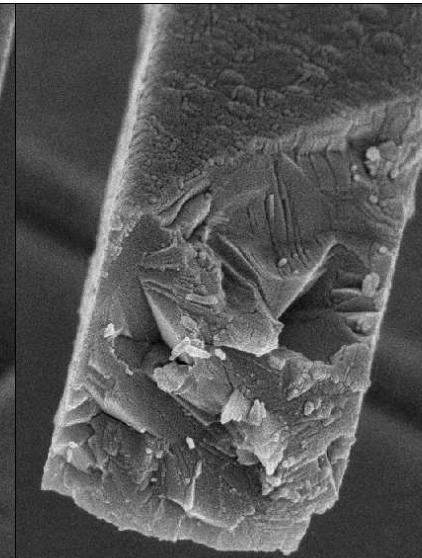
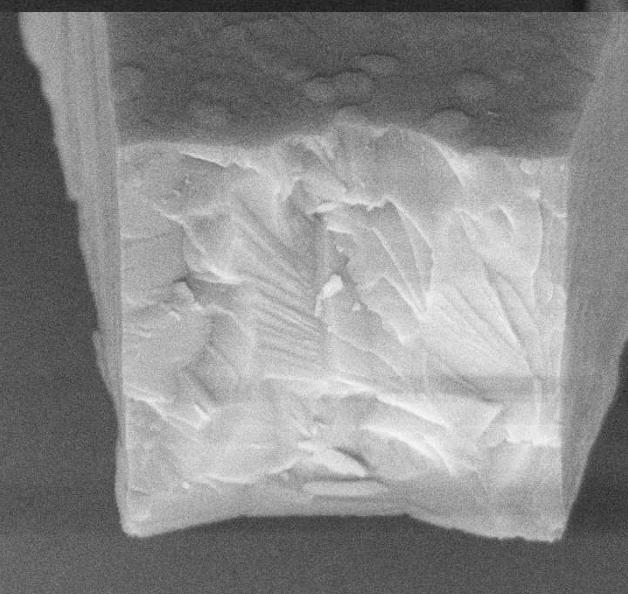
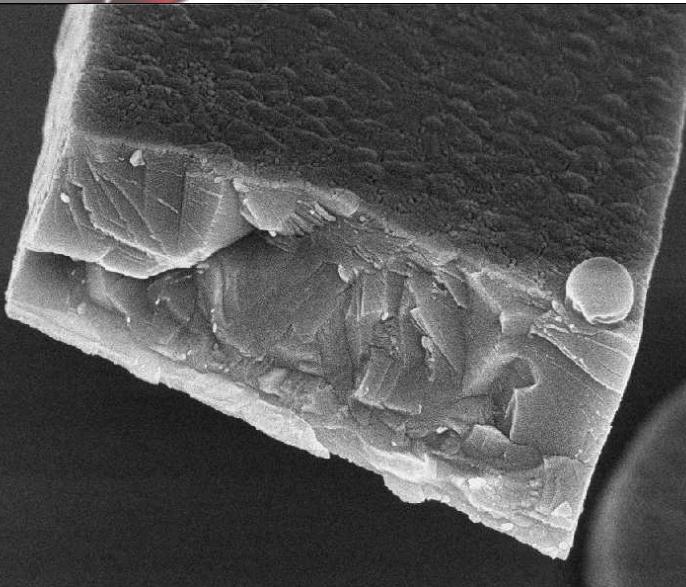
## **What causes poly4 to be twice as strong as poly1?**

- 1. Surface topography**
- 2. Inhomogeneous microstructural stresses at triple junctions**
  - polycrystal elasticity simulations suggests that the differences in microstructure alters the strength by <10%.
- 3. Doping chemistry**
  - all layers are doped at the same level and in the same way.
- 4. Systematic differences in beam dimensions**
  - there is some systematic bias from layer to layer, but the trend is small (<10%) and does not go in the right direction.
- 5. Residual Stresses**
  - residual stresses are ~10 MPa, but would need to be as large as ~1.4 GPa to explain the layer effect.





# Where's The Failure Origin?



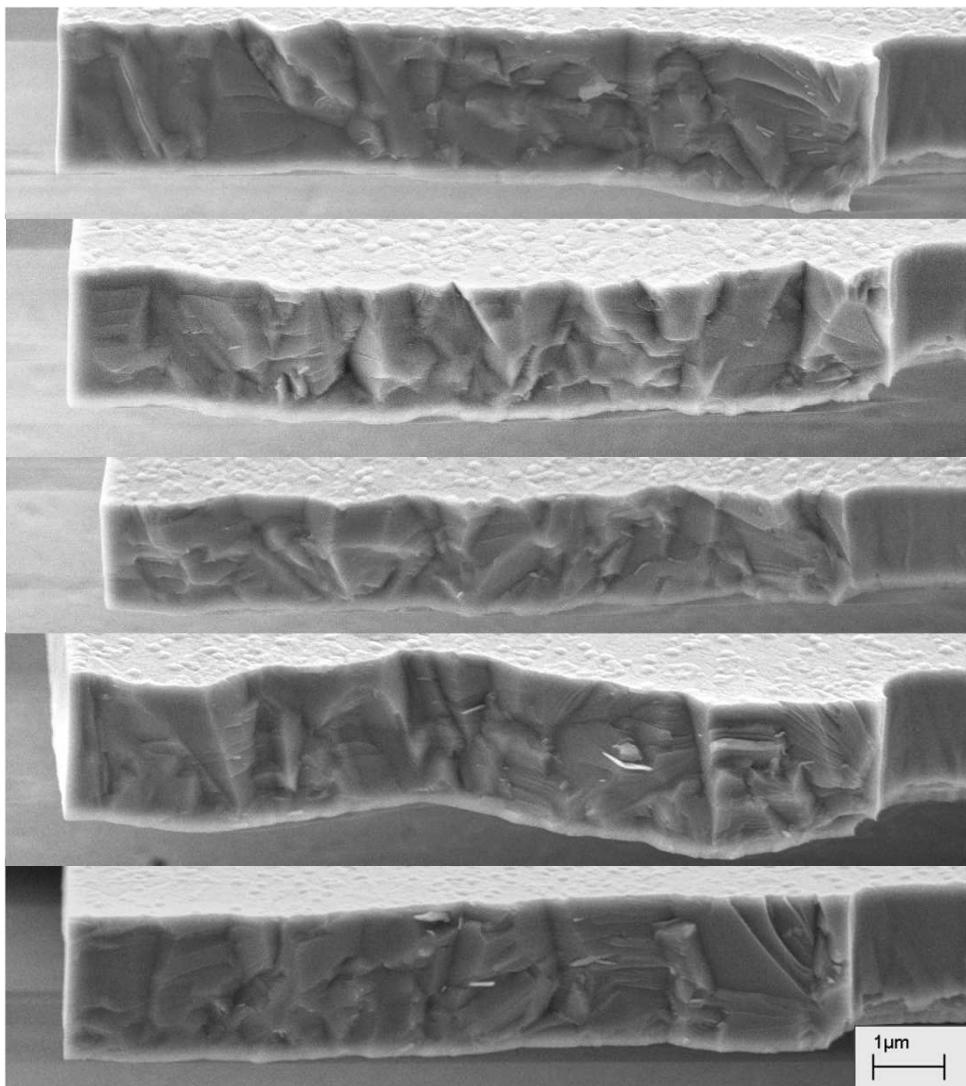
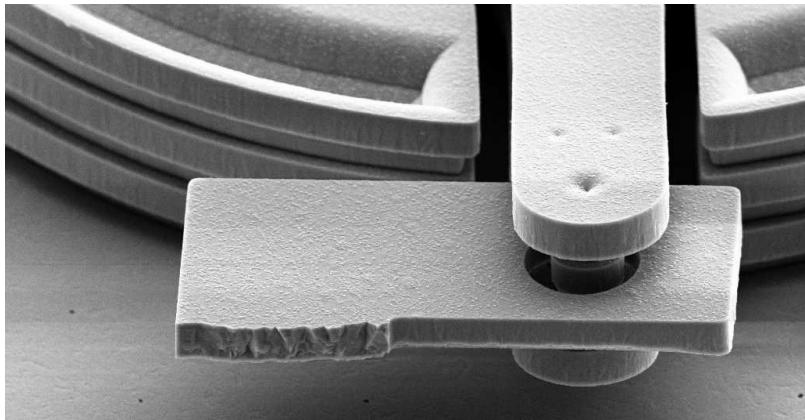
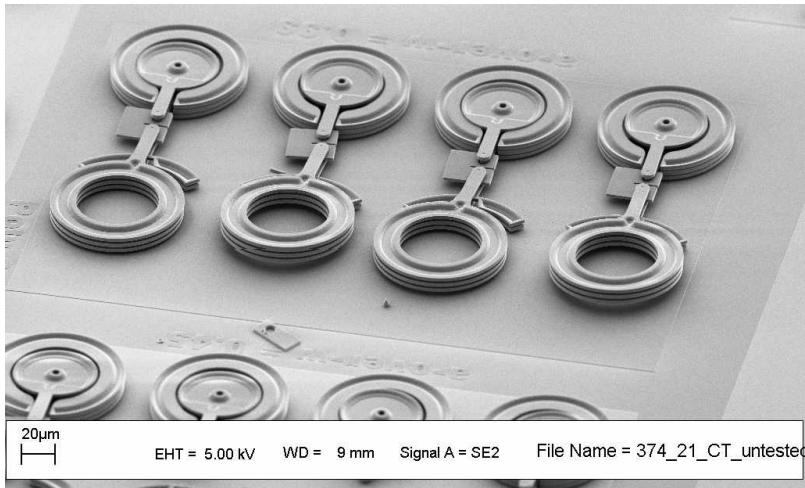
200nm  


EHT = 5.00 kV   WD = 9 mm   Signal A = InLens   File Name = 'EHT = 5.00 kV   WD = 7 mm   Signal A = InLens   File Name = 3'

EHT = 5.00 kV   WD = 9 mm   Signal A = InLens   File Name = 3

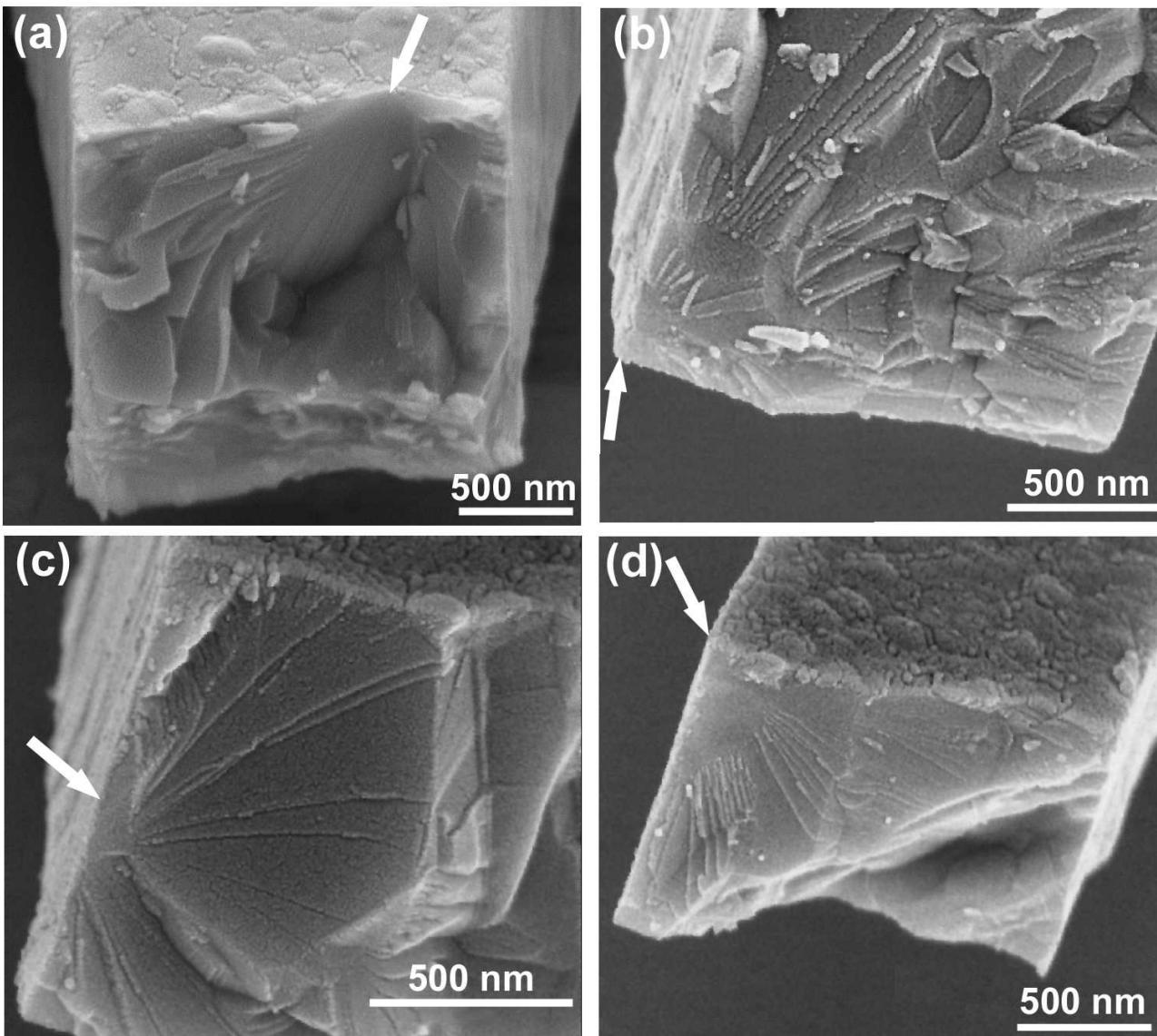


# Fractography: C(T) Specimens



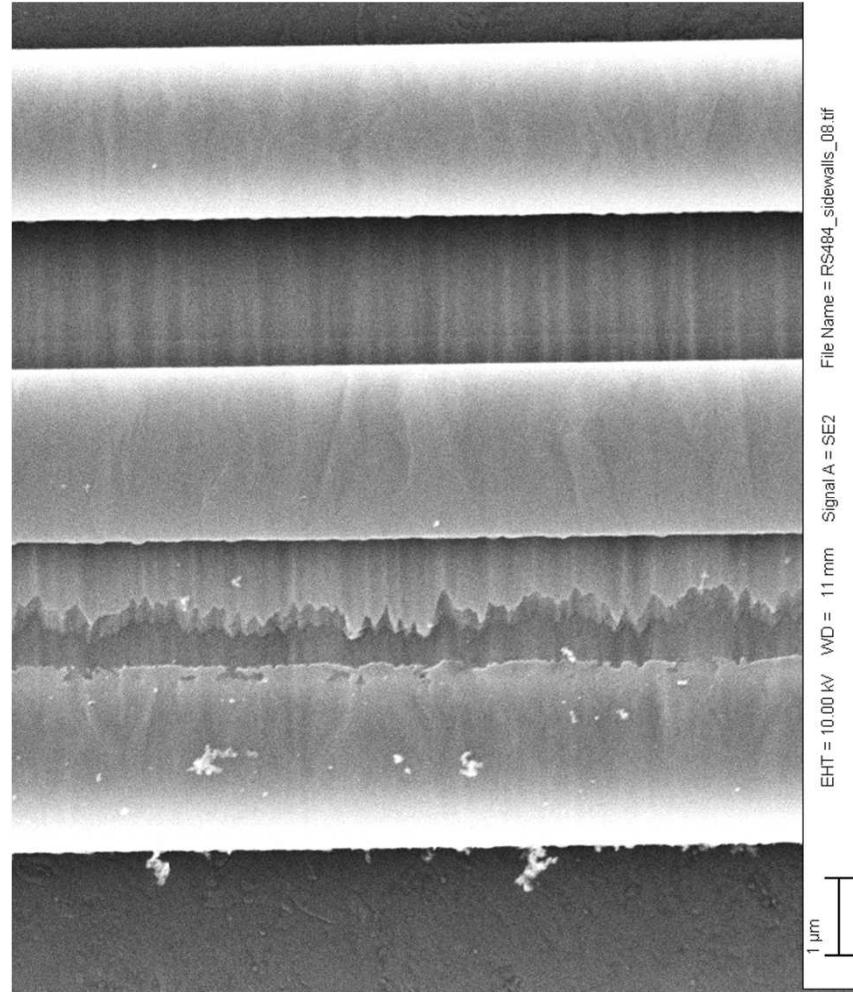
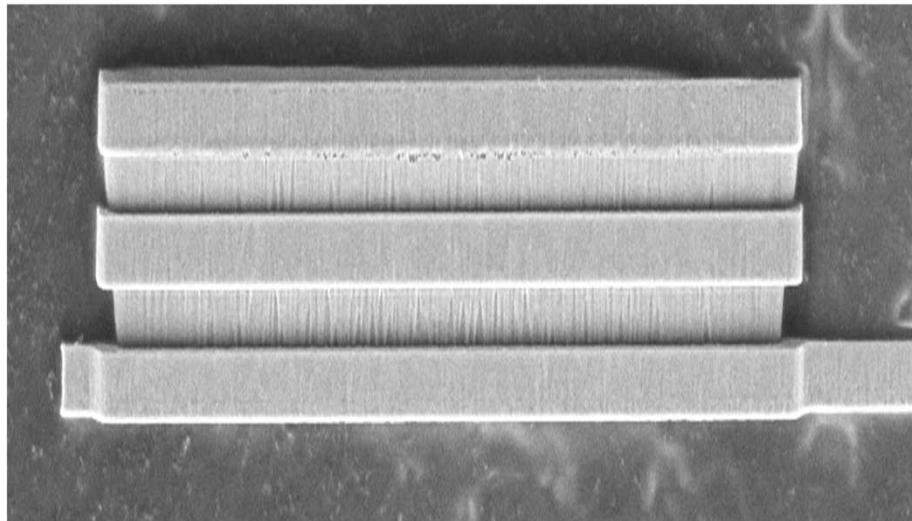
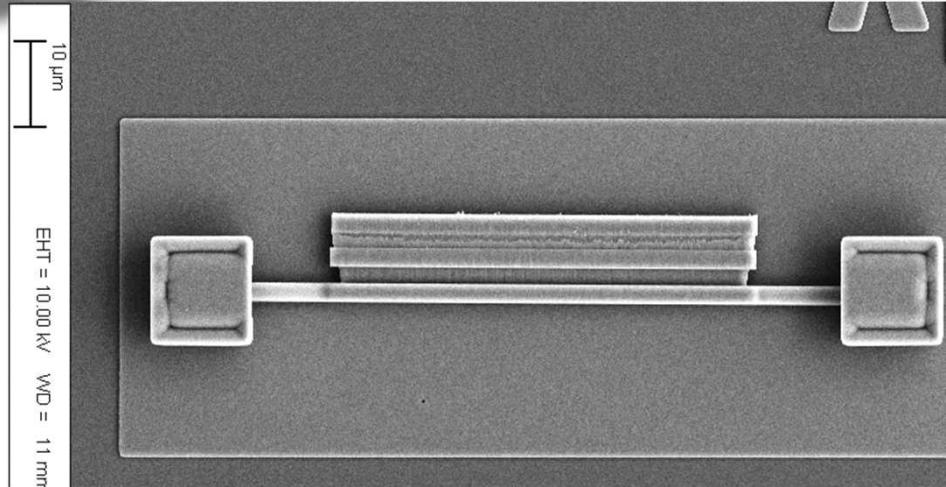
# 1 Release Etching Produces Nanoscale Failure-Inducing Surface Roughness

(A) Sandia's SUMMiT V Polysilicon:



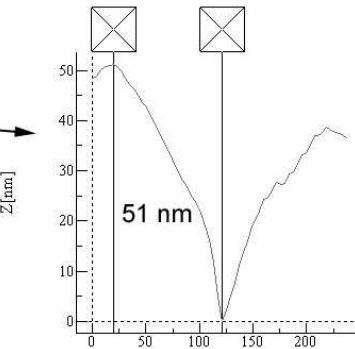
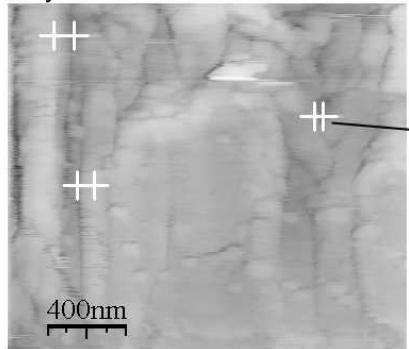
**Characteristic**  
“mirror”, “mist”, and  
“hackle” features can  
be confounded by the  
interplay between the  
relatively coarse  
crystallites and the  
crack path.

# Measuring the Sidewall Roughness Of Polysilicon...

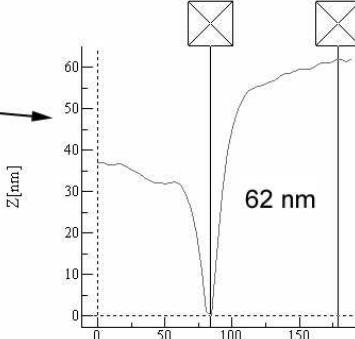
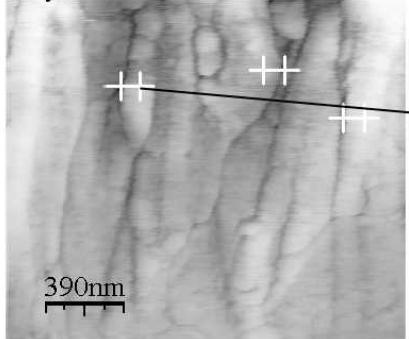


# Why Are Some Layers Stronger Than Others? Surface Roughness!

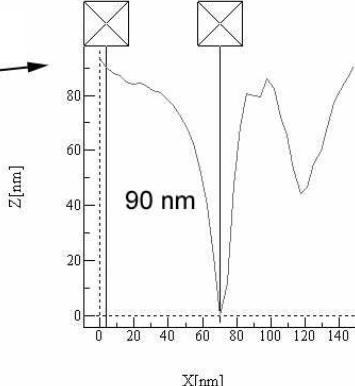
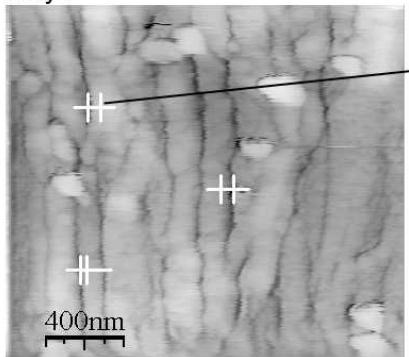
Poly21



Poly3



Poly4



## Sidewall Roughness of Polysilicon measured by AFM

Layer	Average Roughness (nm)	RMS Roughness (nm)
Poly21	12.8	15.9
Poly3	11.7	14.1
Poly4	9.3	12.1

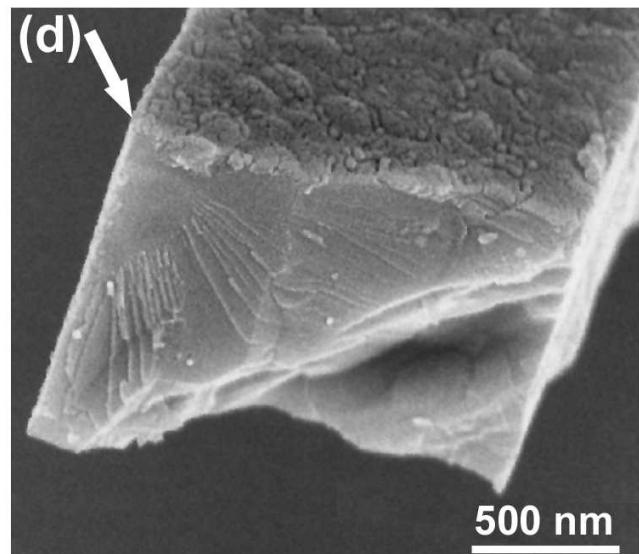
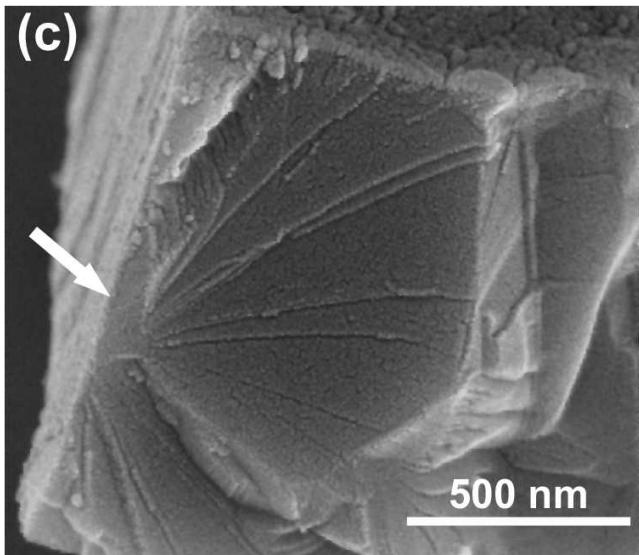
B.L. Boyce et al., J. MEMS 16:179-90, 2007



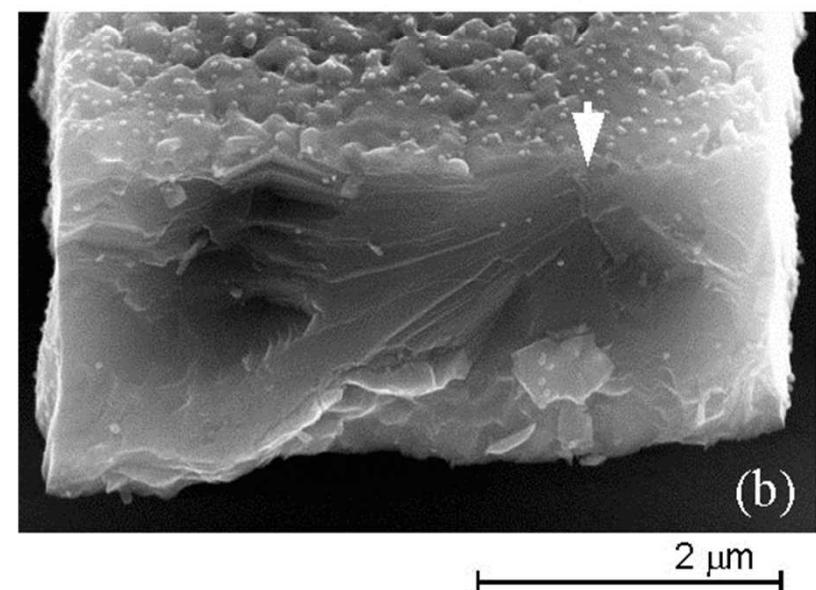
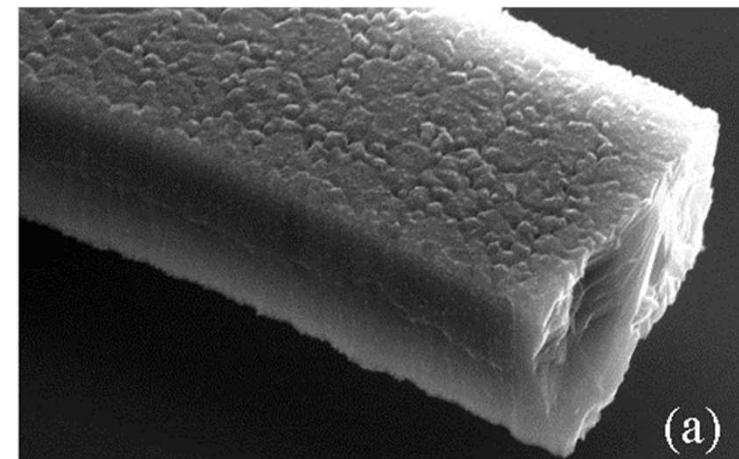
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# SUMMiT V compared to MUMPs

SUMMiT V polysilicon:



MUMPs polysilicon:



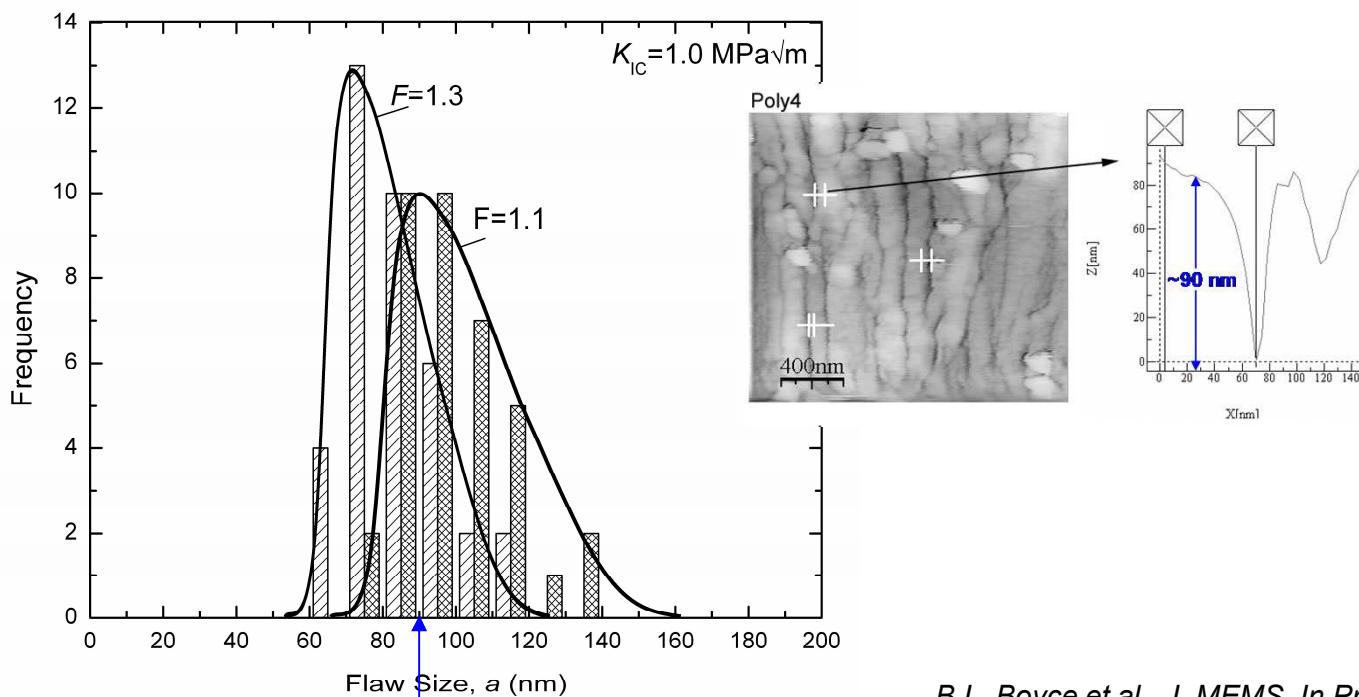
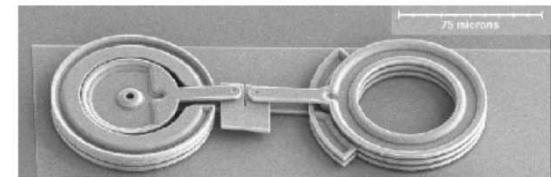
Sandia National Laboratories

# Fracture Mechanics Is Consistent With Surface Roughness as a Critical Flaw

(A) Sandia's SUMMiT V Polysilicon:

$$K_{IC} = \frac{2}{\pi} F \sigma_f \sqrt{\pi a} \Rightarrow a = \frac{\pi}{4} \frac{K_{IC}^2}{F^2} \frac{1}{\sigma_f^2}$$

fracture toughness  
flaw size  
geometry factor  
fracture strength



B.L. Boyce et al., J. MEMS, In Press, 2006



Sandia National Laboratories

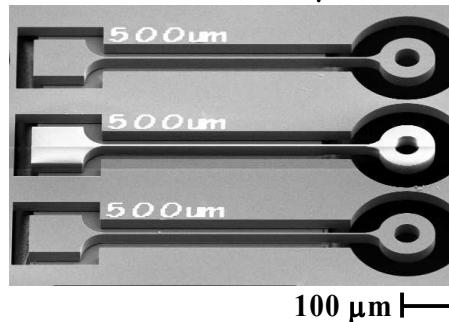
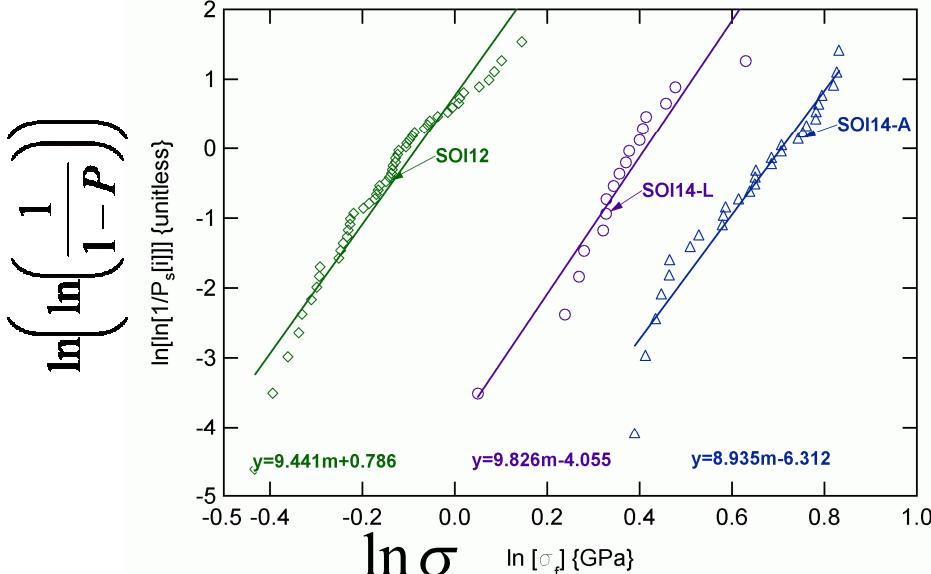
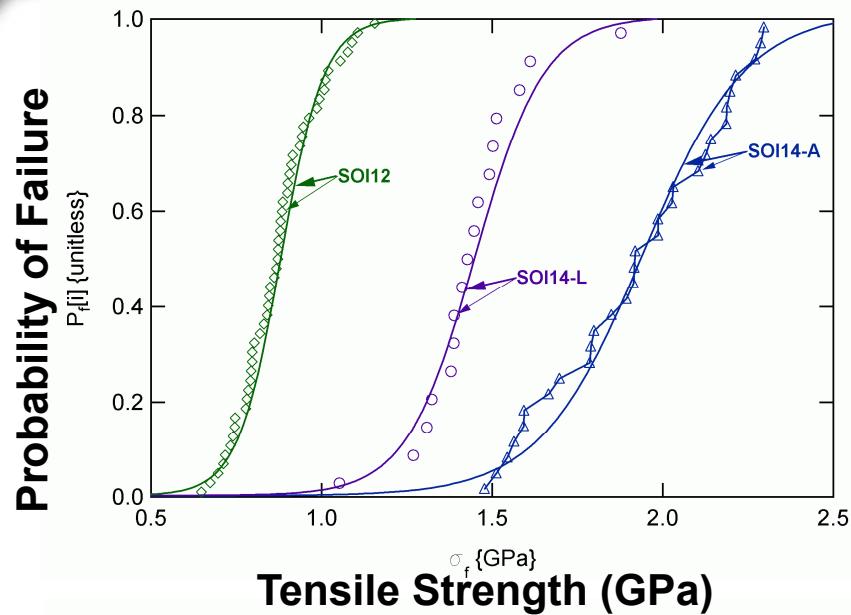


**Q: Do etch-induced sidewall defects affect the strength of single-crystal Si as well?**



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# Silicon-On-Insulator Exhibits Wide, Die-Dependent Strength Distributions



$$P = 1 - \exp\left[-\left(\frac{\sigma}{\sigma_\theta}\right)^m\right]$$

$$\downarrow$$

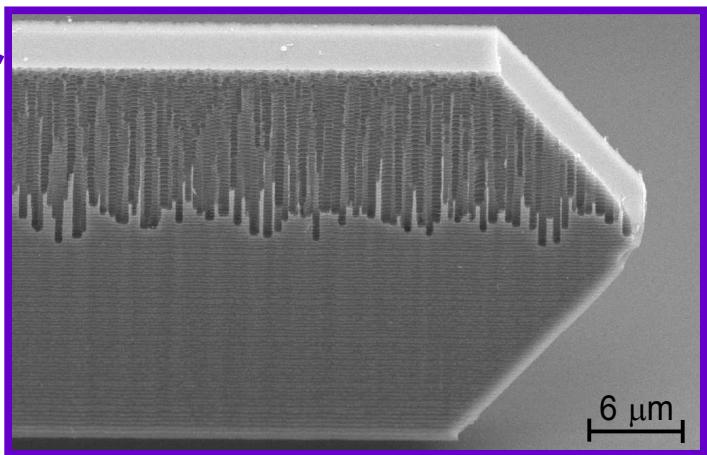
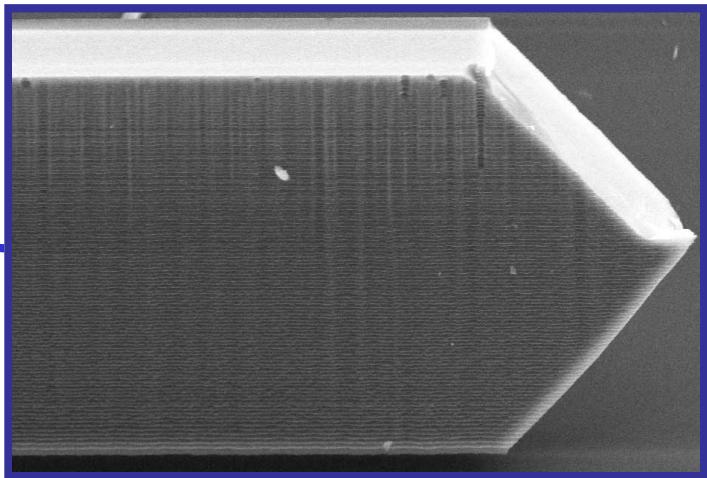
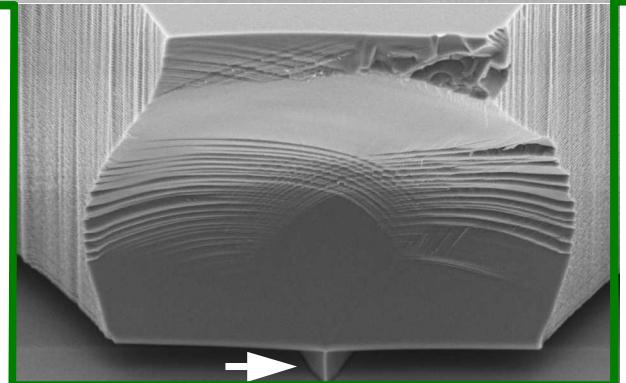
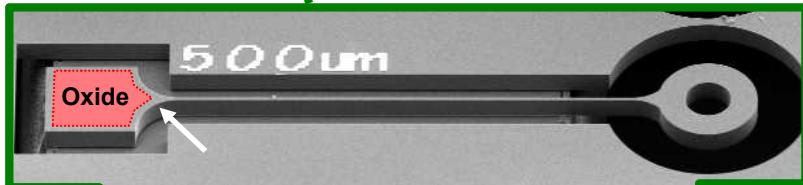
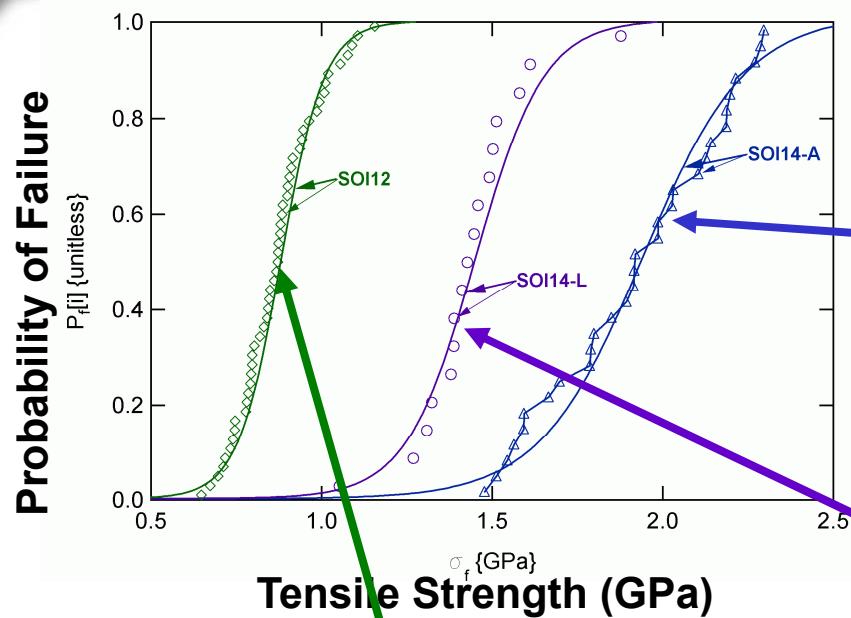
$$\ln\left(\ln\left(\frac{1}{1-P}\right)\right) = m \ln \sigma - m \ln \sigma_\theta$$

D.C. Miller and B.L. Boyce, 2006



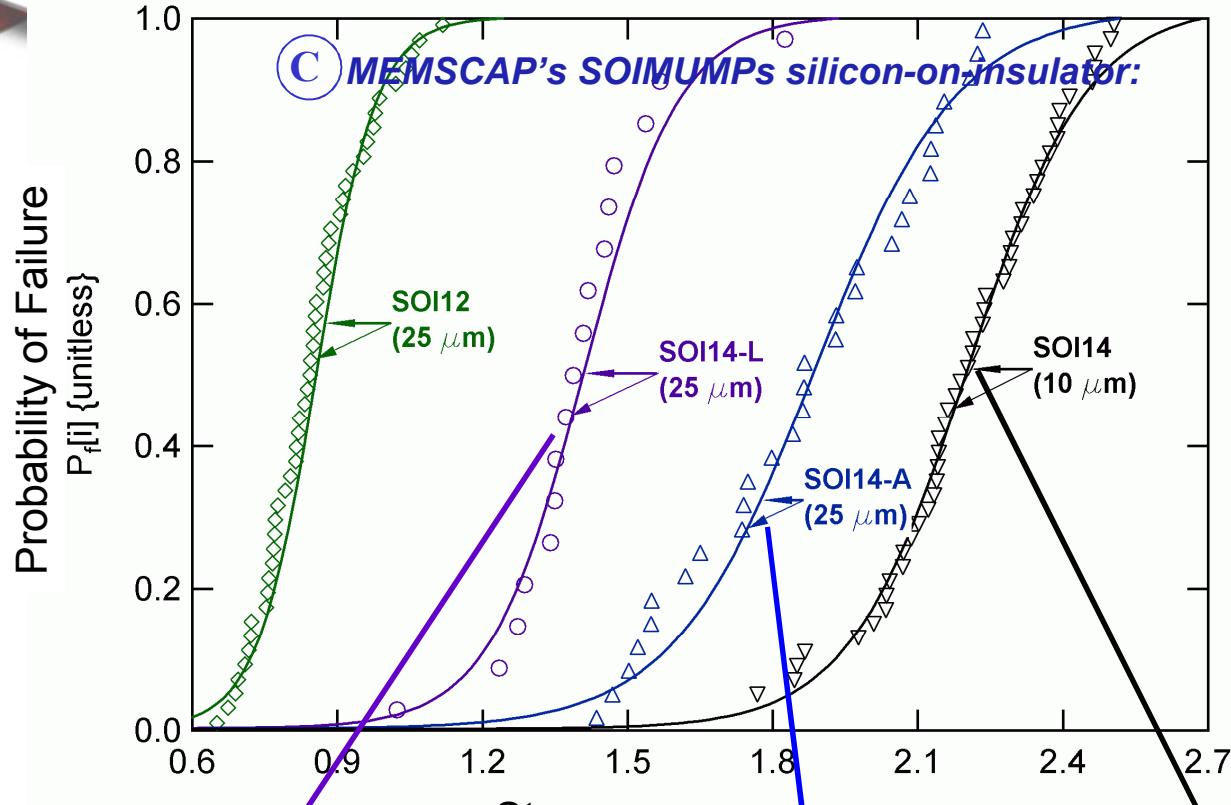
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# Fractography Reveals Process-Induced Failure Origins

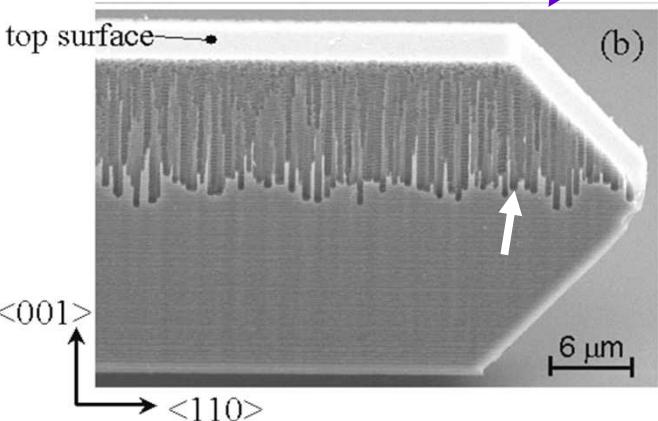


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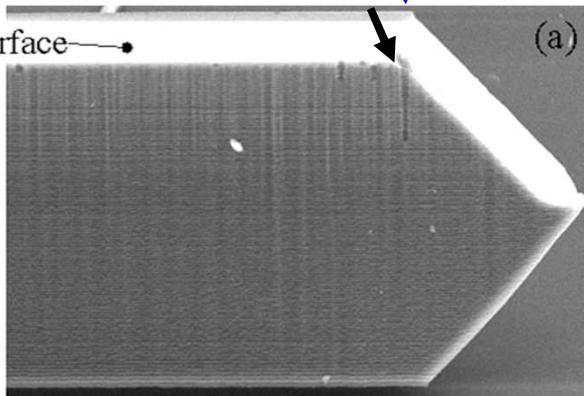
# 1 Example 2: Edge Defects in SOI



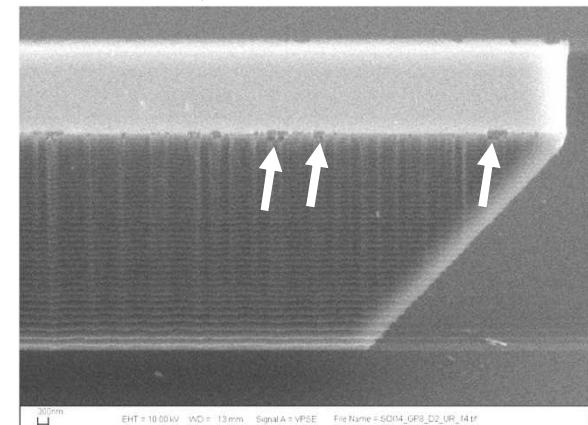
$\sigma_f = 1.39$  GPa



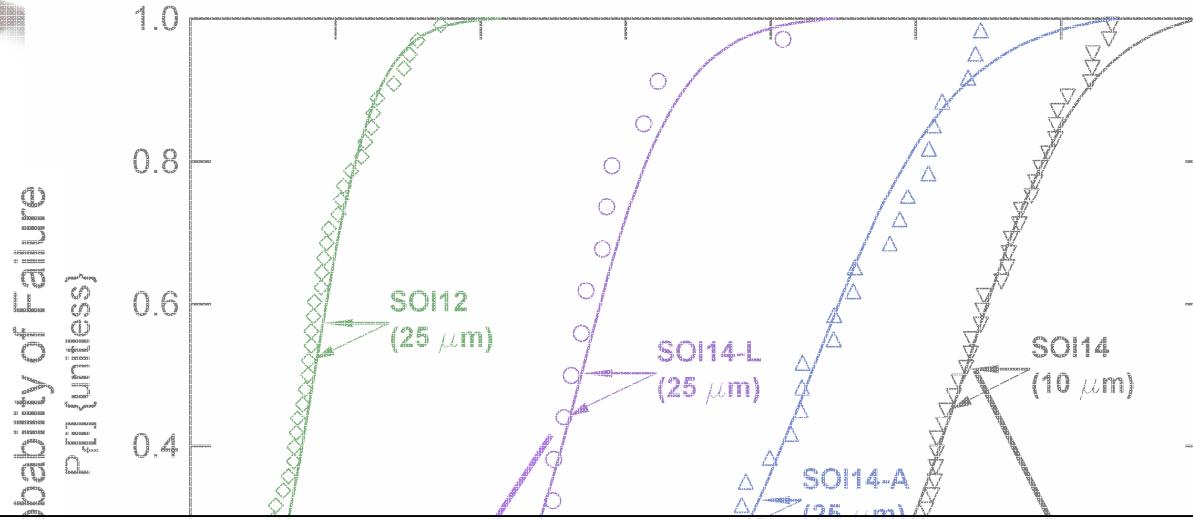
$\sigma_f \approx 1.9$  GPa



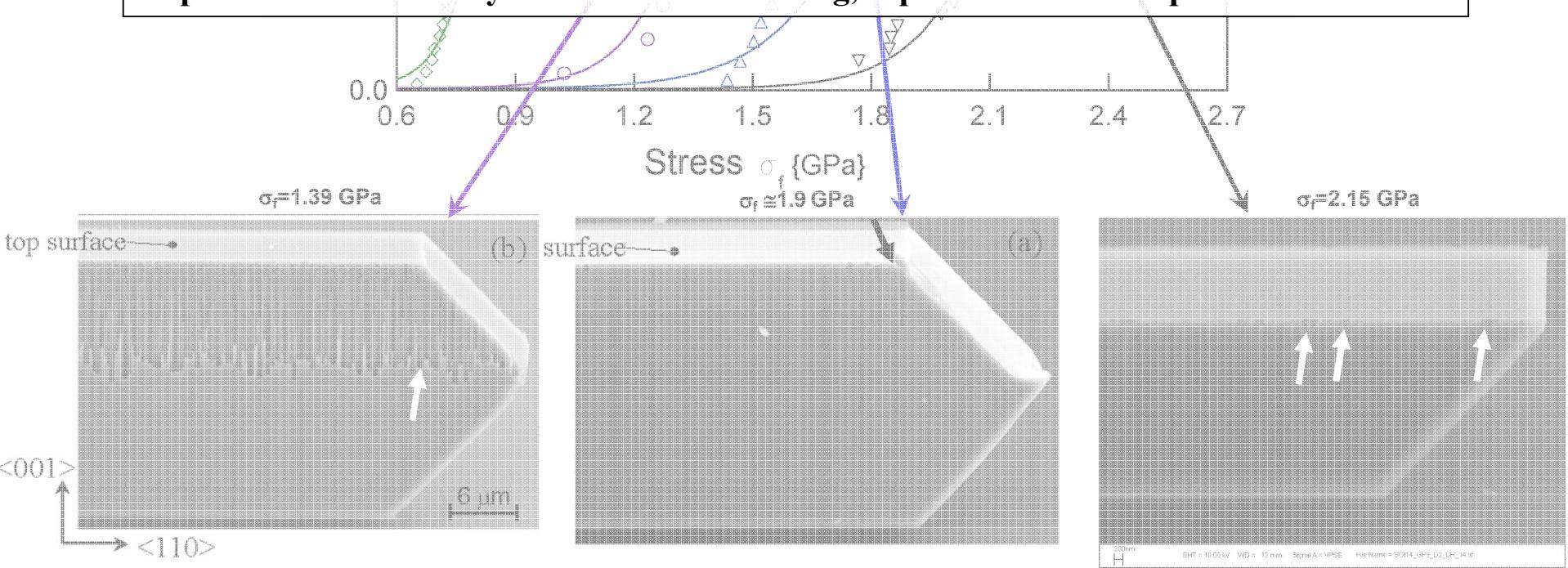
$\sigma_f = 2.15$  GPa



## Example 2: Surface Roughness in SOI



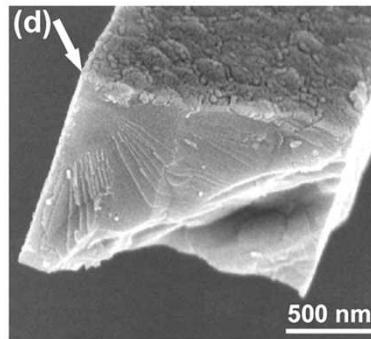
Erosion of the resist pattern's sloped edge is thought to be the cause of these defects. The slope of the resist is very sensitive to the coating, exposure and develop conditions.



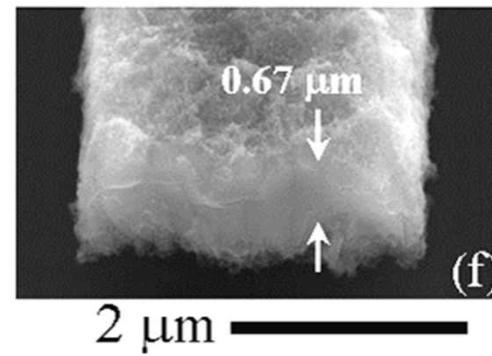
# Outline:

## *Etch-induced Nanoscale flaws affect the strength of all Si microfab technologies*

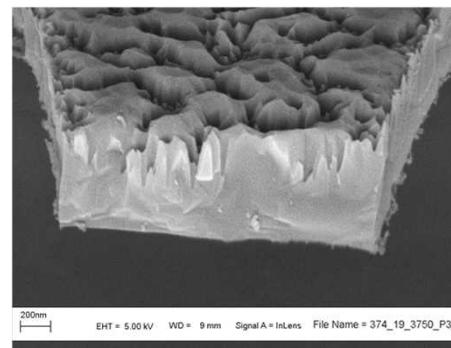
1. As-fabricated surface roughness (etch-induced nanoscale flaws)



2. Galvanic corrosion as a pathway to degraded properties.

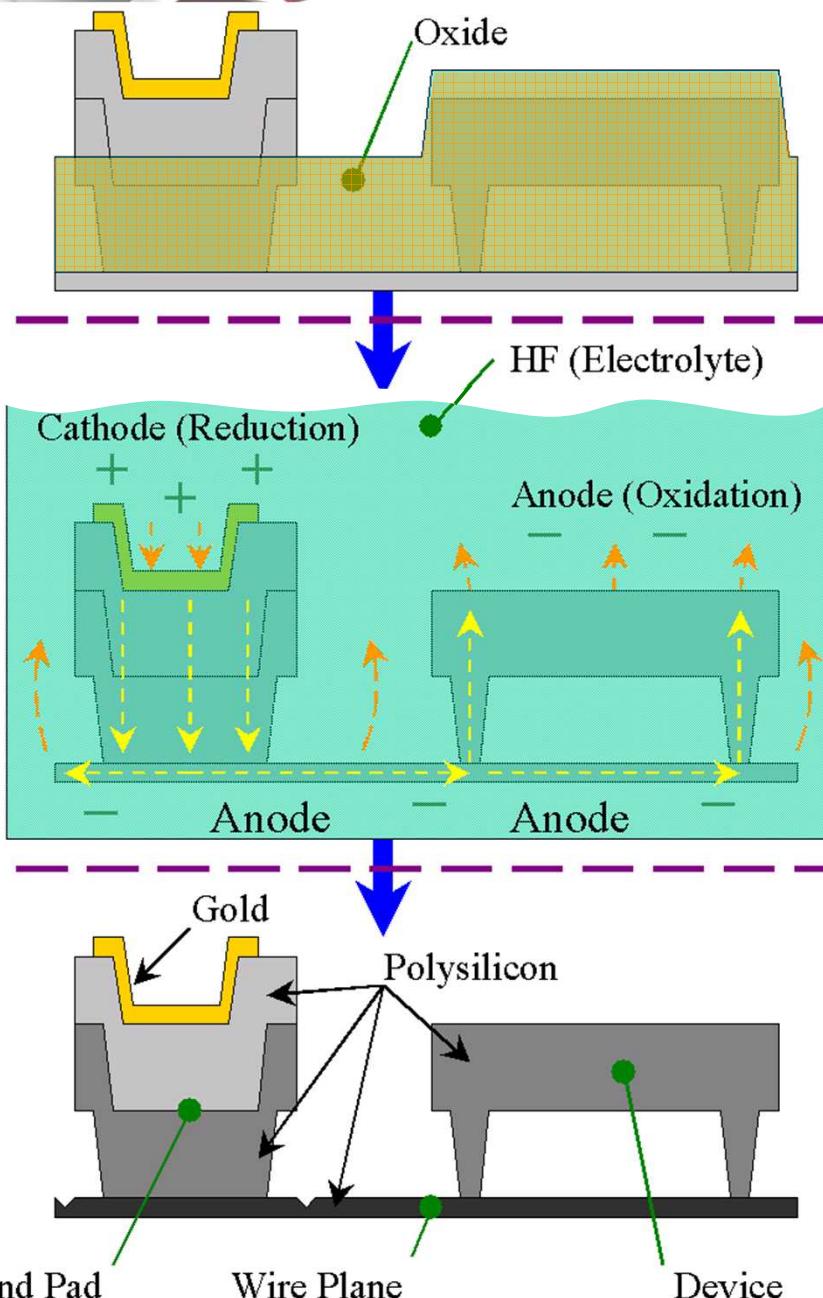


3. Best-case and worst-case scenarios in silicon fabrication processes

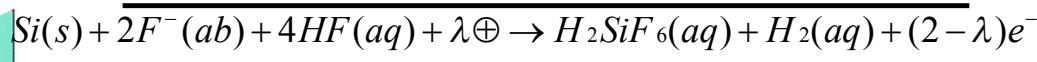


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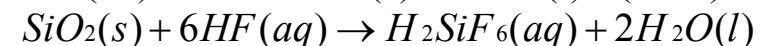
## 2 Au-Si Galvanic Corrosion during HF Release



*Oxygen reduction @ cathode*



*Silicon dissolution, flourine absorbed @ surface,  $\lambda=2$*



*description of net process:*

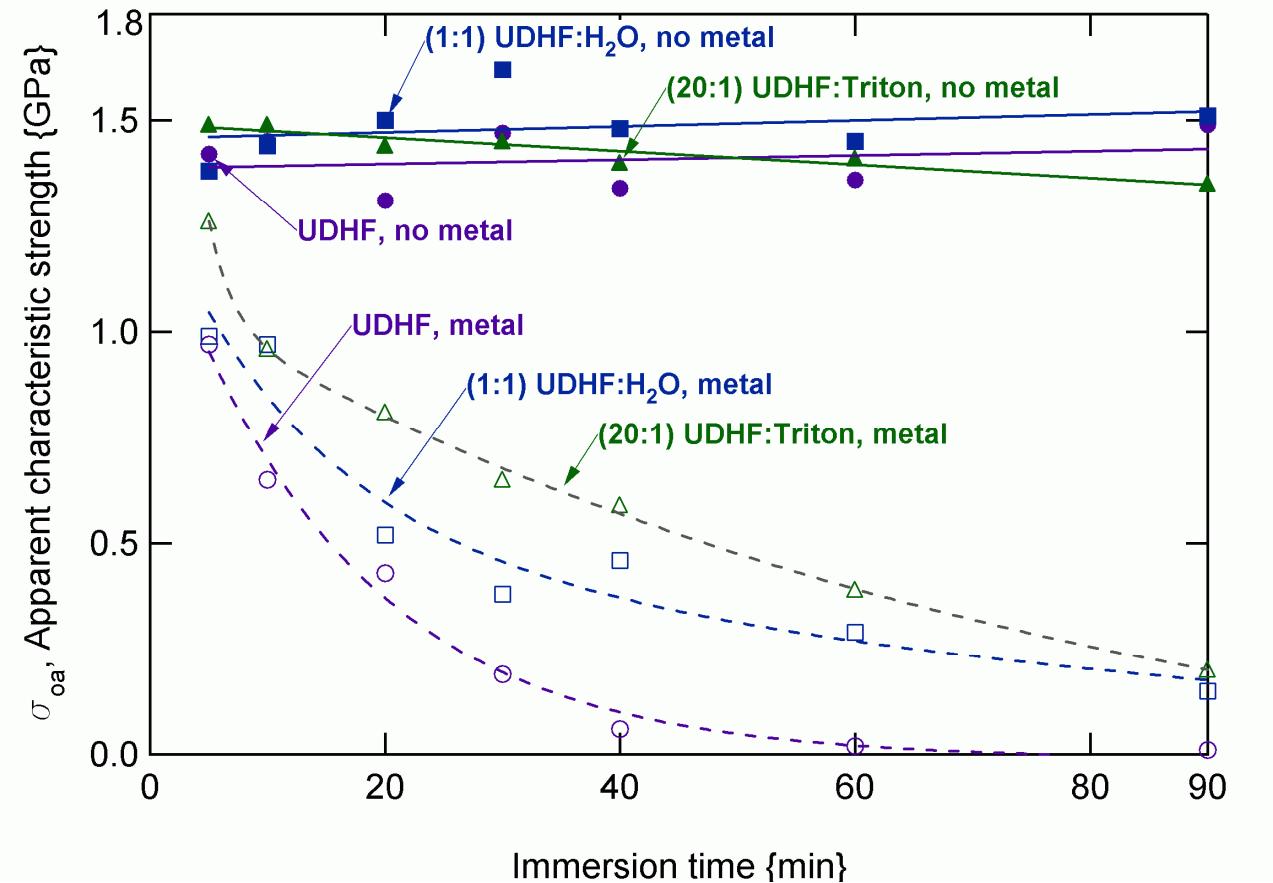
*Zhang et. al., J. Electrochem Soc., 136, 1561 (1989).*



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## 2 Observations on Etch-Time Dependent Strength Reduction

B MEMSCAP's polyMUMPs polysilicon:



D.C. Miller, B.L. Boyce, K. Gall, C. Stoldt, Appl Phys Lett 2007

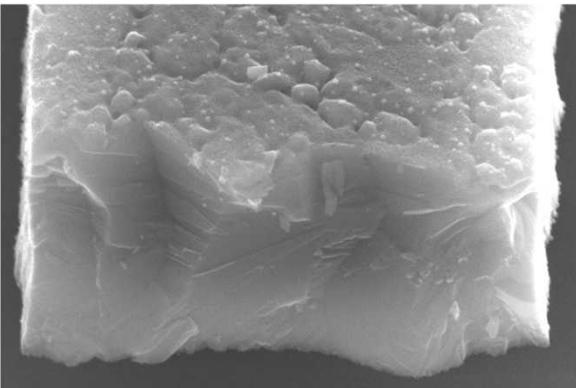


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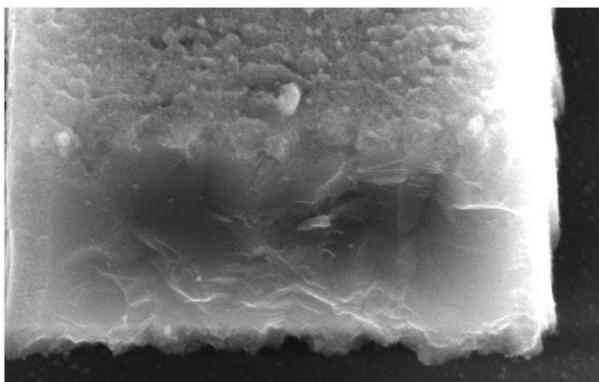
## 2 Corrosion Morphology Progression

B MEMSCAP's polyMUMPs polysilicon:

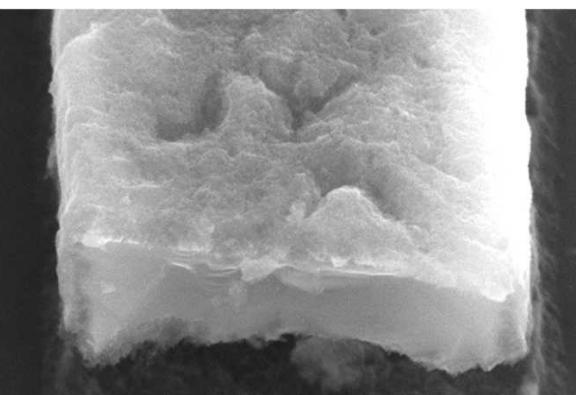
5 min



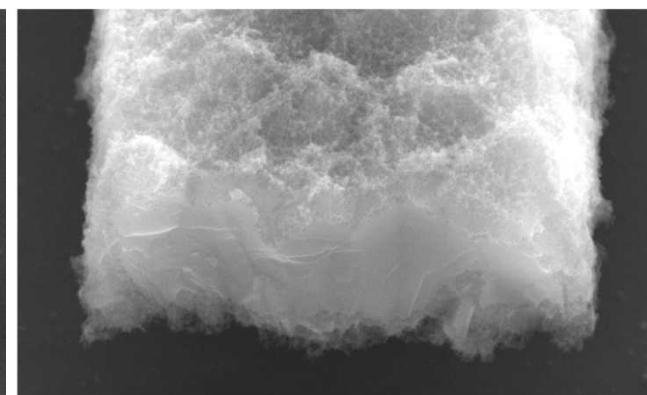
30 min



60 min



90 min



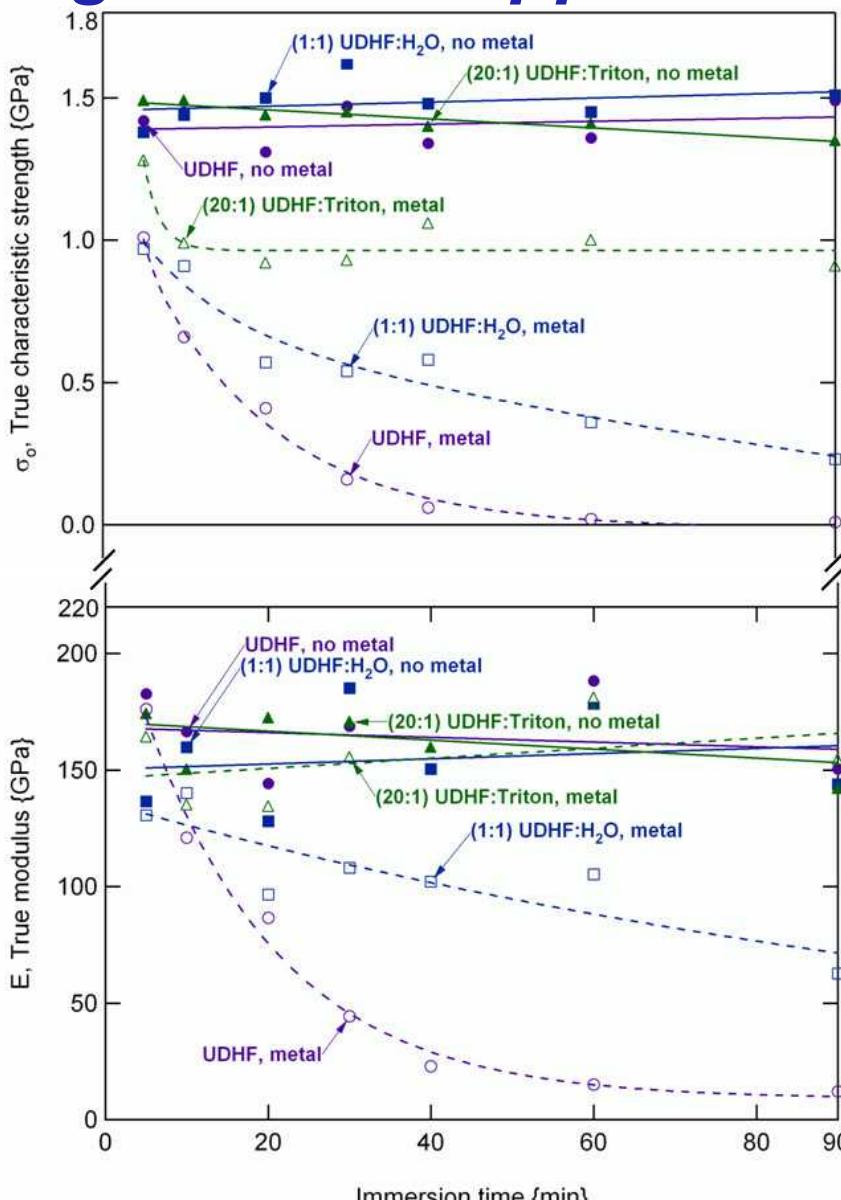
1  $\mu$ m

## 2 | *Effect of Surfactant on Degradation*

## B MEMSCAP's polyMUMPs polysilicon:

D.C. Miller, B.L. Boyce, K. Gall, C. Stoldt, *Appl Phys Lett* 2007

# The corrosion-induced structural damage also degrades the apparent modulus of Si



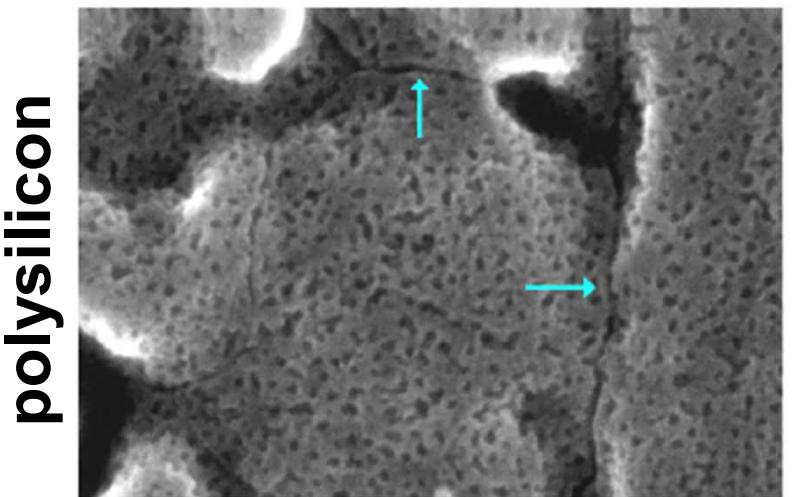


**Q: Does this strength-reducing galvanic damage occur in single crystal silicon as well?**

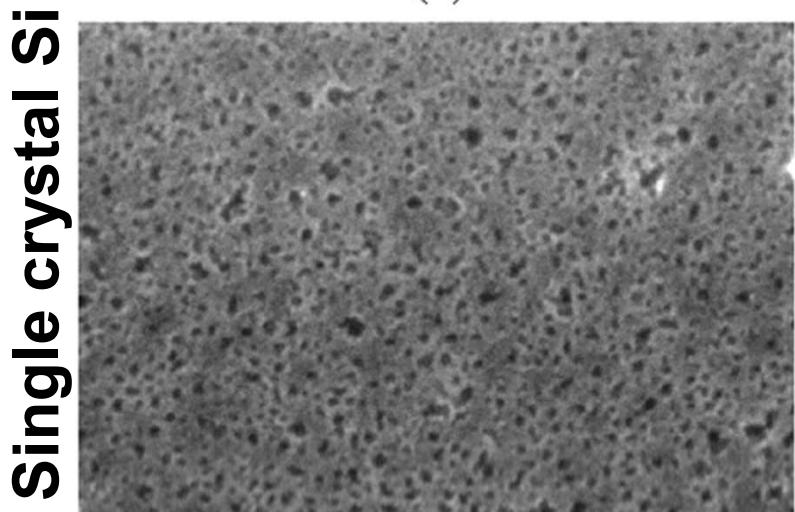


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# Corrosion-Induced Nanoporosity



(a)



(b)

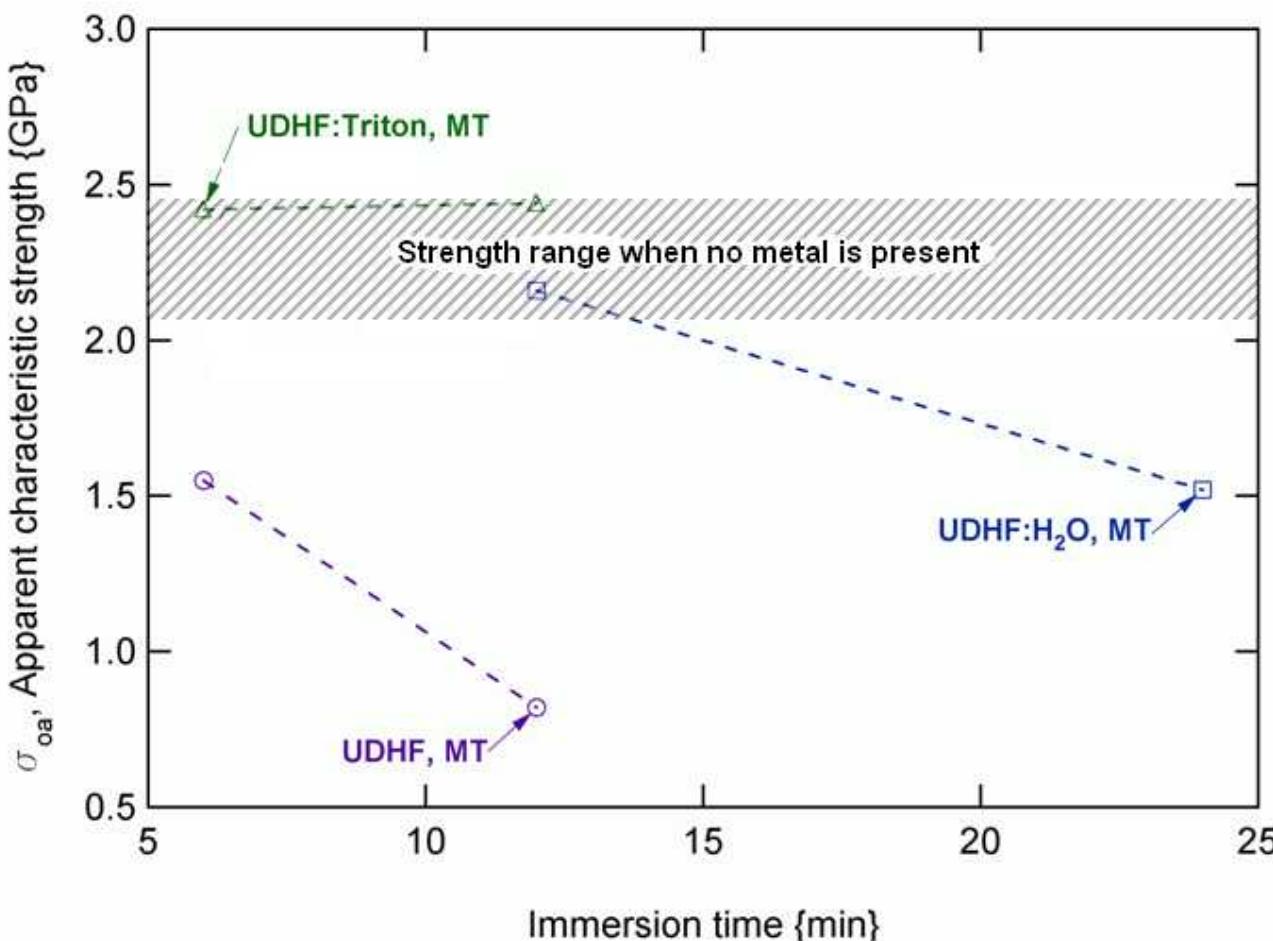
— 40 nm

polysilicon

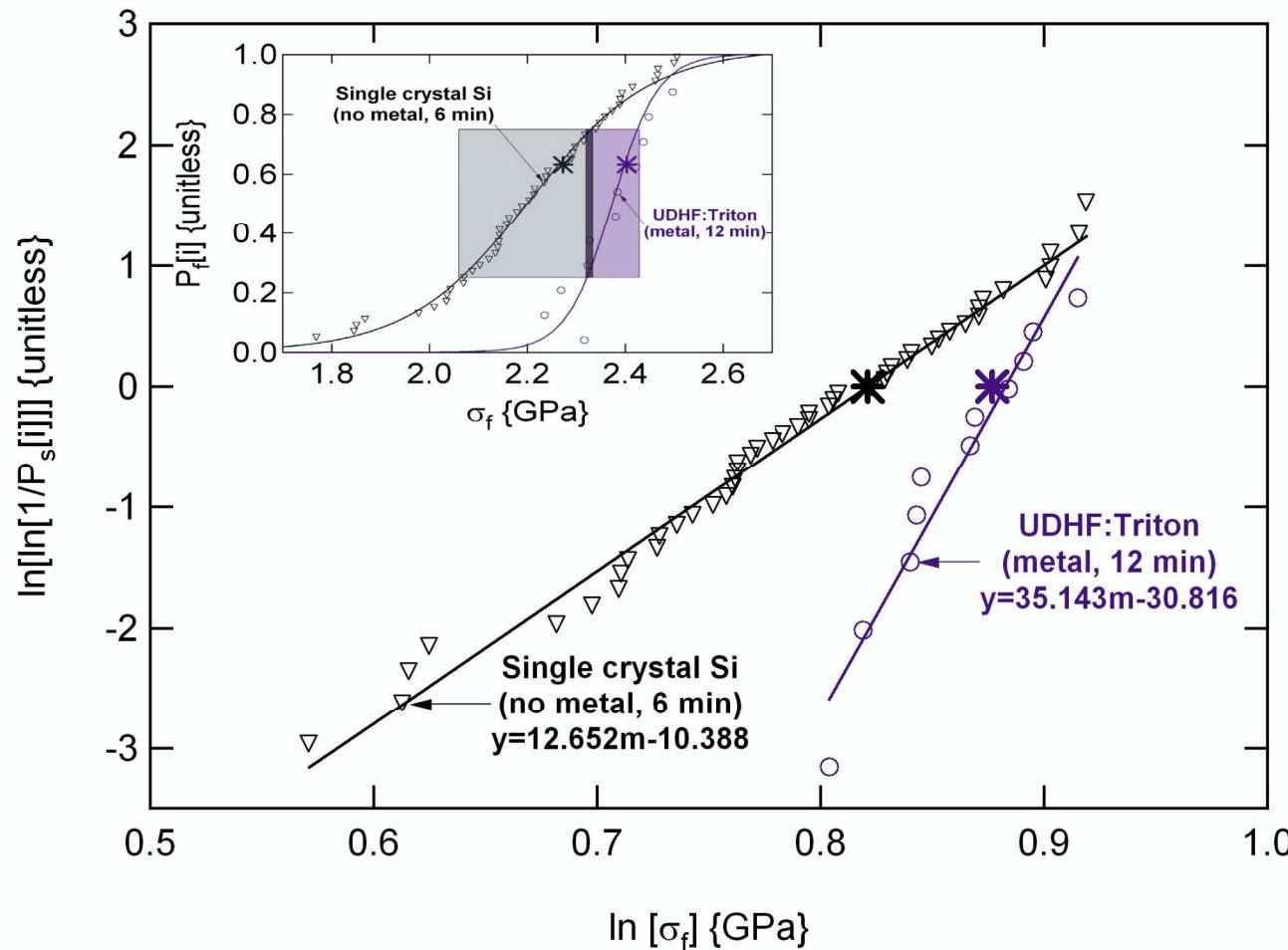
Single crystal Si

In both single crystal and polycrystalline Si, corrosion causes nanopores and ensuing surface oxidation, but of course single crystal Si does not suffer from preferential grain boundary attack.

# Single-crystal Silicon (SOI) Etch-Time Dependent Strength Degradation



# Conundrum: galvanic corrosion of single-crystal Si in Triton actually improves strength!

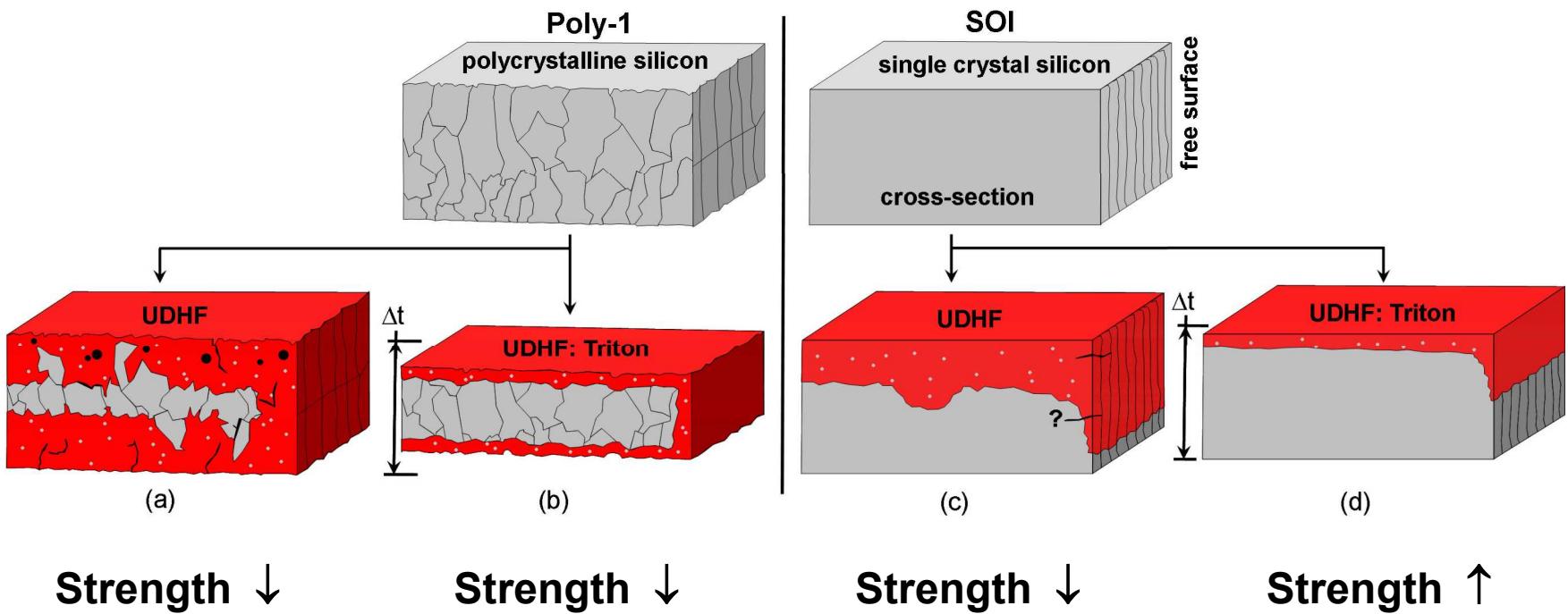


D.C. Miller, B.L. Boyce, P.G. Kotula, C. Stoldt, *J Appl Phys*, In Review



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# Summary of Corrosion Damage Morphology In Silicon



D.C. Miller, B.L. Boyce, P.G. Kotula, C. Stoldt, J Appl Phys, In Review

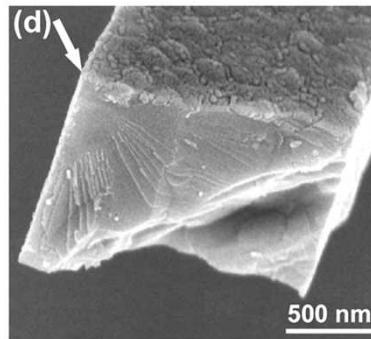


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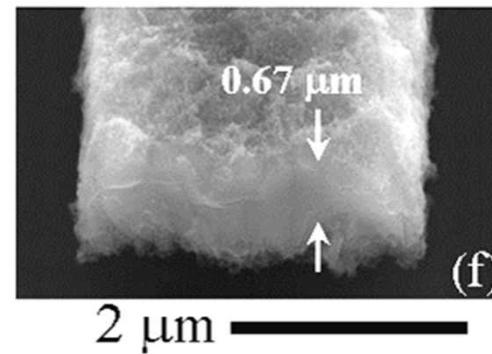
# Outline:

## *Etch-induced Nanoscale flaws affect the strength of all Si microfab technologies*

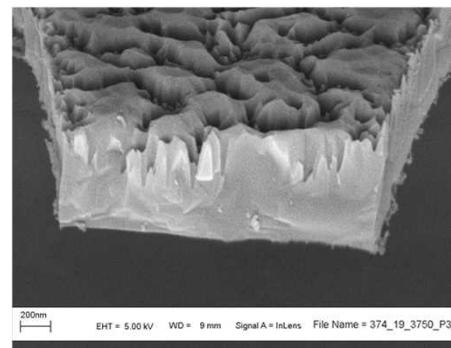
1. As-fabricated surface roughness (etch-induced nanoscale flaws)



2. Galvanic corrosion as a pathway to degraded properties.



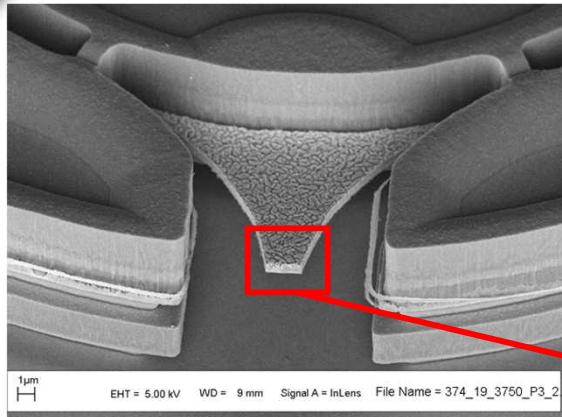
3. Best-case and worst-case scenarios in silicon fabrication processes



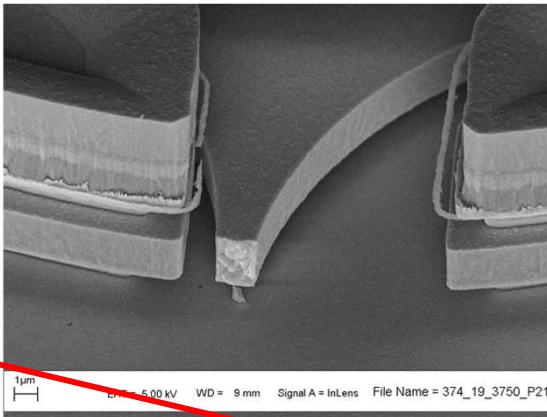
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# Anomalous Surface Roughness

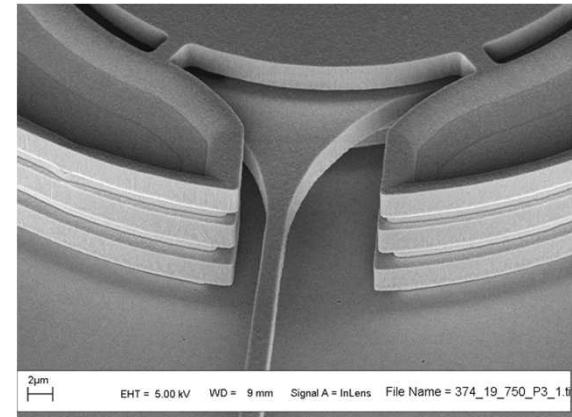
poly3



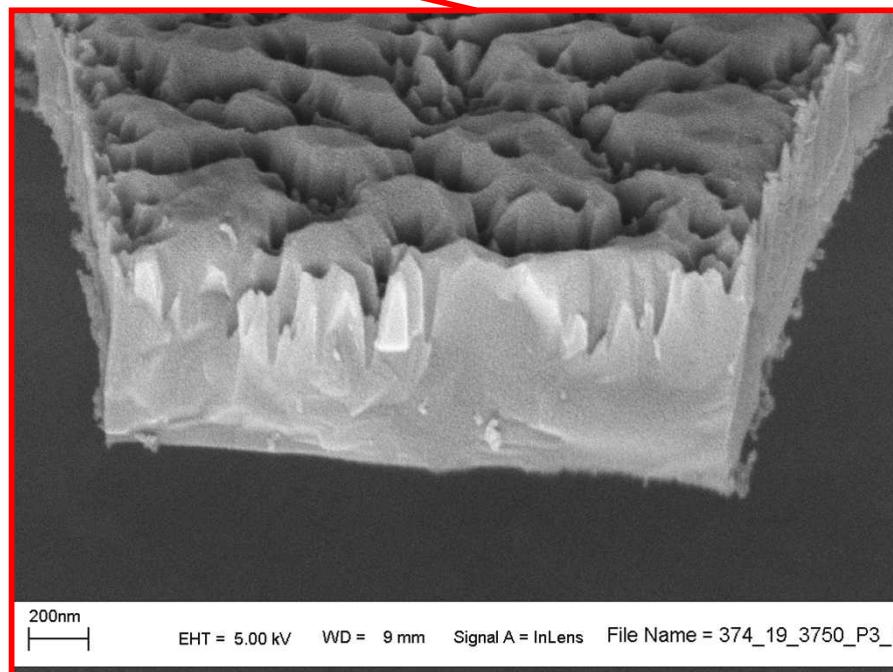
Same die, poly21



Same die, another poly3



During routine tensile testing, of 100's of tensile bars over the past 5 years, one technician noted: “low odd failure”



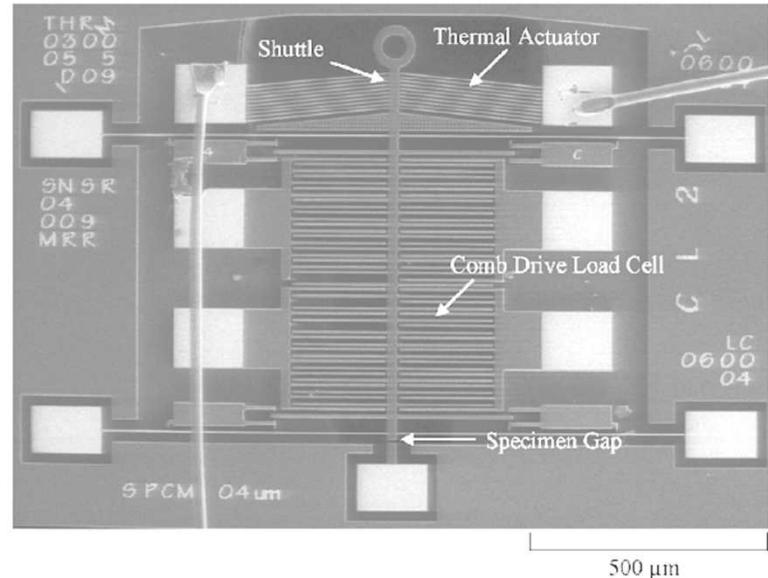
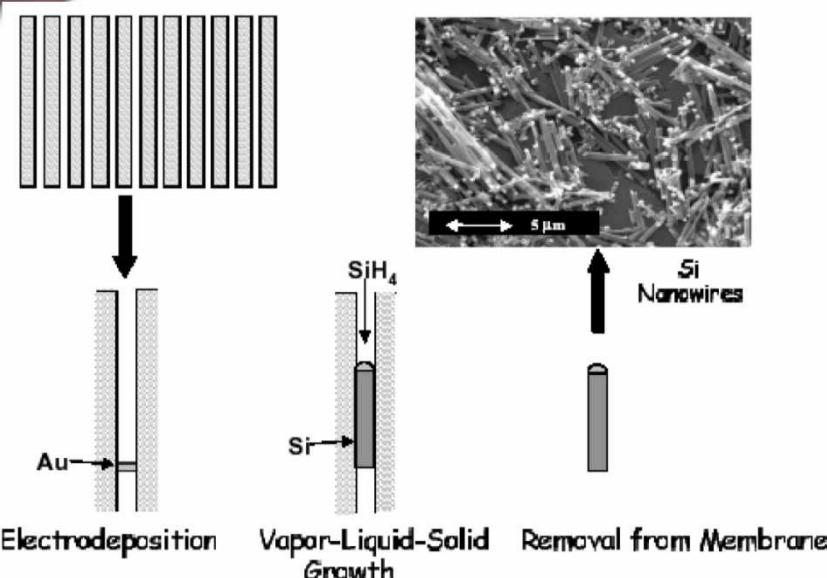
This specimen failed at a stress of <0.1 GPa. “low, odd failure”

This anomalous zone of “bad” Si has terrible implications for the tails of our Weibull distribution.

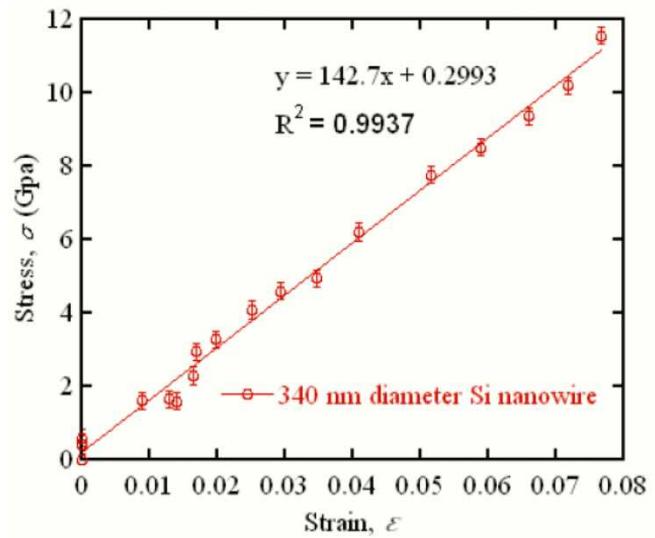
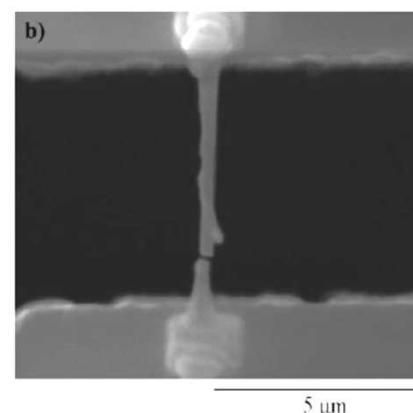
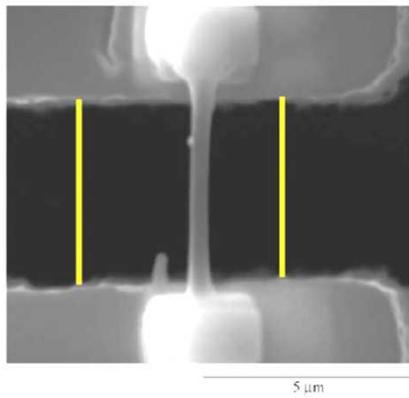


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# “Perfect” Si without etch defects?



43. Redwing, J.M., Lew, K.K., Bogart, T.E., Pang, L., Dickey, E.C., Carim, A.H., Wang, Y., Cabassi, M.A., Mayer, T.S. *Synthesis and properties of Si and Si/Ge/Si nanowires*. in *Quantum Dots, Nanoparticles, and Nanoclusters*. 2004. Bellingham, WA: SPIE.





# **Summary....**

**Not all silicon is made the same.**

**Every type of silicon will have different strength properties... layer-to-layer, die-to-die, wafer-to-wafer, process-to-process.**

**In nearly all cases, the strength of the particular type of silicon is controlled by the etch-induced defects. In the unusual case of**

**Understanding the mechanisms of flaw formation during the etch process may enable future improvement in the reliability of structural silicon devices.**



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