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Characterizing SRAM Single Event Upset in Terms of Single and Double Node Charge Collection

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Abstract: A new mode for SRAM SEU is proposed and demonstrated through TCAD modeling. The SRAM recovery is shown to be based on cell imbalance. Implications of this mode are discussed.

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The study and analysis of static random access memory (SRAM) single event upset (SEU) has been ongoing since the late 1970s [1,2]. Diehl et al. identified strikes to the OFF NMOSFET drain and OFF PMOSFET drain as being the underlying events responsible for SRAM SEU and used circuit modeling to demonstrate the mechanism [3]. Over the years, as SRAM cells have scaled down in size, a new effect was observed: multiple cell upsets (MCU) from a single event [4]. Dodd et al. used mixed-mode device/circuit modeling to demonstrate that the MCU mechanism is due to charge collection in adjacent SRAM cells [5]. Still, the primary mechanism for a single SRAM cell to flip was charge collection at an OFF transistor drain, which we will denote as single node charge collection (SNCC). This paper proposes a new mechanism for SRAM SEU due to charge collection in both OFF and ON transistors, or double node charge collection (DNCC). The double node charge collection mechanism is demonstrated through technology computer aided design (TCAD) device modeling and simulation of a full SRAM cell. The impact of the new mechanism is then discussed.

A basic SRAM cell consists of six transistors: two cross coupled inverters (four transistors) and two access pass-gate transistors. In device and circuit modeling, the SRAM cell is created to be ideally balanced, meaning the device is perfectly symmetric between the two inverters, physically and electrically. An ideally balanced SRAM cell will most likely power up in a metastable state and will need some initial condition in order to drive the cell into one of the two stable states. However, SRAM cells are not ideally balanced in practice. There are a number of manufacturing variations, such as threshold voltage variation and metallization loading, that will unbalance the SRAM cell. In addition, there are some environmental variations, such as noise, which will also work to unbalance the SRAM cell. An unbalanced SRAM cell will power up into one of the stable states [6, 7]. If the imbalance is dominated by manufacturing variations then the cell will mostly power up in the same state, but if the imbalance is dominated by noise, then the cell will power up randomly into one or the other state.

A 3-D TCAD model of a SRAM cell was constructed using Synopsys Dessis. A top view of the cell is shown in Figure 1. The SRAM cell is representative of an unhardened 90 nm SRAM cell. The TCAD design was ideally matched using complete symmetry in the doping definitions and meshing of the node points. This SRAM design was shown to upset in TCAD simulation with a charge deposition of 5 fC/μm (LET = ~0.5 MeV-cm^2/mg) due to an ion strike directly on the drain of the OFF NMOSFET (NHIT). If the ion strike is applied to the center of the SRAM cell, shown at point A, both the OFF and ON PMOSFET will collect charge, though only the OFF PMOSFET initially exhibits a voltage drop. Simulation results displaying the two node voltages after ion strikes with various amounts of charge deposition are shown in Figure 2. Note that node 1 is initially logic high and node 2 is logic low. The lowest charge deposition, 50 fC/μm, causes a slight perturbation in the node voltages, but the voltages quickly return to their original values. The 100 fC/μm plot shows the two node voltage values coming together, staying together for about 150 ps, and then reverting to their original values. The last plot, 200 fC/μm, shows an increase in the time during which these two node voltages stay together and the SRAM eventually upsets. This result suggests that when the two node voltages come together and stay together, the SRAM cell is placed into a metastable state and that the imbalance in the cell, whether due to manufacturing or environment, will dictate the recovery state. Thus, the reason why the cell changes states at 200 fC/μm and not at 100 fC/μm is based on the design of the symmetrical SRAM model and the numerical calculations of the TCAD tool.

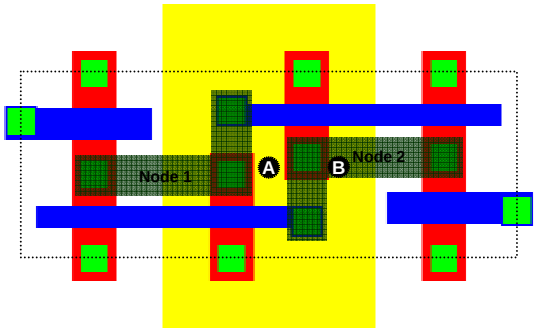
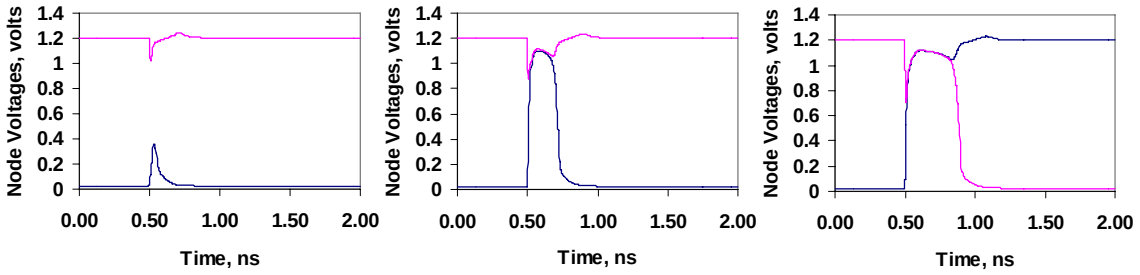


Figure 1. Top view of 3-D TCAD model for a 90nm SRAM cell. The PMOSFETs are located in the N-well (yellow region) in the center of the cell.

Figure 3 shows the proposed modes of SEU in a standard SRAM cell as a function of increasing charge deposition. The first two modes and the onset region are well known and have been described in



(a) LET = ~5 MeV-cm²/mg (50 fC/μm) (b) LET = ~10 MeV-cm²/mg (100 fC/μm) (c) LET = ~20 MeV-cm²/mg (200 fC/μm)

Figure 2. SRAM node voltage plots versus time for three different charge depositions at point A (cf. Figure 1).

numerous publications [3,4,5]. We propose that the upset region can be broken into two pieces, one characterized by SNCC and one characterized by DNCC. These regions are separated by a crossover region where the upset mechanism and resulting observation of the upset change. The region characterized by the SNCC follows classical charge collection at an OFF transistor drain, which can cause the SRAM cell to flip states [3]. If there is enough charge collected on that single node, then the SRAM cell will always upset. Charge collection from ion strikes primarily near an ON transistor drain will cause the SRAM cell to perturb, but will generally not upset the cell. However, there is an ion shunt mechanism through an ON drain (logic high) to the substrate (ground) that can pull this node low and upset the cell [8]. When there is enough charge deposited into the cell, the voltage potential in the N-well beneath both PMOSFET devices drops very low (1.2 → 0.3 volts). The ON PMOSFET drain becomes forward biased and its potential follows the N-well potential differing by the built-in potential for the p+/n junction (1.2 → 1.05 volts). The OFF PMOSFET drain collects charge, raising its potential. The rise in the OFF PMOSFET drain voltage is limited by the same forward bias characteristic. This results in the SRAM cell node potentials collapsing upon each other for a short period of time, shifting the SEU mechanism to being characterized by DNCC. In this case, the SRAM cell enters a metastable state, essentially internally debiasing the cell. As the charge collection subsides, the SRAM re-biases and the resulting final state of the SRAM cell will depend on its imbalance. In this region of charge collection, ion strikes to the OFF transistor drains will not always cause an upset and strikes to the ON transistor drains may cause an upset.

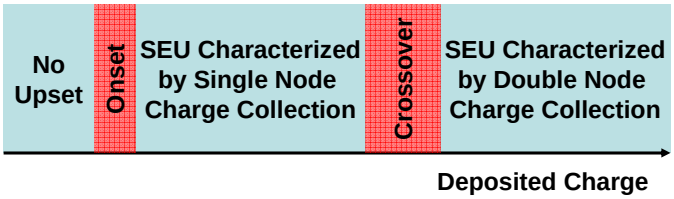
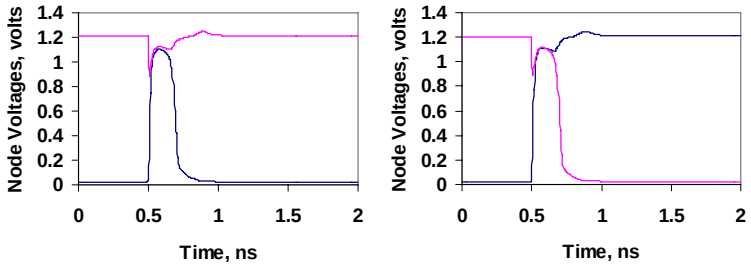


Figure 3. SRAM SEU Modes as a Function of Deposited Charge.

The region of charge deposition where the SEU mode transitions from SNCC to DNCC is defined as the crossover region. The result from a 100 fC/μm event at point A (Figure 2b) best demonstrates the crossover charge deposition point for this SRAM cell model. The SRAM TCAD model was modified to decouple the power supplies to each inverter so that this value can be offset. By inserting a 10 mV offset into one or the other power supply, the SRAM cell was either held from upsetting (Figure 4a) or forced to upset (Figure 4b). Similar results occurred for charge deposition of 200 fC/μm at point A. Threshold voltage mismatches and current-resistance drop variations can account for manufacturing imbalances of this level and charge collection variations can account for environmental imbalances of this level.

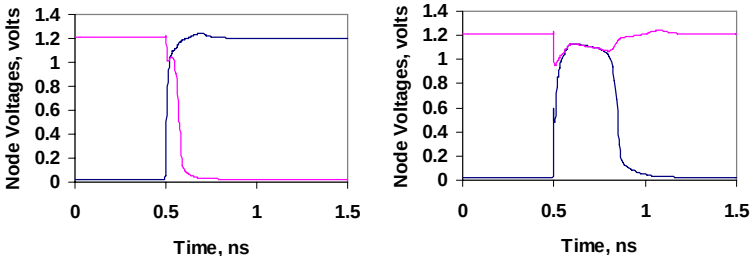
To better illustrate the impact of the DNCC mechanism, consider normally-incident ion strikes to point B, near the OFF PMOSFET drain, in Figure 1. For these TCAD simulations, the bias was offset 10 mV, intentionally preferring the original state of the SRAM cell. Two ion strikes were simulated, 50 fC/μm and 200 fC/μm. The node voltage plots for these simulations are given in Figure 5. With the lower

charge deposition, the SRAM upsets due to SNCC. But, at the higher charge deposition, the SRAM recovers to its original state due to the DNCC.



(a) V_{DD1} = 1.20 volts, V_{DD2} = 1.21 volts (b) V_{DD1} = 1.21 volts, V_{DD2} = 1.20 volts

Figure 4. SRAM node voltage plots for two voltage imbalances with charge deposition of 100 fC/μm at point A (cf. Figure 1).



(a) LET = ~5 MeV-cm²/mg (50 fC/μm) (a) LET = ~20 MeV-cm²/mg (200 fC/μm)

Figure 5. SRAM node voltage plots for ion strikes at point B with 10 mV imbalance.

There is no real impact of considering the upset cross section for a single SRAM cell in characterizing the SEU mode by SNCC or DNCC. For 100 fC/μm charge deposition, characterizing the upset by the traditional SNCC leads one to conclude that strikes to the OFF transistor regions will always induce upset, while strikes in the ON transistors' regions will always fail to produce upset, or that half of the ion strikes will cause upset. Assuming a purely random starting state and no preference for recovery into one state over the other across the SRAM array, characterization by DNCC leads to the conclusion that strikes in both OFF and ON transistors' regions will upset one half of the time. Hence, this analysis leads to the same conclusion that half of the ion strikes will cause upset. If there is asymmetry in the starting state, e.g., all zeros, and asymmetry in the recovery preference, e.g., most cells recover to zero, and/or if an imbalance occurs due to total dose irradiation [6,7], then there may be a difference in the upset cross section for a single SRAM cell.

It is particularly significant to consider the two modes of SRAM SEU when characterizing MCU in SRAM arrays. In the mode characterized by SNCC, the range of possible MCU outcomes is fairly limited. Figure 6 shows the range of MCU outcomes from ion strikes normal to the surface. The strike on the left affects one cell and either upsets it or not. The middle strike affects two cells and causes 0, 1, or 2 upsets. Finally, the ion strike depicted on the right affects four cells and can cause 0, 1, 2, 3, or 4 upsets, depending on charge deposition and SRAM cell initial states. Note that the given layout of the SRAM cell shown in Figure 1 has the two sets of NMOSFET gates on opposite sides of the N-well, so DNCC from a normal ion strike is not likely. So, the range of cells characterized by SNCC may grow above four due to the horizontal carrier transport in Figure 6. Also, as the angle of the ion strike moves from normal to the die surface to a more grazing angle, the number of affected cells can grow, but there may be a way to bound the possible outcomes based upon the number of cells that the ion passes through. As a result, it is straightforward to correlate SEU test results to determine the relative MCU probabilities.

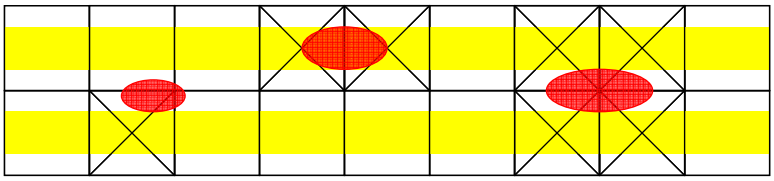


Figure 6. Example Top View of SRAM Array Showing Potential Region of Effect Characterized by Single Node Charge Collection. Figure Displays SRAM Cells as Square Boxes, N-Well Implants as Darkened Horizontal Stripes, Charge Collection Regions as Ovals, and X-ed Boxes as Affected SRAM Cells.

The number of potential outcomes when considering the SEU mode characterized by DNCC will not be as easy to predict. Figure 7 shows an example of an affected region where the initial charge from the ion strike has diffused down the N-well. In the example, each cell in the affected region has collected enough charge for DNCC characterization. Since all seven SRAM cells entered a metastable state, it is likely that each of the seven cells will recover into a state defined by its imbalance. It is important to note that this type of example could lead to a measured upset pattern of 0X000XX, which might be interpreted as errors from two separate single events. However, if the experimenter knew that the experimental conditions were in the region dominated by DNCC, then he could correctly identify this pattern as resulting from one event.

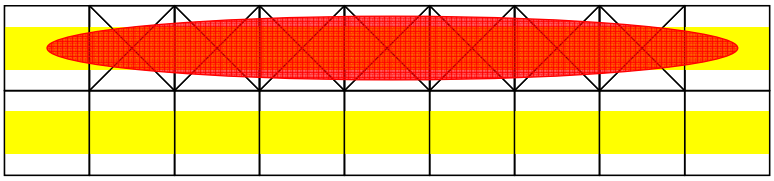


Figure 7. Example Top View of SRAM Array Showing Potential Region of Effect Characterized by Multiple Node Charge Collection.

In conclusion, a new SEU mechanism has been described that is associated with the natural metastability of an initially stable SRAM cell. Cell imbalances largely determine the recovery state following the metastable state. Understanding the SRAM SEU mode characterized by DNCC can lead to a better understanding of the MCUs observed in single event testing and to better prediction of MCU rates. In the full paper, we will also demonstrate the significance of this effect for hardened technologies using cross coupled resistors.

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