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5-Level MEMS Technology with Integrated n-MOS Electronics

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Abstract: *The Sandia SUMMiT™ technology is a 5-layer planarized silicon surface micromachining process for fabricating microelectromechanical systems (MEMS). A simple modification of the SUMMiT process flow allows for simultaneous fabrication of n-MOS devices that can be used for applications such as digital switching and on-chip charge amplification.*

Keywords: Integrated MEMS; n-MOS; silicon; micromachining.

Introduction

The Sandia SUMMiT™ fabrication process uses in-situ doped polycrystalline silicon (n-type, phosphorous doped) for both mechanical structures and electrical trace routing. The standard substrate material is lightly n-type doped (2-20 Ω-cm) silicon. An iterative process of depositing sacrificial oxide films, followed by deposition and patterning of mechanical polysilicon films is used to fabricate complex devices with 4 mechanical layers. Chemical mechanical polishing (CMP) of the interlevel sacrificial films is used to maintain planarity between the upper mechanical layers. Numerous high temperature anneals are used in the process flow to relieve residual stress in the doped polysilicon films, such that complex meshing structures (e.g., gears and latches) can be fabricated with minimal stress-induced bow. Finally, a "release" etch is performed in which concentrated hydrofluoric acid is used to remove the sacrificial oxide films, resulting in free moving mechanical structures.

Often there exists a need to incorporate electronics with MEMS devices. This may be required for charge detection applications, where decreased signal-noise ratios from parasitic capacitance would make the use of off-chip electronics difficult or impossible. Other applications include the use of digital electronics for switching or detecting the position of individual mechanical elements. However, integration of electronics with the SUMMiT™ process is complicated by the long, high temperature anneals that are required for stress relief. Also complicating this integration is the requirement that the integrated electronics must survive exposure to aggressive release chemistries.

Previously, integrated process flows were developed that involved fabricating the MEMS structures first, within a trench that was etched out of the substrate [1]. The trench was capped after the MEMS structures had been fabricated, and then complimentary metal oxide semiconductor (CMOS) devices were fabricated outside of the trench. This process is lengthy and complicated, as MEMS and CMOS processes must be completed sequentially, in their entirety. Addition steps must be included for creating the trench as well encapsulating the mechanical devices within the trench. Finally, modifications to the CMOS process must be made such that these devices will survive the aggressive release etch chemistry.

A greatly simplified process has been developed in which n-MOS transistors are fabricated using solid state diffusion of dopant from the MEMS polysilicon to create source and drain regions. Initial attempts to fabricate these n-MOS transistors yielded functional devices with reproducible characteristics [2]. However, further testing showed vulnerability to the release chemistry. Subsequent process modifications now yield robust transistors that easily tolerate the release etch. This process requires only one additional lithographic mask level beyond standard SUMMiT™ processing; the additional mask is used to define the transistor gates. Although limited to n-type devices only, this integrated approach still has numerous applications where full CMOS is not needed.

Fabrication

SUMMiT™ is typically fabricated on n-type Si <100>. Because the polysilicon that is used for mechanical layers as well as electrical traces is in-situ doped with phosphorous, n-type substrates are used so that junctions will not form where the polysilicon/substrate contacts are made. MEMS structures are also typically fabricated on a dielectric stack comprised of low-stress (Si rich) silicon nitride on top of a thermally grown oxide film. The first mask level is a cut through this dielectric stack, to provide electrical contact to the substrate. Mechanical layers are all fabricated with n-type doped polysilicon, which is deposited on sacrificial silicon dioxide films. SUMMiT™ includes 4 mechanical layers on top of one heavily doped layer that is used as a ground plane. Figure 1 shows an example of a complex gear train that was fabricated in the SUMMiT™ technology

To fabricate n-MOS devices, a p-type substrate is used instead of n-type. Thus, wherever a nitride cut occurs such that doped polysilicon contacts the substrate, a p-n junction will be created. However, before the junctions are defined with etched patterns in the dielectric stack, a gate oxide is grown on the substrate. The same type of doped polysilicon that is used for electrical traces is used to create the gate electrode. After the gate is defined, the MEMS

isolation dielectric stack is deposited using low pressure chemical vapor deposition (LPCVD). The one additional photolithographic mask level required for this integrated process is used to define the transistor gate. Contact to both the gate and the source/drain regions is accomplished using the nitride cut mask, already included in the SUMMiT™ flow. A cross-section of a transistor, fabricated through the first mechanical polysilicon deposition, is shown in Figure 2. This image was created from a CAD layout of the device.

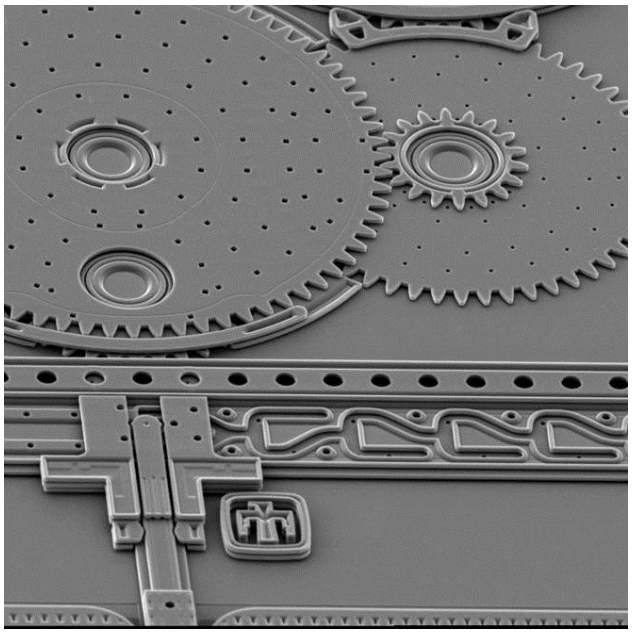

Figure 1. SEM image of 5-Layer MEMS gear train fabricated in SUMMiT

The profile and position of the p-n junctions are determined by subsequent thermal processing. Throughout the SUMMiT™ process flow, multiple high temperature furnace anneals are performed to relieve residual stress in the mechanical polysilicon layers. Without such anneals, stress induced bow would make the fabrication of complex, meshing structures impossible. However, such anneals are

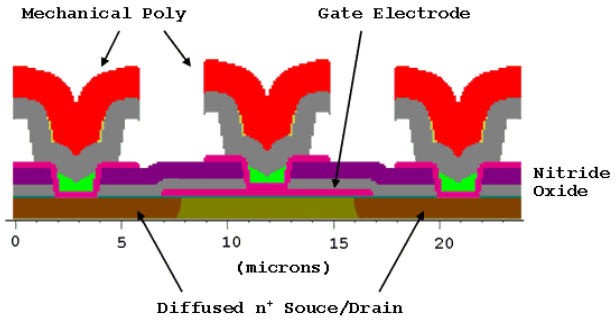

Figure 2. Cross-section of transistor generated from AutoCAD drawing.

also incompatible with typical CMOS processing, as the added thermal budget would have undesirable effects on junction profiles, and non-refractory metals such as AlCu or Cu are typically used for device interconnects. In this integrated process, the high temperature anneals are used to drive dopant (phosphorous) from the mechanical polysilicon into the device region, under the gate. Gate dimensions and spacing between the gate and source/drain regions must be carefully selected such that the source and drain underlap the gate, but adequate distance between these regions remains so that short channel effects do not occur. For device interconnect, the remaining polysilicon layers can be used. These layers can either remain encased within the sacrificial oxide, or they can be air-bridged as necessary.

Results and Discussion

Because of the substantial thermal budget required to relieve stress in the mechanical poly layers, phosphorous from the n-type polysilicon diffuses extensively. Figure 3 shows simulated and measured diffusion lengths as a function of the number of proprietary anneal cycles. After the full compliment of anneals required for SUMMiT™ fabrication, the dopant diffusion length is about 6 µm. Therefore a sufficiently long transistor must be fabricated to prevent short channel effects or punch through caused by merging of the source and drain regions. Transistor I-V curves for various channel lengths are shown in Figure 4, where short channel effects and merging of the source and drain regions are seen with gate length less than 8 µm (all devices have a 3 µm separation between gate and source/drain). Although such large devices are not amenable to fabricating highly integrated circuits, they are ideally suited for applications where size is not a significant constraint.

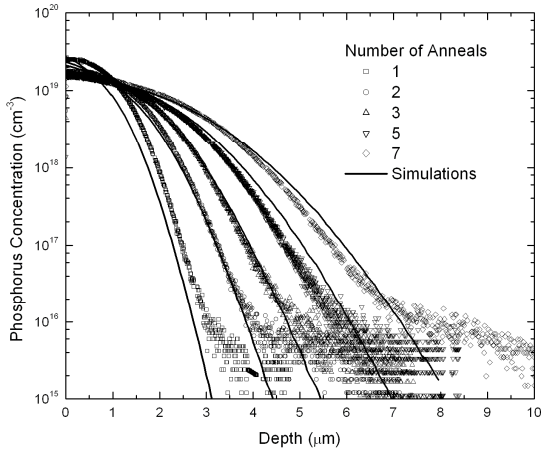

Figure 3. Simulated and measured diffusion length as a function of anneal cycles

An example of such an application is the switching fabric used to control individually addressable mirrors in a large

mirror array [3]. A row-column addressing scheme has been implemented such that under each mirror electrode, transistors for the row and column are connected in series. When the gates of both the row and column transistor are charged, current can flow through both transistors, thereby charging the mirror electrode. A third transistor can be included to discharge the actuation electrode. Once the

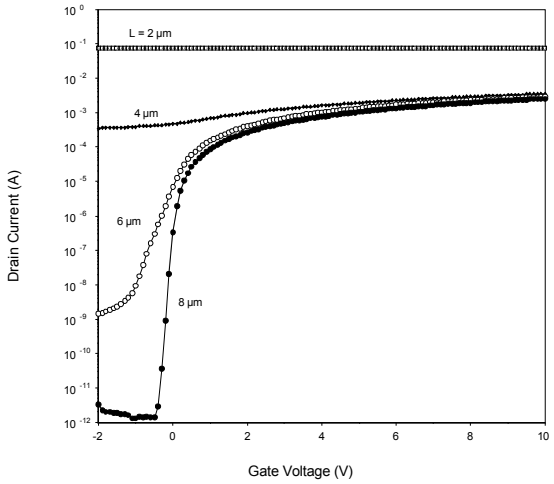

Figure 4. Drain current vs. gate voltage for various channel lengths

electrode is charged, electrostatic force pulls the mirror toward the electrode. Flexural beams are used to support the mirrors and provide restoring force. The layout for a single cell, as well as an optical micrograph of the array, are shown in Figure 5. Each mirror is 150 µm x 150 µm. Without the transistor based switching scheme, an array comprised of n x n mirrors would require n^2 wires for simple actuation (one axis of motion). For more complex control, such as east-west tilting, $2n^2$ leads would be needed. With row-column addressing, the number of wires needed to control the array becomes 2n for simple piston motion. In the example shown in Figure 5, actuation of a 1024 mirror array (32x32) can be accomplished with 66 leads (includes wires for V_{DD} and ground), rather than the 1026 leads required without the switching transistors, thus greatly simplifying the requirements for packaging the device. Reset transistors, although included in the design, were not required for actuation.

For this mirror application, psuedo-analog piston motion is achieved by controlling how much charge is applied to a given electrode per unit time. The mechanical structure acts an integrator. This pulse width modulation control approach requires that the transistors and supporting circuitry operate at frequencies much higher than the mechanical resonance frequency. An 11-stage ring oscillator was fabricated and tested to evaluate transistor switching speed. Measured ring oscillator performance and SPICE simulation results as a function of drain voltage are shown in Figure 6. Transistor speeds between about 28 and 42 MHz were obtained at drain voltages that ranged from 10 to 30 V. These speeds are many orders of magnitude greater than the natural frequency of the mirrors. Thus, transistor speed is sufficient for this demanding application and should prove suitable for most MEMS control approaches.

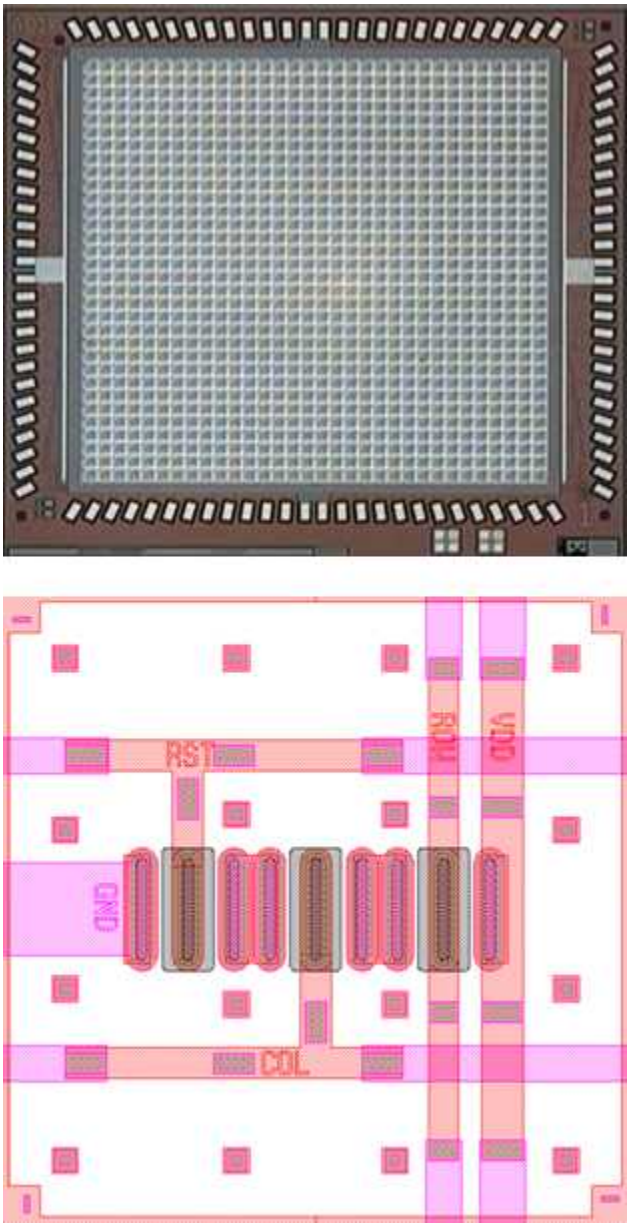

Figure 5. Optical micrograph of mirror array (above) and layout of switching fabric beneath each mirror.

Because the intended application for this integrated transistor is for on-board electronics mated to MEMS devices, maximum operating voltage and current must be considered. Devices fabricated in SUMMiT^{TM} may be electrostatically driven, which requires high voltage with

virtually no current, or thermal actuators may be used, which require low voltage and higher current (up to hundreds of milliamps). To achieve high current performance, the transistors must be sufficiently wide; current carrying capacity scales with transistor width. Therefore, layout of high current transistors simply becomes a footprint consideration. For high voltage transistors, performance degradation due to hot carrier effects must be considered. Figure 7 shows an I-V curve for transistors operating at a drain voltage of 40V, with gate voltages as high as 40V. These curves indicate a well behaved transistor response. Indeed, extended operation of these transistors at 40V in a ring oscillator showed no deleterious effects. Many electrostatically operated MEMS devices, including the piston mirrors shown in Figure 5, can be actuated at 40V or less. For applications that require greater voltages for actuation, higher voltage designs have been fabricated.

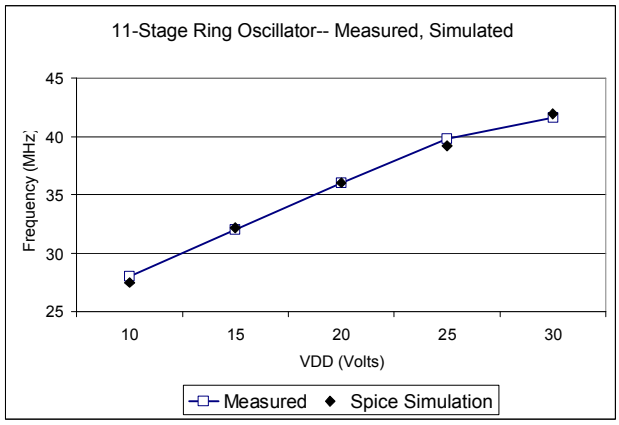

Figure 6. Ring oscillator performance, measured and simulated.

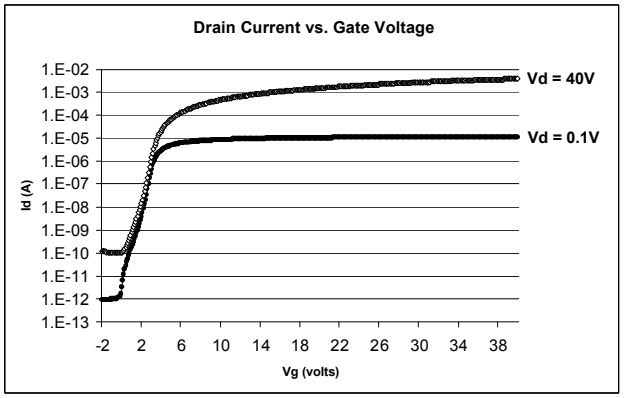

Figure 7. High voltage transistor performance

Conclusions

A simple process flow modification, which includes the addition of a single photolithographic mask layer, has been used to fabricate n-MOS transistors in the SUMMiT^{TM} MEMS technology. These robust transistors, which survive both extended stress relief anneals and the aggressive release chemistry, perform well at speeds as high as 40 MHz and operating voltages over 40V. These performance characteristics are ideally suited for control or position sensing of MEMS devices. SUMMiT^{TM} is the most complex surface micromachining technology available; with the addition of on-chip electronics, the application space for silicon MEMS has been greatly expanded.

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