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# MOSFET based Nanoelectronics

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Transport Group Team Members

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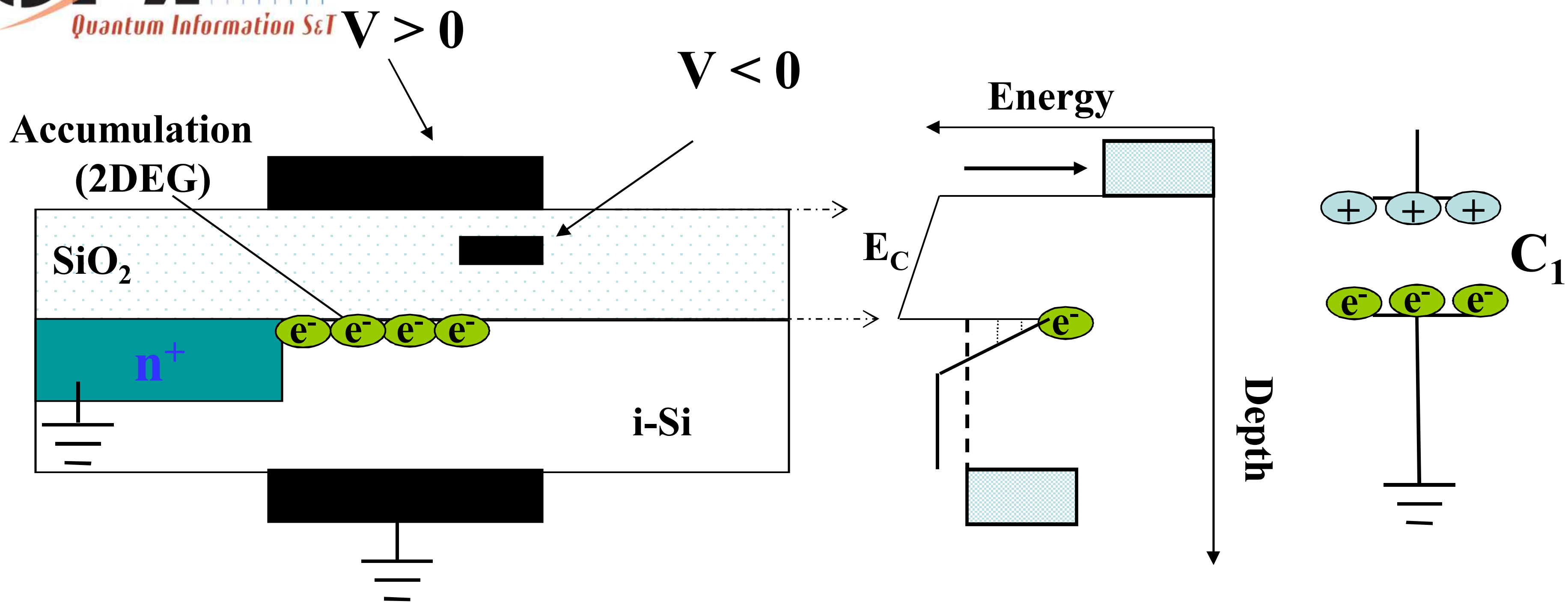
*Sandia is a multiprogram laboratory operated by Sandia Corp., a Lockheed Martin Co., for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.*

- Background: double quantum dot qubit
- Progress
  - MOSFETS
  - Valley splitting
  - Nanolithography and initial transport

# Two Dimensional Electrons

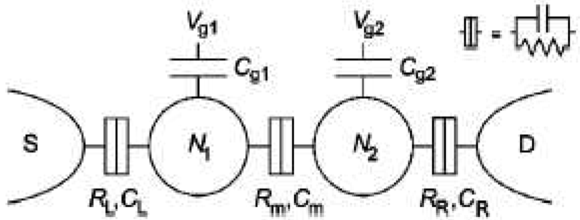



- A positive bias on the top gate draws electrons from the doped region towards the plate
- The insulator provides a barrier on to which the electrons accumulate
- Charge in the 2DEG goes as:

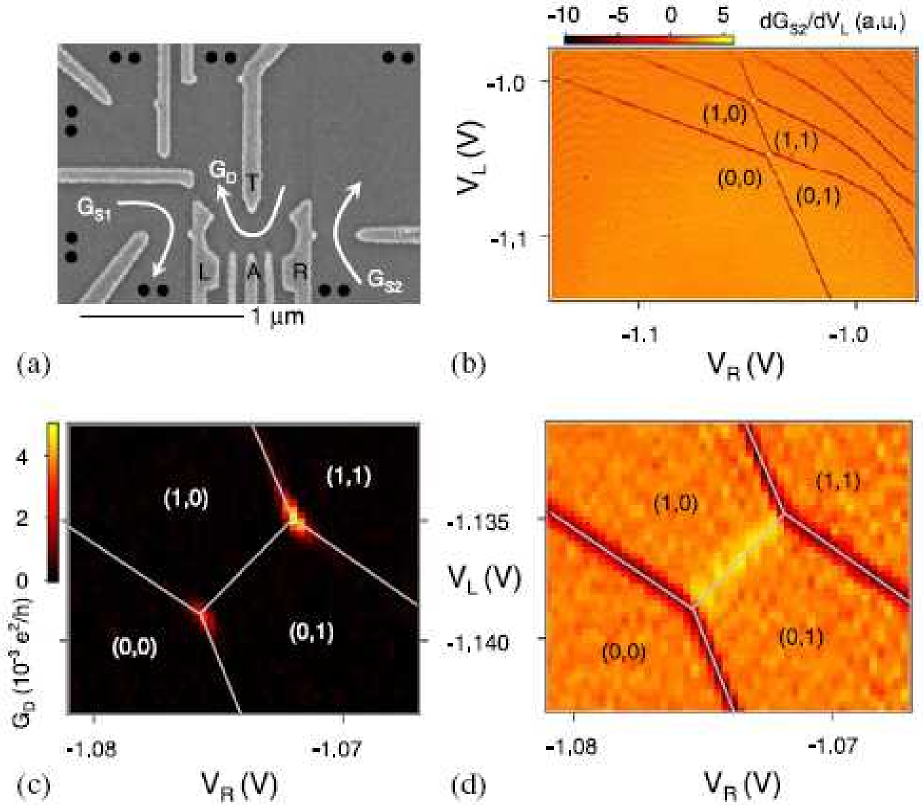
$$n_{2D} = \frac{C_1' \times \left(V_G - V_t\right)}{q}$$

# Double Quantum Dot

**V. d. Wiel, et al., Rev. Mod. Phys., vol. 75, 1 (2003)**




**Petta, et al., Phys. Rev. Lett, vol. 93, 186802 (2004)**




- Charging diagram shifts with increased coupling
- Diagram can be used to determine electron occupation
- Voltage pulses can carry you through different occupations

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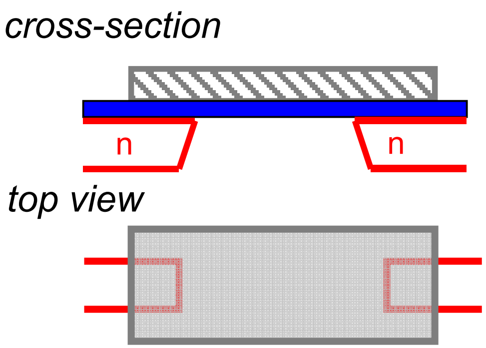
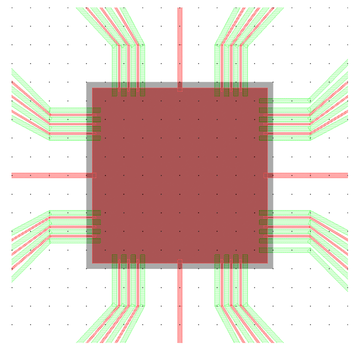
# Overview of Silicon Qubit

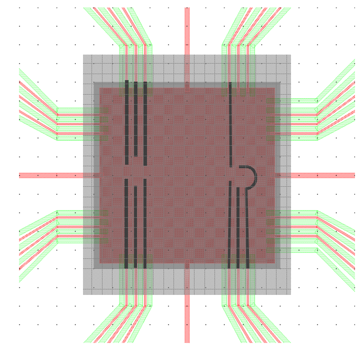
## MOSFET



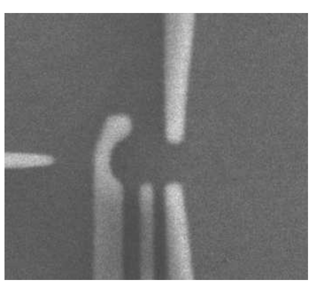

## MOSFET modified for nanolithography



## Nanolithography

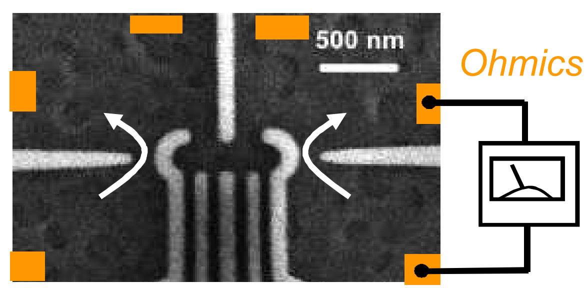


## Many-electron quantum dot



Coulomb blockade,
Coulomb diamonds

## Double dot with integrated detectors




Stabiltiy diagrams,
electrometer coupling

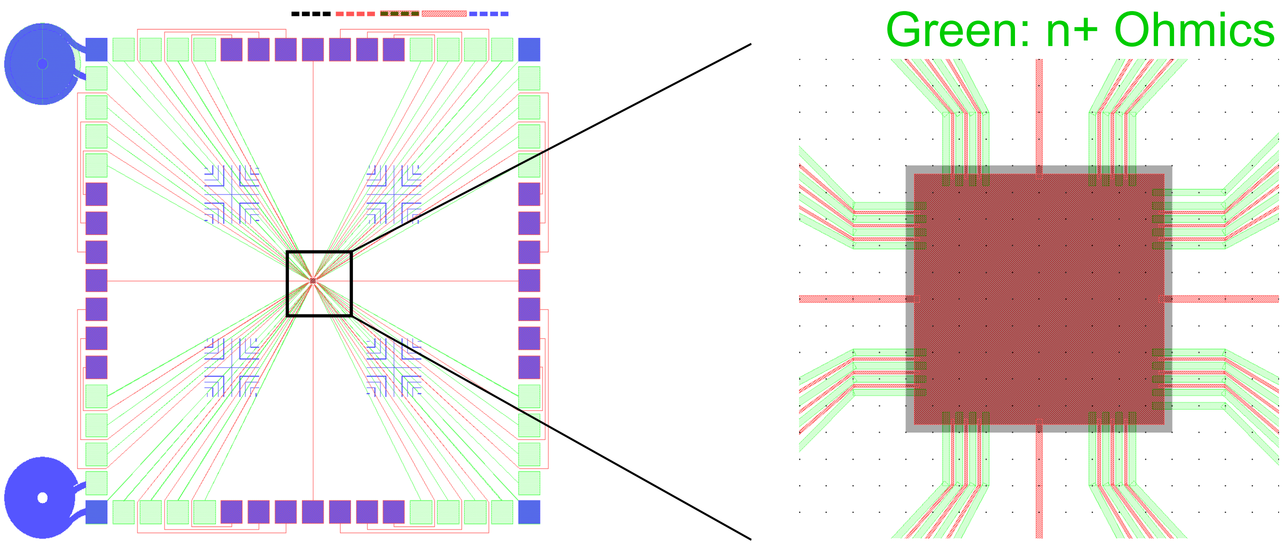
## Control of quantum states

Coupling between dots,
Moving electrons,
Pulsing techniques,
Fast measurements

- Background: double quantum dot qubit
- Progress
  - MOSFETS
  - Valley splitting
  - Nanolithography and initial transport

# MOSFET Fabrication

Red: n+ polysilicon (100$\mu m^2$)
Green: n+ Ohmics



- Metal oxide semiconductor field effect transistors (MOSFETs) will be fabricated in Sandia's silicon facility (MDL)
- Structures were initially a modified version of the widely available CINT discovery platform for electronics
- Minimum features size = 180 nm.  Nanolithography is outside MDL.

# MOSFET Process Flow

- Silicon Wafer
- Gate Oxide Grown
- Source-Drain Lines Implanted
- Poly-silicon Deposited, Doped, and Patterned
- Contacts and Vias Formed

**High Resistivity Silicon Wafer**

# MOSFET Process Flow

- Resistivity Silicon Wafer
- Gate Oxide Grown
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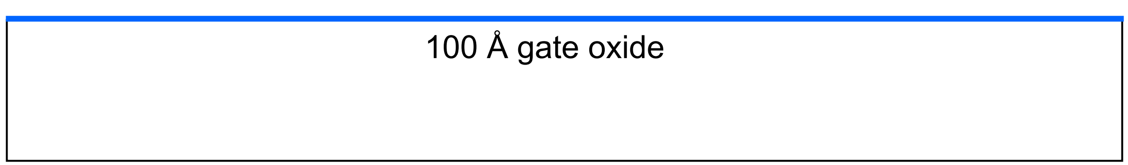

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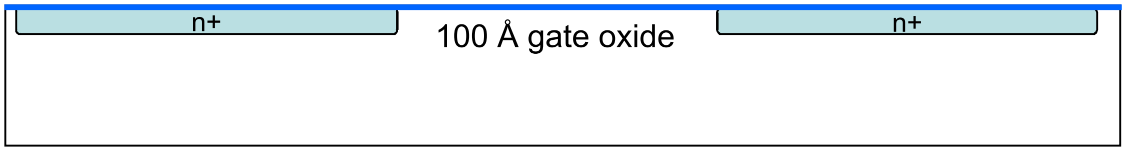

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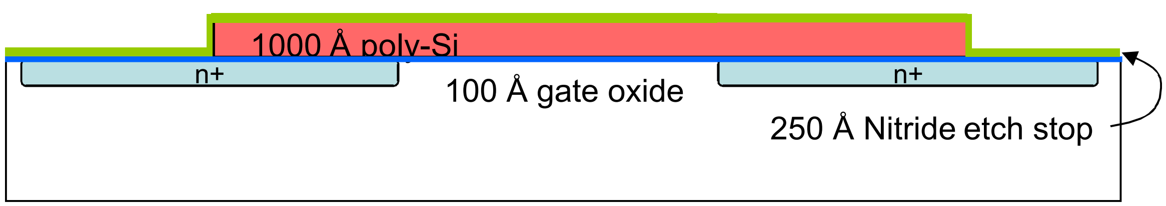

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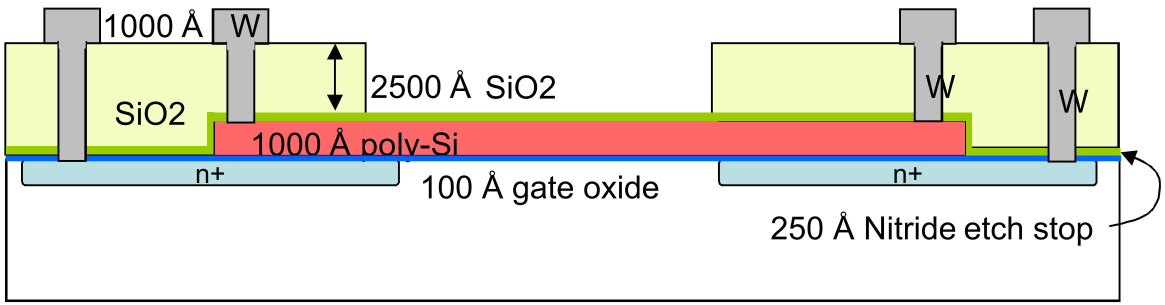
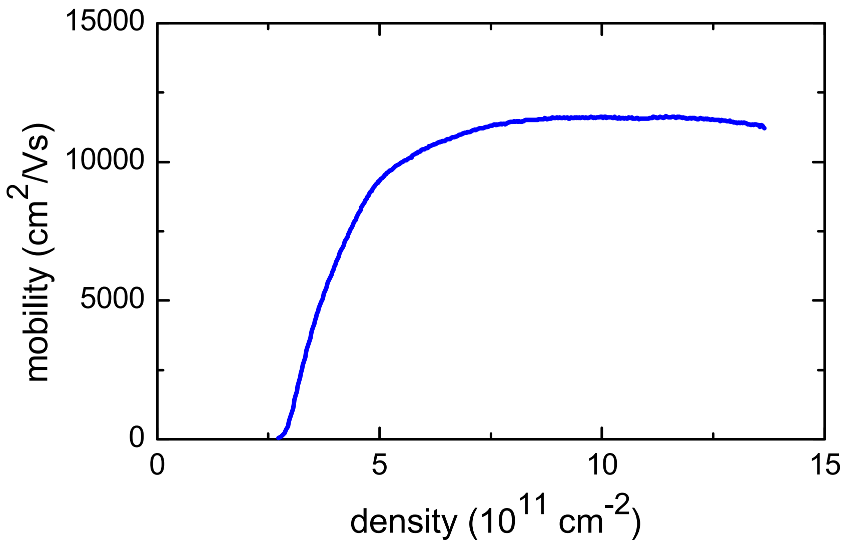



- Process characterization used to optimize critical steps (e.g. C-V on gate oxide)
- Many devices can be fabricated on the 6” wafers

# Initial 2DEG Transport

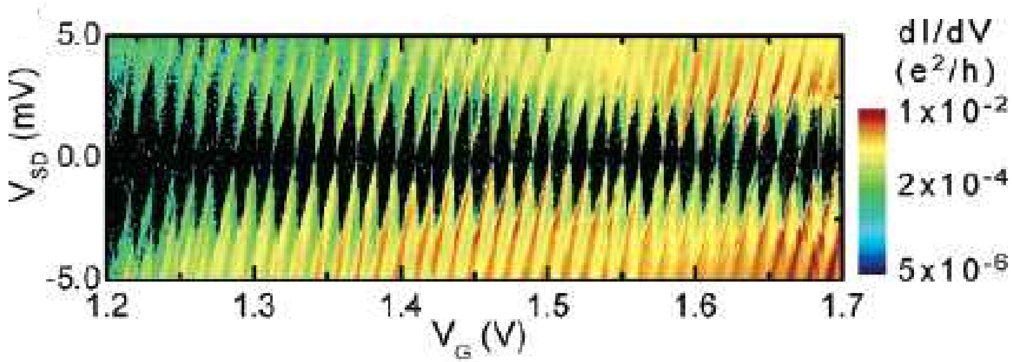
- Ongoing MOSFET developement
  - Polysilicon can transition to insulator at low T.
  - Contact resistance is very high (300 kΩ) for narrow implant lines.
  - Oxide induced 2DEG
- Iteration to improve mobility will occur throughout the project

***MOSFET from Si substrate***




**Quantum dot properties can be observed in MOSFETS**

Recent examples of quantum dot transport (e.g. Coulomb diamonds from CQCT) have been published.




*Angus, et al. Nanoletters* ***7****, 2051 (2007)*

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## Slide 13

**m3** add image from Angus paper

image of poly sheet and MOSFET

point out low T challenges

motivate alternate structures (even though Angus results suggest role of mobility is reduced)
mplilly, 1/6/2008

- Background: double quantum dot qubit
- Progress
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  - Valley splitting
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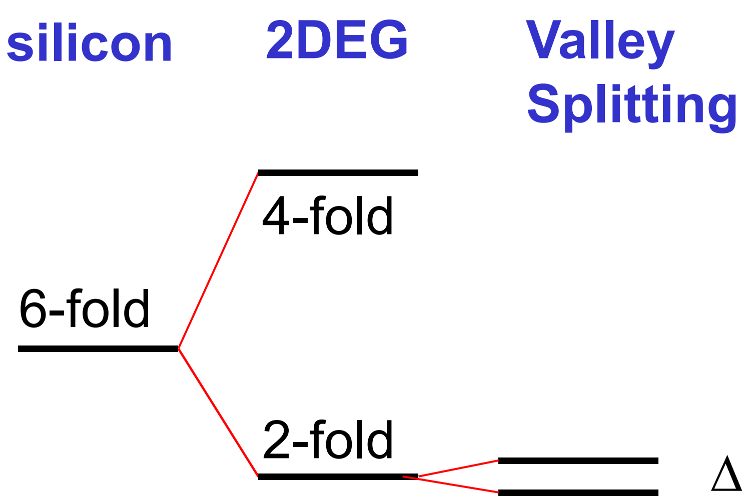
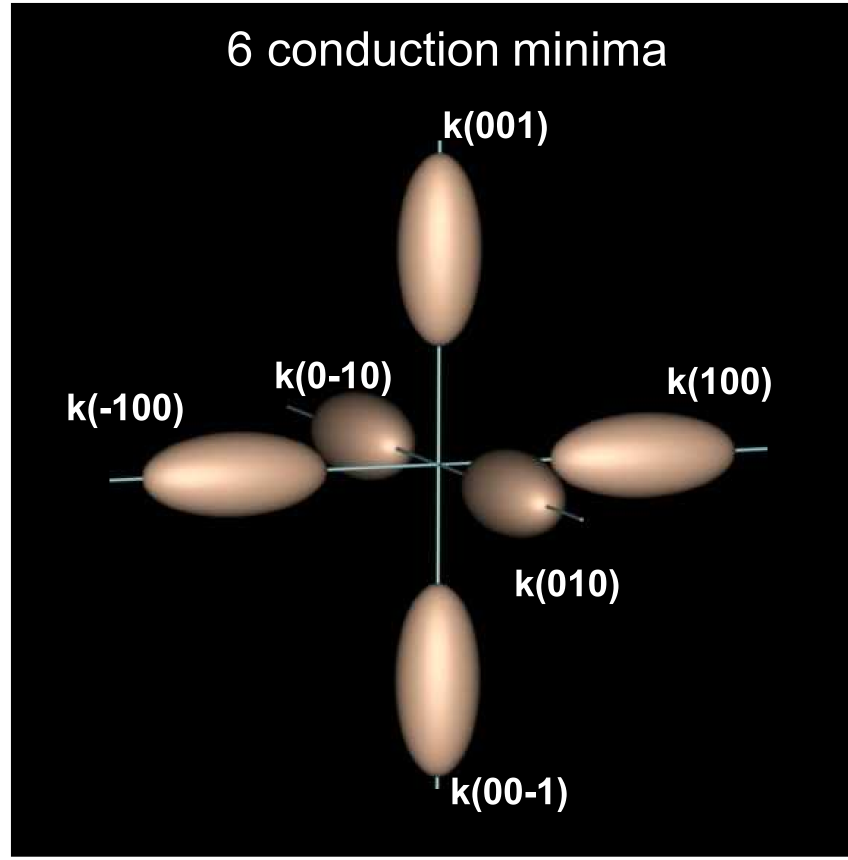
# Valley Splitting in a Si-MOSFET

Valley degeneracy → decoherence



# Energy scales in magnetic fields

Cyclotron

$$E_c = \hbar\omega_c = \hbar\frac{eB_\perp}{m^*}$$

=7.17K/T

Zeeman

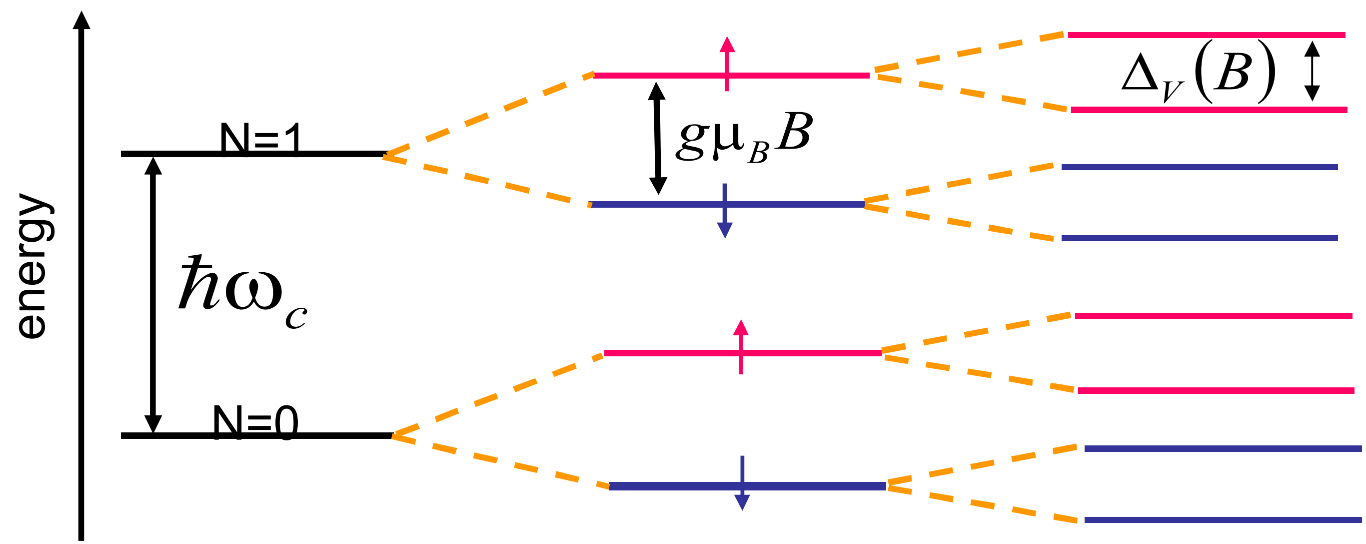
$$E_{Zeeman} = g\mu_B B_{total}$$

=1.36K/T

Valley splitting

$$E_V = \Delta_V(B)$$

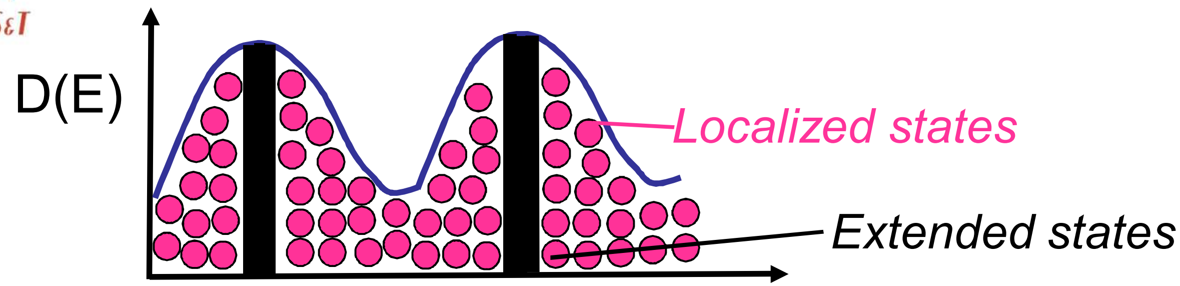
= ?

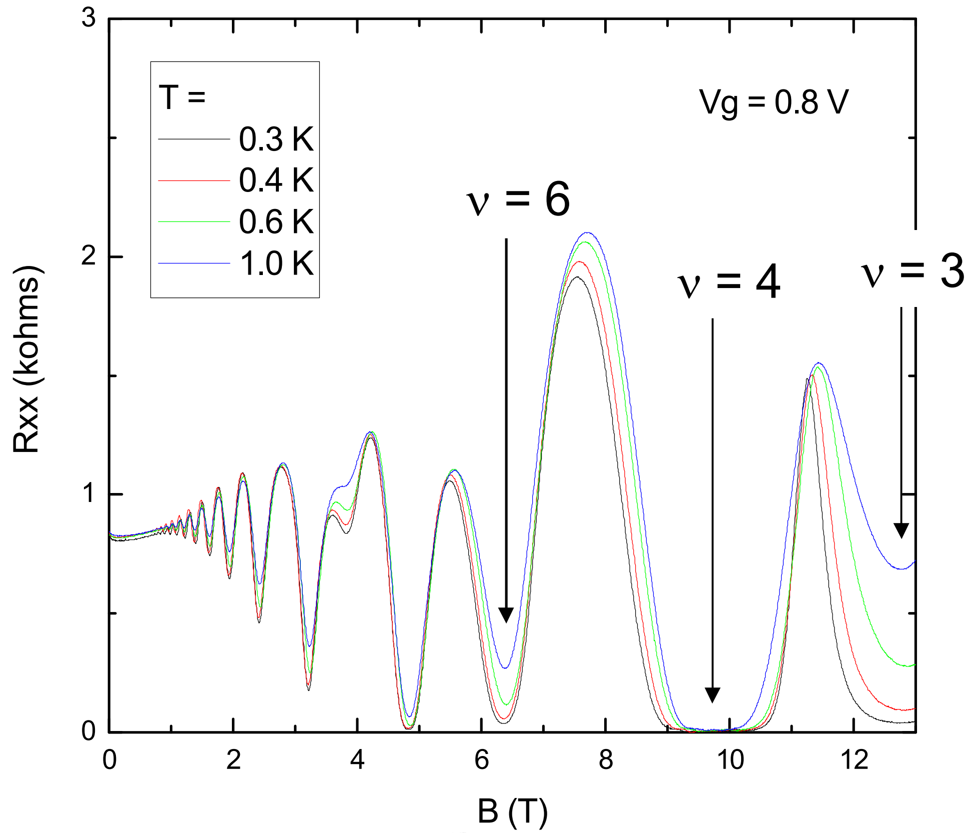



$$E = \hbar\omega_c\left(N+\frac{1}{2}\right) \pm \frac{1}{2}g^*\mu_B B \pm \Delta_V(B)$$

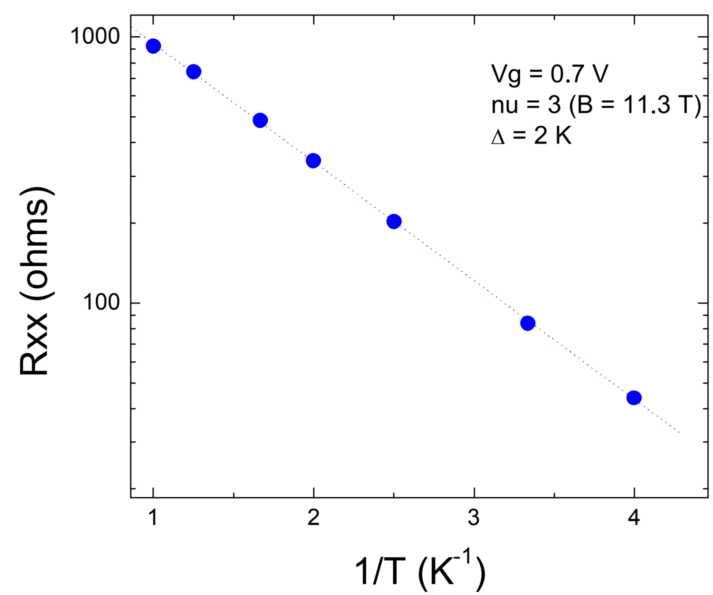
(*Assumed g* =2 and m* =0.19m$_o$*)

# Activation of Quantum Hall States



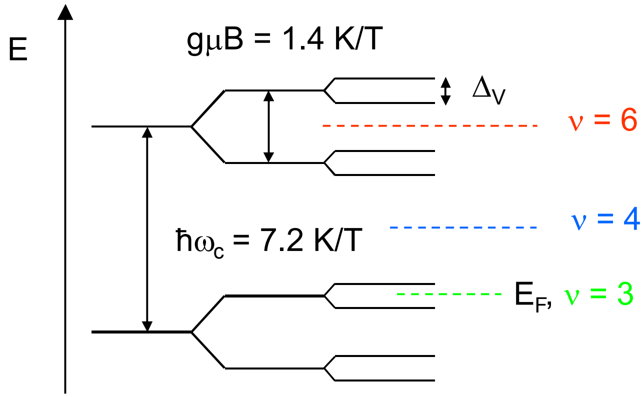




$R_{xx} \sim R_o \exp(-\Delta/2k_BT)$

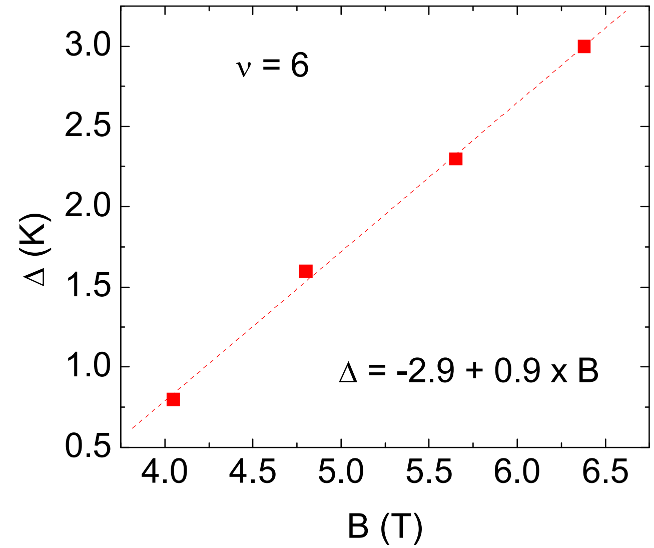



Made activation measurements at ν = 6,4,3 for various Vg's

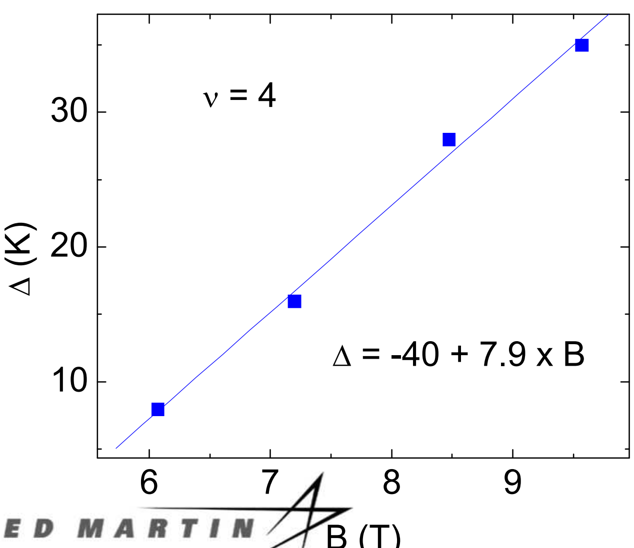
# Activation Measurement Summary



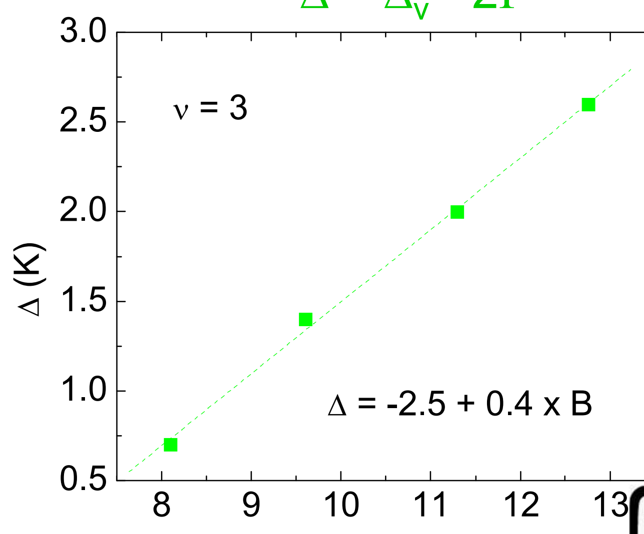

$\Delta = g\mu B - \Delta_v - 2\Gamma$




$\Delta = \hbar\omega_c - g\mu B - \Delta_v - 2\Gamma$



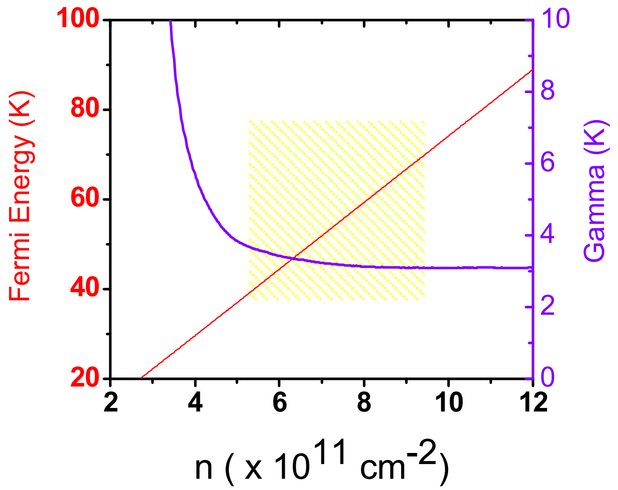

$\Delta = \Delta_v - 2\Gamma$



# LL Broadening ($\Gamma$) – Low B-field estimate

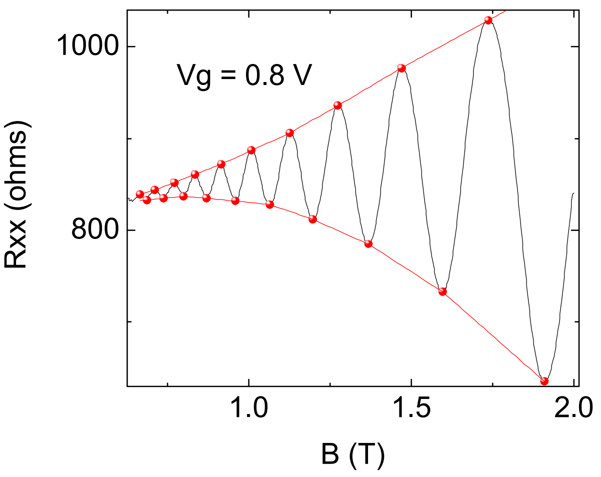
1. B = 0 mobility:

$\Gamma = \hbar/2\tau \sim 3.3$ K



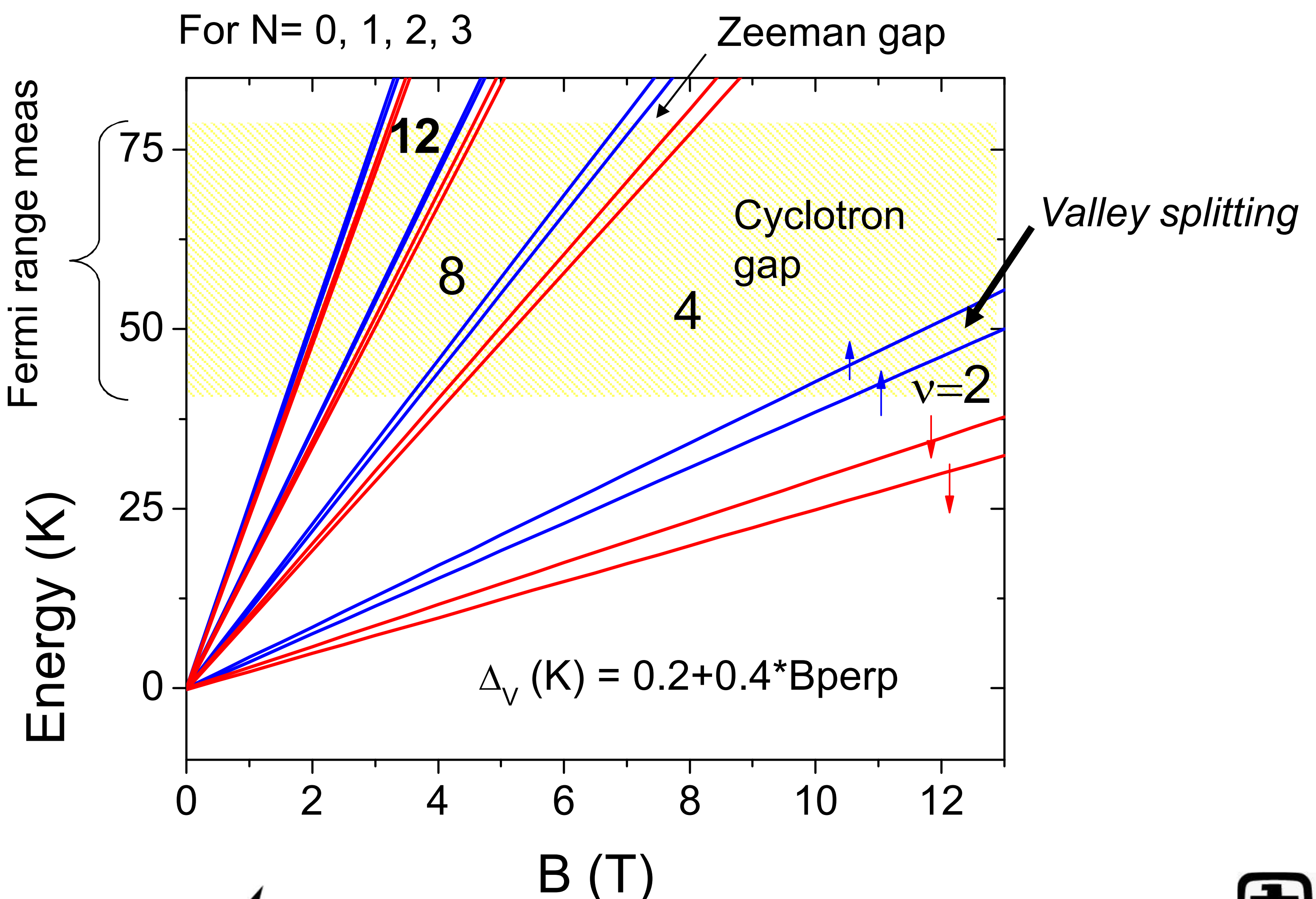

2. From low B-field SdH data:

$\Gamma = 4.5 – 4.7$ K




- Disorder effects are larger than valley splitting
- Depending on which disorder is used, the extrapolation to B = 0 is impacted.

# Energy Spectrum



# Summary

Thermal activation measurements of the valley splitting yields:

$$\Delta_V = 0.2 + 0.4B_{perp}$$

Device characteristics:

| | |
|---|---|
| Peak mobility | ~10,000 $cm^2/Vs$ |
| mean free path | ~200nm |
| phase coherence length | 1$\mu$m (peak) |
| Disorder ( $\Gamma$ ) | 3-4K |

Future Experiments:

- RF resonance measurement
- Quantum point contacts (magnetic depopulation)

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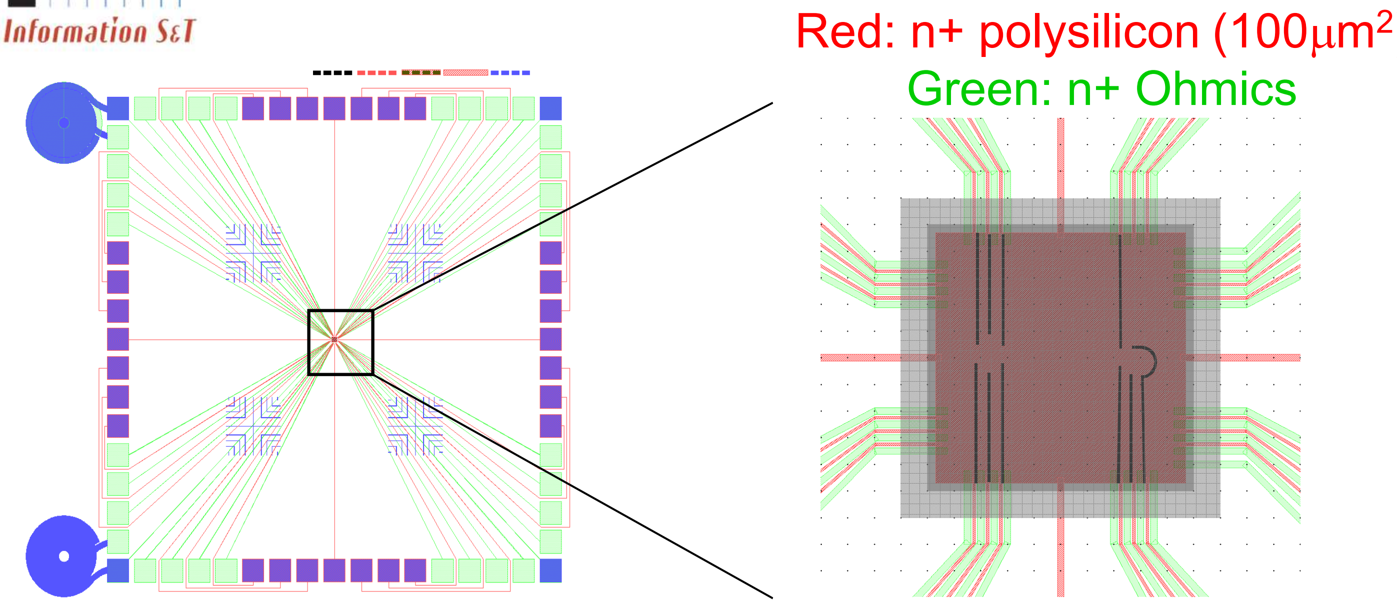
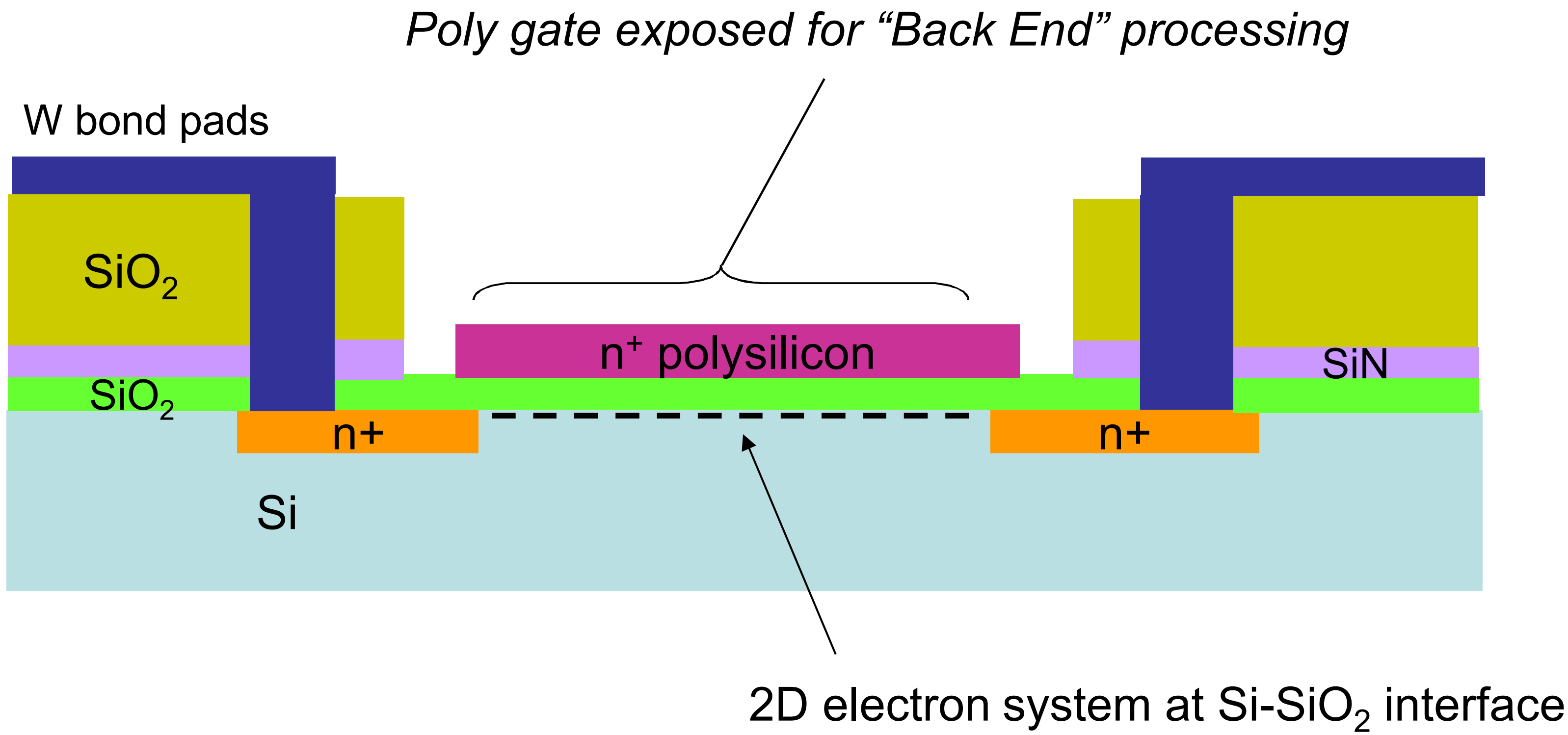
# Nanolithography



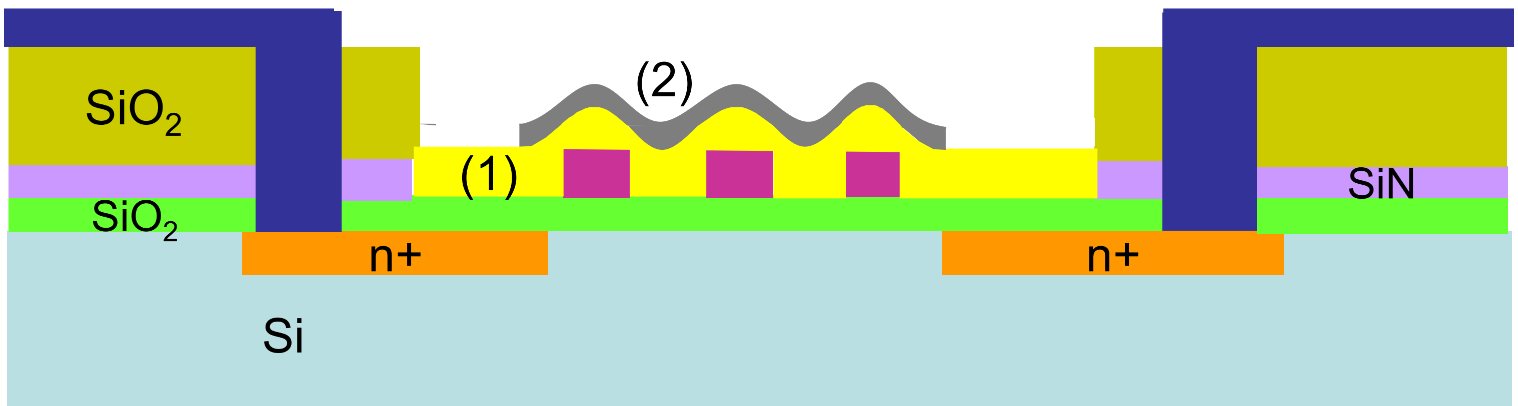

- Electron beam lithography defines 50 nm features (negative resist process)
- Polysilicon etching, insulator deposition using ALD and a second top gate are deposited in the uFab or CINT cleanrooms.
- Variations of desired structure can occur rapidly

# "Front End" Processing: Si MOSFETs



# "Back End" nanolithography

1. Ebeam lithography
2. polysilicon patterning with plasma etch
3. Deposit 2nd dielectric: atomic layer deposition of Al2O3
4. Top gate: sputtered Al or ALD metal

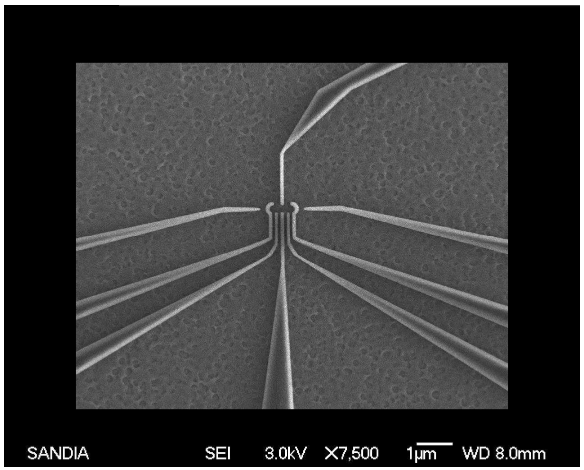



Issues: electrical characteristic of ALD, new etch out of MDL for poly

- C-V used to characterize and optimize ALD process
- Other oxides can be substituted if necessary
- Working to incorporate EBL in silicon fab – allows better control

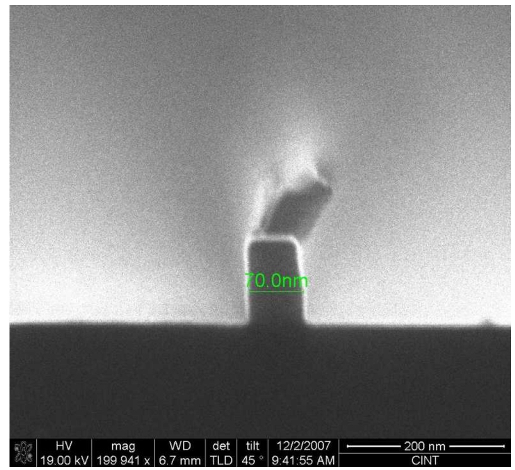
# Nanolithography Progress

### Electron beam lithography



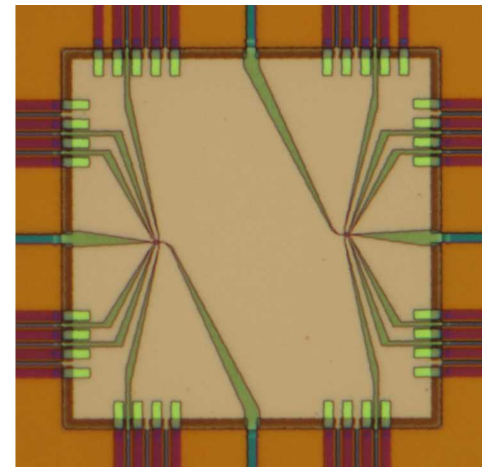

- State-of-the-art Ebeam writer capabilities
- NEB negative ebeam resist

### Plasma etching




- MESA/uFab bromine plasma etch of polysilicon
- 70 nm poly linewidth after EBL and etching.

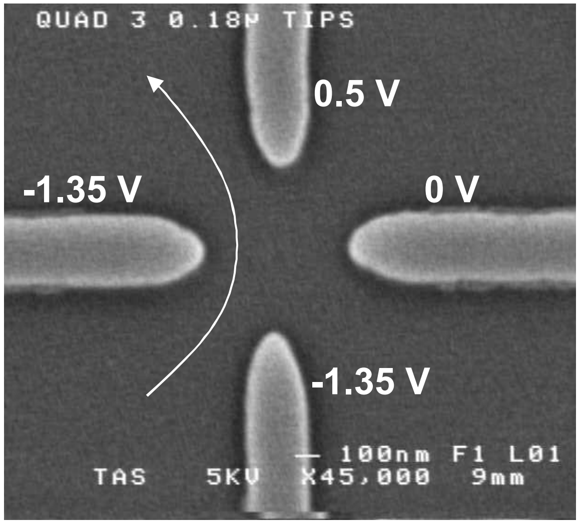
### Status

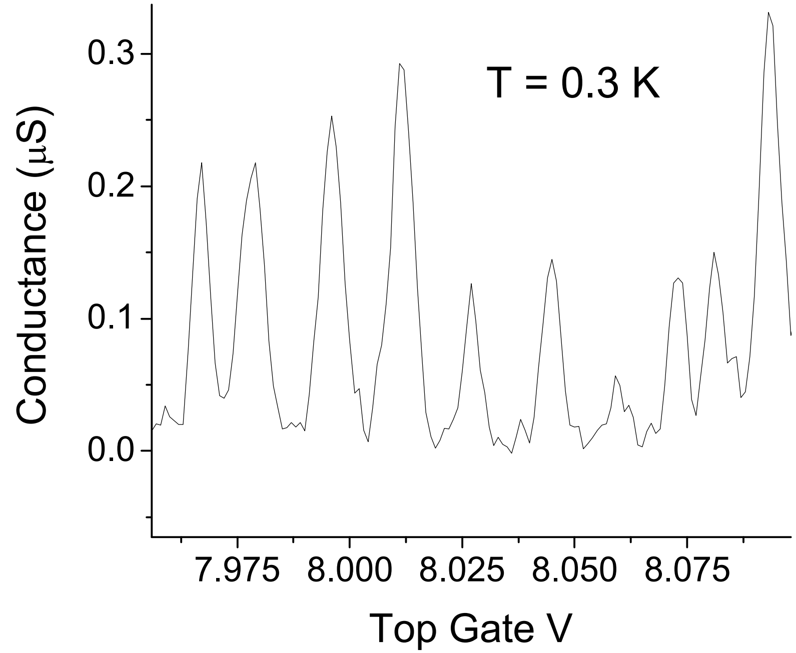


- Point contact, dot and double dot experiments will use double dot gates
- Two full devices finished. Measurements starting ...

# Coulomb Blockade

*Cross operated as quantum point contact*




- Cross structure is operated as a point contact
- This early device has silicon fab processing only (180 nm features)
- Quantum dot behavior occurs near complete pinch-off

# Silicon Qubit Summary

- Highlights
  - Surface accumulation mode approach complements existing efforts
    - Possible benefits over other approaches & experimental platform to better study surface effects, “dopant free” devices & single dopant-surface coupling
  - Integration with Si CMOS line
    - Experimental platform integrating custom cryogenic CMOS with single electron devices (i.e., heating tests & fast or low noise sense)
- Progress
  - MOSFETs fabricated for this work have relatively high mobility and can be used for both gated nanostructures and donor structures
  - Valley splitting is present for the 2DEG, and is expected to be larger for nanostructures
  - Nanolithography for making point contacts and dots is underway.
    - Transport on very large structures shows complicated blockade
    - We anticipate significant improvements for ebeam defined dots.