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MOSFET based Nanoelectronics

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Transport Group Team Members

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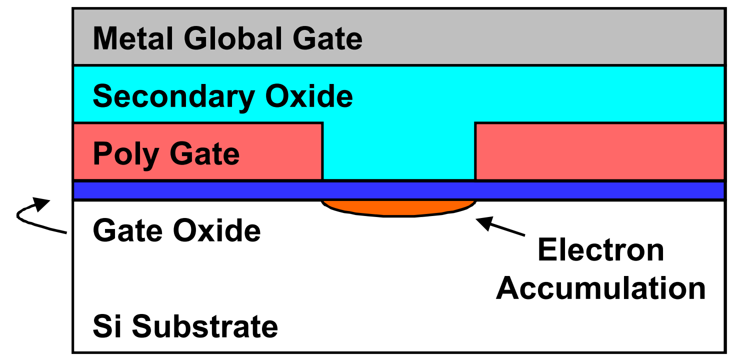
Sandia is a multiprogram laboratory operated by Sandia Corp., a Lockheed Martin Co., for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

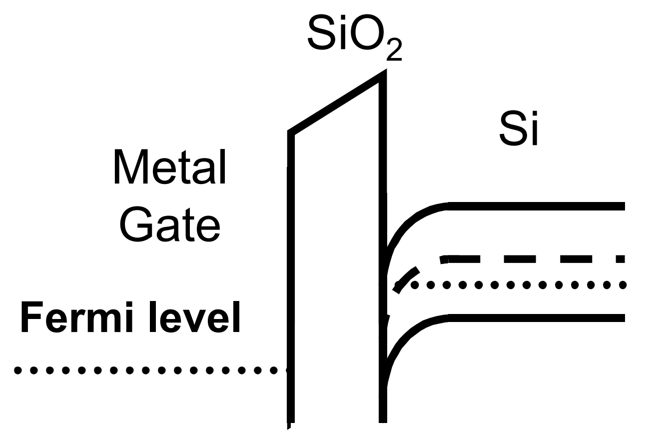
- Background: double quantum dot qubit
- Progress
  - MOSFETS
  - Valley splitting
  - Quantum point contacts and quantum dots

MOS Double Top Gate for Nanoelectronics



Advantages Si Quantum Dot Spin Qubits:

- Low spin-orbit coupling
- High percentage Si^{28} reduces nuclear spin coupling

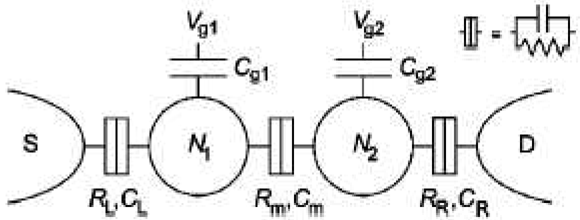


Advantages of the MOS System:

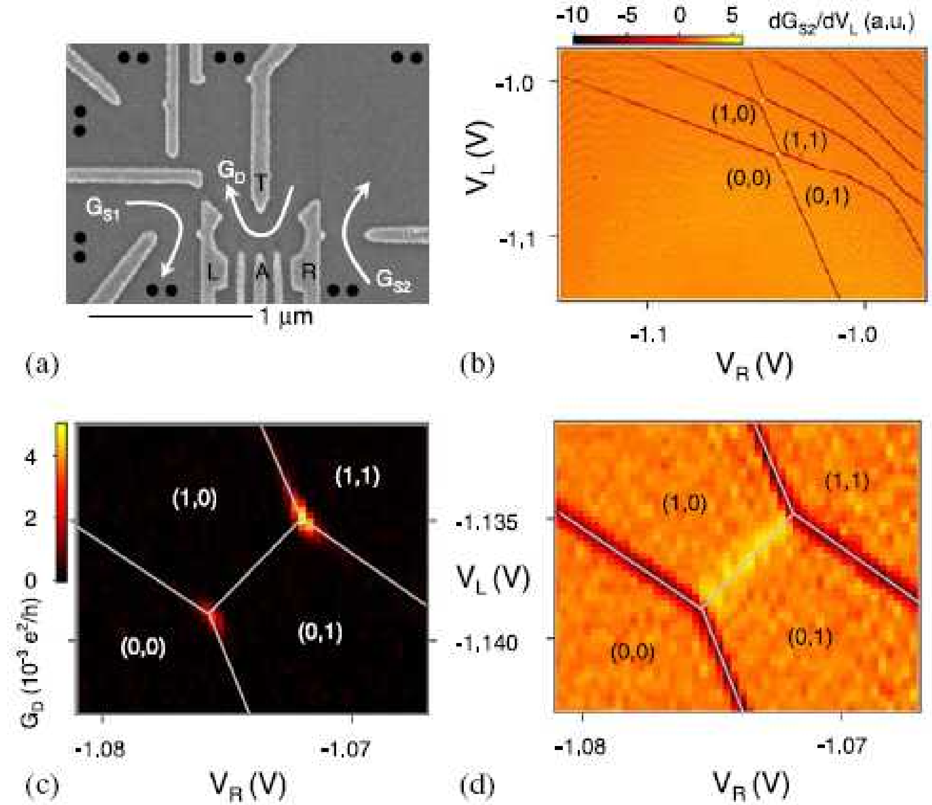
- Scaling advantage due to gate proximity to electrons
- No dopants required for transport
- Readily CMOS compatible

Double Quantum Dot

V. d. Wiel, et al., Rev. Mod. Phys., vol. 75, 1 (2003)



Petta, et al., Phys. Rev. Lett, vol. 93, 186802 (2004)



- Charging diagram shifts with increased coupling
- Diagram can be used to determine electron occupation
- Voltage pulses can carry you through different occupations

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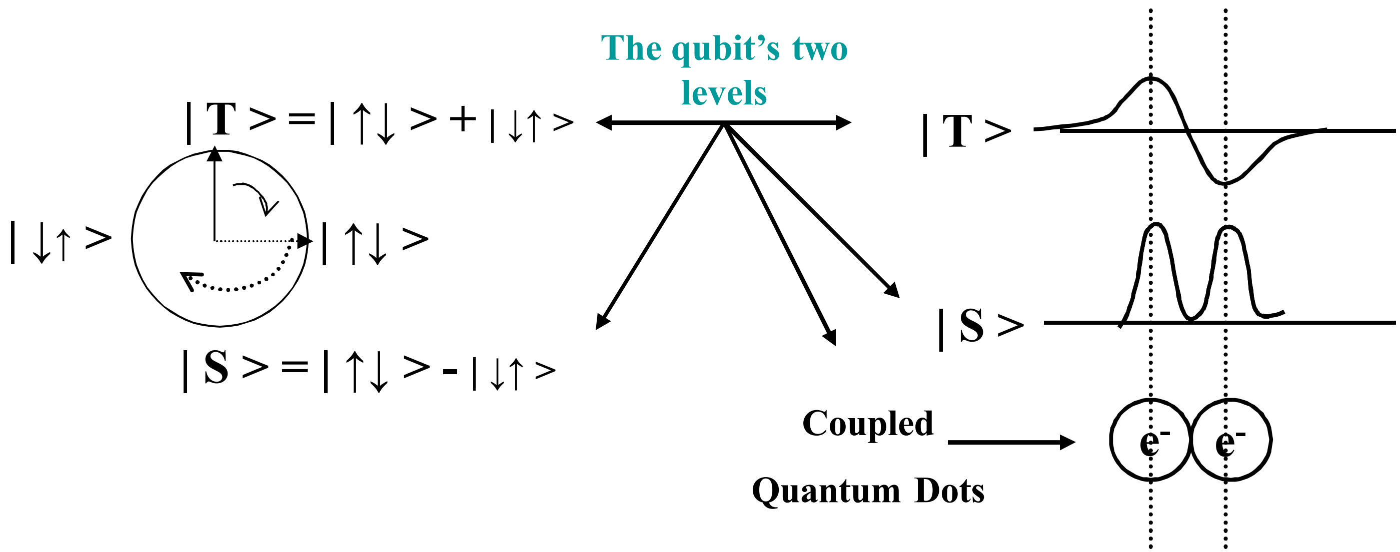
Two Electron DQD Wavefunctions

Spin Wavefunction

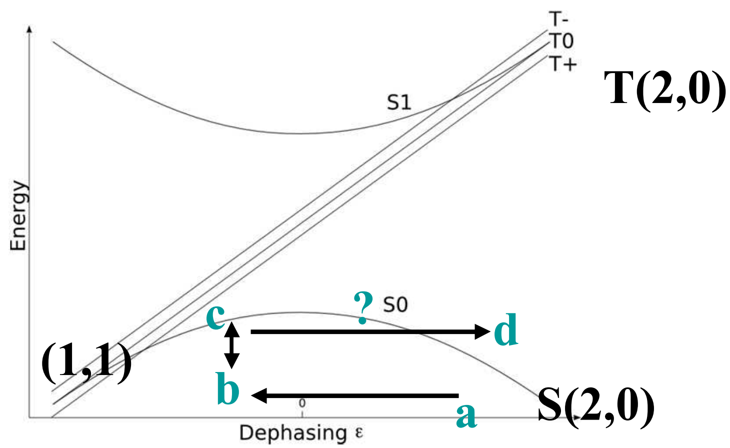
Spatial Wavefunction



- GaAs community showed a singlet-triplet DQD qubit in 2005
- The qubit basis states are (1) singlet and (2) triplet state of the DQD
  - Magnetic field splits the two other triplets off (m = +/- 1)
- The spin configuration is sensed through its charge distribution

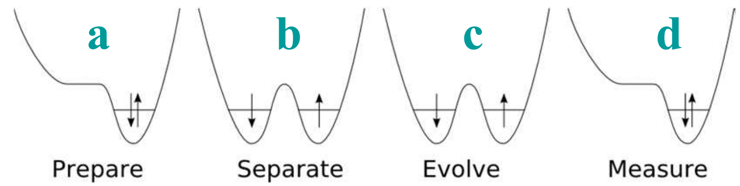
Double Quantum Dot Qubit

Energy levels

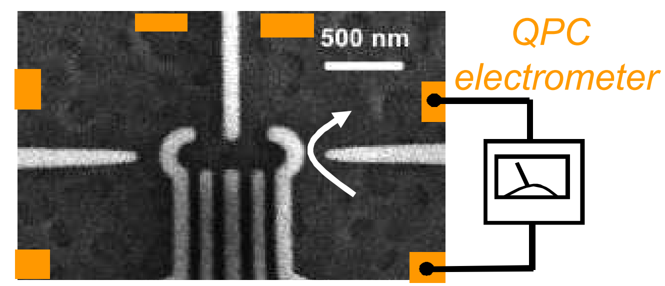


Petta et al., Science 2005

Electron sequence



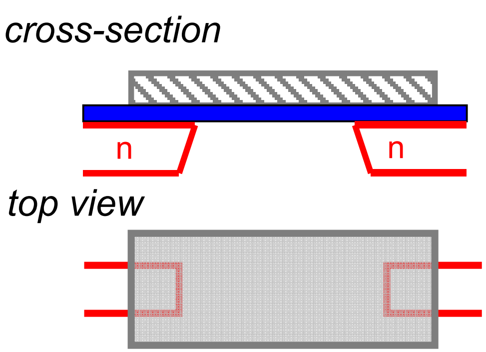
Electrometry



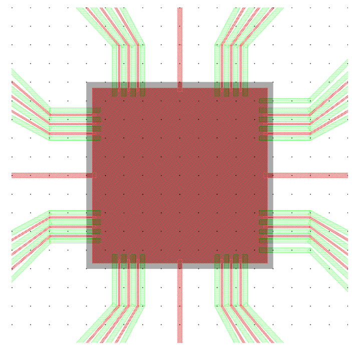
- Sequence of pulses (a => d) used to initialize and read-out
- The state is detected through single charge electrometry
- Electrometer can be QPC (shown above), Si SET or Al SET

Overview of Silicon Qubit

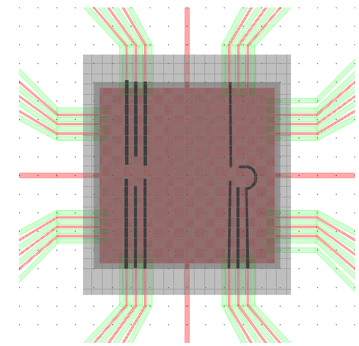
MOSFET



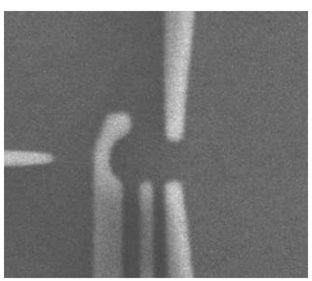
MOSFET modified for nanolithography



Nanolithography

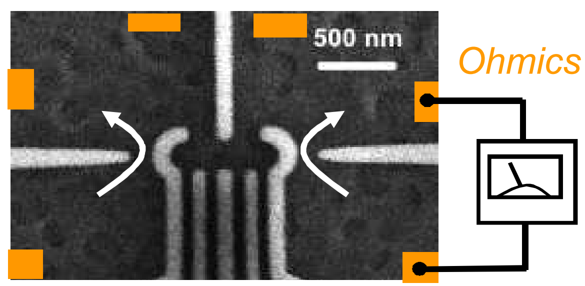


Many-electron quantum dot



Coulomb blockade,
Coulomb diamonds

Double dot with integrated detectors



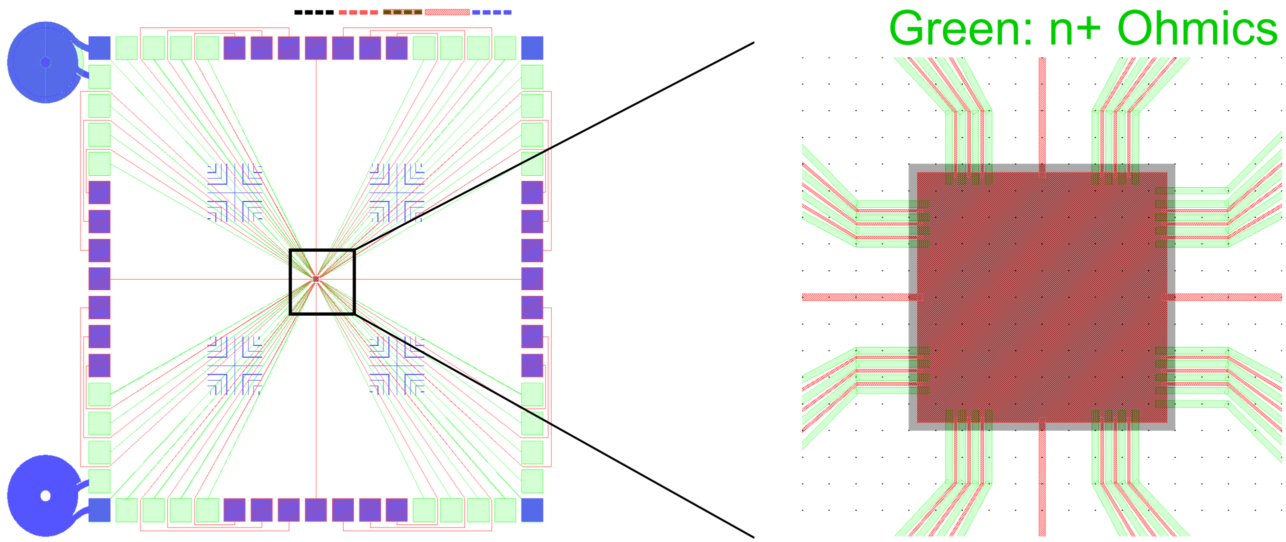
Stabiltiy diagrams,
electrometer coupling

Control of quantum states

Coupling between dots,
Moving electrons,
Pulsing techniques,
Fast measurements

- Background: double quantum dot qubit
- Progress
  - MOSFETS
  - Valley splitting
  - Quantum point contacts and quantum dots

MOSFET Fabrication: Front End



- Metal oxide semiconductor field effect transistors (MOSFETs) will be fabricated in Sandia's silicon facility (MDL)
- Minimum features size = 180 nm. Nanolithography is outside MDL.

MOSFET Process Flow

- Silicon Wafer
- Gate Oxide Grown
- Source-Drain Lines Implanted
- Poly-silicon Deposited, Doped, and Patterned
- Contacts and Vias Formed

High Resistivity Silicon Wafer

MOSFET Process Flow

- Resistivity Silicon Wafer
- Gate Oxide Grown
- Source-Drain Lines Implanted
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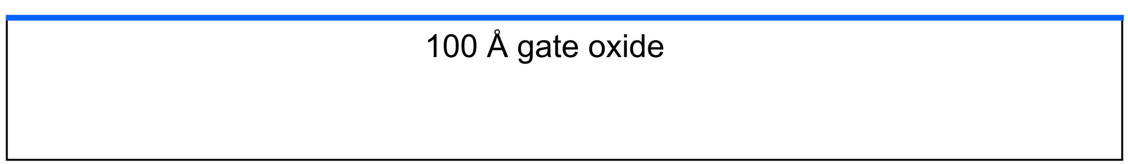

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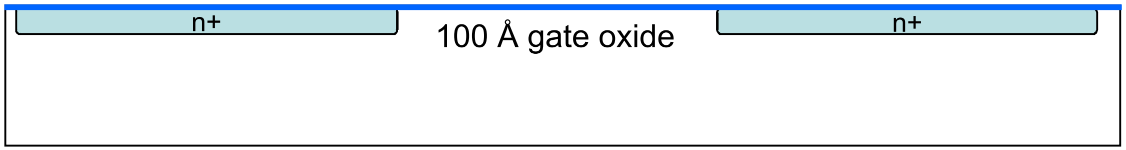

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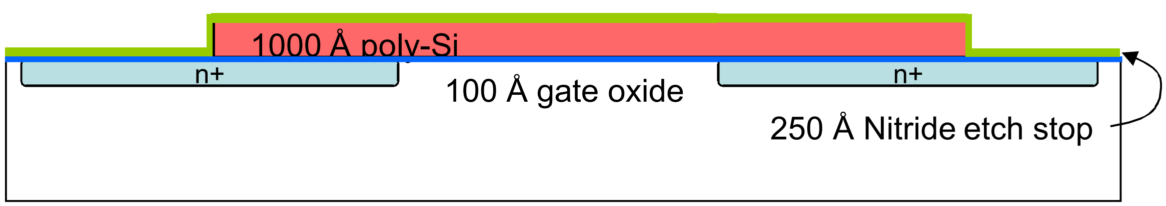

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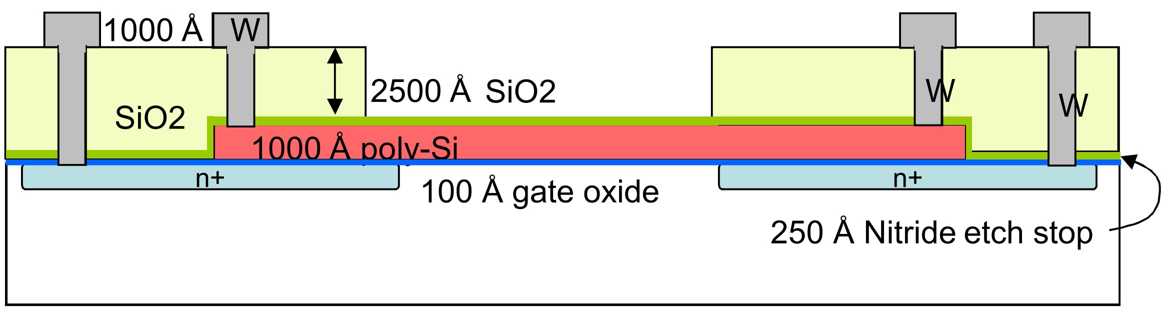


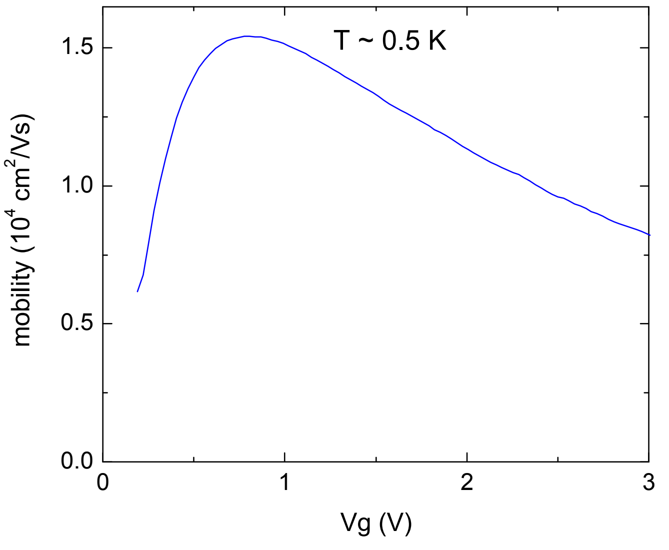
- Process characterization used to optimize critical steps (e.g. C-V on gate oxide)
- Many devices can be fabricated on the 6” wafers

m3

Initial 2DEG Transport

- Ongoing MOSFET developement
  - Polysilicon can transition to insulator at low T.
  - Contact resistance is very high (300 kΩ) for narrow implant lines.
  - Oxide induced 2DEG

MOSFET from Si substrate



Slide 15

m3 add image from Angus paper

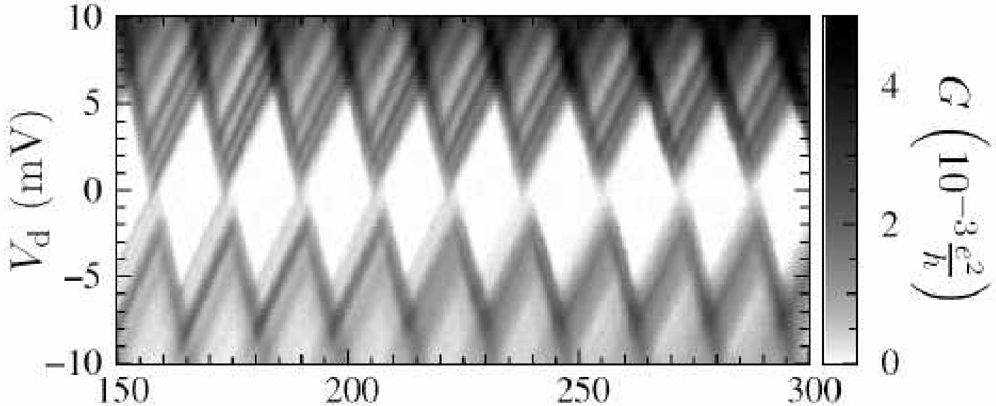
image of poly sheet and MOSFET

point out low T challenges

motivate alternate structures (even though Angus results suggest role of mobility is reduced)
mplilly, 1/6/2008

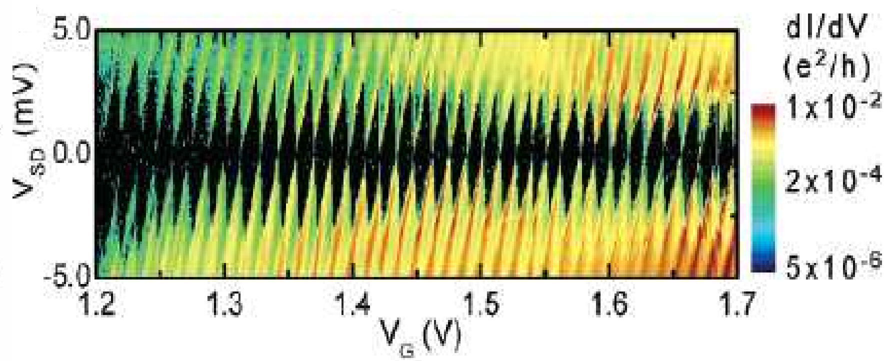
FY08/09: less damage, smaller, different relationship to interface

~ 16 nm lithographic channel [Hofheinz et al.]



V_g [mV]

~ 40x60 nm lithographic dot [Angus et al.]



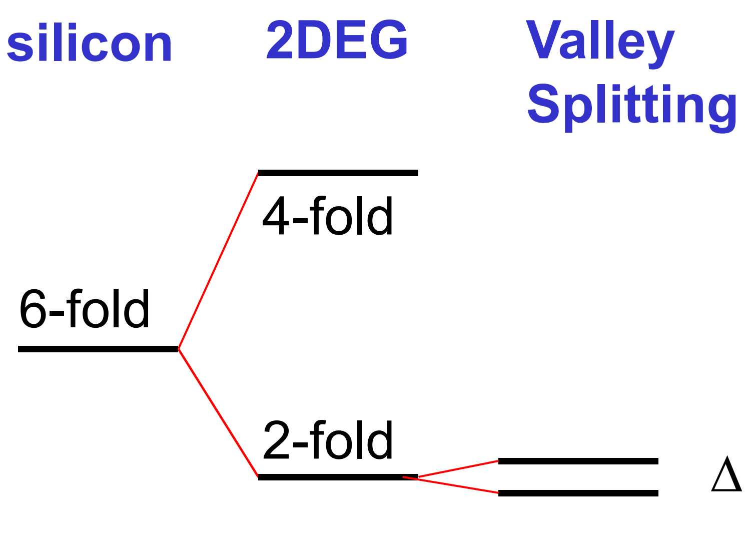
*Angus, et al. Nanoletters **7**, 2051 (2007)*

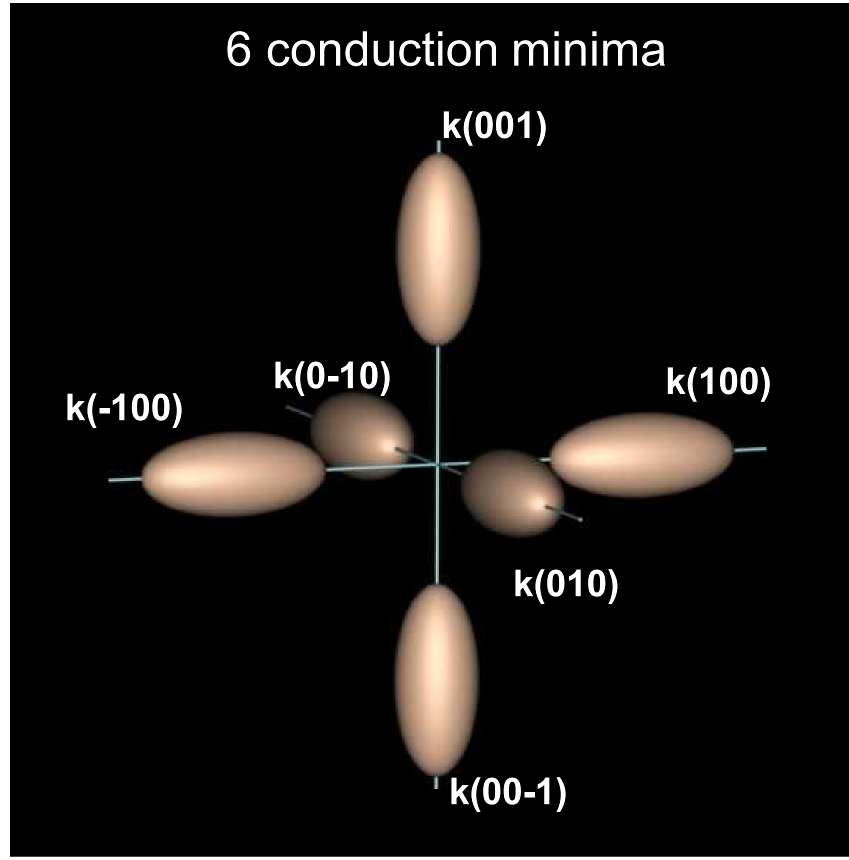
- The good news: there are many existence proofs of well defined Si quantum dots
- Usually those dots are small d<65 nm
  - EBL can reach these sizes and CMOS nodes manufactures at 45 nm!
- Future direction: shrink size, improve damage & look at derivative structures like higher mobility SiGe/sSi => <u>lots of permutations!</u>
- Right now we are using the disorder dots to learn about electrometry (e.g., measurement technique & later circuit integration)

- Background: double quantum dot qubit
- Progress
  - MOSFETS
  - Valley splitting
  - Quantum point contacts and quantum dots

Valley Splitting in a Si-MOSFET

Valley degeneracy → decoherence





Energy scales in magnetic fields

Cyclotron

$$E_c = \hbar\omega_c = \hbar\frac{eB_\perp}{m^*}$$

=7.17K/T

Zeeman

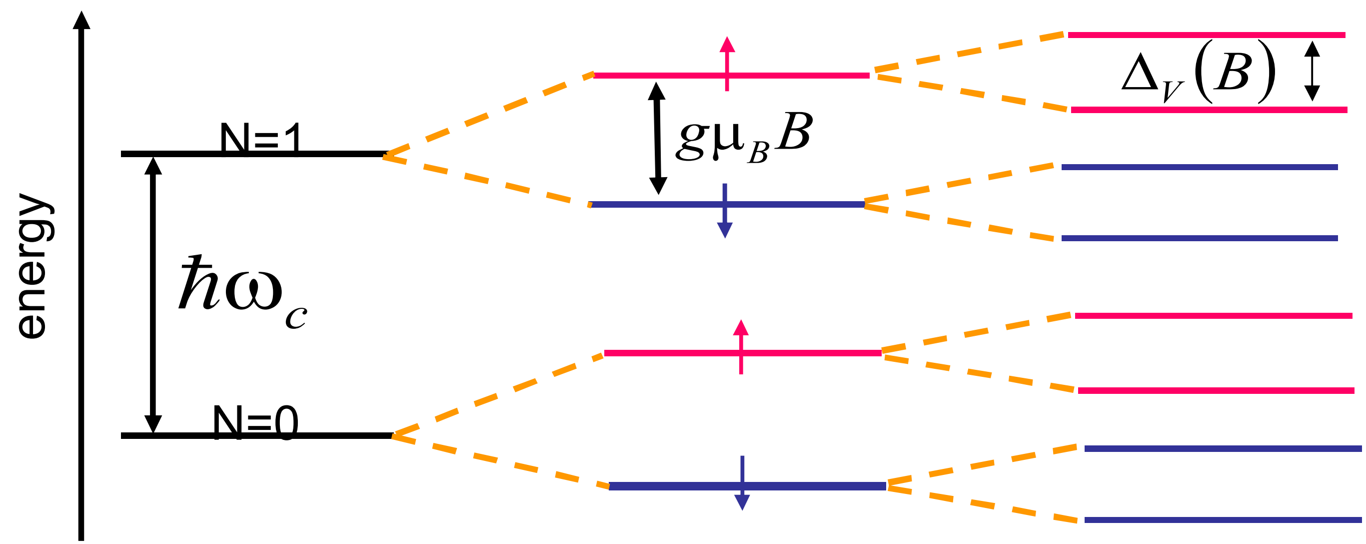
$$E_{Zeeman} = g\mu_B B_{total}$$

=1.36K/T

Valley splitting

$$E_V = \Delta_V(B)$$

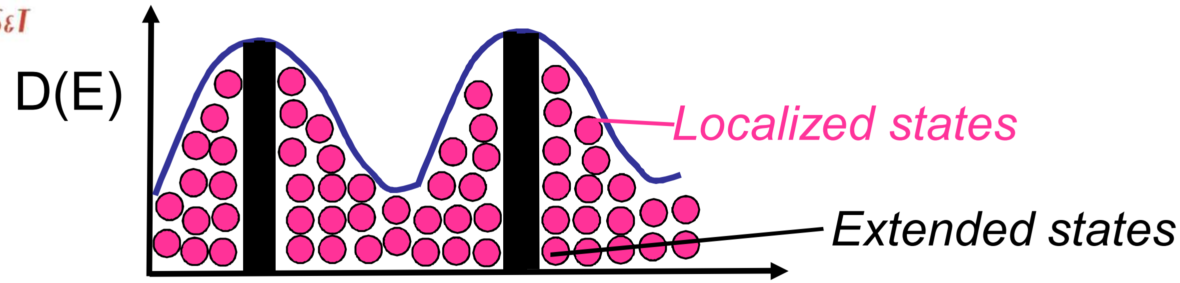
= ?

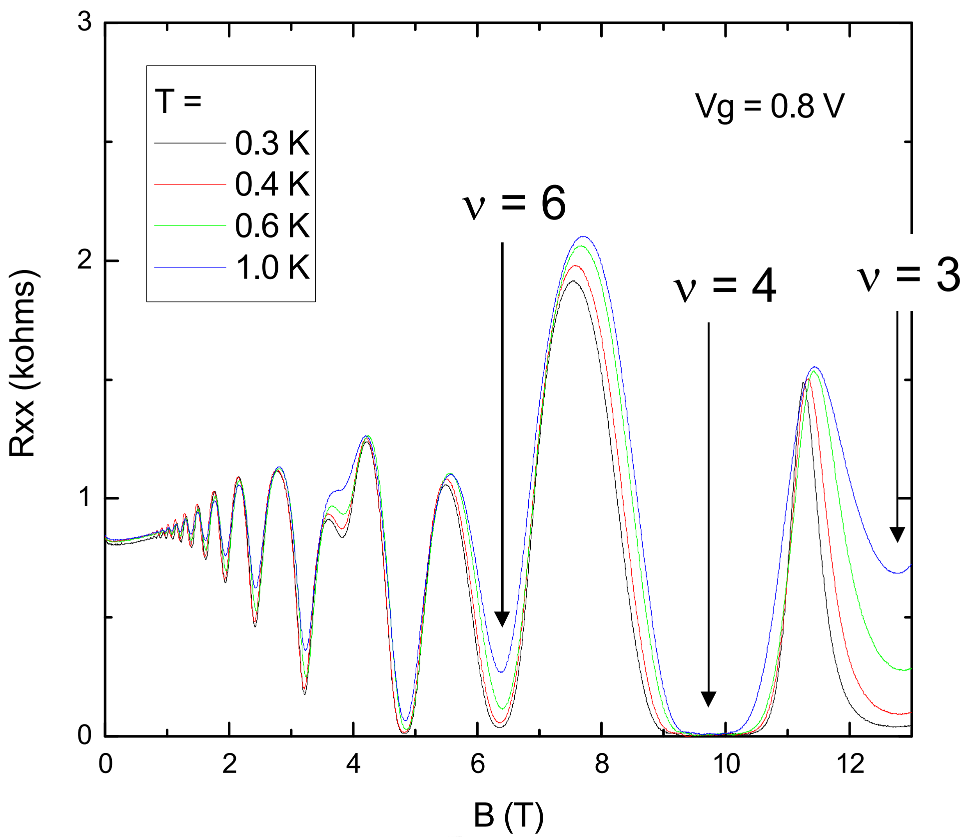


$$E = \hbar\omega_c\left(N+\frac{1}{2}\right) \pm \frac{1}{2}g^*\mu_B B \pm \Delta_V(B)$$

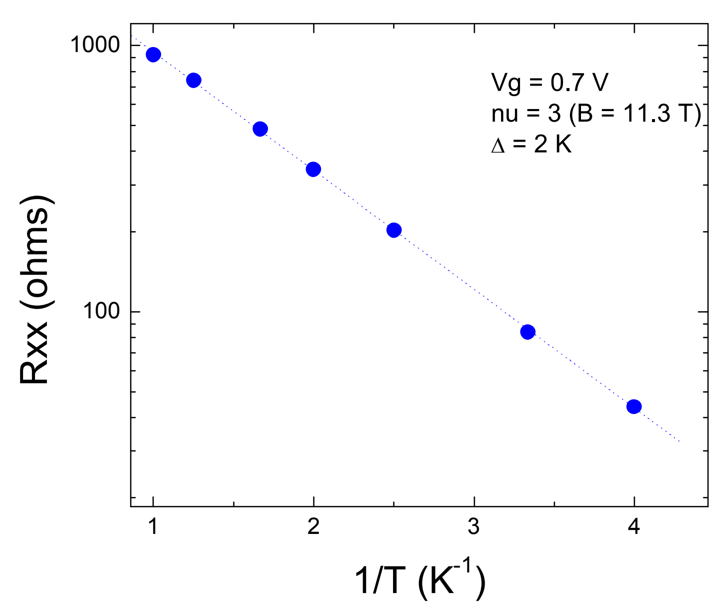
(*Assumed g* =2 and m* =0.19m_o*)

Activation of Quantum Hall States



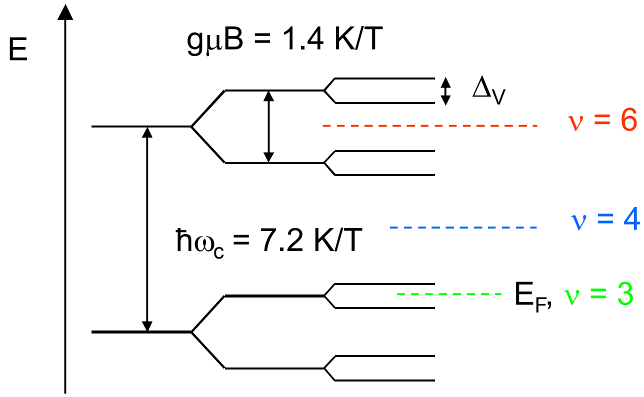


$$R_{xx} \sim R_o \exp(-\Delta/2k_BT)$$

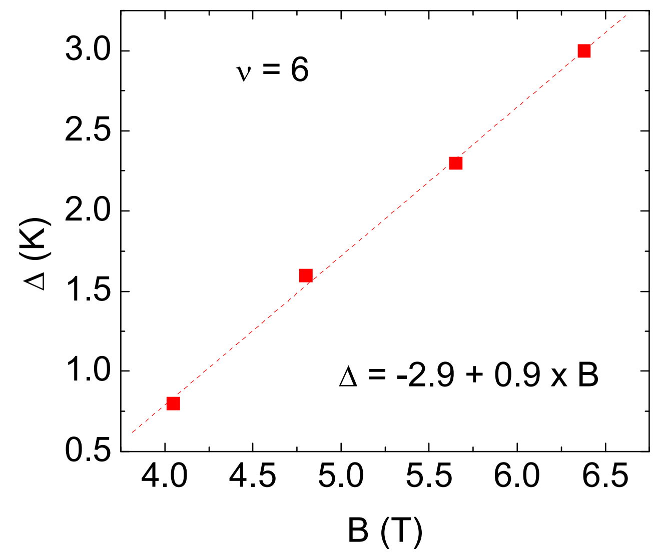


Made activation measurements at ν = 6,4,3 for various Vg's

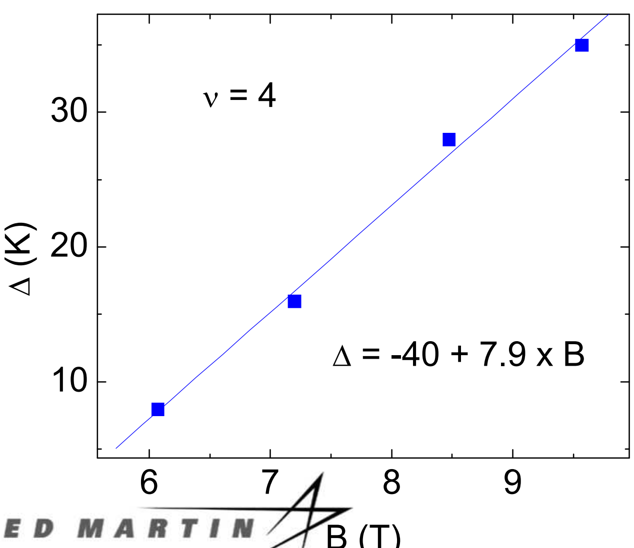
Activation Measurement Summary



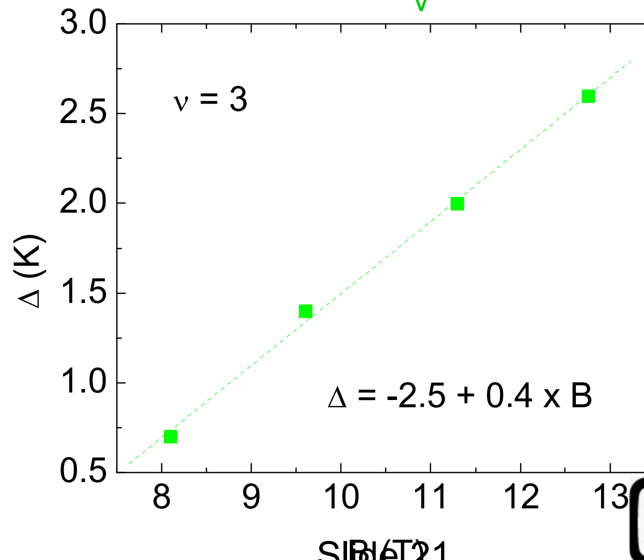
$\Delta = g\mu B - \Delta_v - 2\Gamma$



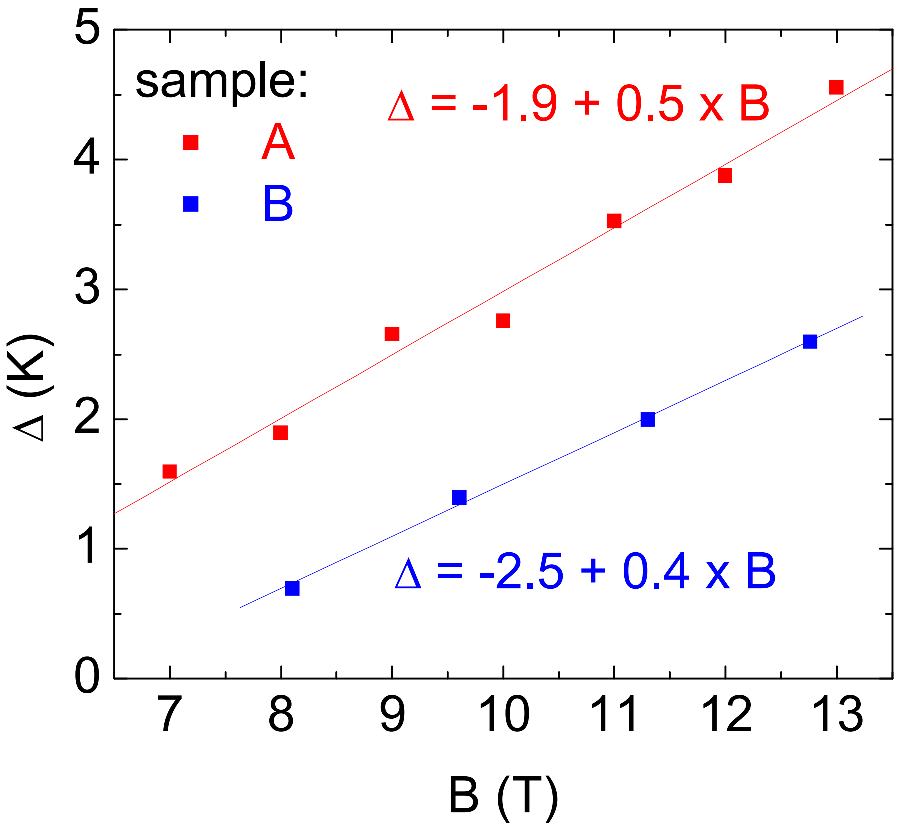
$\Delta = \hbar\omega_c - g\mu B - \Delta_v - 2\Gamma$



$\Delta = \Delta_v - 2\Gamma$



Activation of Valley-Split Minima

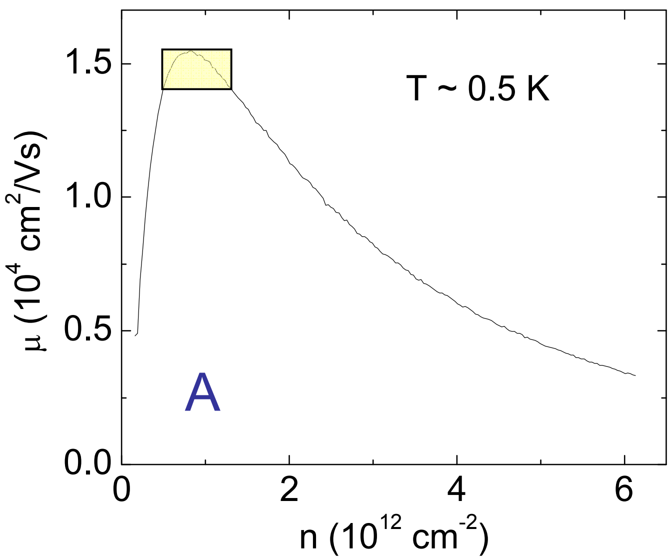


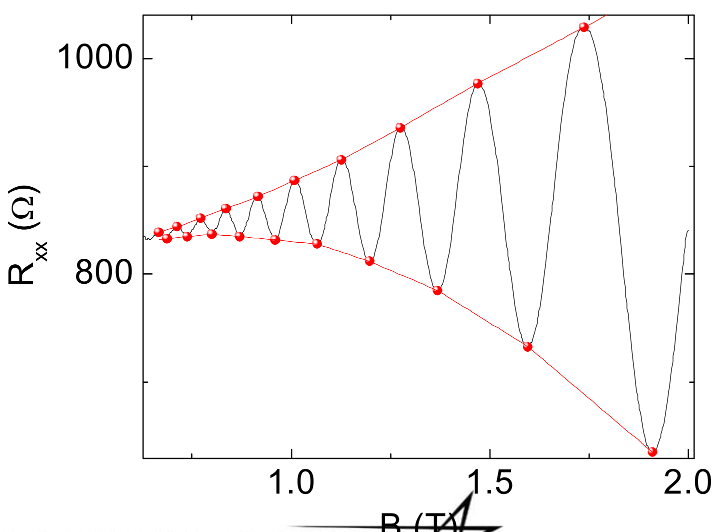
$\nu = 3$

$\Delta = \Delta_v - 2\Gamma$

- Linear trend seen previously for valley and spin-splitting in many material systems

LL Broadening (Γ) Estimate





From low B-field SdH data:

Γ ~

A: 4.3 K

B: 4.6 K

At ν = 3

$\Delta = \Delta_v - 2\Gamma$, then:

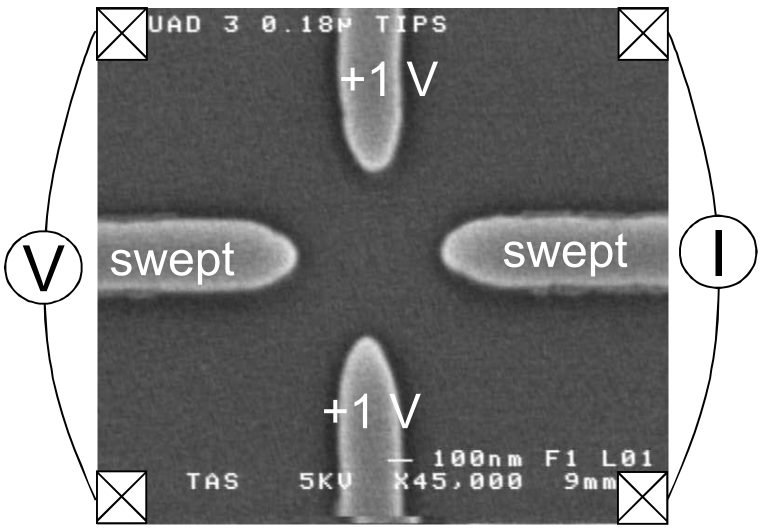
$\Delta_V = \Delta_V^0 + 0.5\ (K/T)\ \times B_\perp$

$\Delta_V^0 \sim 7\ K$

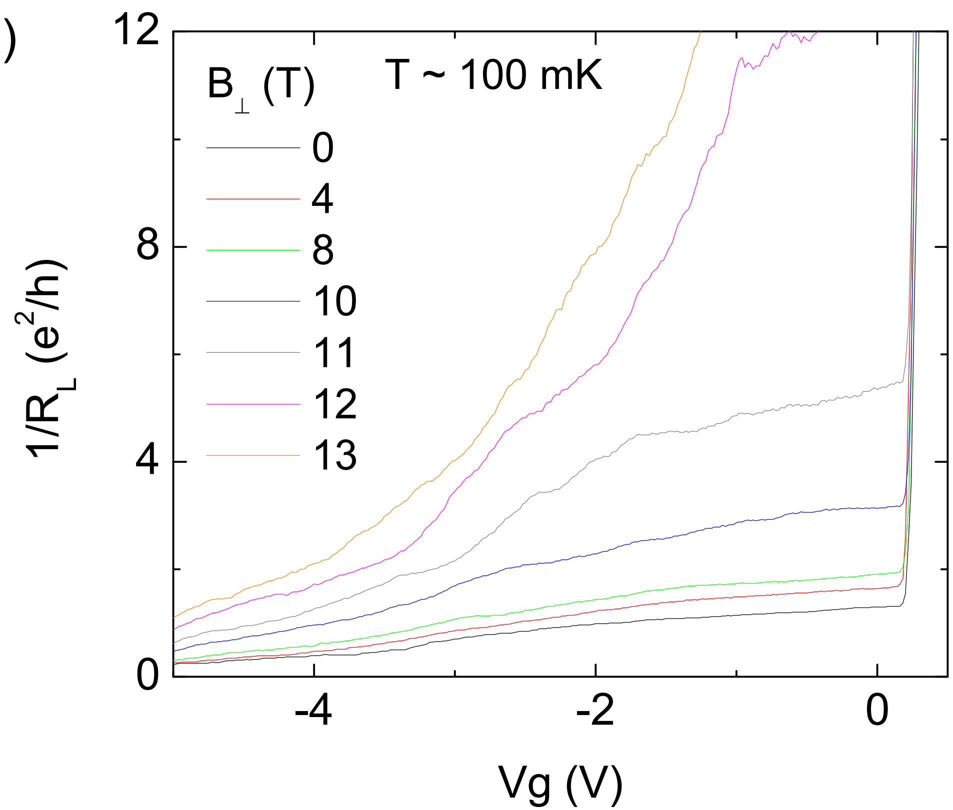
Disorder comparable to valley splitting
→ extrapolation to B = 0 difficult

QPC Transport and Valley Splitting

Valley splitting from 1D subband behaviour?
(S. Goswami *et al*., Nat. Phys. 2006)



V_{tg} = +10 V



- Evidence for 1D subband in large (~500 nm) gap unclear.
- New structures with 20 nm gaps are about to be measured

Summary

Thermal activation measurements of the valley splitting yields:

$\Delta_V = \Delta_V^0 + 0.5\ (K/T) * B_{perp}$

$\Delta_V^0 = 0.2$ to 6 K (vary by device)

Device characteristics:

Peak mobility	~15,000 cm^2/Vs
mean free path	~300nm
phase coherence length	1μm (peak)

Future Experiments:

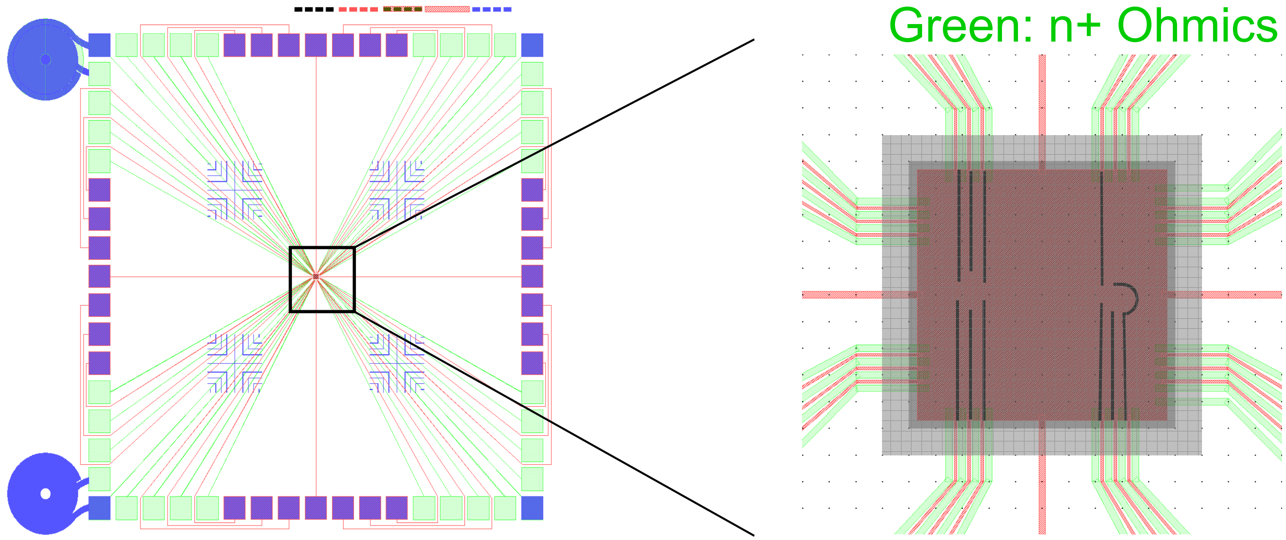
- RF resonance measurement
- Quantum point contacts (magnetic depopulation)

- Background: double quantum dot qubit
- Progress
  - MOSFETS
  - Valley splitting
  - Quantum point contacts and quantum dots

Nanolithography

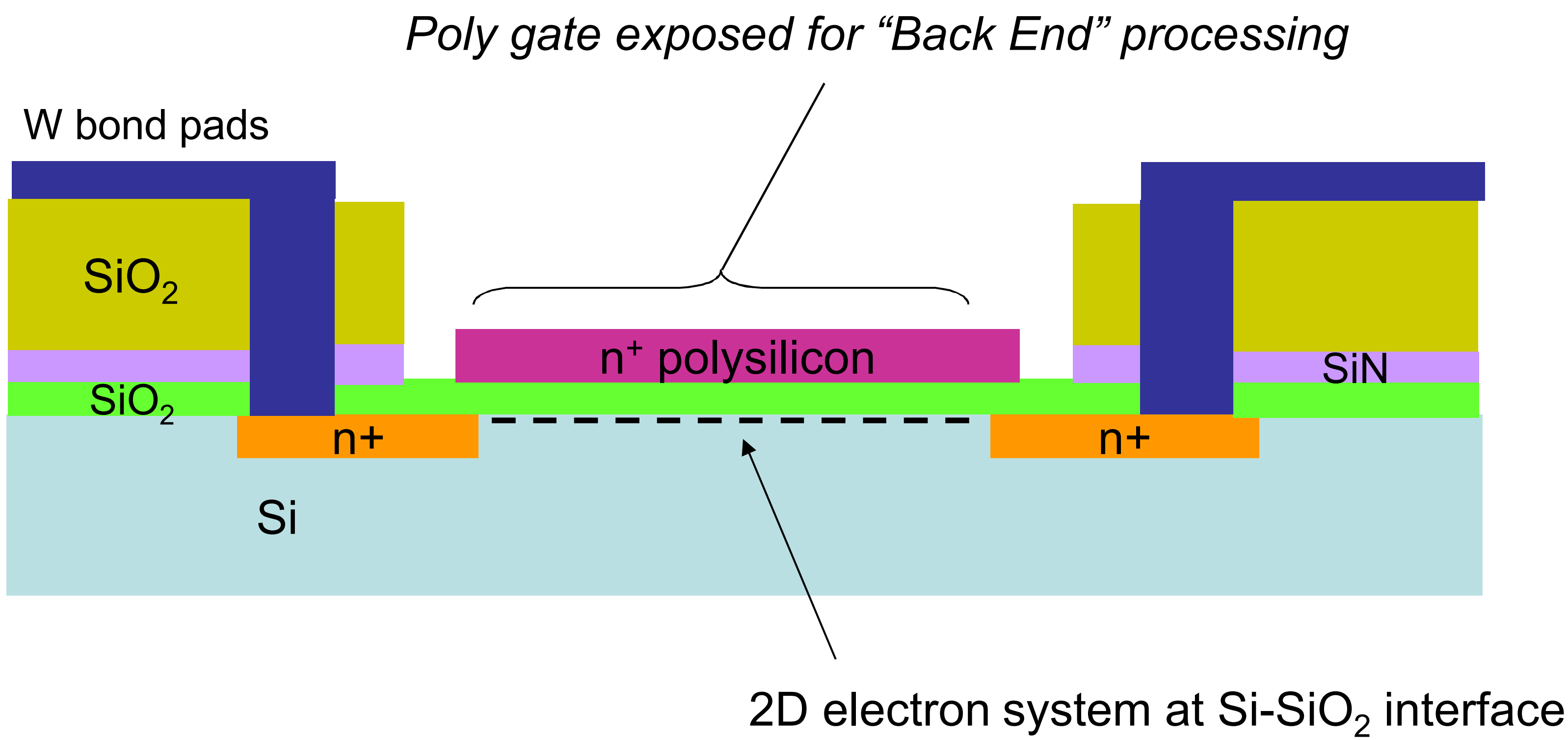
Red: n+ polysilicon (100μm^2)

Green: n+ Ohmics



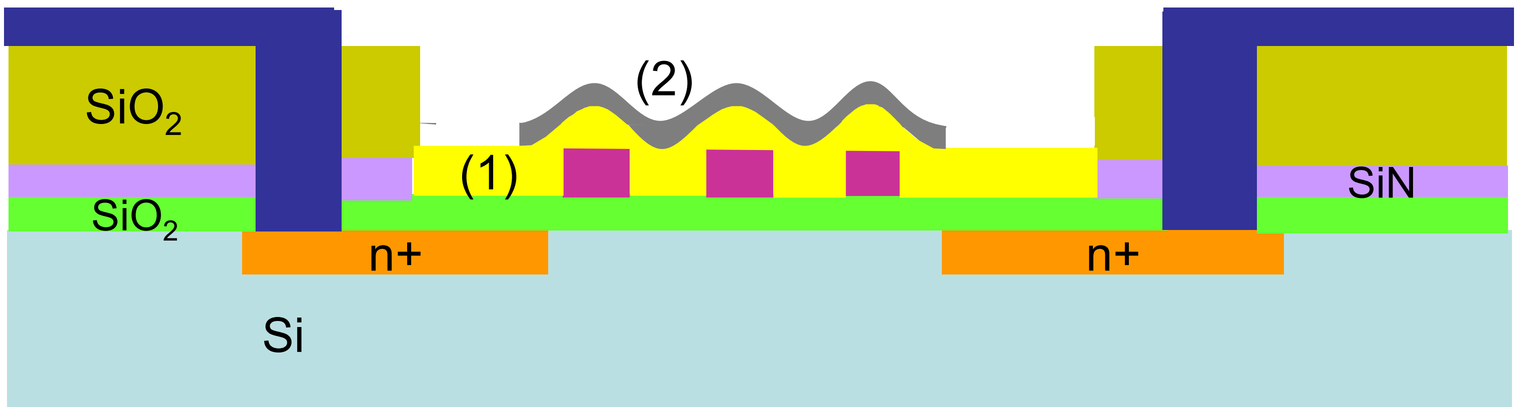
- Electron beam lithography defines 50 nm features (negative resist process)
- Polysilicon etching, insulator deposition using ALD and a second top gate are deposited in the uFab or CINT cleanrooms.
- Variations of desired structure can occur rapidly

"Front End" Processing: Si MOSFETs



“Back End” nanolithography

1. Ebeam lithography
2. polysilicon patterning with plasma etch
3. Deposit 2nd dielectric: atomic layer deposition of Al2O3
4. Top gate: sputtered Al or ALD metal

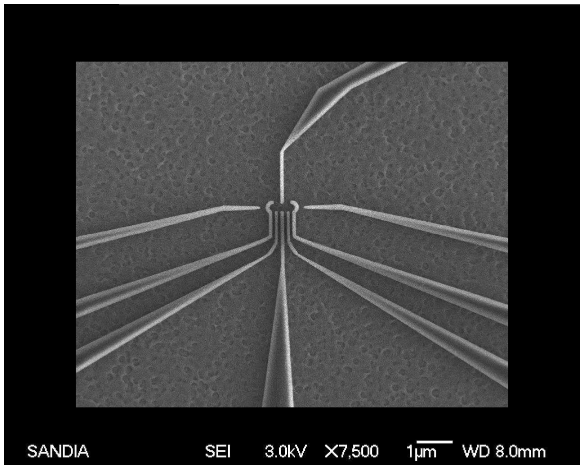


Issues: electrical characteristic of ALD, new etch out of MDL for poly

- C-V used to characterize and optimize ALD process
- Other oxides can be substituted if necessary
- Working to incorporate EBL in silicon fab – allows better control

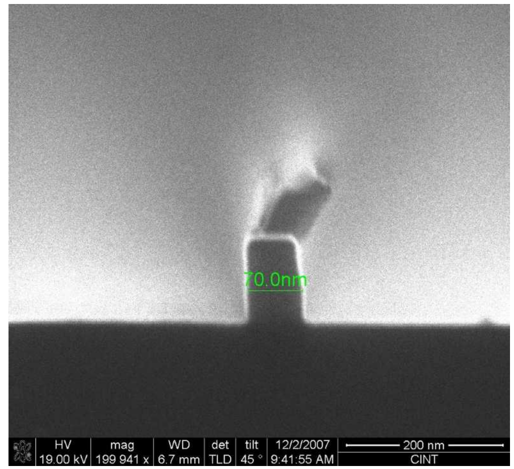
Nanolithography Progress

Electron beam lithography



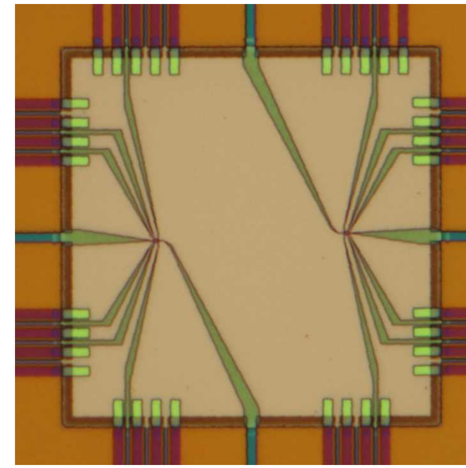
- State-of-the-art Ebeam writer capabilities
- NEB negative ebeam resist

Plasma etching



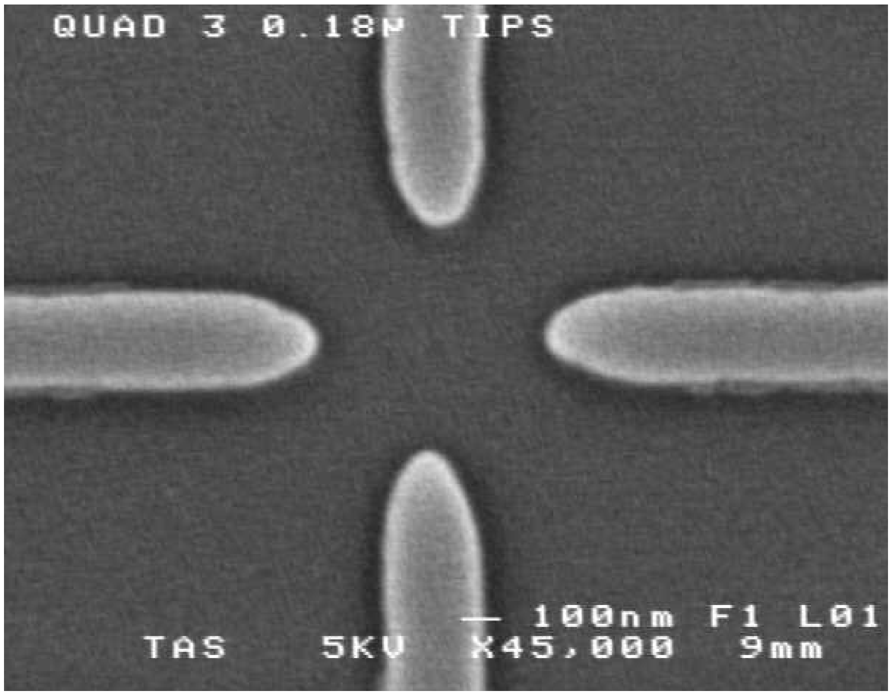
- MESA/uFab bromine plasma etch of polysilicon
- 70 nm poly linewidth after EBL and etching.

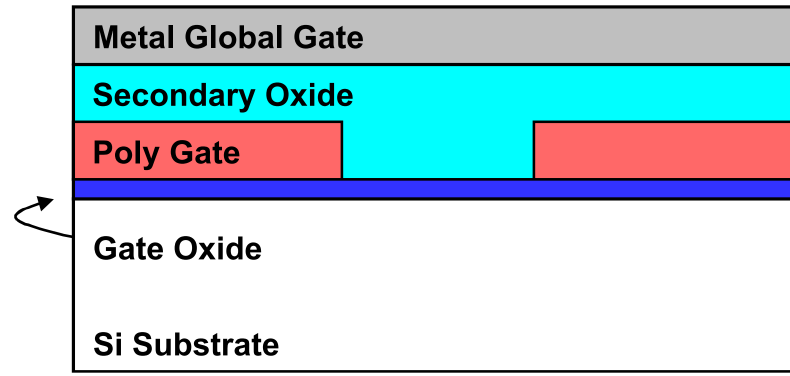
Status



- Point contact, dot and double dot experiments will use double dot gates

Front End Devices with 180 nm Feature Sizes

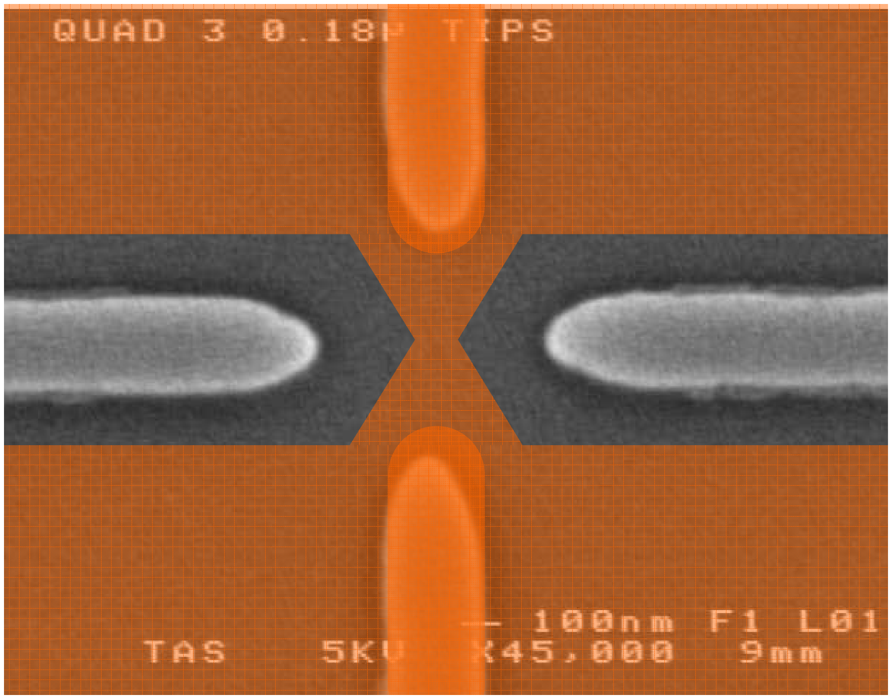




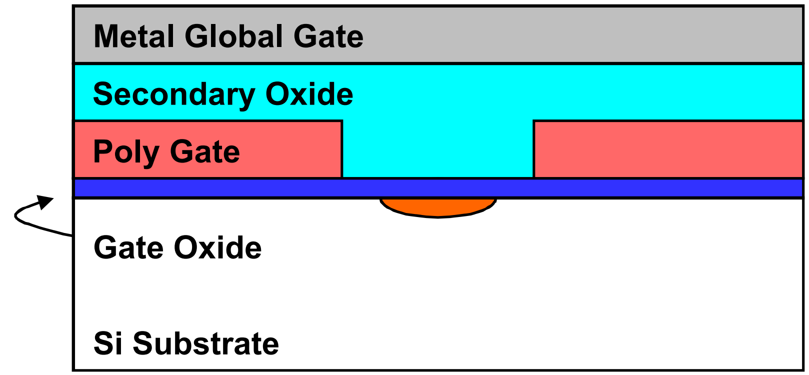
Polysilicon gates can be used for either accumulation or depletion in addition to the global accumulation gate

*G.M. Jones et al. PRL **89**, 073106 (2006)*

Device Operation



Global top gate accumulating, polysilicon gates depleting to form a 1D Channel



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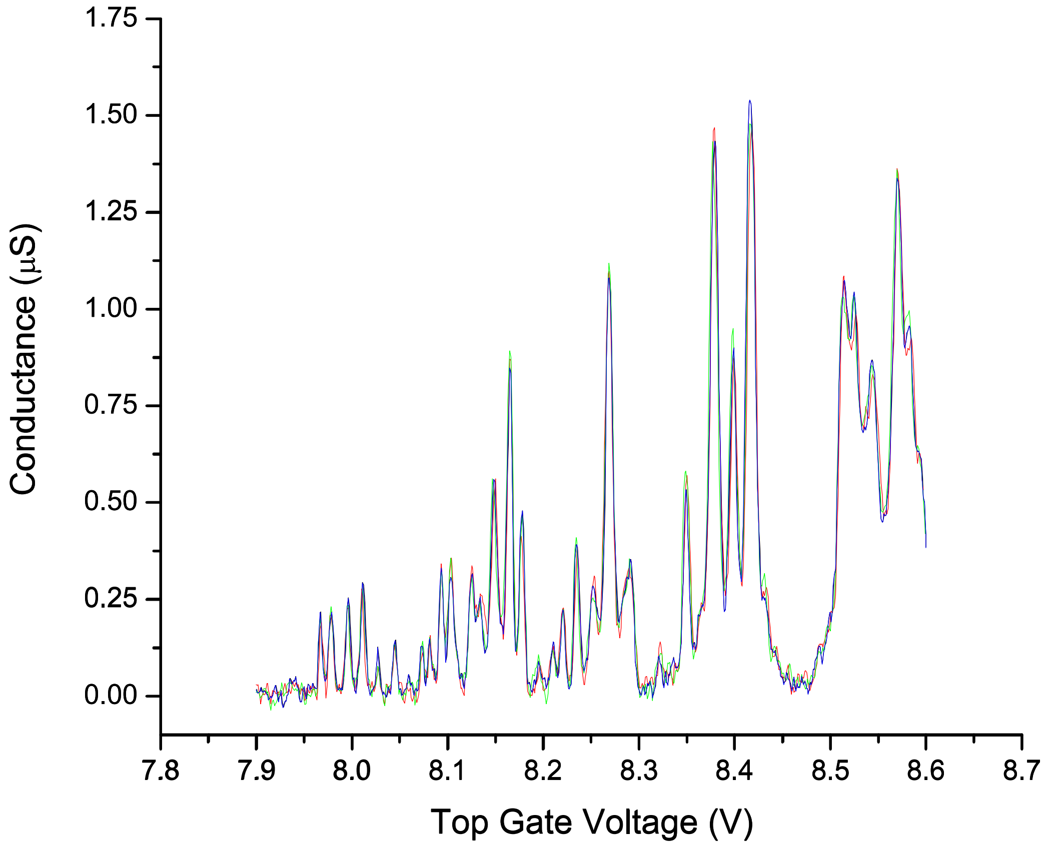
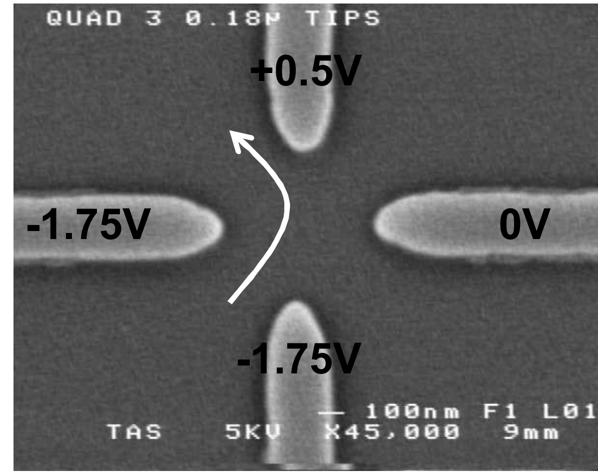
Cross Structure



(Corrected for .1% drift over 12hrs)

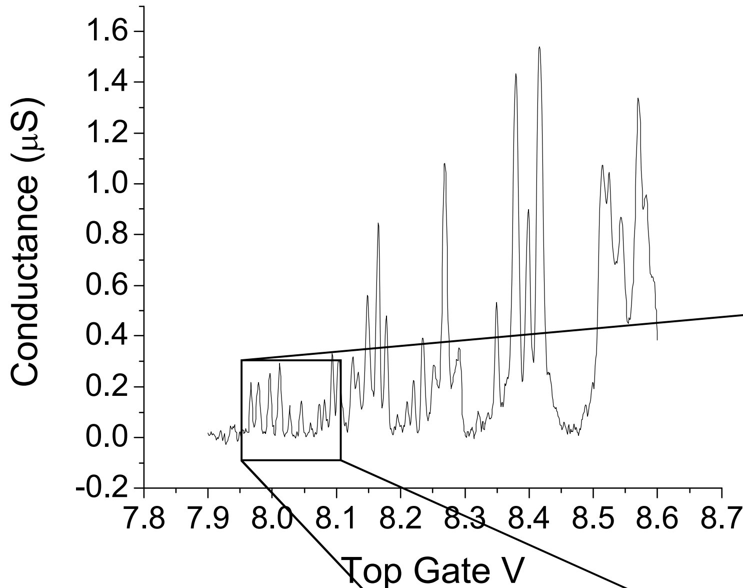


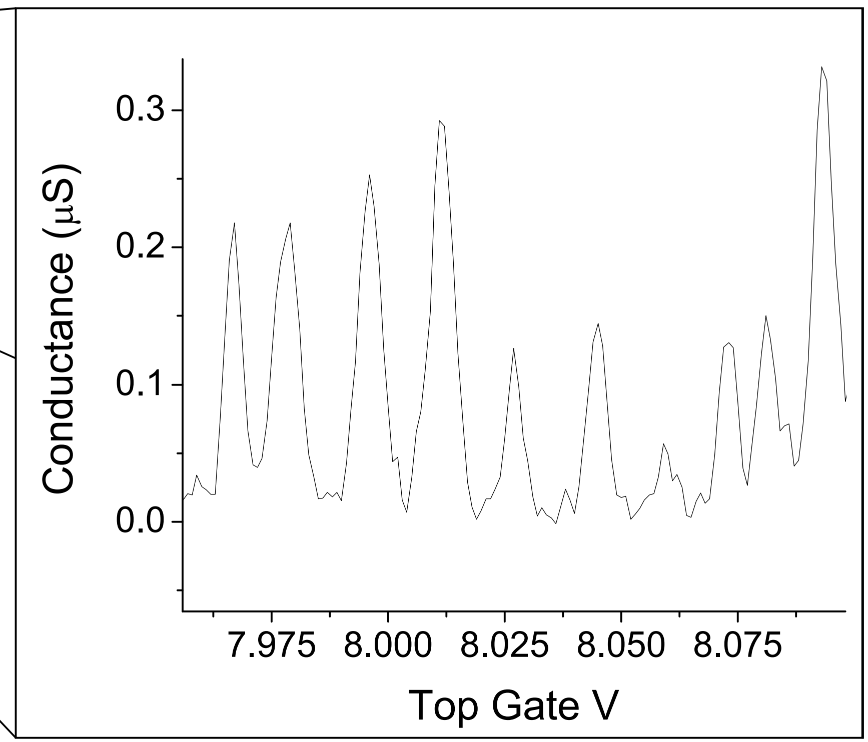
Top Gate = Swept

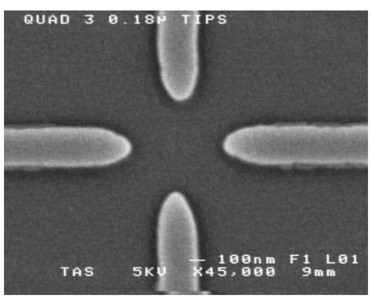
- No repeatable QPC steps
- Periodic, repeatable resonances near pinch-off

Cross Structure

- Peak spacing corresponds to a dot diameter of ~65nm
- Longer period oscillations would correspond to a 25nm diameter







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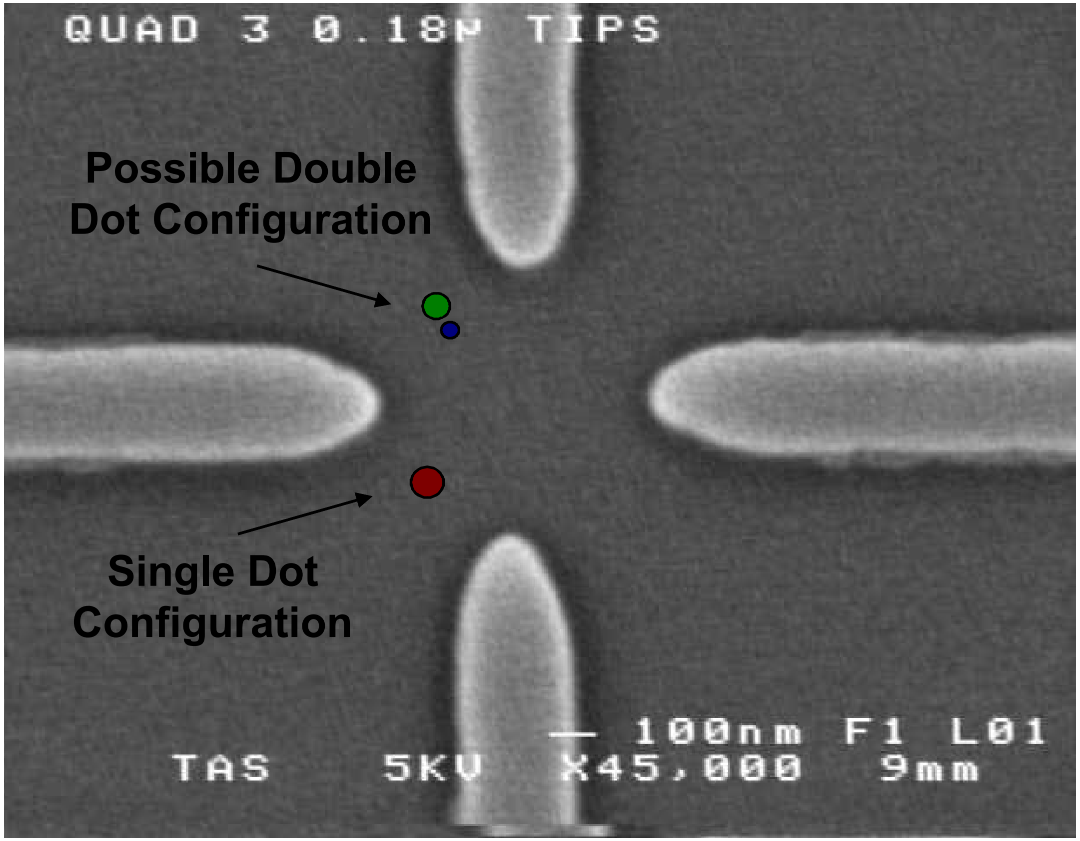
"Disorder" Dots

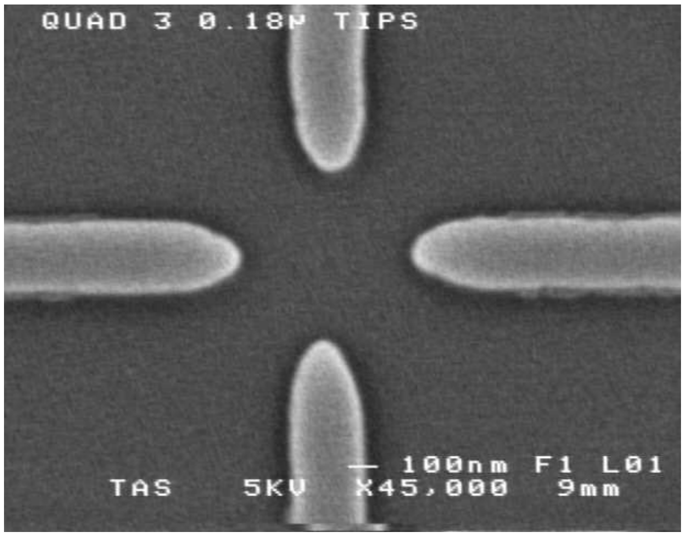
- Apparent dot sizes fit neatly between polysilicon gates
- Reducing feature size should reduce the probability of overlapping with a disorder site
- Process improvement can increase general sample "cleanliness"



Quantum Information S&T

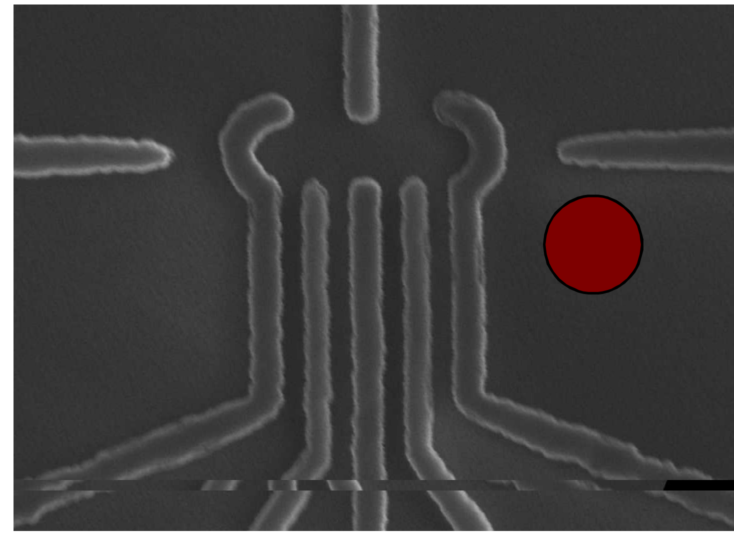
Geometries

MDL Cross Structure



Distance between:
Adjacent Gates: ~350nm
Opposite Gates: ~650nm

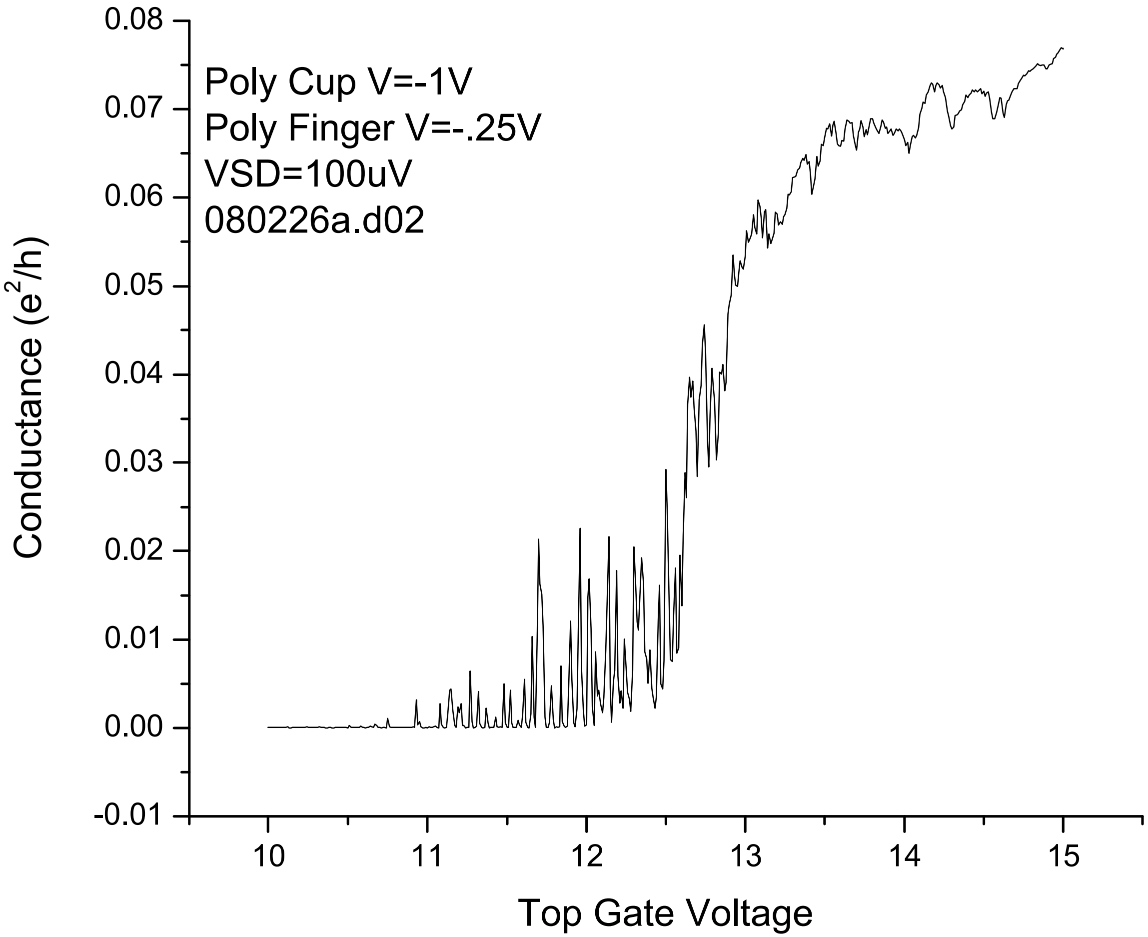
Double Quantum Dot Structure

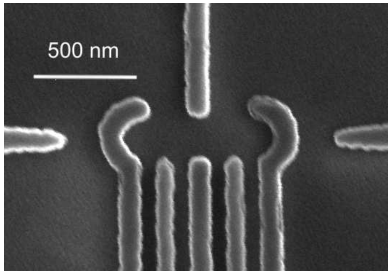


1µm

QPC Gaps: ~ 150nm

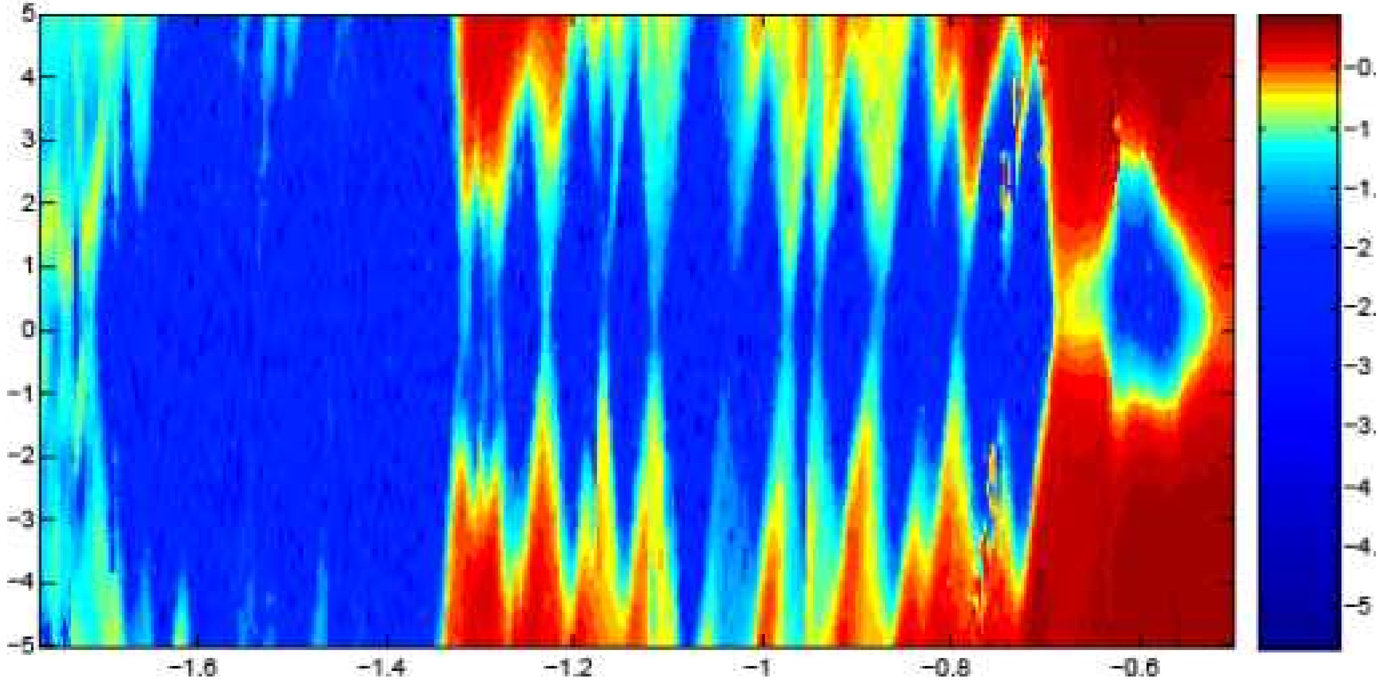
DQD Structure





- QPCs on double quantum dot structure each exhibit similar behavior to cross structure

Coulomb Blockade



- Diamond structures suggest conductance resonances are Coulomb Blockade

Beating the Disorder

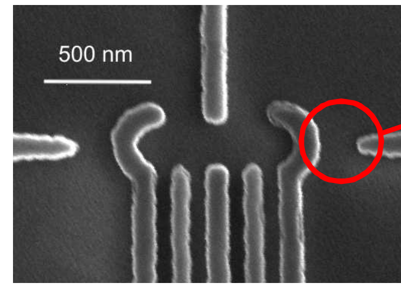
Materials Improvement

- Gate Oxide Growth
- Forming Gas RTA
- Plasma Etch
- ALD Al_2O_3 Deposition

- Disorder is inherently present but from other SET work we know small enough sizes minimize impact (50 nm).
- Additional disorder induced by processing may be repaired.

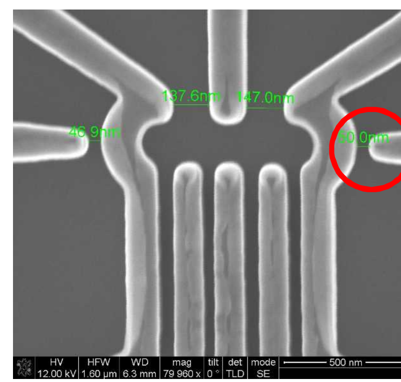
Size Reduction

Large gaps – disorder more important



200 nm

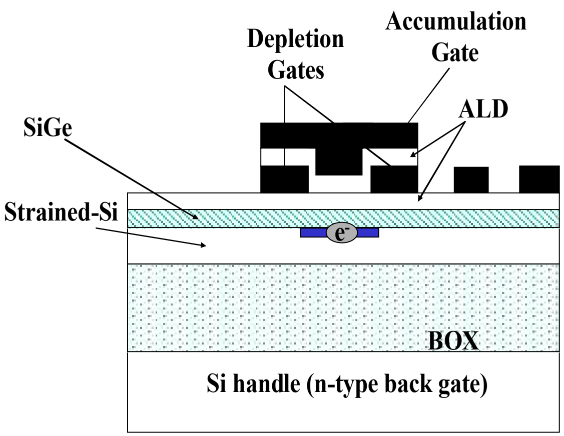
Small gaps minimize role of disorder



50 nm

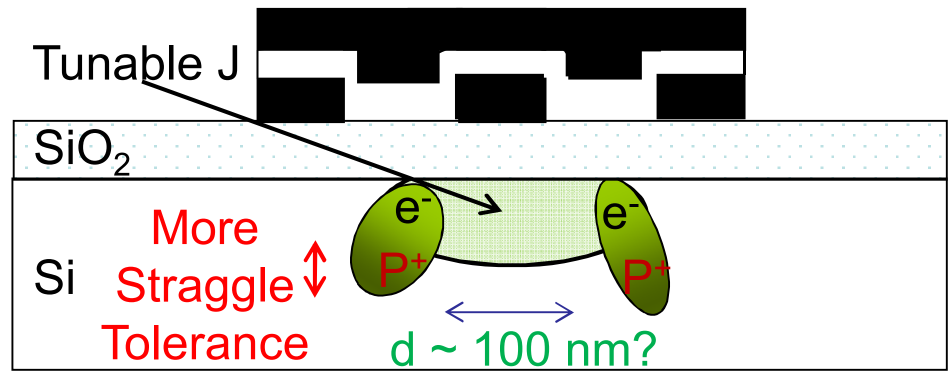
2nd Generation Nanoelectronics

SiGe barriers



- Replace disordered oxide with epitaxial SiGe barriers
- Compatible with front-end/ back-end device flow

Hybrid donor-dot devices



- Use single donor implant technology to place donors below gated dots
- Donor location moves electron away from the oxide interface

Silicon Qubit Summary

- Highlights
  - Surface accumulation mode approach complements existing efforts
    - Possible benefits over other approaches & experimental platform to better study surface effects, “dopant free” devices & single dopant-surface coupling
  - Experimental platform is available for custom nanoelectronics

- Progress
  - MOSFETs fabricated for this work have relatively high mobility and can be used for both gated nanostructures and donor structures
  - Valley splitting is present for the 2DEG and is expected to be larger for nanostructures
  - Nanolithography for making point contacts and dots is underway.
    - Transport nanostructures shows complicated blockade
    - We anticipate significant improvements as size decreases and material improvements are implemented..