Power Conversion Conference – May 5-8, 2008

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Presentation #29

Comparison of Two Forward Topologies as the Front End Converter for a Space-Qualified Distributed Power System

5/7/2008

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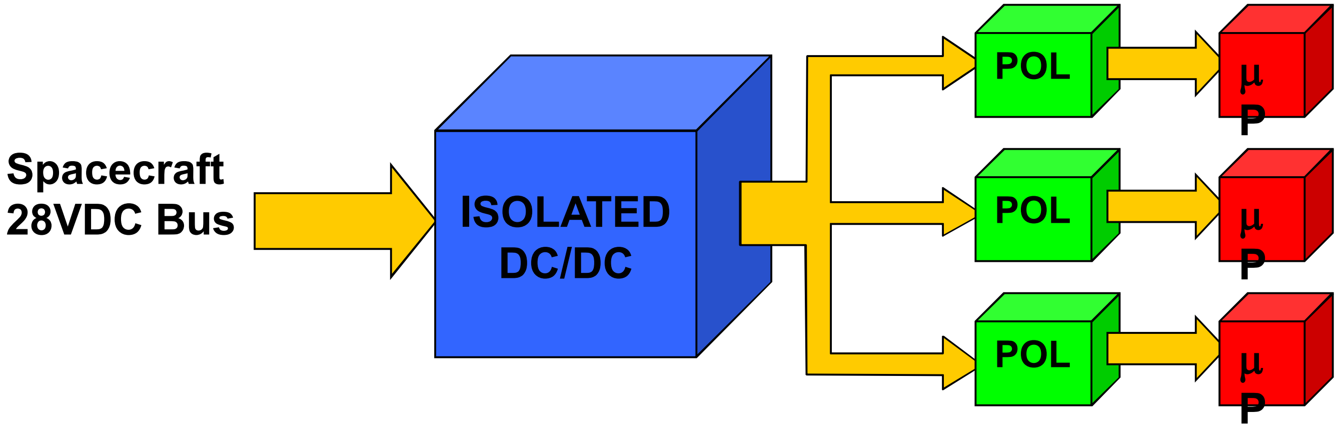
Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Purpose

- To develop a high efficiency (>90%) isolated power converter as an intermediate power stage between the Spacecraft Bus and Point-of-Load Converters.



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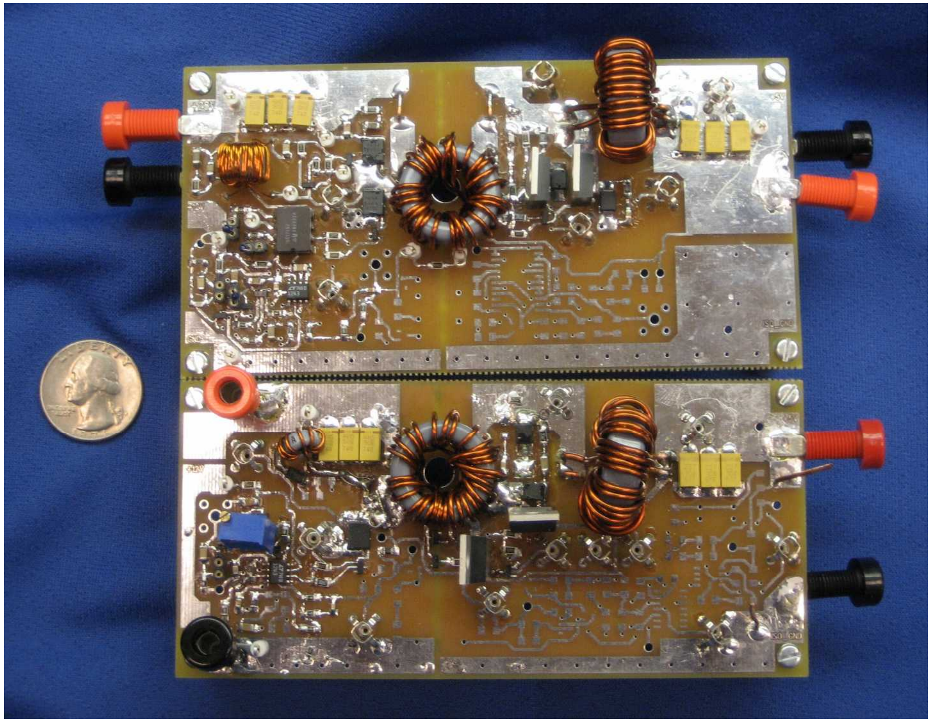
Project Goals

- $22V < V_{IN} < 34V$
- $V_{OUT} = 5V$, $I_{OUT} = 10A$ max
- $\eta \geq 90\%$ at nominal V_{IN} and max load
- Efficient at high frequencies
- Suitable rad-hard components available
- Low FET voltage and current stresses



Active Clamp

LC Snubber

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Outline

- Comparison of Prototype Topologies
- LC Snubber Forward Operation
  - Experimental Results
- The Active Clamp Forward Operation
  - Experimental Results
- Conclusions

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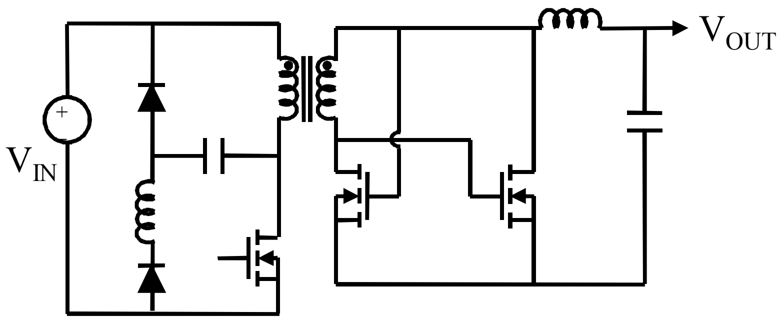
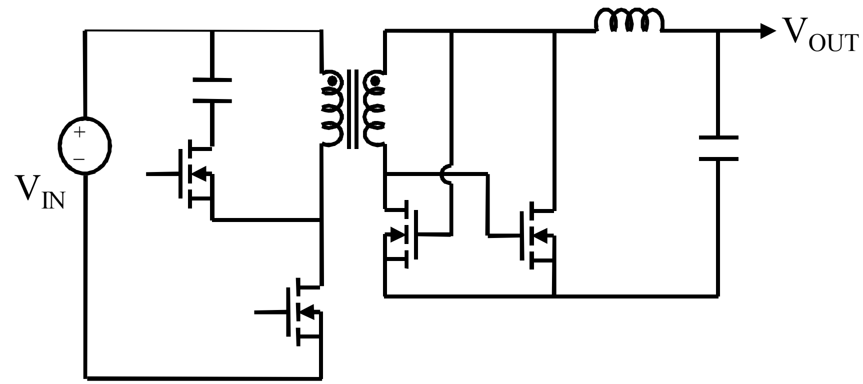
Two Converter Prototypes





<u>LC Snubber Forward</u>

- Simple control (one low side switch)
- Possible turn-on/off soft transitions
- Duty cycle greater than 50%
- Clamped transformer leakage
- Controlled turn-off dv/dt

<u>Active Clamp Forward</u>

- Near ideal self-driven sync rectifiers
- Possible turn-on soft transition
- Duty cycle greater than 50%
- Clamped transformer leakage
- Low, nearly constant V_{DS} stress

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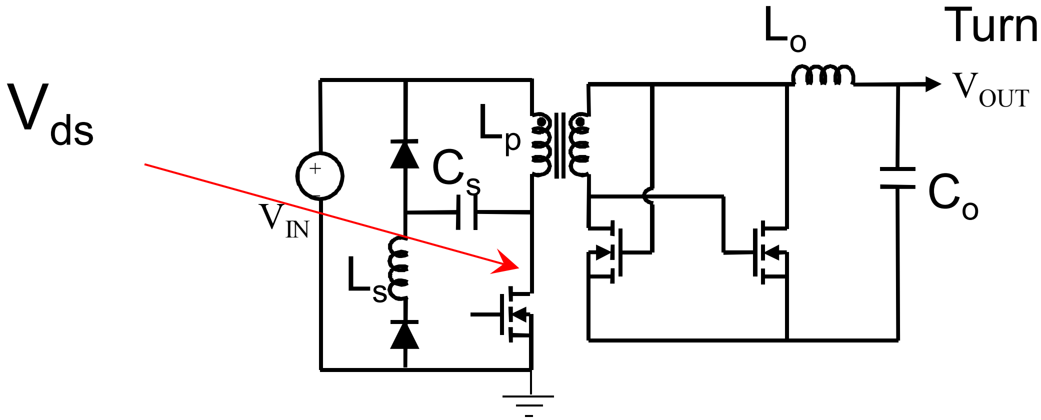
LC Snubber Waveforms



Turns Ratio : 16:6 (2.67:1)

L_p = 400 μH

L_o = 11 μH

C_o = 660 μH

L_s = 5 μH

C_s = 2.2 nF

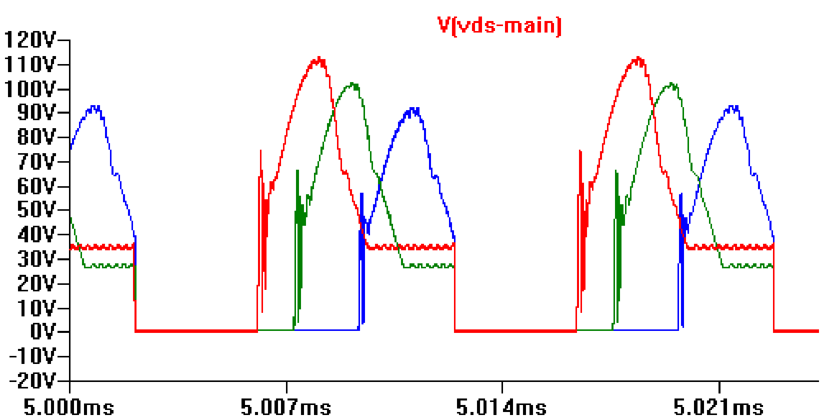
V_{in} = 20V

V_{in} = 28V

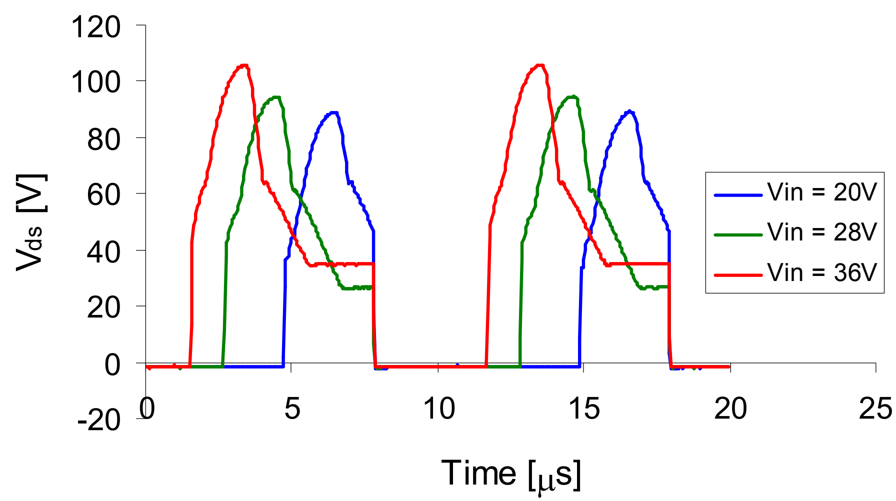
V_{in} = 36V

Drain Voltage of Main Switch

Simulation Results

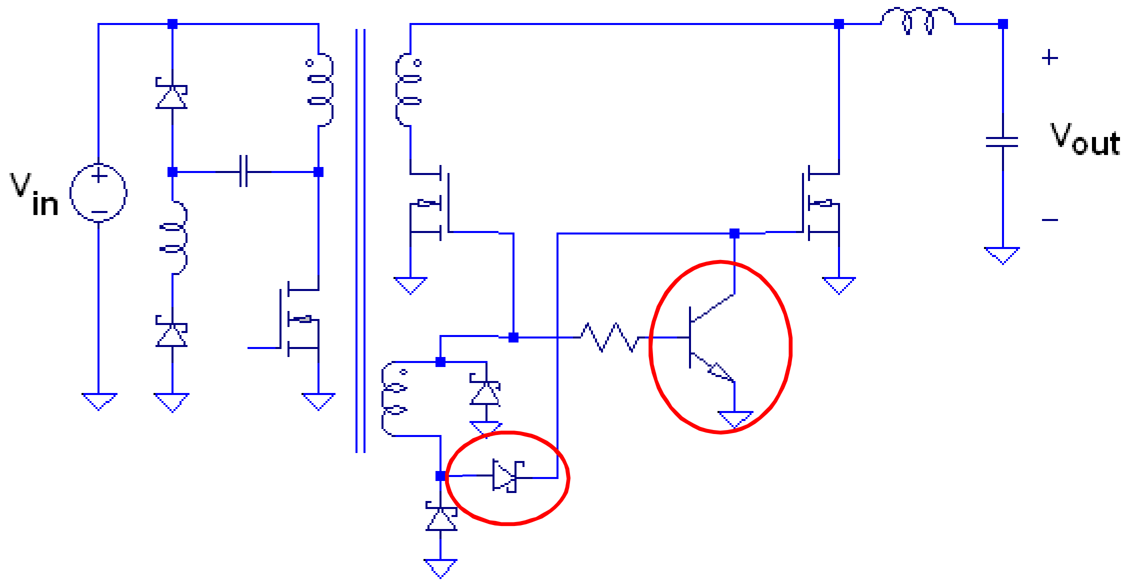


Measured Results

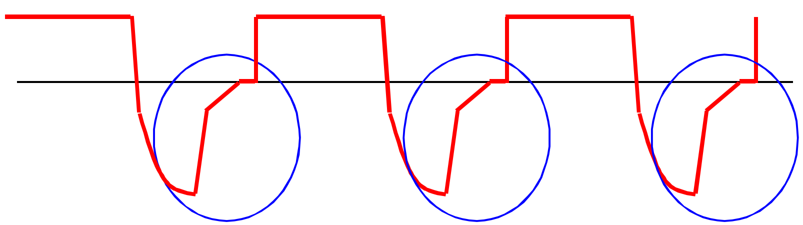


Gate Charge Retention (GCR)

For LC Snubber Converter

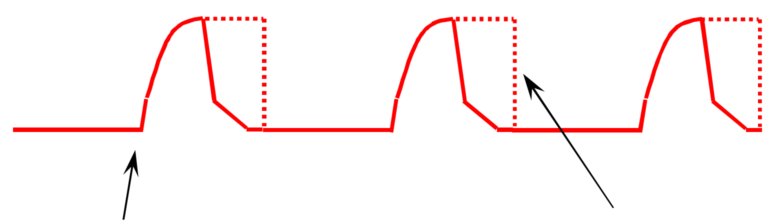


Voltage Across primary



Early reset of transformer core is insufficient to keep free-wheeling switch on

Free-wheeling Synchronous Gate Voltage



Without GCR

With GCR

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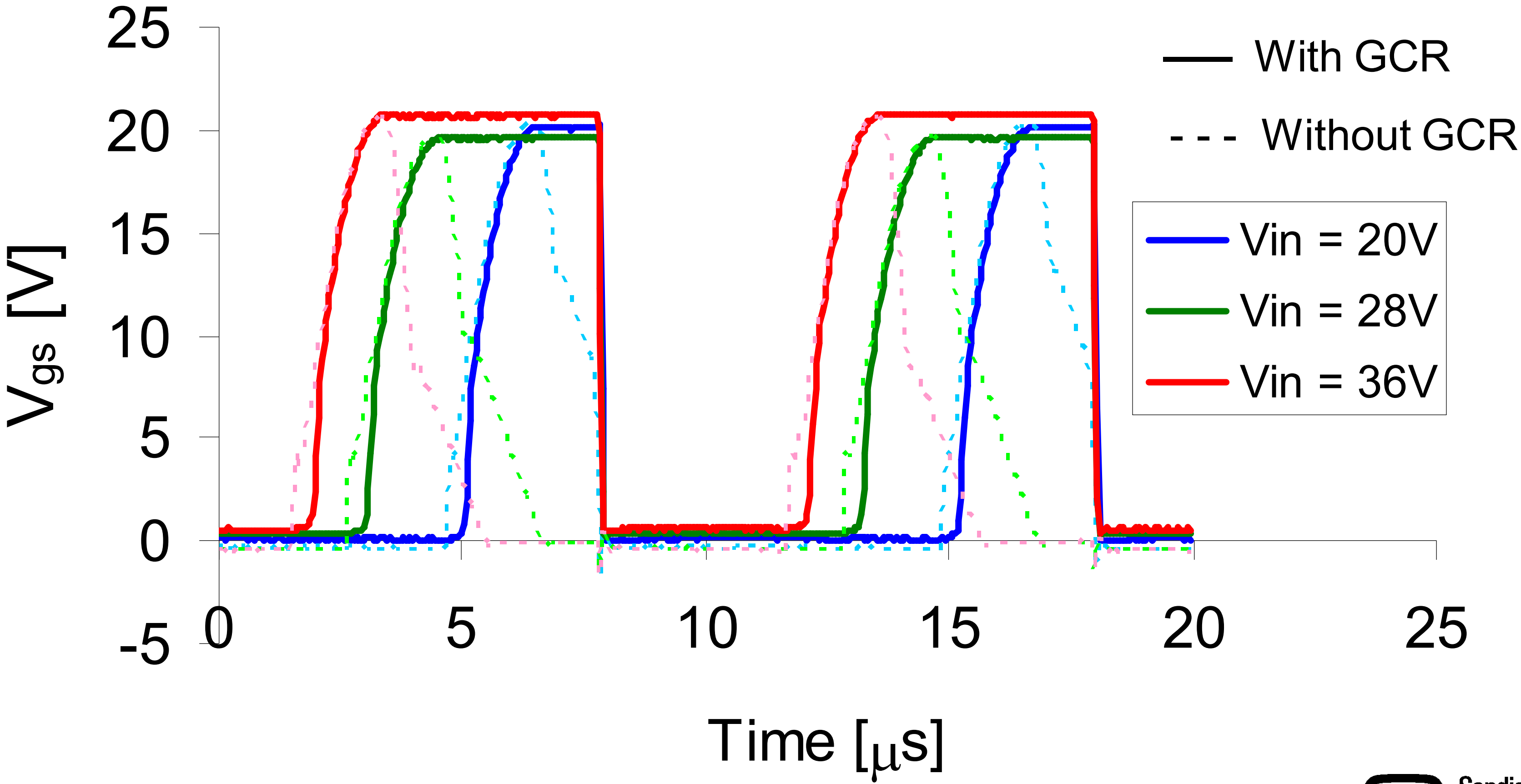
Actual Free-Wheeling Gate Voltage

With and Without GCR



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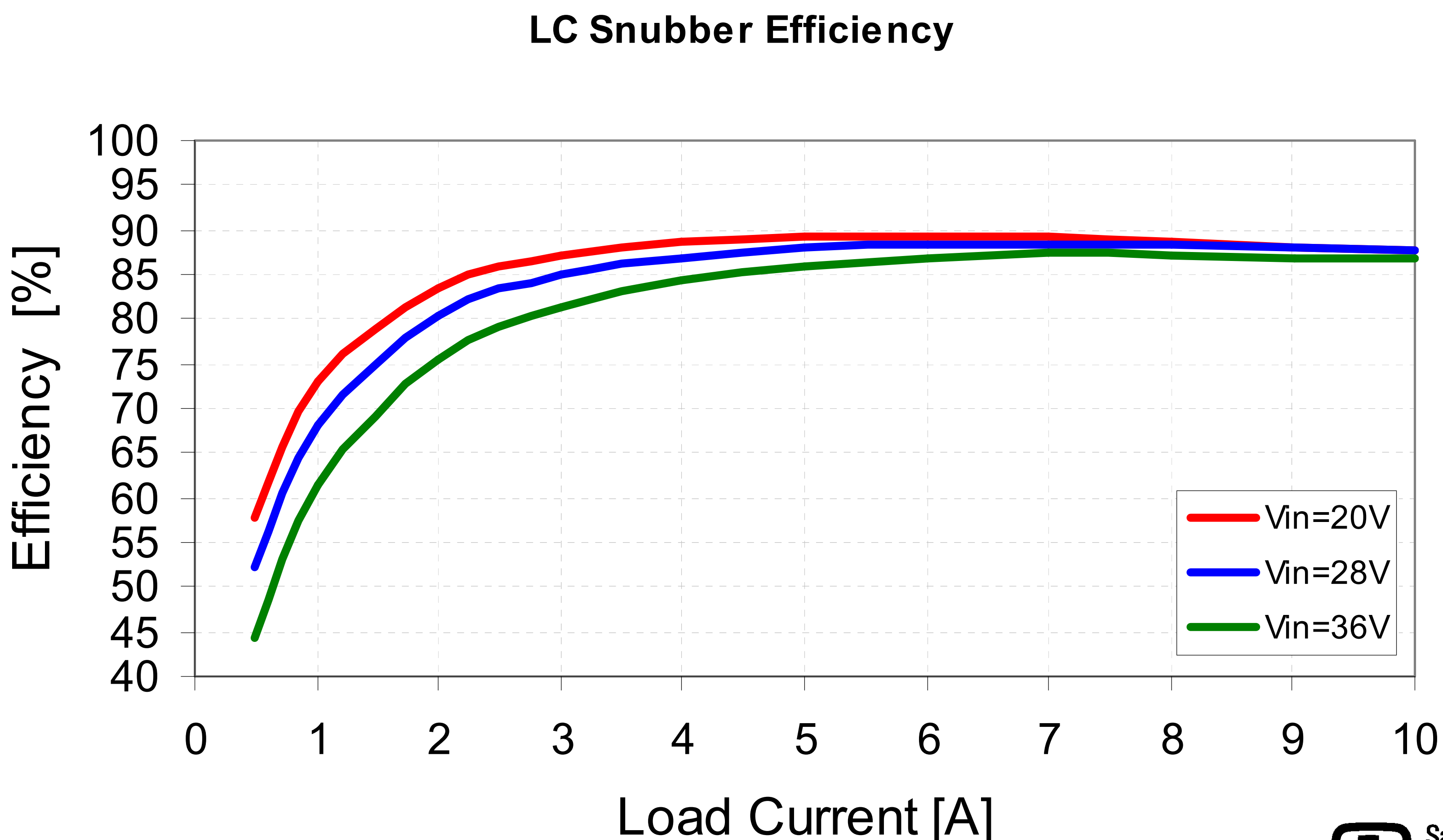
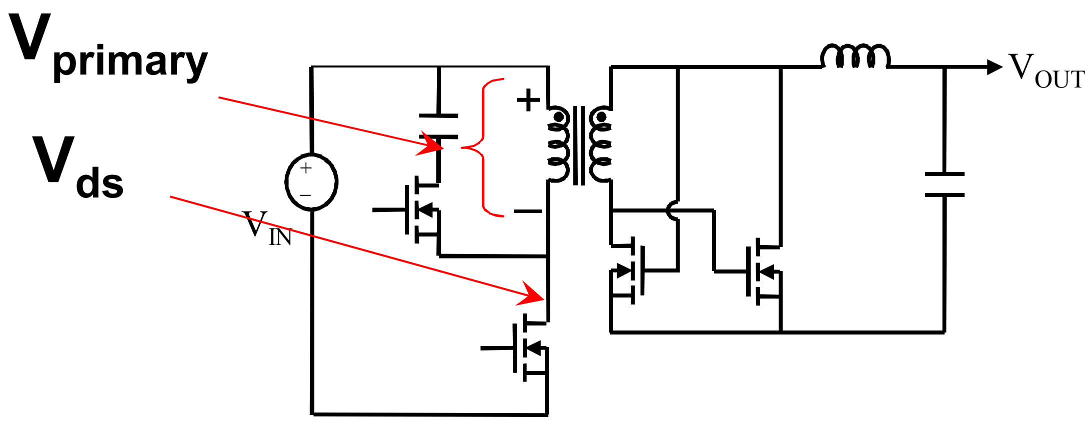
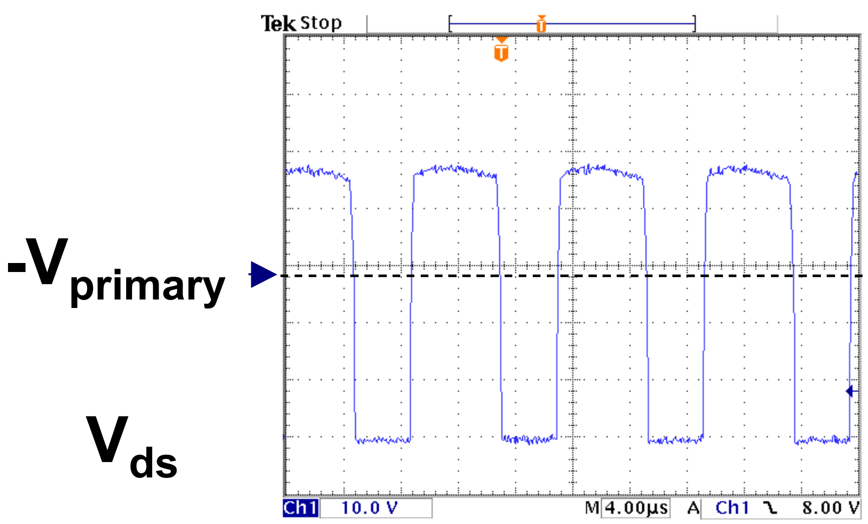
Efficiency of LC Snubber Converter



Active Clamp Basic Operation





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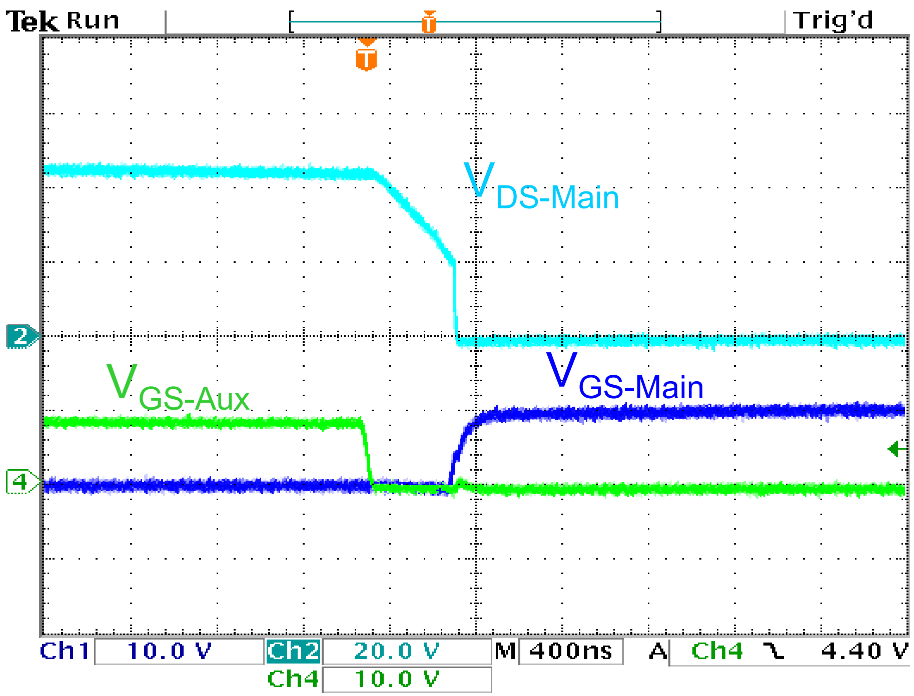
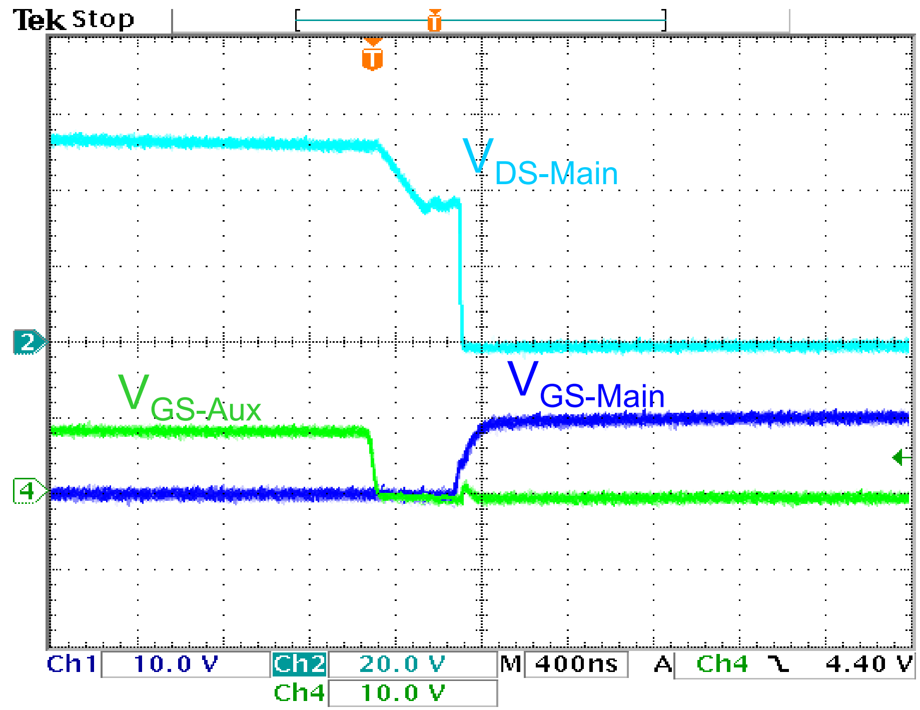
Setting the Main FET Driver Delay



V_{IN} = 20V, I_{OUT} = 0A

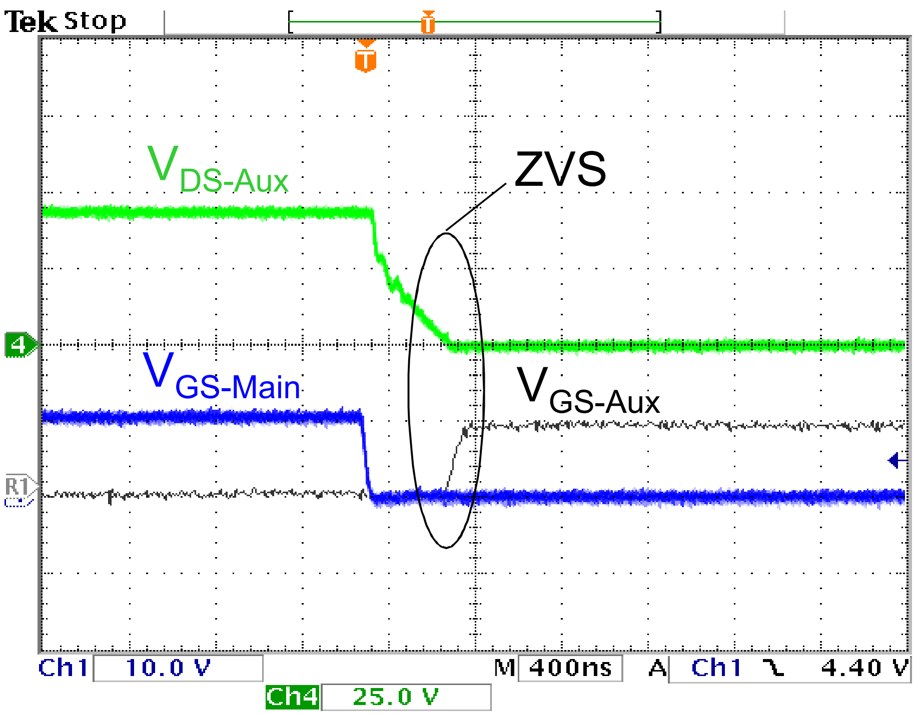


V_{IN} = 36V, I_{OUT} = 10A

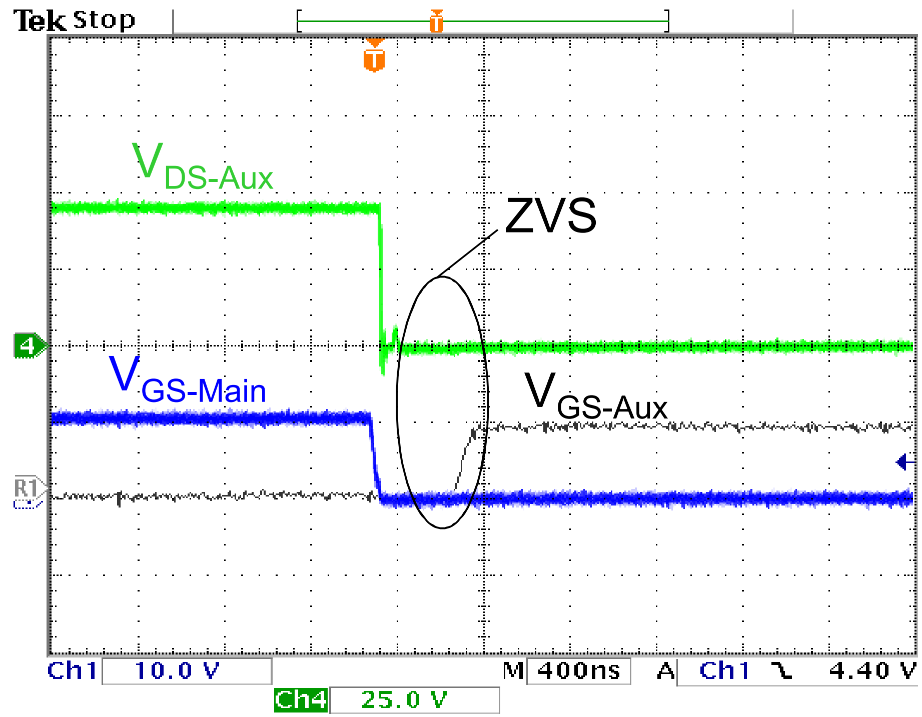
- The delay between the Aux FET turn-off and Main FET turn-on is chosen such that $V_{DS\text{-}Main}$ falls to V_{IN} under all input voltage and load current conditions.

- When $V_{DS\text{-}Main}$ drops to V_{IN}, it is clamped at VIN for the remainder of the off time.

Setting the Aux FET Driver Delay



V_{IN} = 20V, I_{OUT} = 0A



V_{IN} = 20V, I_{OUT} = 5A

- The delay between the Aux FET turn-off and Main FET turn-on is chosen such that $V_{DS\text{-}Main}$ falls to V_{IN} under all input voltage and load current conditions.

- ZVS of the Aux switch gets easier to achieve with increased load current.

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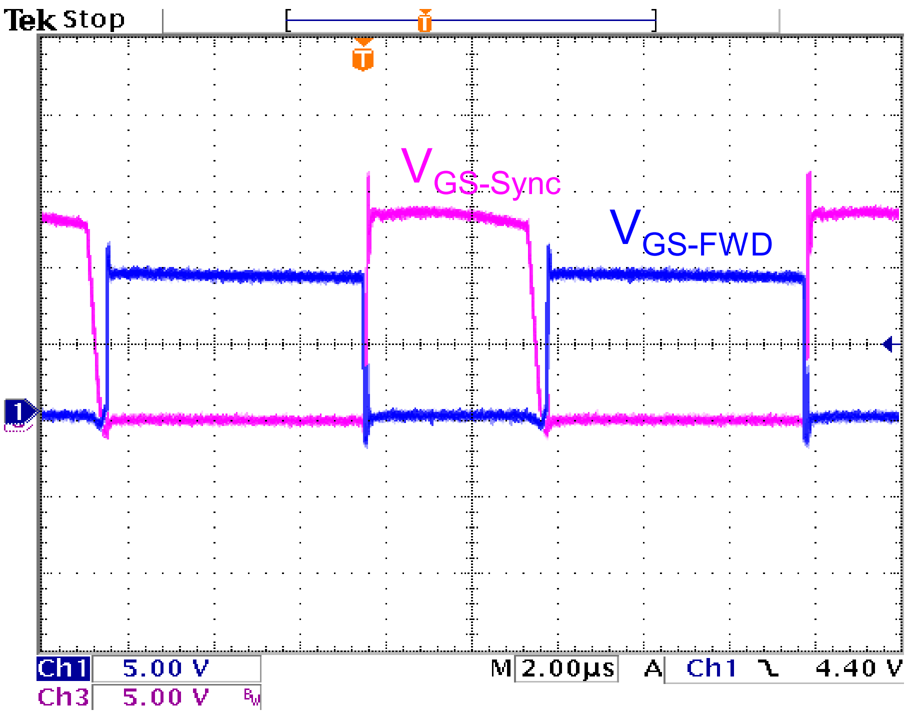
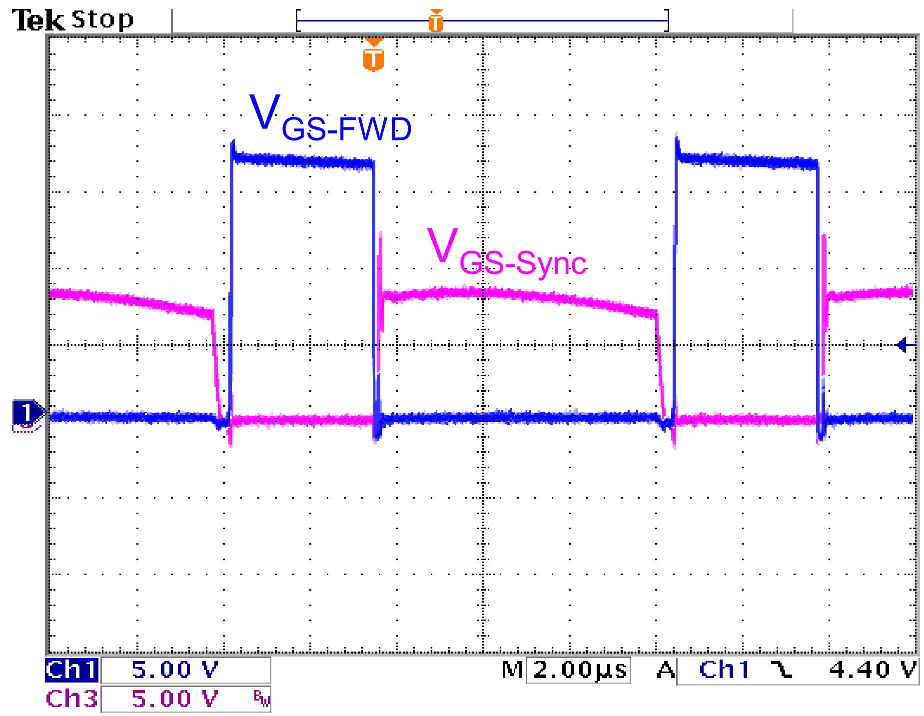
Self-driven Gate Drives



V_{IN} = 20V, I_{OUT} = 10A



V_{IN} = 36V, I_{OUT} = 10A

- The secondary-side rectifiers are self-driven with gate voltages ranging from about 8-17V over all line and load conditions. This is accomplished by a good choice of transformer turns ratio (which also determines duty-cycle range).

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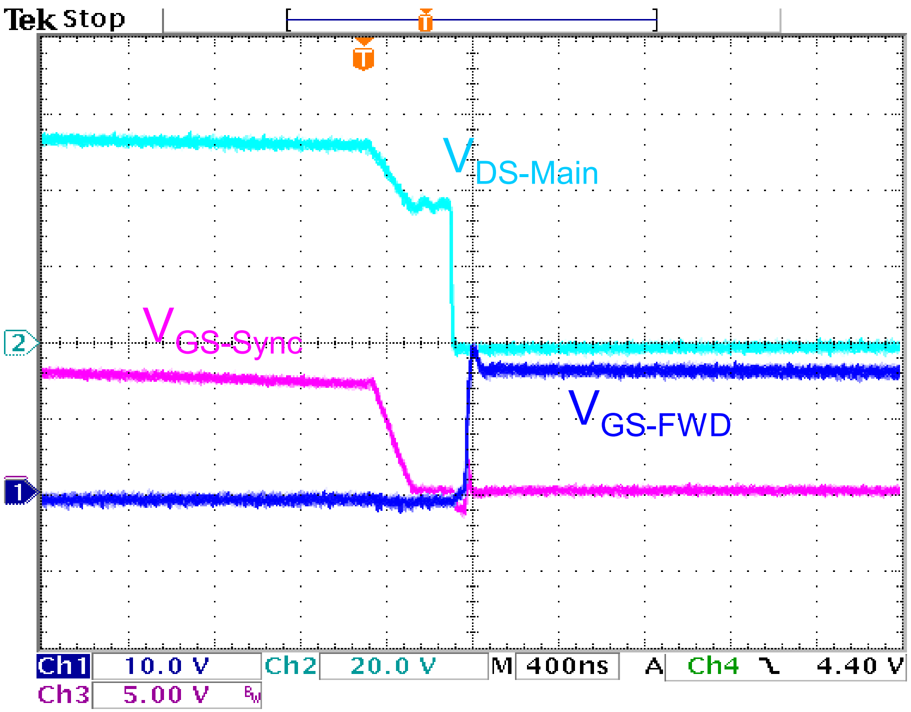
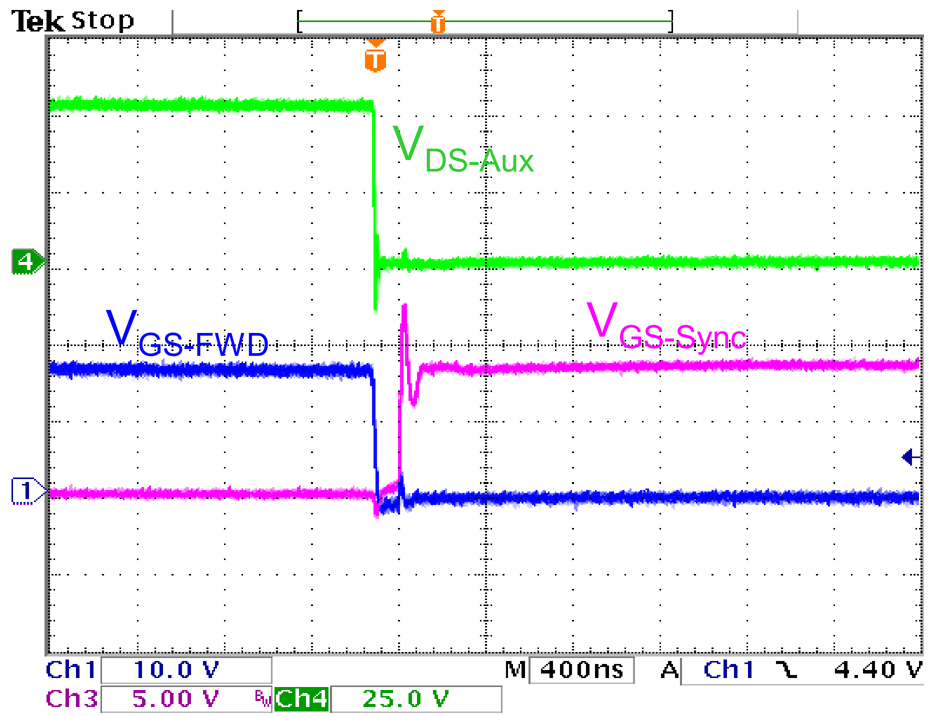
Delays in the Self-Driven Gate Drives



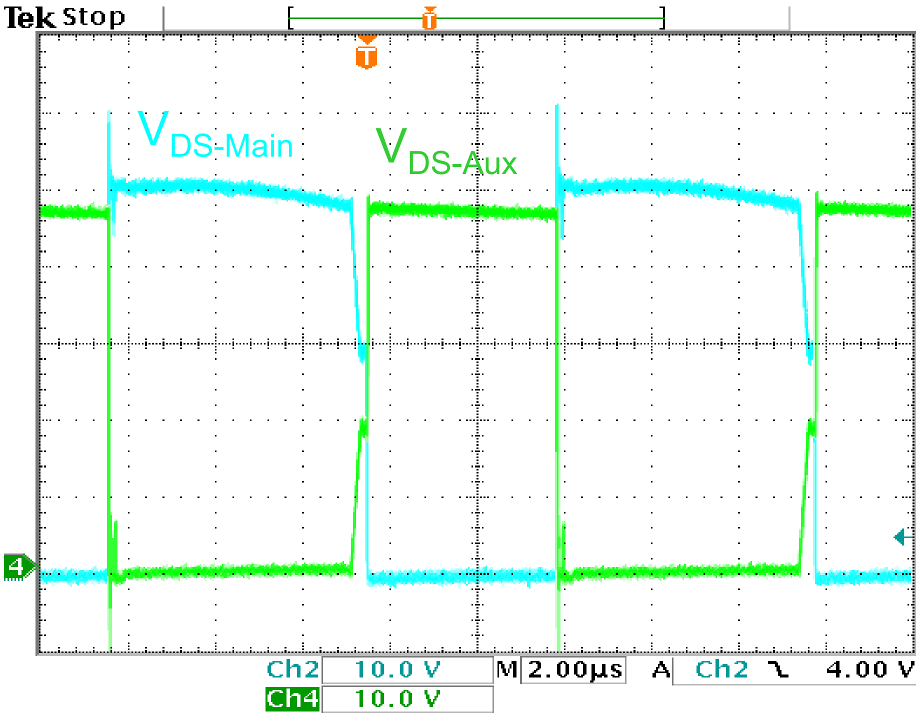
V_{IN} = 36V, I_{OUT} = 10A



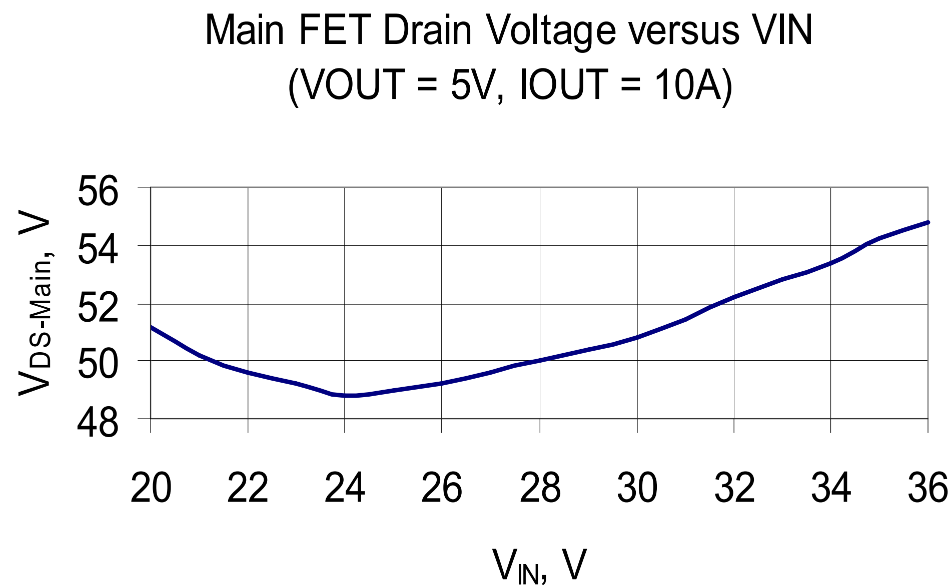
V_{IN} = 36V, I_{OUT} = 10A

- When the delays for the Main and Aux FET are set too high, large deadtimes are observed in the gate drives for the self-driven rectifiers. During the deadtimes, the antiparallel diodes conduct and efficiency decreases.

Drain-source Stress

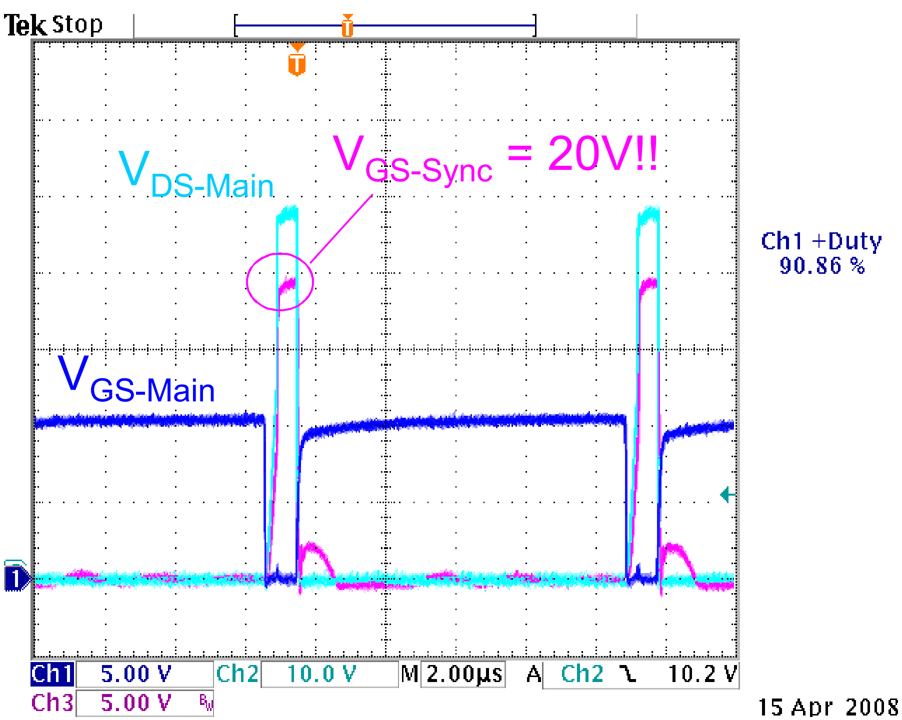


V_{IN} = 28V, I_{OUT} = 10A



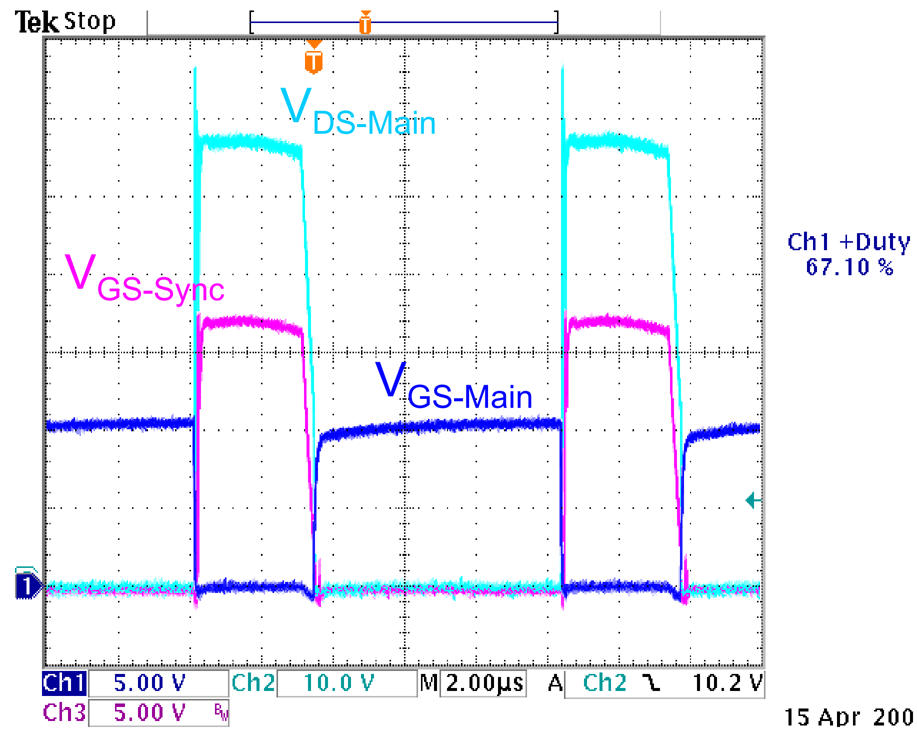
- Low drain-source stress for both FETs
- Drain-source stress is nearly constant

Duty Cycle Clamp



V_{IN} = 3V, I_{OUT} = 0A, D_{MAX} ~ 90%

- With no duty cycle clamp, the gate drive for the Sync FET on the secondary will be very high, even for low input voltage



V_{IN} = 17.6V, I_{OUT} = 10A

- With the duty cycle clamped to about 67%, the maximum gate drive for the Sync FET on the secondary is limited.

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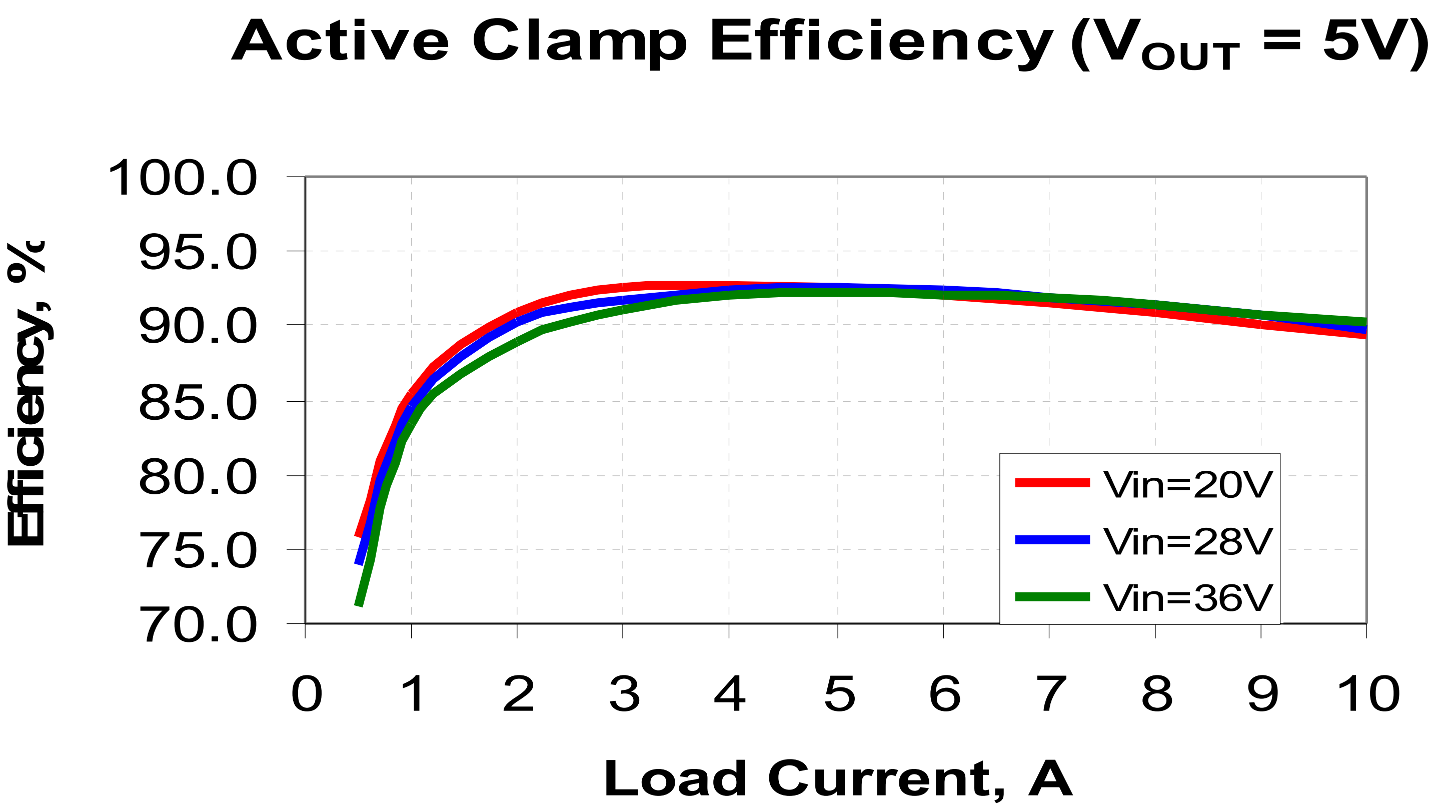
Efficiency of the Active Clamp



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Conclusions

- The circulating current from the magnetizing energy in the LC Snubber is relatively independent of load, resulting in lower efficiency at light load.
- The resonant resetting of the core in the LC snubber results in higher voltage across the main switch.
- The turns ratio of the synchronous gate winding is selected according to the maximum V_{gs} rating and the highest peak voltage across the primary winding.
- Although the LC snubber can achieve self-driven synchronous rectification, it needs Gate Charge Retention in order to approach the efficiency of the Active Clamp.

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Conclusions

- The gate drive timing in the Active Clamp requires a compromise between switching and conduction losses.
- The Active Clamp is very well suited to self-driven synchronous rectification.
- If the turns ratio (and range of duty cycles) is chosen well, the Main FET voltage stress will be low and nearly constant.
- The duty cycle should be clamped to limit voltage stresses.
- The Active Clamp can give efficiencies ≥ 90% from 20-100% of full load.

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