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High-Speed Connections for Storage Systems:
HIPPI, Fibre Channel, and ATM - Whats Happening?

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An ATM-Based Workstation Cluster Driving a HIPPI-Based HDTV Frame Buffer

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Abstract

A group of eight Digital Equipment Corporation Alpha workstations is interconnected with ATM to form a cluster with supercomputer power. For output, each workstation drives a single "tile" on an 8-tile high-resolution frame buffer. A special purpose adapter is used to convert the workstation's ATM format to the frame buffer's HIPPI format. This paper discusses the rationale behind the workstation farm, and then describes the visualization output path in detail. To provide the system quickly, special emphasis was placed on making the design as simple as possible. The design choices are examined, and the resultant system is described. The oral presentation will include operational experiences.

Introduction

Los Alamos National Laboratory is working with Digital Equipment Corporation to link advanced workstations into farms, or clusters, that provide the power of multi-million-dollar, massively parallel supercomputers. A goal of the project is to help establish workstation farms as a cost-effective alternative to expensive massively parallel systems. Most of the world's computing power is not in supercomputers, or even in workstations; it's in the personal computers that sit on everybody's desktops. The key to harnessing that tremendous amount of power is to connect them with a high-speed, cost-effective network, so they can be used as a single computing resource on a large, complex problem. This joint Los Alamos and Digital Equipment Corporation work emphasizes developing a communications network that binds together the central processing units of the independent workstations.

Because the compute job is divided into smaller, more manageable components and then processed in parallel, many complex computational problems can be solved in a fraction of the time it took only a few years ago. While massively parallel processing has provided significant advances over conventional computing, the limited number of massively parallel machines, and their high cost,

has prevented many computer scientists from tapping their benefits. It is felt that many more researchers can tap much of the power available in parallel processors by using farms of low-cost high-powered computer workstations.

System Architecture

Project plans included the use of Asynchronous Transfer Mode (ATM)[1,2] to interconnect eight Alpha workstations, and a High Definition television (HDTV) frame buffer display system for visual output. Figure 1 is a block diagram of the system.

The eight Alpha workstations are model number 3000/600S with a 175 MHz processor speed. Each has 64 MBytes of memory and 7.8 GBytes of disk. Each workstation is responsible for a single 512 x 512 pixel "tile" of the eight-tile output display, as shown on the right side in figure 1.

The ATM switch is a 20-port Digital Equipment Corporation AN2. Each switch port uses SONET OC-3c, 155 Mbit/s, ATM communications, over limited distance multi-mode fiber optic connections. Eight ports go to the Alpha workstations, eight ports go to the Adapter, and one port goes to a Digital Equipment Corporation GIGAswitch for communications with other Los Alamos networks.

The Los Alamos ATM-HIPPI Frame Buffer Adapter, called the "Adapter" for short, converts the ATM-format data received from the Alpha workstations into a High Performance Parallel Interface (HIPPI)[3,4] format to drive the frame buffer. HIPPI is an ANSI standard, has been in use since 1988, and is available on many vendor's high-end computing equipment. The Adapter is a custom hardware design built specifically for this project.

The PsiTech HFB360-24 HIPPI Frame Buffer, called the "HFB" for short, is a commercially available display system for use with high resolution display screens. A 1600 Mbit/s HIPPI physical interface is used between the Adapter and the HFB. PsiTech does not presently have an ATM interface for their system, but may offer one in the future.

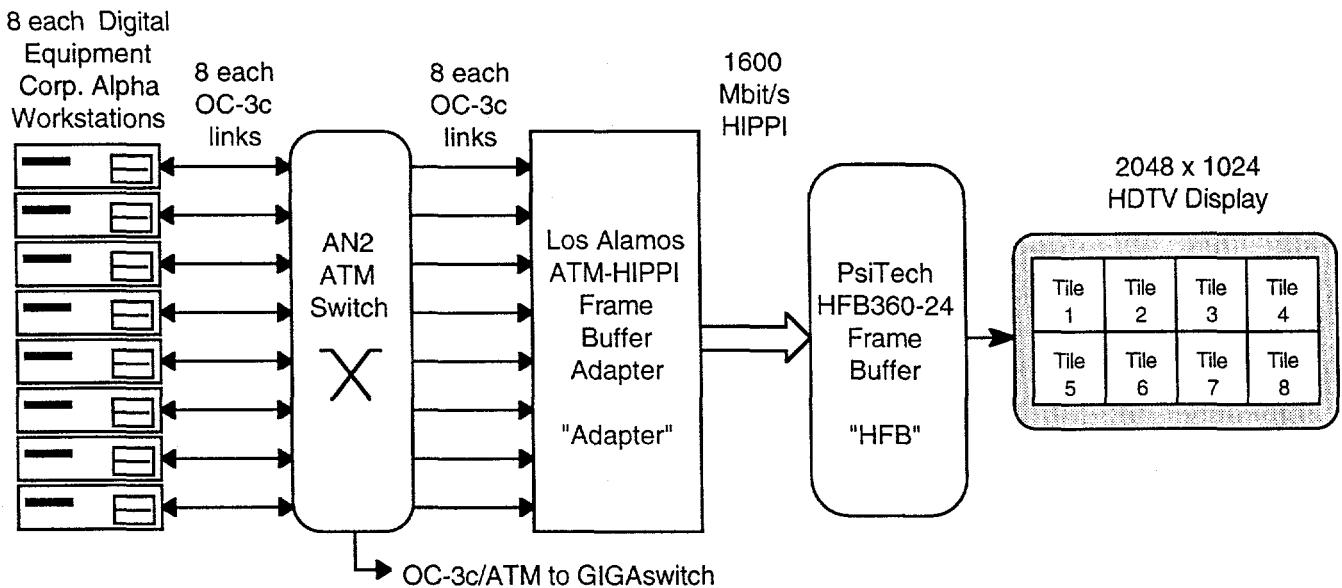


Figure 1. Overall system

The 2048 x 1024 HDTV-like display will be partitioned into eight tiles, each 512 x 512 pixels. The HDTV standards are not complete at this time, and seem to be going towards a 1920 x 1080 format. A 1920 x 1080 format was awkward with image compression, which operate on multiple 8 x 8 pixel cells. Hence, a 2048 x 1024 format was selected as being close to the HDTV proposal, but easier to implement.

Minimizing Bandwidth Requirements

A project goal is to display the information with the maximum resolution, and maximum frame rate, so the user can gain insight into the data being presented – the better the picture the greater the potential insight. Unfortunately, this is difficult to achieve because of data rate bottlenecks. For example, a 2048 x 1024 display, with 24-bit color per pixel, requires about 6.3 MBytes per frame. At 60 frames per second (fps) this translates into 378 MByte/s, or about 3 Gbit/s – much greater than can be sustained by any component in the system.

The Alpha workstations process the data in parallel, and store the partial results at each workstation. Maximum display performance could be achieved only if the data could also be transmitted and displayed in parallel. It would be a bottleneck if all of the data funneled through a single processor or communications path on its way to the display. The tack taken was to split the display screen into multiple "tiles", with each

workstation responsible for the data for that tile. Separate communications paths were used, coupling each workstation individually to the display system with a reasonable communications link speed, i.e., OC-3c at 155 Mbit/s.

Initially we will be limited to a maximum of 20 fps when using 24-bit color. 60 fps is possible with 8-bit color. The choke point is the OC-3c ATM bandwidth. This assumes that all eight workstations are transmitting at the full OC-3c rate simultaneously.

Joint Photographic Experts Group (JPEG)[5] data compression will be used in the future to effectively increase the data rate by requiring less data to be transferred through the system. Data compression also decreases the storage requirements on the workstations. JPEG compression will be done by software in the workstations, and decompression will be done by hardware in the PsiTech frame buffer. JPEG works on 8 x 8 pixel "cells", allowing multiple JPEG chips to be operated in parallel. Early experiments have shown that JPEG compression ratios of up to 7:1 do not cause significant picture degradation. The compression ratio will be variable to allow experimentation.

Motion Picture Experts Group (MPEG)[6] data compression was also considered since we are in essence transmitting movie data. At the time, the MPEG standards and integrated circuits did not address HDTV size displays. The possibility of using several MPEG chips, one for each tile, was

explored, but discarded due to a concern about picture artifacts at the tile boundaries. JPEG does not need to pass information between the 8 x 8 pixel cells, but MPEG does. If we increased the bandwidth by using multiple MPEG chips, then we would also need to pass this motion information between the chips, and we did not see a way to do it. Advanced algorithms and chips should allow future HDTV systems to use MPEG-2 with compression ratios better than that obtainable with JPEG.

Simplifying the Adapter Design

The display portion of the workstation farm is viewed as a proof-of-principle system with no plans for future commercialization. To provide the system quickly, special emphasis was placed on making the design as simple as possible. This led us to put many of the special features in the workstation software, which in turn made the final unit more flexible than if the features were wired into the hardware.

At the start of the project Los Alamos considered building the whole frame buffer, basing it on the design of a previous Los Alamos HIPPI-based frame buffer. That design had 1024 x 1024 pixels and 8-bit color. It was decided that in the interest of time and minimal complexity it would be better to purchase a commercial frame buffer rather than design one ourselves. A factor that contributed to this decision was that the resolution of the new system was about 6 times greater, i.e., 1024 x 2048 and 24-bit color. Hence, it requires a higher bandwidth, resulting in a tougher design and layout task. The design of a high-end frame buffer is a complex task even if you discount the bandwidth problems.

The workstation interfaces used ATM communications, and it would have been nice to use ATM throughout. Unfortunately, we were not able to find a suitable frame buffer system with an ATM interface. A frame buffer, capable of driving an HDTV display, was obtained from PsiTech Inc. Unfortunately, PsiTech did not offer an ATM interface, only a HIPPI interface. Hence, an "Adapter" to convert the multiple ATM streams from the workstations into a single 1600 Mbit/s HIPPI stream to the PsiTech HFB had to be designed and built. Los Alamos had considerable experience with HIPPI, and a large set of HIPPI test equipment. Hence, HIPPI in the middle of the system was not viewed as a major detriment.

While the PsiTech HIPPI Frame Buffer (HFB) had some extra features that would not be used in the final system, the extra features did not seem to

add significantly to the price or complexity. For example, the HFB provided a path to read out the contents of the internal display buffers, and to transmit graphical input from a pointing device like a mouse or trackball. By omitting the possibility of these operations that used a reverse direction data flow, a reverse direction communications channels could also be omitted.

Omitting the reverse direction ATM path — Once the idea of omitting a reverse direction data path was considered, we looked at what other features could not be supported if we did it. Switched virtual circuit (SVC) negotiation, Interim Local Management Interface (ILMI) used for status and control, and Operation Administration and Maintenance (OAM), need a reverse path. While SVCs, ILMI and OAM should probably be part of any commercial production system, it was felt that they were not required in this proof-of-principle system. Omitting them resulted in a major software reduction, and allowed a less complex processor to be used in each ATM interface, further simplifying the system and shortening the design cycle.

The workstations use UDP/IP (User Datagram Protocol/Internet Protocol) to transmit the data. UDP was chosen over Transmission Control Protocol (TCP) because UDP does not require return messages for ACK/NAK, and window control, further negating the need for a reverse data path. If a UDP packet is lost or errored, it is discarded rather than retransmitted. Like voice data, if the tile data is not present at the right time, it is better to ignore it and go on, than to delay everything while waiting for a retransmission.

We had originally planned for a feedback mechanism from the Adapter to the workstations to synchronize the workstations and keep the tile data from each workstation in frame-to-frame step. This also would have required a data path from the Adapter to the workstations. The workstations are now responsible for synchronization, either through close clock synchronization, or having a master workstation send periodic synchronization messages to the other workstations. By moving the responsibility for synchronization from the Adapter to the workstations, we removed the last barrier to deleting the return ATM path.

Hence, the Adapter's eight ATM interfaces were simplified by implementing the receive side only. Hooks were included for a transmit section if it was needed, but they do not seem necessary now. Figure 1 shows bi-directional ATM paths between the workstations and the ATM switch, allowing the workstations to communicate with each other. A

uni-directional path is shown from the ATM switch to the Adapter's ATM interfaces.

Protocols — ATM Adaptation Layer 5, (AAL5) was selected to carry the data from the workstations. Other possible choices were AAL1, AAL3/4. AAL5 seems to be the AAL most commonly used for computer data, and was originally intended for use with TCP/IP. AAL5 was also the easiest to implement. The AAL5 format allows ATM packets up to 64 KBytes in size.

The workstations use UDP/IP to transmit the data. Neither protocol is necessary for operation, they are just used since they are standards and readily available on the workstations. Hence, no return messages were required with UDP, and IP allows the messages to be routed in LANs if necessary. If UDP/IP were not used, some sort of special driver would have been required to pass the user data to the ATM interface in the workstation, and it would have probably been more work than using the available standards.

Using the UDP/IP protocols results in an 8-byte UDP header, and a 20-byte IP header, being added to the data packet from the workstation. No options are used, and the headers are always the same size, simplifying their removal. The Adapter removes these headers, without examining or using their contents, before sending the data to the HFB. This is another case where extra capability is available, but in the interest of simplicity it is not used.

ATM Virtual Circuits Identifiers (VCIs) are used for routing and addressing, and hence in this system the IP addressing and routing functions can be ignored. Each workstation sends its tile data to the Adapter using VCI = 1024. Which tile on the display the data is directed to is determined by XY coordinates in the HFB command at the beginning of each tile data set. Using a single VCI value allowed all of the Adapter's ATM boards to be hard coded with the same VCI value. Multiple tiles can be sent one at a time over a single OC-3c interface, but multiple tiles cannot be interleaved on a single OC-3c. This limitation made the Adapter design considerably simpler, and was deemed reasonable for this project.

Permanent virtual circuits (PVCs) are used in the ATM switch. The switch routing tables are set so that workstation 1's VCI = 1024 is routed to ATM interface #1 on the Adapter. Likewise workstation 2's VCI = 1024 is routed to ATM interface #2 on the Adapter, etc.

Minimizing the AAL5 processing — AAL5 includes a 32-bit cyclic redundancy check (CRC),

and a length field, in the 8-byte trailer of each AAL5 packet. While the workstation hardware will produce the CRC and length, the Adapter's ATM interfaces will toss the CRC without checking it. The length field is only checked to find the last AAL5 packet; the actual number of bytes received is not verified against the length parameter. Ignoring the CRC, and not verifying the AAL5 packet length, allowed the use of a complex programmable logic device (CPLD) for the ATM processing. Otherwise, using available ATM segmentation and reassembly (SAR) ICs would have required additional support hardware to configure and control the SAR IC. Further minimization included using a fixed format for the AAL5 packets with no pad bytes as discussed in section 5.

Ignoring the received CRC was based on the assumption that the communications circuits would be reliable, negating the need for checking. Random bit errors, resulting in CRC errors, should be extremely rare due to the short cable distances and benign machine-room environment. Likewise, lost cells due to congestion in the switch should not occur since no other ATM operations are going through the ATM switch at this time. Also, only permanent virtual circuits (PVCs) are used, giving the administrator the ability to completely control the interconnections. Detected errors will cause the associated tile to be discarded, resulting in the in the previous frame's information being re-displayed.

Data Flow

It is expected that the workstations will generate the visualization data one frame at a time, communicating with each other through the ATM switch. Each frame will be stored on the disks of the individual workstations. When complete, the data can be recalled from the disks, queued in memory, and the individual frames sent one after the other to the display as a movie.

A fixed AAL5 packet format is used for transmitting the data from the workstations. The workstation passes the first 9128 bytes of tile data to the software UDP driver, where an 8-byte UDP header is prepended to the data. The UDP driver in turn passes it to the IP driver where a 20-byte IP header is added. A maximum AAL5 packet data size of 9156 bytes was chosen to avoid potential IP packet fragmentation. For data sets longer than 9156 bytes, the first, and any intermediate AAL5 packets, are exactly 9156 bytes long. The last AAL5 packet of a data set is something other than 9156 bytes long to differentiate it from the other AAL5 packets.

When the Adapter receives an AAL5 packet with VCI = 1024, it reassembles the complete data set for the tile before passing it to the HFB. Any AAL5 packets with unknown VCIs are discarded. Reassembly involves discarding the first 28 bytes, i.e., the UDP and IP headers, and concatenating the data with the following AAL5 packets. The last AAL5 packet is marked by having other than 9156 bytes.

An AAL5 packet with 9156 bytes, plus the 8-byte AAL5 trailer and 4-byte pad, exactly fills an integral number of 48-byte ATM cell payloads. The 4-byte pad is used to align the data on 8-byte boundaries (the width of the HIPPI interface). Since the pad is always four bytes, except possibly on the last AAL5 packet, it is much easier to concatenate the ATM data to form the HIPPI packet, i.e., you do not have to throw away a variable amount of pad bytes. Also, a simple comparison on the Length field in the AAL5 Trailer tells whether this is the last AAL5 packet in the data set. If it is the last AAL5 packet, then the concatenated data set is queued to be sent to the HFB.

Figure 2 is a summary of the data flow from a workstation to the display. Each step, as numbered in figure 2, is explained in more detail below. Note that compression is not mandatory, it just reduces the volume of data transferred.

1) The user's software in the workstation does the scientific calculation and generates the raw graphics data for a single tile. In this example, a tile with 512 x 512 pixels, and using 24-bit color, will occupy about 786 KBytes. Note that it is possible to use 8-bit color, or other tile sizes, hence with different numbers of bytes.

2) The user's software in the workstation compresses the raw graphics data using the JPEG compression algorithm. Tests have shown that compression ratios of up to 7:1 do not degrade the picture quality significantly. This compression reduces the volume of data that must be stored on the workstation's disk and transmitted through the ATM interface.

After compression, the user's workstation software prepends a PsiTech HFB command to the front of this data block. All of the HFB commands are 16 bytes in length. For example, a command may give tile coordinates for the graphics data that follows.

The user's workstation software then prepends an 8-byte HIPPI Framing Protocol (HIPPI-FP)4 header ahead of the HFB command. The size of the data block is contained in the HIPPI-FP header.

3) The user's workstation software then segments the data block into multiple AAL5 payloads. Each payload is exactly 9128 bytes in length, except for the last payload of the data block that is shorter.

The value of 9128 bytes was chosen so that when an 8-byte UDP header and a 20-byte IP header were prepended, the total would exactly fill an integral number of ATM cells with a 4-byte AAL5 pad. The 9128-byte size was also chosen to ensure that IP packet fragmentation would not occur.

The last AAL5 payload is filled with zeros, if necessary, to exactly fill an integral number of ATM cells.

The user's workstation software then sends each AAL5 payload to the UDP/IP software driver. The resulting AAL5 packets for a particular tile are sent in the proper order, and as a contiguous set.

The UDP/IP drivers will prepend an 8-byte UDP header, and a 20-byte IP header. The contents of these headers are immaterial as they will be discarded by the Adapter. The AAL5 packets, containing the HIPPI-FP, UDP, and IP headers, will then be forwarded to the ATM interface.

4) The ATM interface will transmit the data according to the AAL5 specification, over a SONET OC-3c physical link.

AAL5 specifies that 48 bytes of data be placed in the payload of each 53-byte ATM cell. The last cell of the packet will include an 8-byte AAL5 trailer containing, among other things, a length parameter denoting the number of user bytes in the AAL5 packet, and a CRC-32 checksum. If the number of user bytes, plus the bytes in the AAL5 trailer, is not evenly divisible by 48, then pad bytes are used to fill out the last ATM cell, or possibly the last two cells. Note that by a careful choice of the AAL5 packet size, we have made sure that a consistent 4-byte pad will be used except on the last AAL5 packet of a HIPPI packet.

5) The Adapter, as shown in figure 1, receives the SONET OC-3c stream and extracts the ATM cells from the SONET payload. If a cell does not contain a known VCI, then the cell is discarded.

6) If this is the first cell of an AAL5 packet, then the 20-byte IP header, and 8-byte UDP header are discarded without looking at their contents.

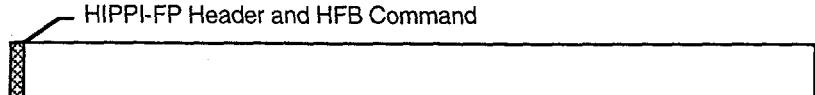
7) If this is the last cell of an AAL5 packet, then the AAL5 trailer length parameter is extracted and compared to 9156, i.e., (9128 bytes of data) + (20-byte IP header) + (8-byte UDP header). If the length parameter = 9156, then this is an intermediate AAL5 packet for the tile and the data is concatenated with other data, if any, for this tile. If the length parameter ≠ 9156, then this is the last AAL5 packet of the tile, and the full tile

Alpha Workstation -

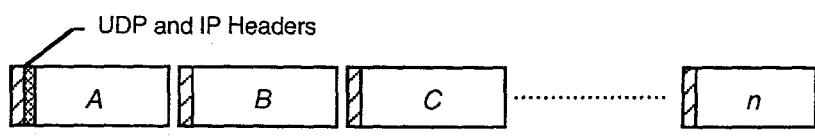
1) Software generates raw graphics for a 512 pixel x 512 pixel "tile" with 24-bit color = 786 Kbytes.



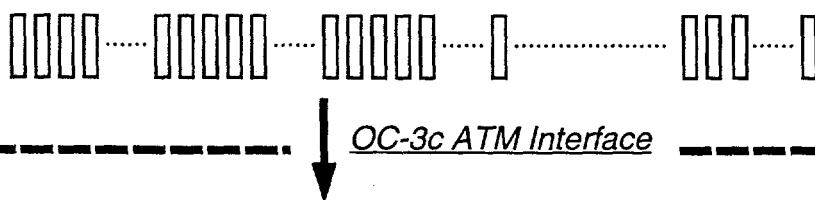
2) Software compresses the raw data approximately 7:1 with JPEG, to approx 112 KBytes, then adds a 16-byte HFB command and 8-byte HIPPI-FP Header



3) Software segments into approx 12 ea 9128-byte AAL5 payloads. Software UDP/IP drivers add 8-byte UDP header and 20-byte IP header to each AAL5 packet.



4) ATM interface segments each AAL5 packet into approximately 191 each 53-byte ATM cells. Then encapsulates the ATM cells in a SONET OC-3 stream.

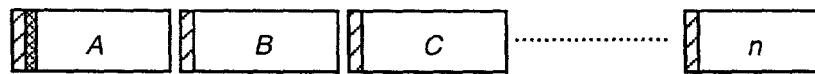


Los Alamos ATM-HIPPI Adapter -

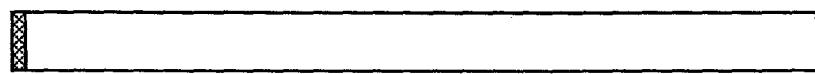
5) Receives the SONET OC-3 stream and extracts the ATM cells.



6) Reassembles the ATM cell payloads into AAL5 packets.



7) Discards 8-byte UDP header and 20-byte IP header. Reassembles the AAL5 payload into a HIPPI packet of compressed data. Re-arranges the bytes, and sends the HIPPI packet to the HFB.



PsiTech HIPPI Frame Buffer -

8) Receives the HIPPI packet of compressed data, uses HIPPI-FP header, then discards header



9) Decompresses the JPEG stream and displays the original tile data



Figure 2. Data segmentation and reassembly

data will be queued for transmission from the Adapter to the HFB.

8) The HFB uses the HIPPI-FP header values to determine the actual number of bytes in the HIPPI packet. The HIPPI packet header is stripped off in the HFB.

9) The HFB decompresses the data using the JPEG decompression algorithm implemented in hardware. The resultant pixel data is stored in the load buffer.

An Update Image Buffer command is sent from the workstations to transfer the pixel information just sent, and stored in the HFB's load buffer, to the HFB's display buffer. A single Update Image Data command is sent to update the whole screen, i.e., it is independent of the number of tiles used. The Update Image Buffer command may be sent by any of the workstations, but must be timed so that it occurs after all of the tile data has at least started transferring to the Adapter. Timing is the responsibility of the workstations; there is no feedback from the Adapter or HFB to the workstations.

Adapter Hardware Implementation

The Adapter is built using a modular design. Each ATM channel is located on a plug-in card with commercial ASICs providing the SONET and ATM layer processing. A specially designed CPLD provides the streamlined AAL5 processing. Initialization and monitoring of the channel is exercised by an on-board microprocessor which also provides a serial interface for connecting to a personal computer (PC). The AAL5 packets

are processed (i.e. UDP/IP headers and AAL5 trailers are removed) as they are received with minimal buffering, and then the processed data is placed in a small byte-wide FIFO. Each ATM channel card plugs into a PC-like motherboard containing additional memory buffers, double-wide HIPPI logic, and control logic.

The byte-wide data stream from each of the eight channels is assembled into packets in that channel's separate 4 MByte buffer memory. "Packets" at this level are HIPPI packets that may be either the data set for a display tile or a command for the PsiTech frame buffer. When a packet is complete, it is forwarded on to the PsiTech frame buffer at double-wide HIPPI speed. With data compression, the packet lengths may vary; a packet sequence of first started, first forwarded is followed to keep the packets in order. Other than a few simple length checks to capture gross errors (the packet is assumed to consist of an

integral number of 64-bit words), the content of the packets is ignored by the adapter memory controller. This gives workstation software complete control of the PsiTech frame buffer, and allows flexibility for experimentation at the software level without hardware changes. The 4 MByte/channel memory allows double buffering of packets up to twice the expected normal packet maximum.

Summary

This joint project between the Los Alamos National Laboratory and Digital Equipment Corporation is using ATM as the interconnection mechanism for a "farm" of eight Alpha workstations. The workstations function as a parallel multiprocessor, generating graphics images for visualizing the results of scientific computations. A special ATM to HIPPI Adapter is used to convert the ATM formatted data to HIPPI format to drive an HDTV display. The display screen is organized as eight separate tiles, with each workstation responsible for a single tile. JPEG compression will be used to reduce the amount of data stored and transmitted, allowing the display frame rate and resolution to be increased to the maximum supportable by the frame buffer. Simplifications involving the protocols, packet formats, and ATM processing, drastically reduced the Adapter's complexity, hardware components, and time-to-implement.

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