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Steps toward on chip integration of single electron devices with CMOS electronics

Kevin Eng

Sandia Team:

Tom Gurrieri, Doug Trotter , Kent Childs, Jason Hamlet, Ralph Young, Erin Longeria, James Levy, Jin Kim, Mike Lilly, Malcolm Carroll

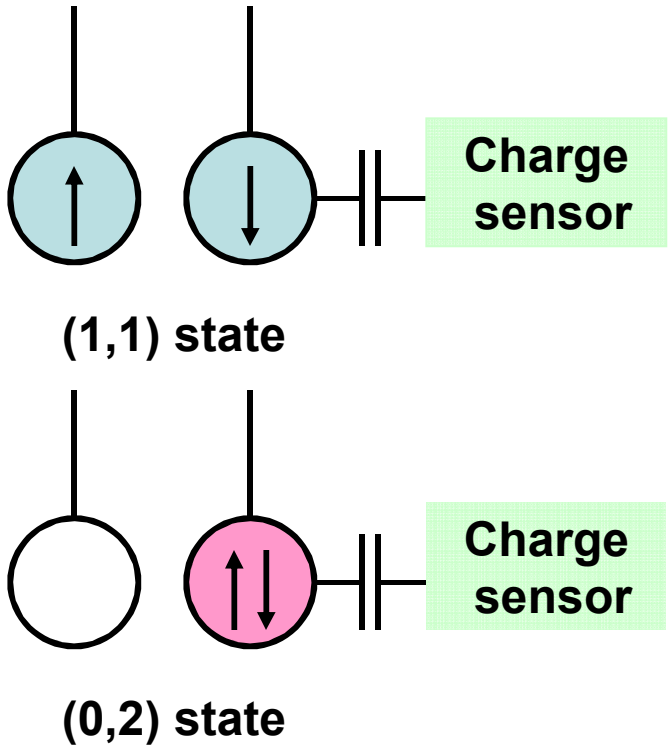
Talk after:

"Classical CMOS Electronics for Logical Qubits"

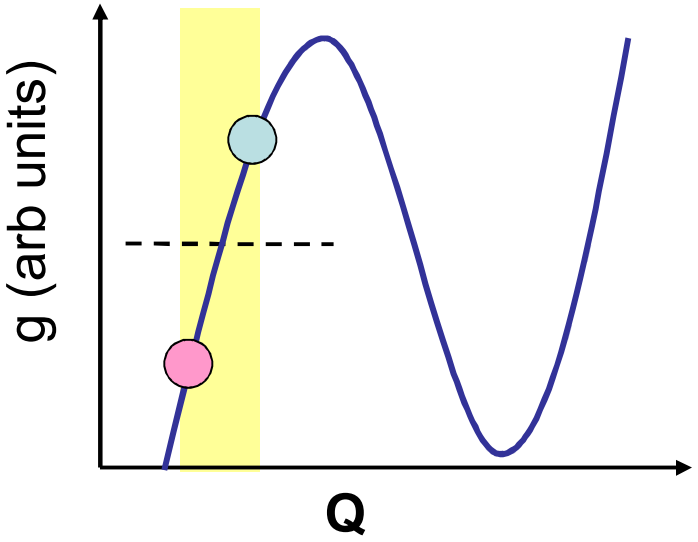
Tom Gurrieri & James Levy

Introduction: Charge Sensing

Example: In a Double quantum dot (DQD), the state of the qubit is read through a charge sensor that is capacitively coupled



Typically SET has conductance resonances that strongly depend on charge on the island



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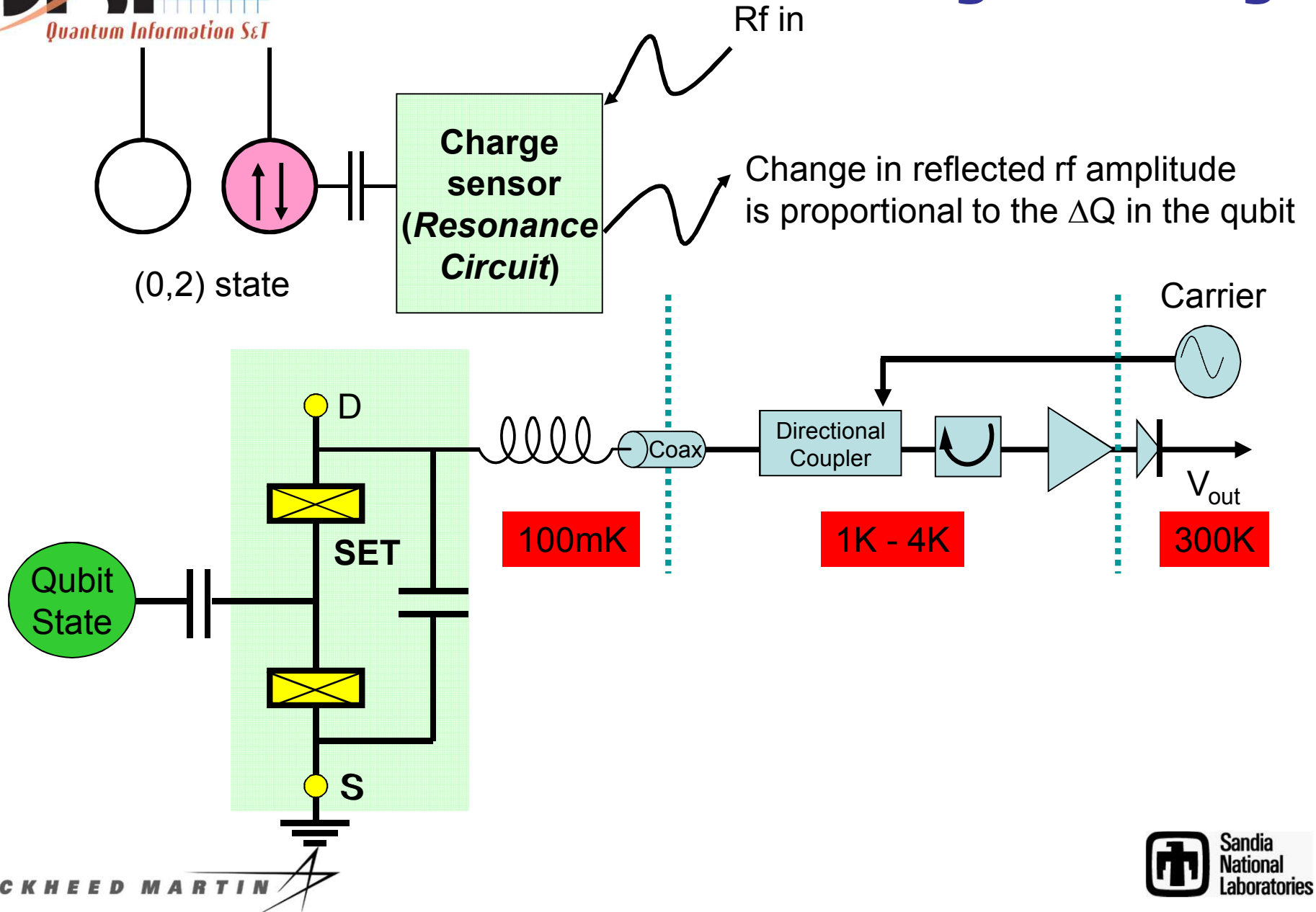
Introduction: rf charge sensing



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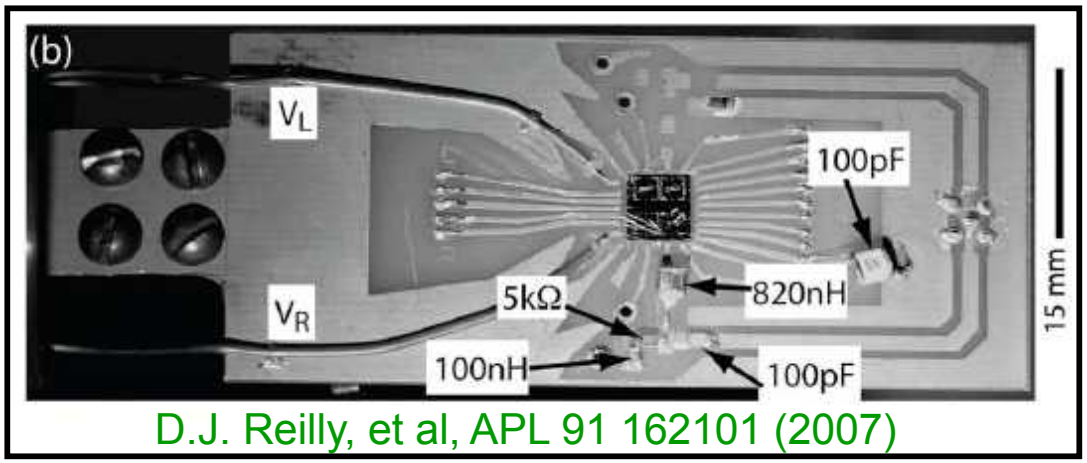
RF SET or QPC

- **Micro-second readout**
  - ***Limited by carrier frequency and Q of tank circuit***



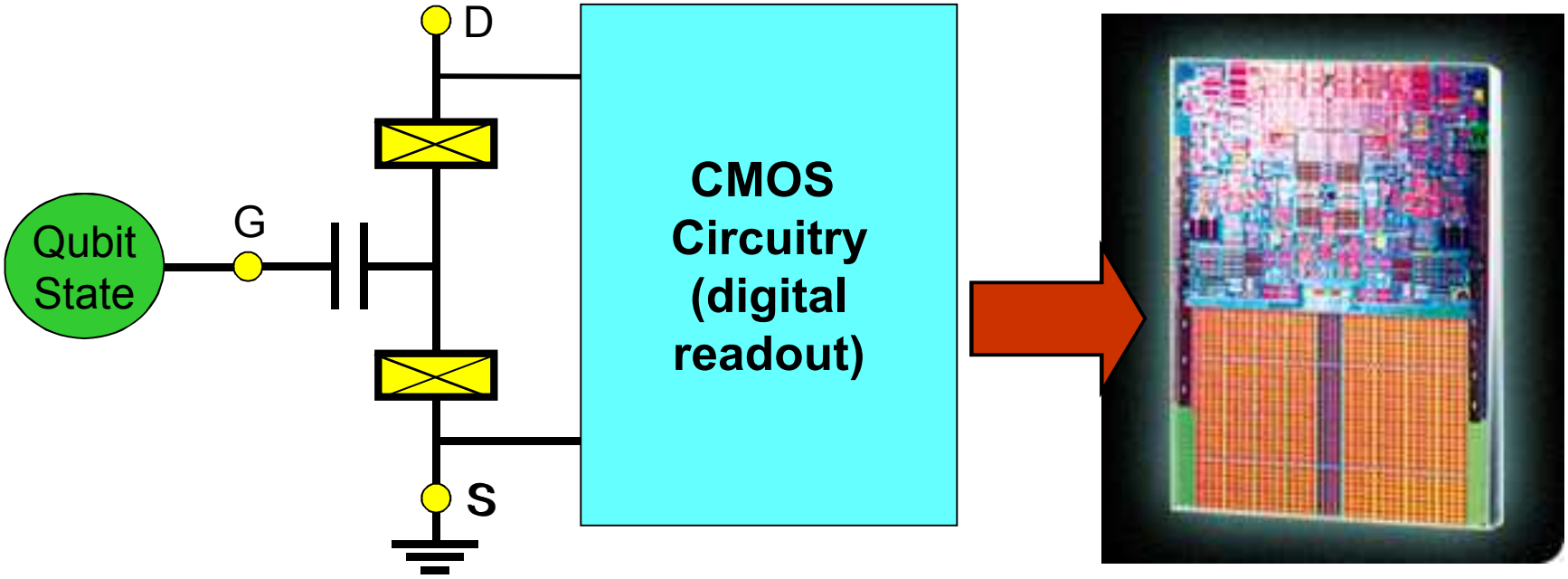
D.J. Reilly, et al, APL 91 162101 (2007)

- **Requires relatively high power (μW) dissipating discrete components**

- **Physical area required produces challenges to implementing to many physical qubits**

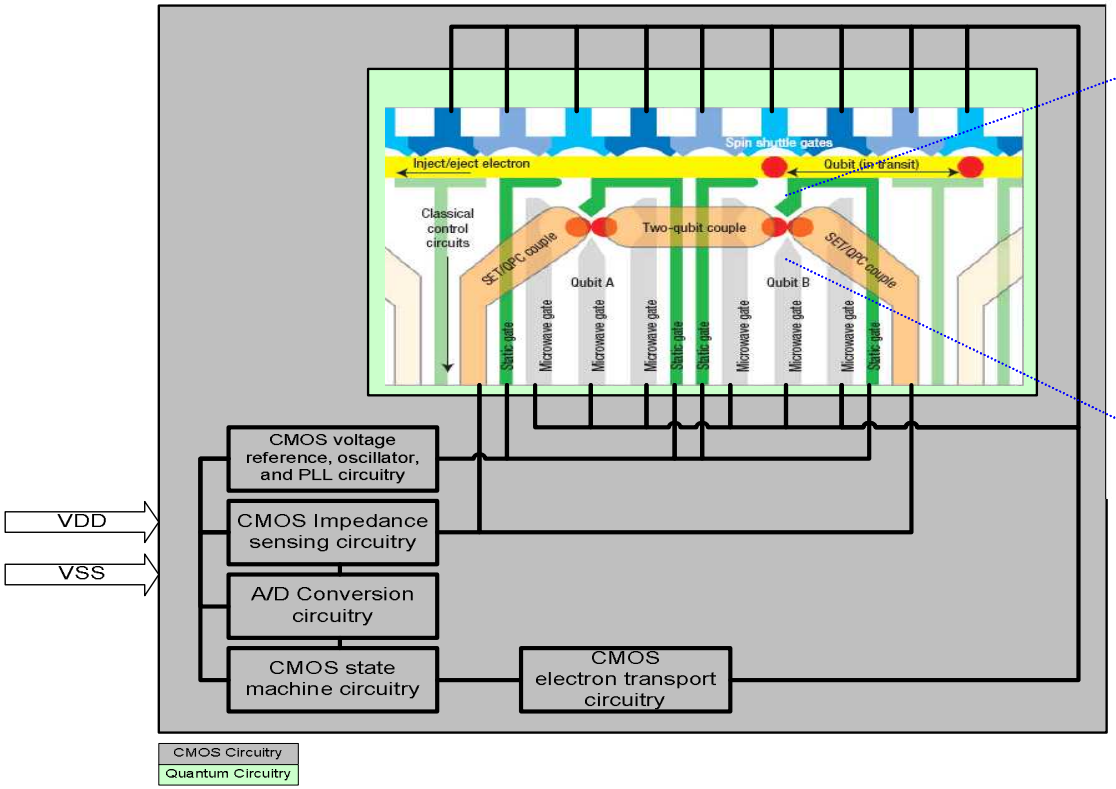
Alternative solution

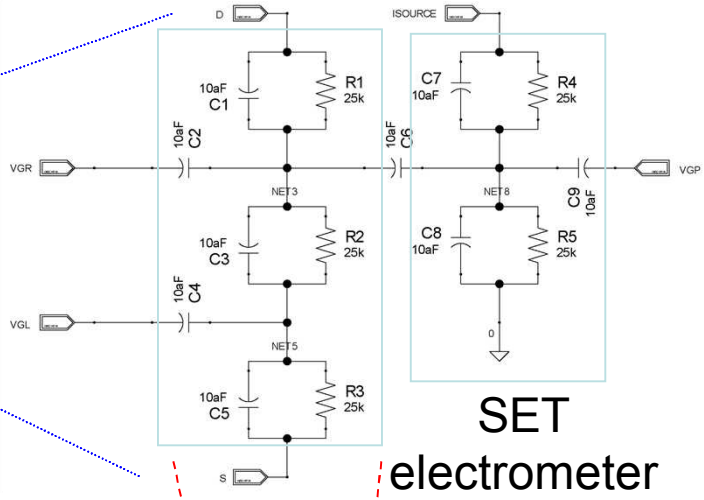
Readout integrated on chip

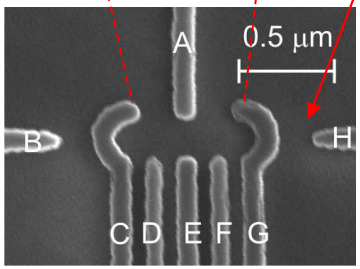


- *On chip integration of readout allows easier scaling to logical qubit*
- *Power & speed (?) will be discussed by Tom*

Classical to Quantum Interface







- CMOS electronics required for logical qubit:
  - Control of quantum circuits
  - Read-out & sensing circuits
  - Rapid decision for conditional states (logic & memory)
- Integration of CMOS with Si quantum devices (SETs) required

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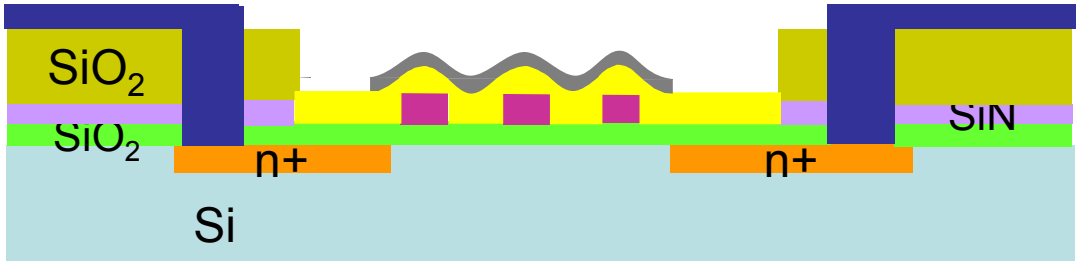
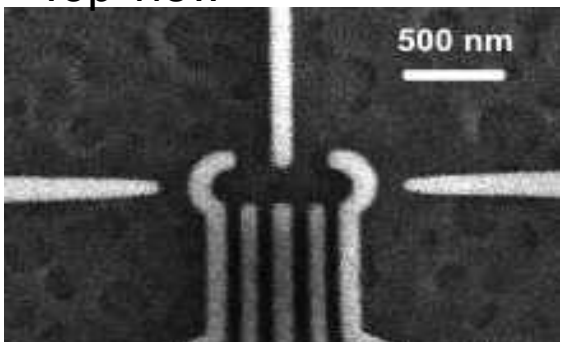
Integration ?

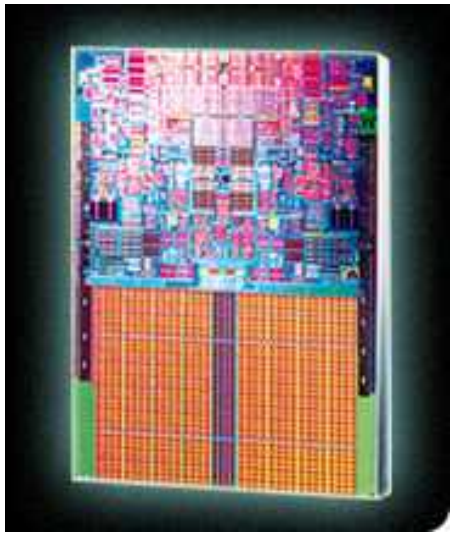
Cross-section



Top view



Single electron devices



+ operate at 100mK

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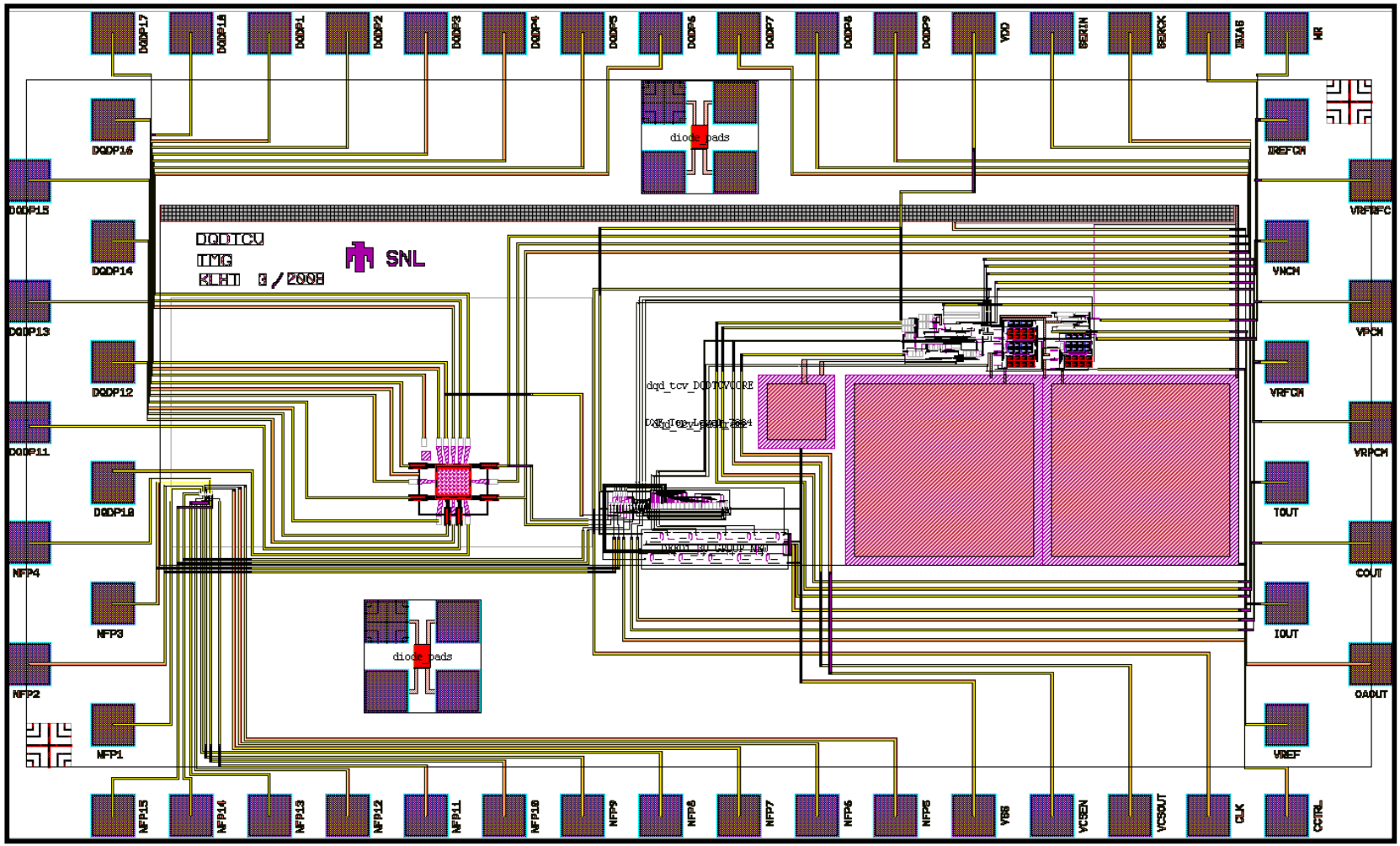
Single electron device design integrated with CMOS process

Fabrication started ~4/1/08



Quantum Information S&T

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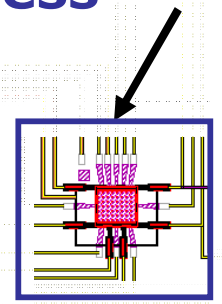
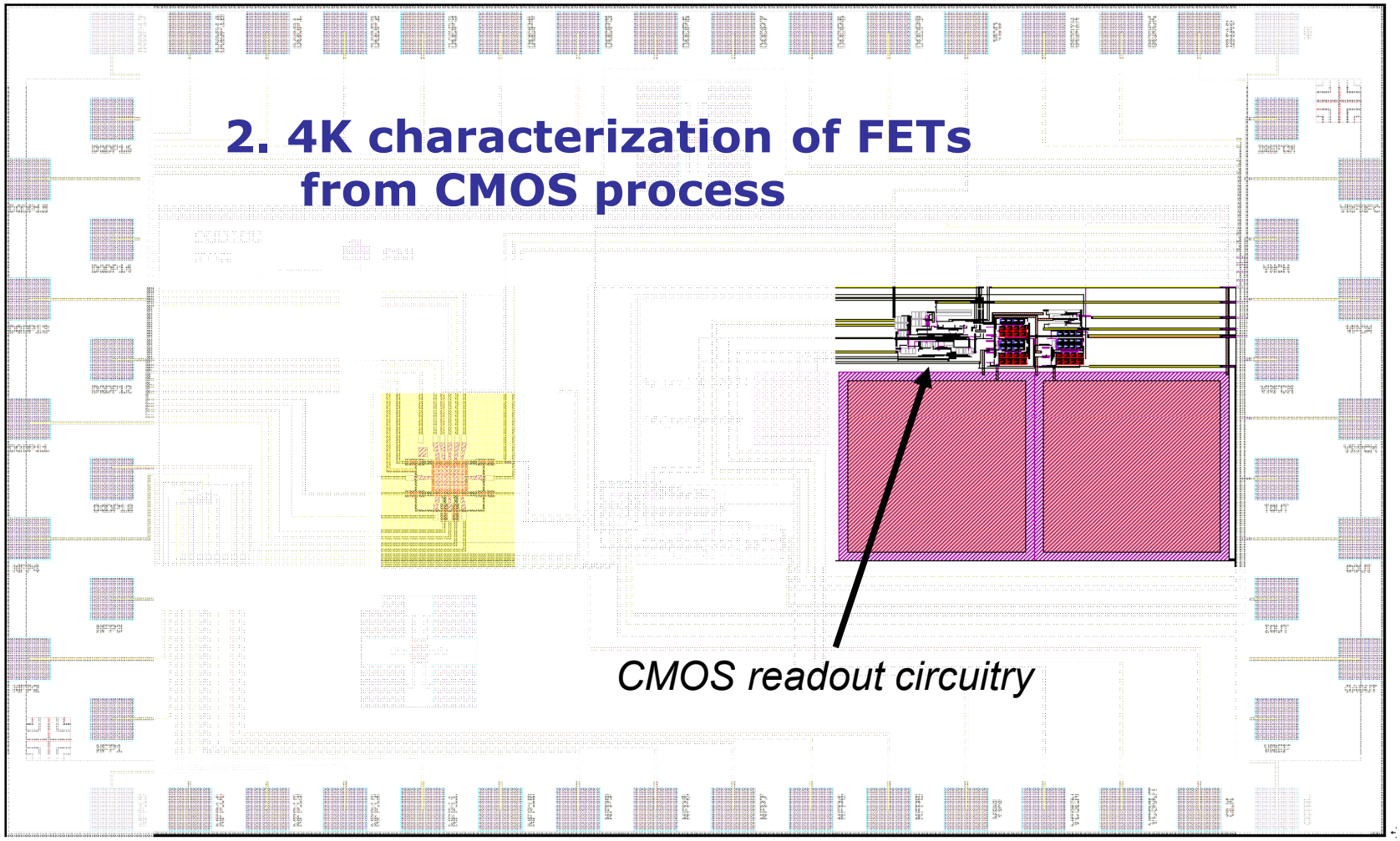
Outline

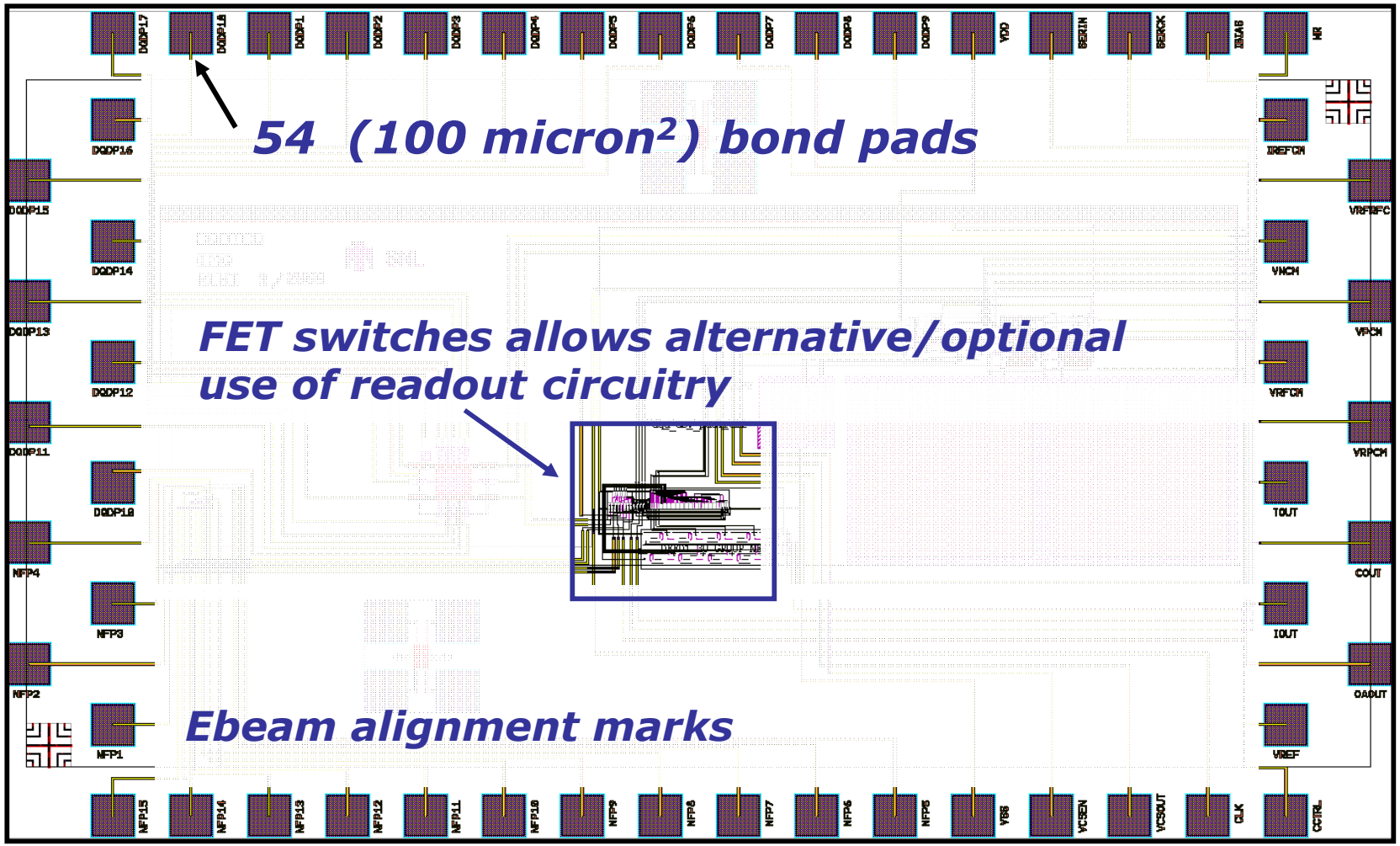
1. Integration of single electron device design process with Sandia's CMOS process



Outline


2. 4K characterization of FETs
from CMOS process
CMOS readout circuitry

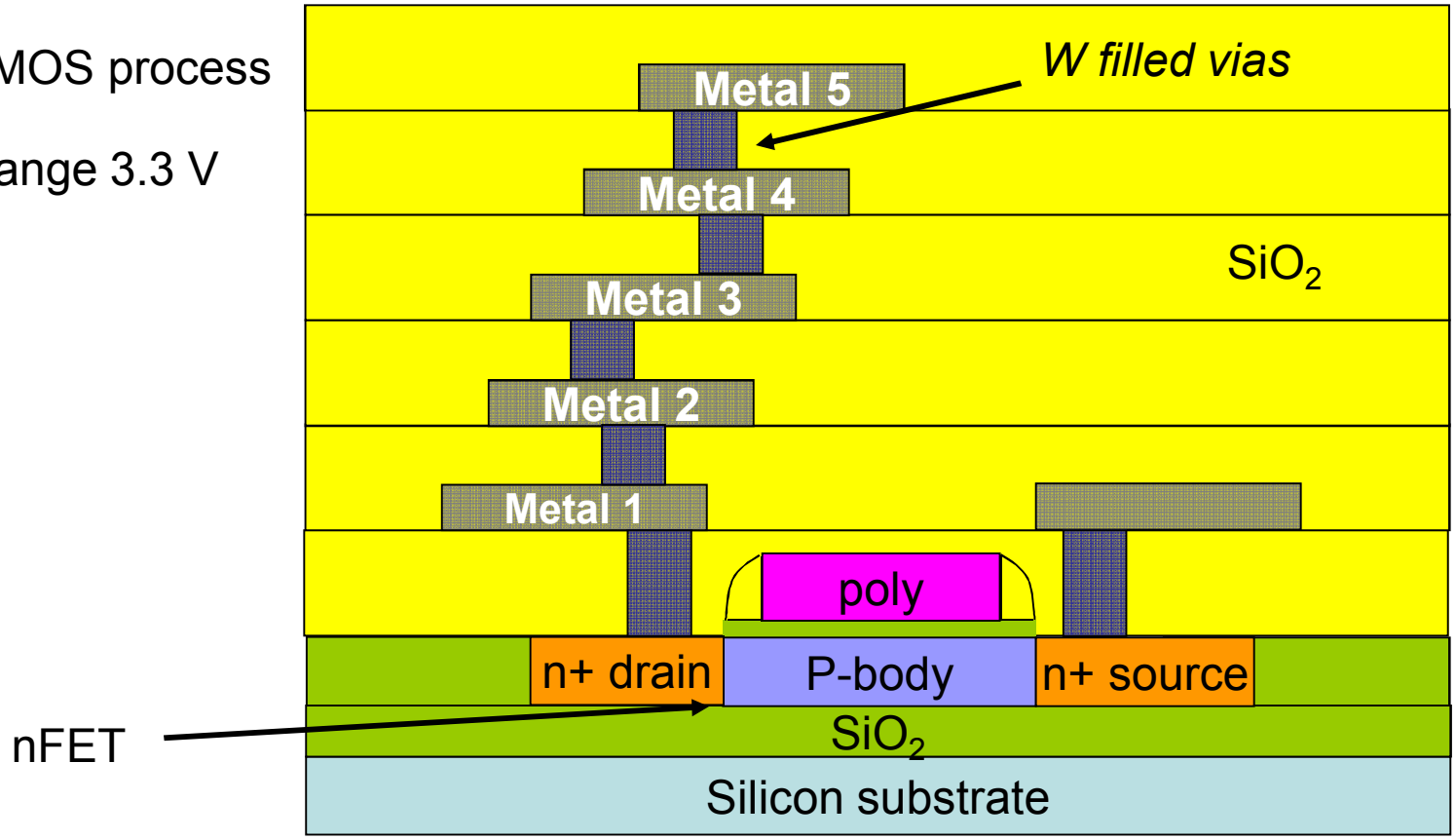
Key Design Features



Sandia's CMOS process

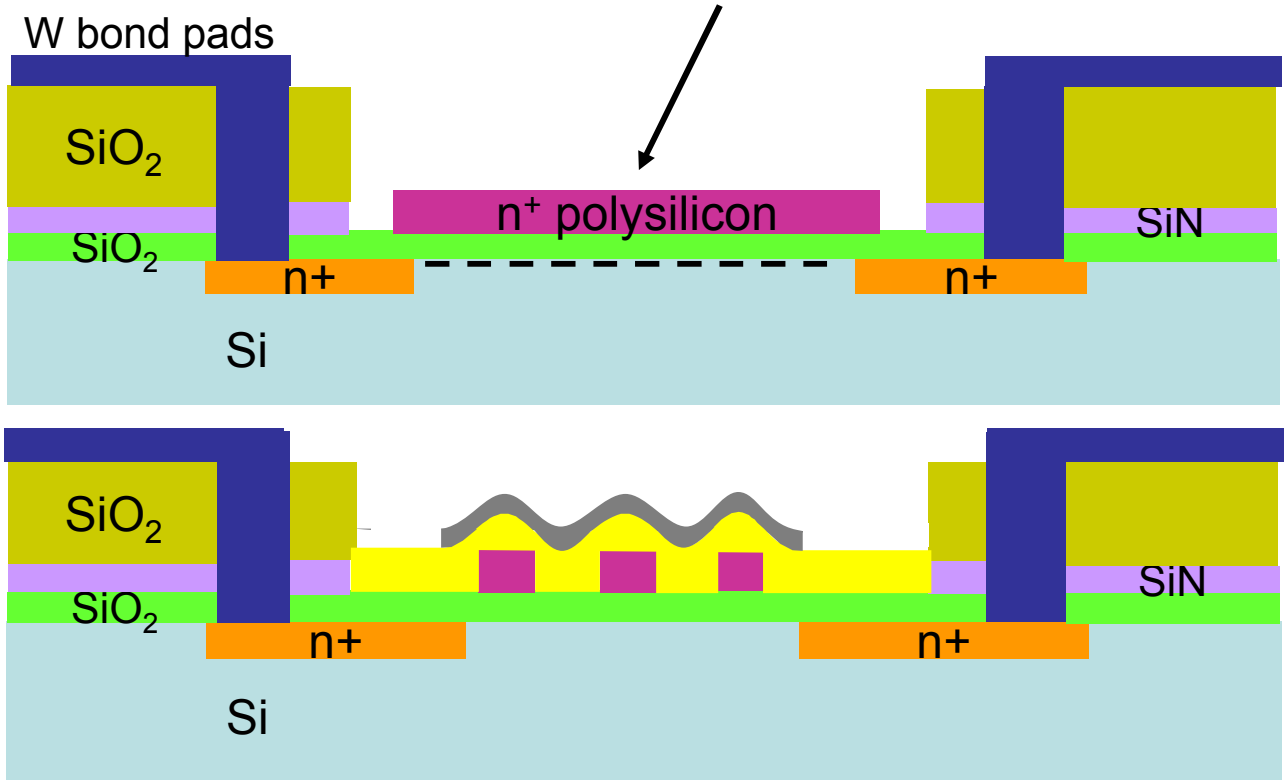
0.35 mm CMOS process

Operation range 3.3 V



Requirements for integration

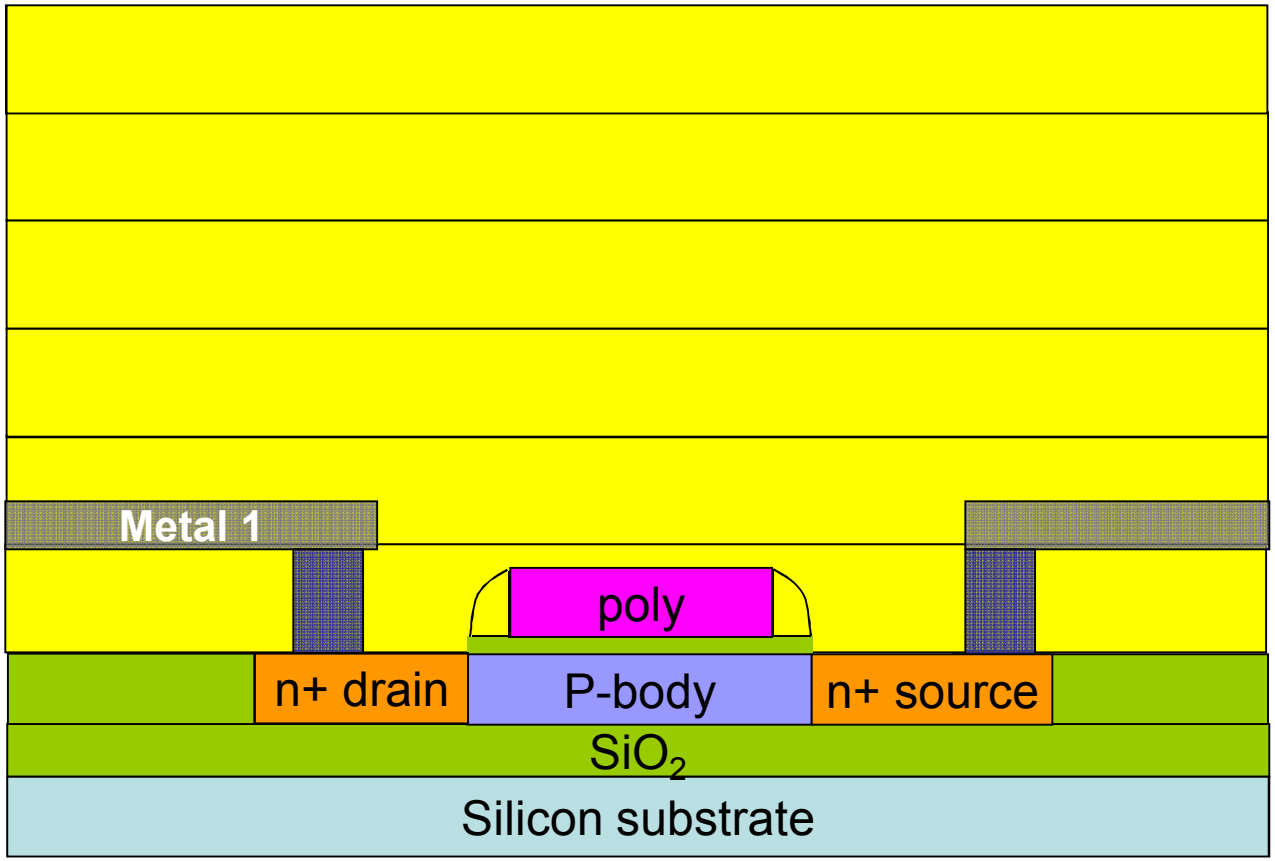
1. ***Need access to polysilicon in order to pattern via ebeam***



2. ***Block implants of dopants that will add unwanted impurities***

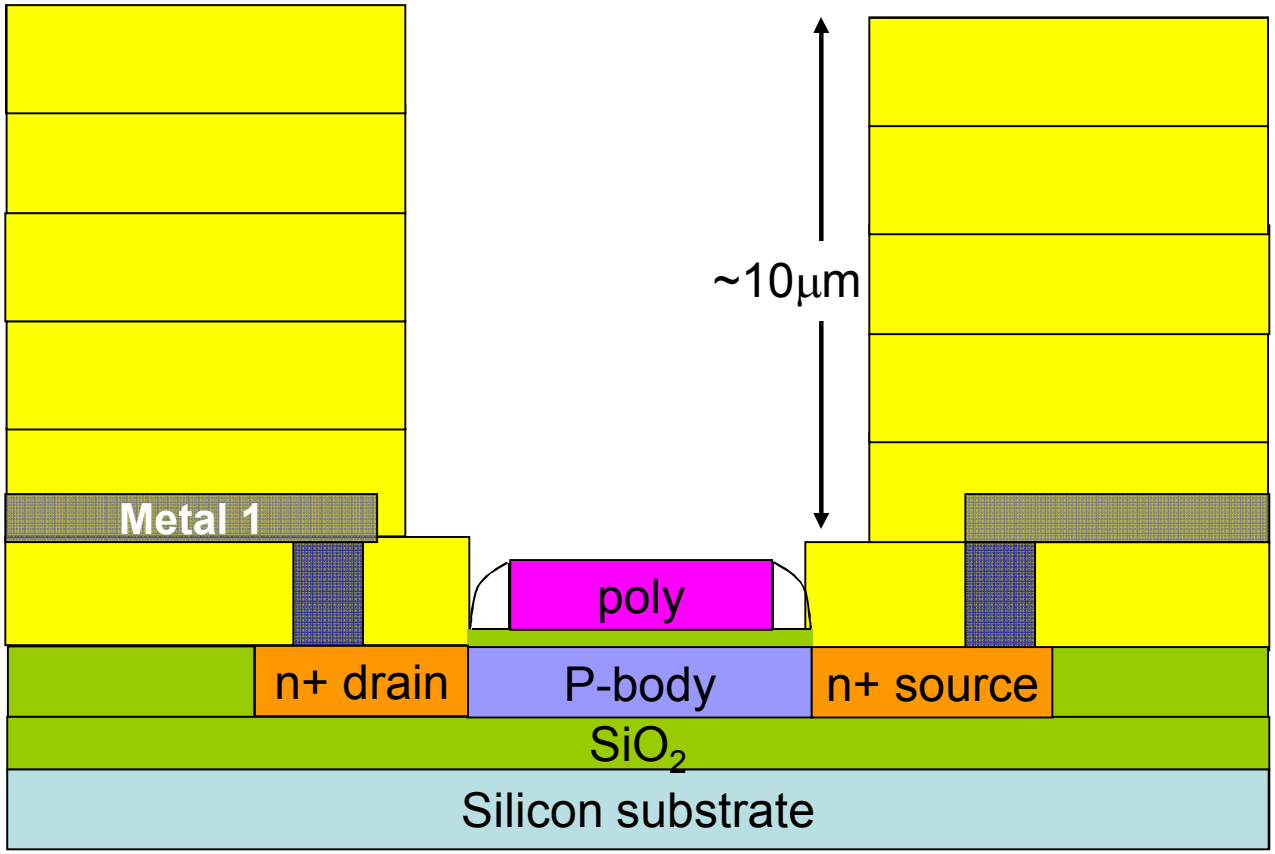
Integration of single electron devices with CMOS

Routed circuitry only using metal 1 & polysilicon



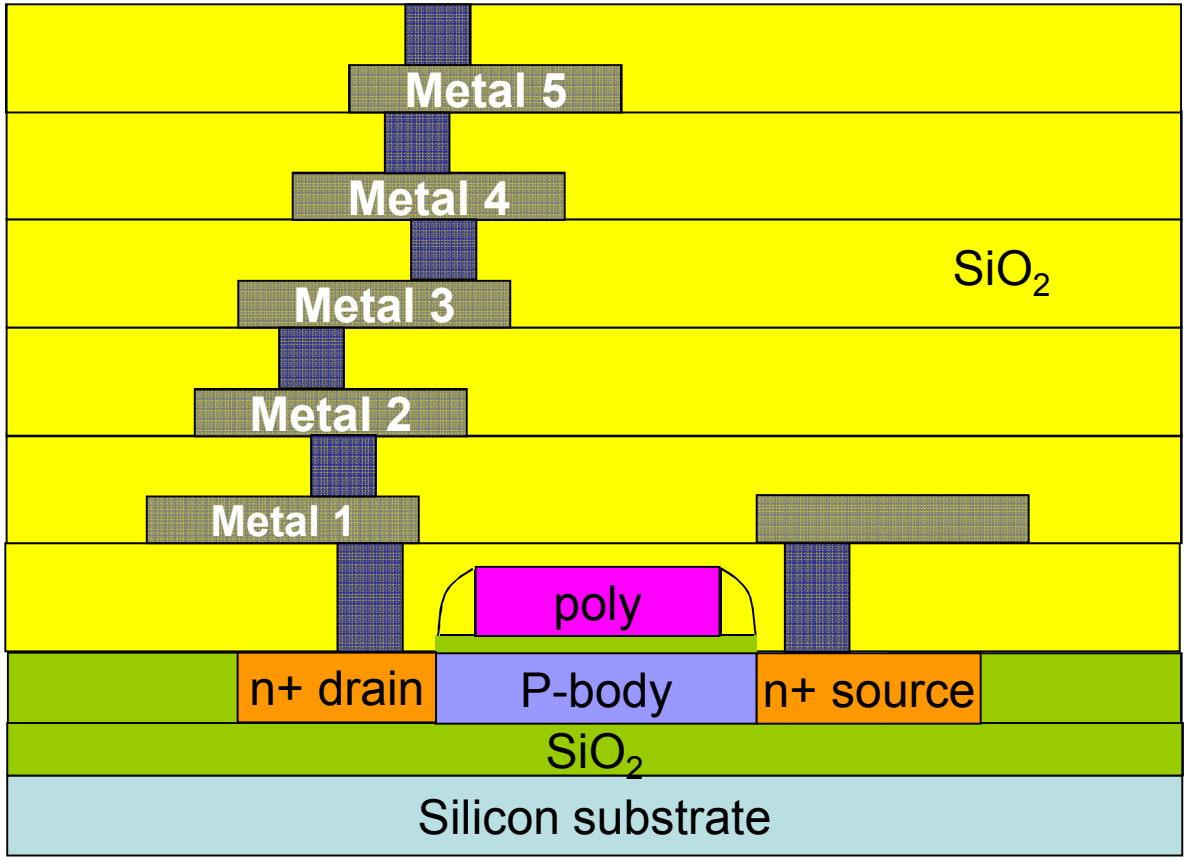
Integration of single electron devices with CMOS

Dry etch window to polysilicon gate



Alternative integration

Josephson junction circuits



CMOS at 4K

Advantages of low temp operation:

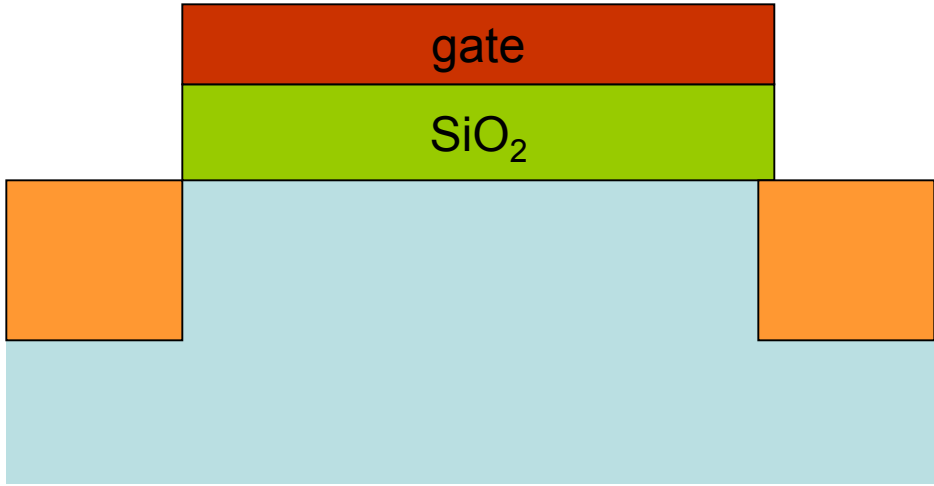
- Increase in operational speed:
  - *increase carrier mobility*
  - *reduction in wiring resistance*
  - *junction capacitance*
- Reduction in subthreshold swings
- Reduced thermal noise

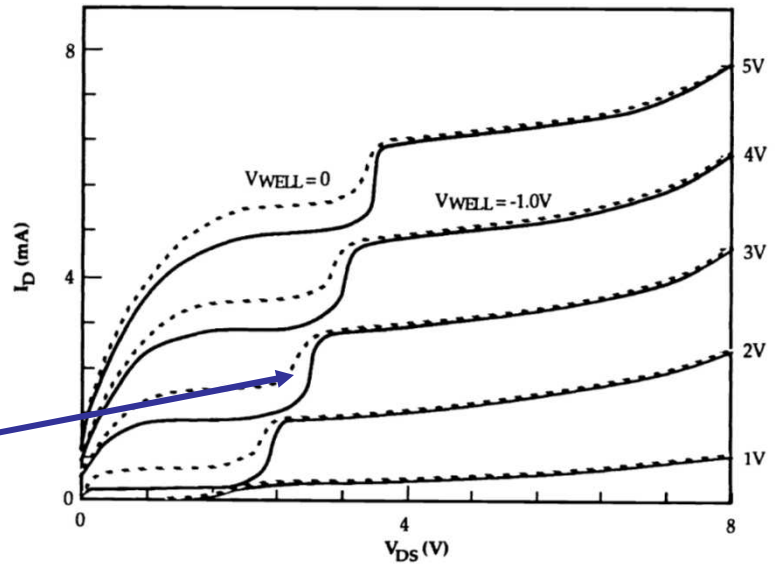
Disadvantages:

Freezeout of dopants

Hot carrier effects (impact ionization)

Kink effect

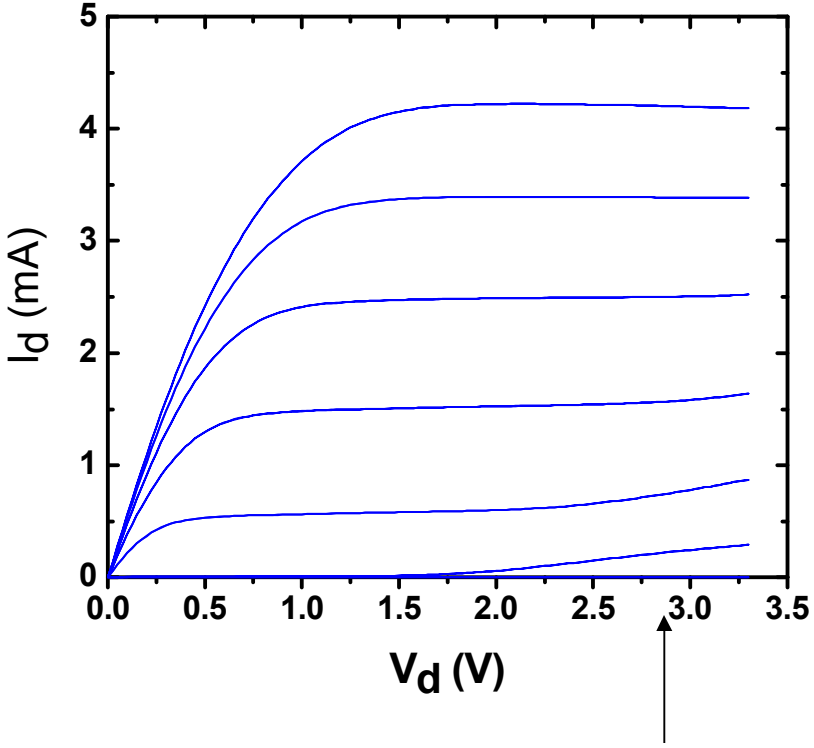


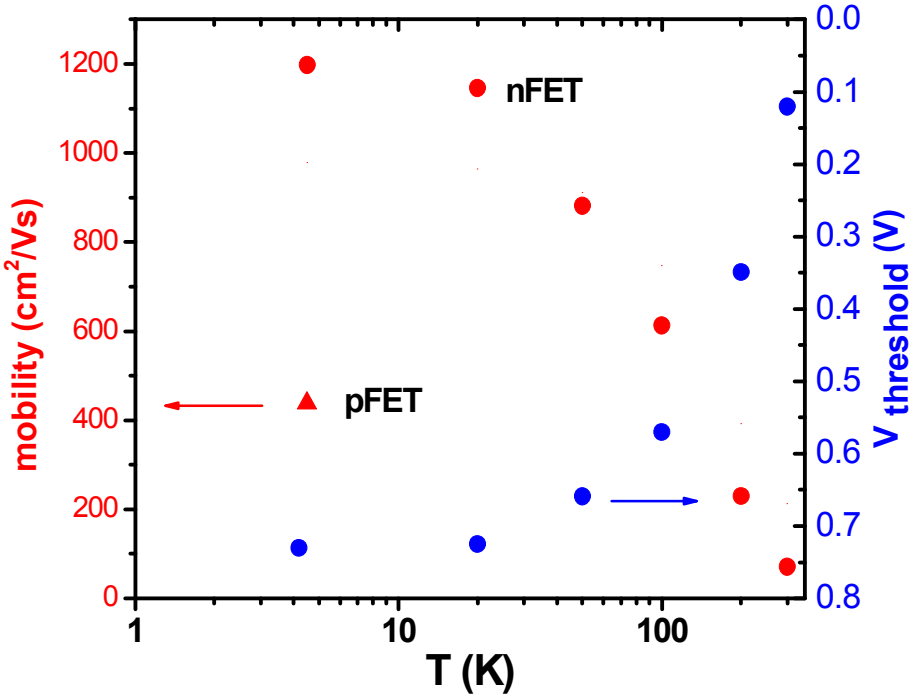


Add reference

CMOS characterization at 4K

Preliminary measurements show FETs work at T= 4K





(Need to add more temp traces)

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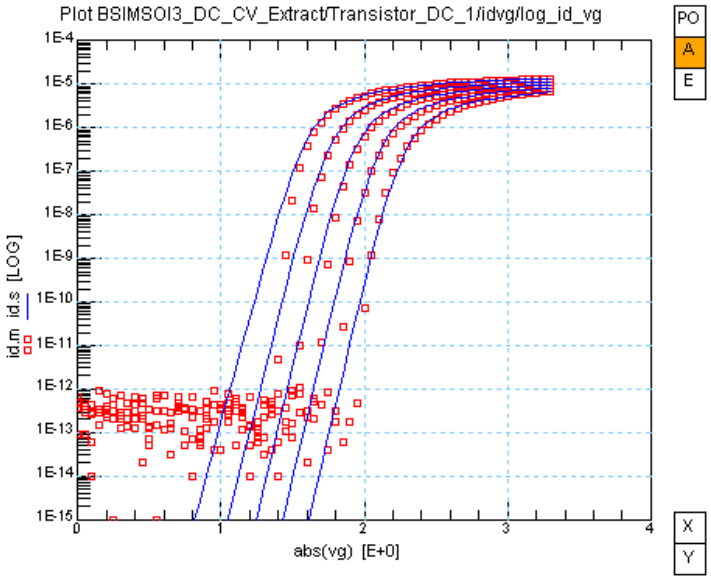
Modeling cryogenic CMOS

In process of performing spice modeling at Sandia



Device physics modeling down to 100mK will be performed at:

Optimization of designing IC working at 100mK -4K

Continue work will include:

- *100mK characterization*
- *High frequency measurements*
- *Noise*
- *Power consumption*

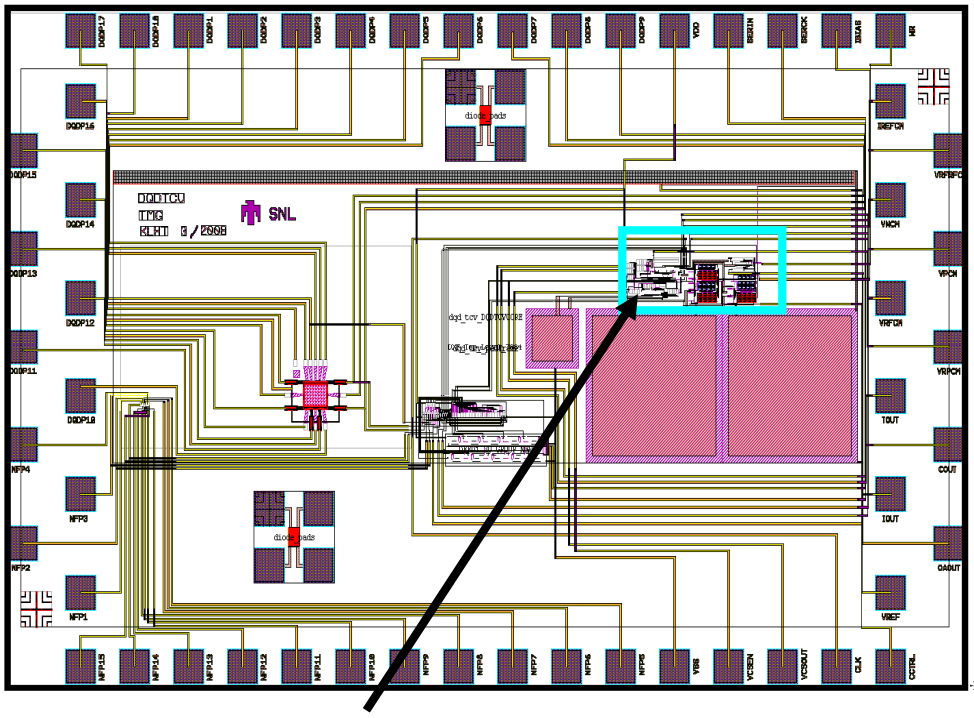
Summary

- **Integrated single electron design into Sandia's CMOS process**

Each has its own process flow which will be optimized in parallel.
Have integrated amplifiers within the single electron device process flow

- **Fabrication will be completed this summer**
- **Basic components (FETs) of readout circuit operate at 4K & will be tested down to 100mK**

End Goal is general cryo-CMOS (100mK< T<4K) capability for custom Si based quantum device integration



Tom will discuss the design and operation of the readout circuits

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