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CHARACTERIZATION OF SOI MEMS SIDEWALL ROUGHNESS

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ABSTRACT

Deep reactive ion etching (DRIE) of silicon enables high aspect ratio, deep silicon features that can be incorporated into the fabrication of microelectromechanical systems (MEMS) sensors and actuators. The DRIE process creates silicon structures and consists of three steps: conformal polymer deposition, ion sputtering, and chemical etching. The sequential three step process results in sidewalls with roughness that varies with processing conditions. This paper reports the sidewall roughness for DRIE etched MEMS as a function of trench width from 5 μm to 500 μm for a 125 μm thick device layer corresponding to aspect ratios from 25 to 0.25. Using a scanning electron microscope (SEM), the surfaces were imaged detecting an upper region exhibiting a scalloping morphology and a rougher lower region exhibiting a curtaining morphology. The height of rougher curtaining region increases linearly with aspect ratio when the etch cleared the entire device layer. The surface roughness for two trench widths: 15 μm and 100 μm were further characterized using an atomic force microscope (AFM), and RMS roughness values are reported as a function of height along the surface. The sidewall roughness varies with height and depends on the trench width.

INTRODUCTION

A wide variety of microsystems devices such as microactuators [1], optical switches [2], accelerometers, and nanopositioners [3] are fabricated with DRIE using SOI (silicon on insulator) materials due to the high aspect ratios that can be achieved [4]. DRIE silicon etching is commonly referred to as Bosch etching and was patented by Lärmer and Schlip [5]. A thorough review of DRIE high aspect ratio silicon etching is presented by Wu et al. [6]. In SOI MEMS fabrication, the initial wafer has three layers: a single crystal silicon substrate wafer, a thin thermally grown silicon dioxide layer referred to as the buried oxide, and a mechanically thinned single crystal silicon layer called the device layer. A DRIE process enables high-aspect ratio, deep etching of features in silicon wafers using repeated cycles of conformal polymer deposition, ion sputtering, and chemical etching of the silicon. DRIE can be performed on either side of the initial wafer enabling the fabrication of MEMS structures from the device layer and removal of the substrate underneath them [7].

One of the issues for DRIE SOI MEMS is sidewall roughness of the structures fabricated from the device layer. The sidewall roughness impacts mechanical characteristics such as the fracture strength [8-11] and adhesion and friction behavior of structures [12-16]. Recent work has shown that fracture strength depends on the roughness, in particular the deepest flaw size [11]. Earlier investigations of SOI MEMS reported on sidewall roughness [17-20] but a comprehensive study on the effects of etched trench width (aspect ratio) on the roughness characteristics is not known to the authors.

This paper reports sidewall characteristics for SOI MEMS with trench widths from 5 µm to 500 µm for a 125 µm thick device layer corresponding to aspect ratios from 25 to 0.25. A sidewall characterization die was designed and fabricated at Sandia National Laboratories. The SOI wafers had a 125 µm thick device layer and contained ten trench widths: 5, 10, 15, 20, 25, 50, 75, 100, 300, and 500 µm. SEM and AFM characterization of the sidewalls for the varying trench widths are presented.

SIDEWALL CHARACTERIZATION TEST STRUCTURE DESIGN AND FABRICATION

To investigate the effects of trench width on the sidewall roughness, a sidewall characterization die was designed with three characterization surfaces as shown in Fig. 1. The green lines designate etched trenches in the 125 µm device layer, the red lines specify trenches etched in the backside handle wafer for die singulation, and the blue lines show metallization for labeling the die location on the wafer and trench distances. After singulation, there are four pieces of the sidewall characterization die. Section 1 has ten trench widths: 5, 10, 15, 20, 25, 50, 75, 100, 300, and 500 µm, corresponding to a maximum aspect ratio of 25 and a minimum aspect ratio of 0.25. Section 2 contains five trench widths: 5, 15, 25, 75, and 300 µm, aspect ratios from 25 to 0.42. The trench widths and corresponding aspect ratios for Sections 1 and 2 of the sidewall characterization die are listed in Table 1. The trench in Section 3 is initially 5 µm wide and then increases linearly to be 500 µm wide. The SOI sidewall characterization structures were fabricated from a wafer with a 550 µm thick substrate wafer, a 2 µm buried oxide layer (BOX), and a 125 µm thick device layer. On top of the device layer, gold was deposited and used for labeling.

As implemented for this investigation, the DRIE process consisted of three steps lasting for a total of 5.4 seconds in a PlasmaTherm SLR770 inductively coupled plasma (ICP) etch tool. The first step was a 1.7 seconds Ar/C_4F_8 plasma deposition (30 sccm Ar, 100 sccm C_4F_8) with minimum bias (10 V) applied to the wafer. The second step was a 2.2 seconds Ar/SF_6 step to remove the halocarbon gas and deposit polymer at the bottom of the etched feature (30 sccm Ar, 100 sccm SF_6, 750 V bias applied to the wafer). The third step was 1.7 seconds of the main Ar/SF_6 etch (30 sccm Ar, 250 sccm SF_6, 50 V bias applied to the wafer). This three-step cycle was repeated until the Si device layer was cleared to the underlying BOX.

TEST FIXTURE

A fixture was designed to position and secure the pieces of the sidewall characterization during imaging. The sections of the sidewall characterization die are oriented upwards exposing the device layer, buried oxide layer, and supporting substrate in the thickness direction, with a total thickness of 677 µm. Figure 2 shows a schematic of the test fixture, and Fig. 3 is a picture of the fixture containing three sidewall test structure sections. The test fixture uses spacing washers and a clamping screw to hold the sections so that the etched device layer is exposed. At the bottom of the fixture is a mounting post that is compatible with the scanning electron microscope (SEM) stage. The mounting post is removable, and the fixture was used without the post during the atomic force microscope (AFM) characterization.

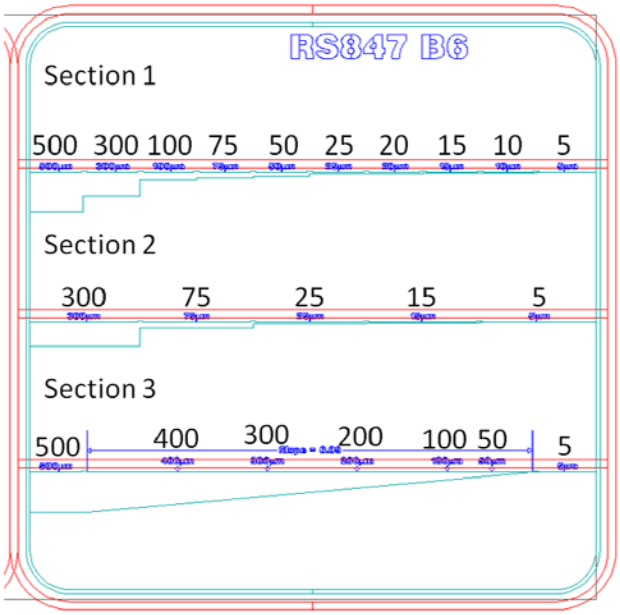


Figure 1: Schematic of the SOI die design containing the sidewall characterization surfaces. The green lines outline etched trenches in the 125 µm device layer, the red outlines trenches etched in the backside handle wafer for die singulation, and the blue shows metallization for labeling. The black labels indicate the trench widths in microns for the three die sections with characterization surfaces. The resulting section dimensions are roughly 1.9 mm wide.

Table 1: Trench widths and aspect ratios for Sections 1 and 2 of the sidewall characterization die.

Section 1		Section 2	
Trench Width	Aspect Ratio	Trench Width	Aspect Ratio
5 µm	25	5 µm	25
10 µm	12.5	15 µm	8.33
15 µm	8.33	25 µm	5
20 µm	6.25	75 µm	1.67
25 µm	5	300 µm	0.42
50 µm	2.5		
75 µm	1.67		
100 µm	1.25		
300 µm	0.42		
500 µm	0.25		

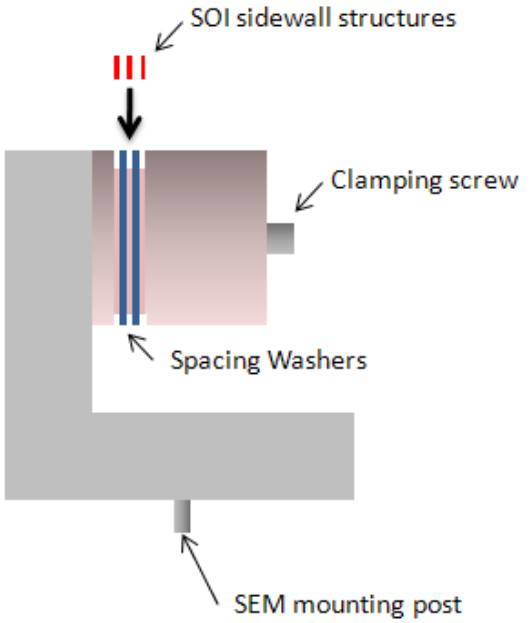


Figure 2: Schematic of the fixture used to hold the sections of the sidewall characterization die vertically in place during SEM and AFM imaging.

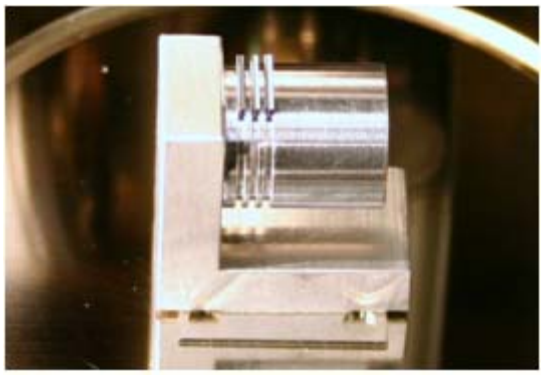


Figure 3: Image of fixture containing three sections of a sidewall characterization die.

SCANNING ELECTRON MICROSCOPE (SEM) IMAGING RESULTS

An objective of this study was to determine the effects of trench width on the SOI device layer sidewall roughness from DRIE. Two Section 2 surfaces which have five trench widths were imaged using an SEM. One of the die came from the center of the wafer; the other was located closer to the edge of the wafer. No discernible differences were observed based on die location on the wafer. Two Section 1 die with ten trench widths were then imaged. Characteristic SEM images for smaller trench widths: 10 µm, 15 µm, and 25 µm are shown in Fig. 4, and characteristic SEM images for larger trench widths: 50 µm, 100 µm, and 500 µm are shown in Fig. 5. The SEM images pictured in Figs. 4 and 5 are from Die C7, Section 1, a die location near the center of the wafer.

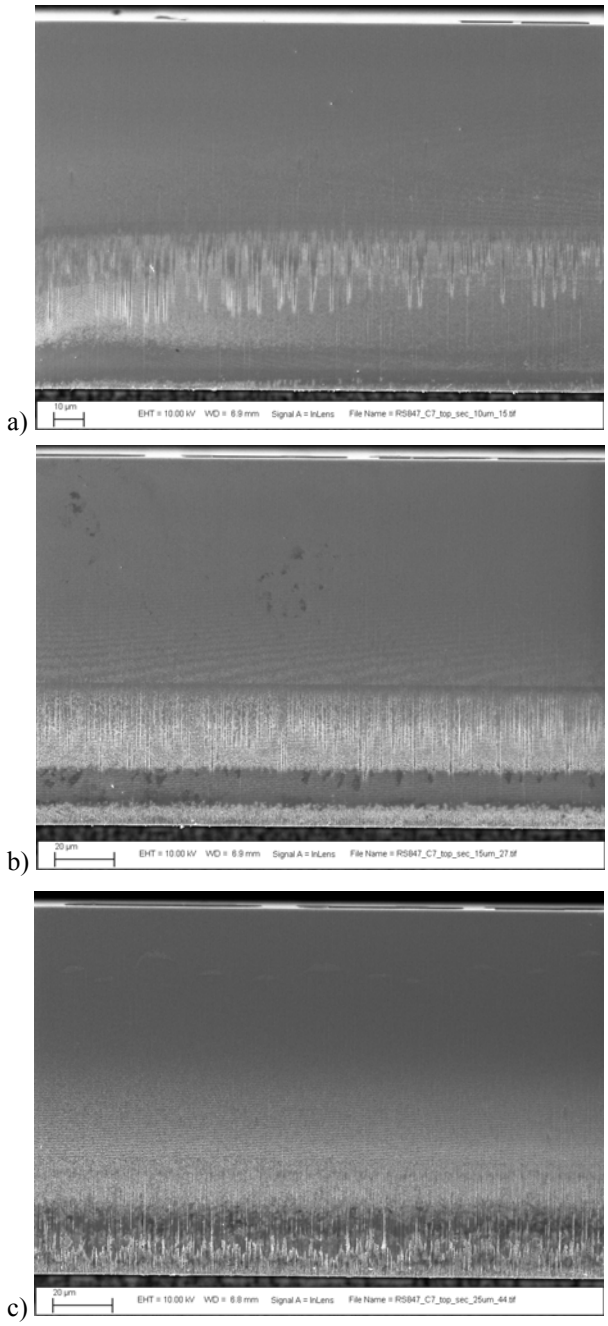
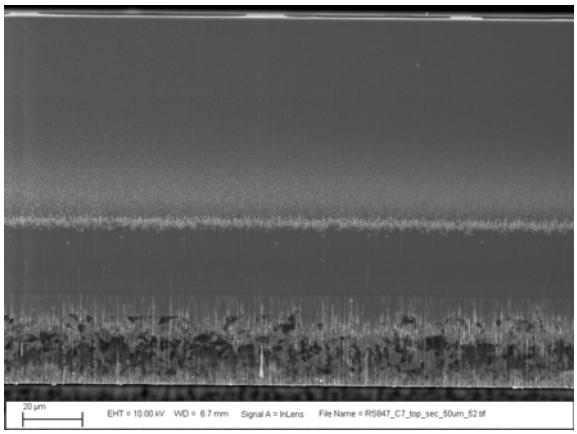
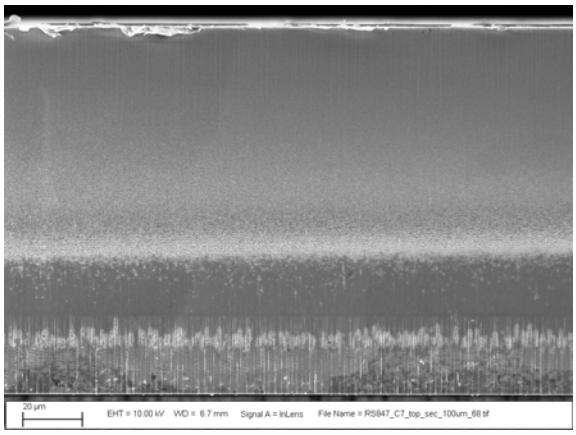


Figure 4: Scanning electron microscope (SEM) images of sidewall roughness for trench widths a) 10 µm, b) 15 µm, and c) 25 µm. The scale bar for the image in (a) is 10 µm and the scale bars in (b) and (c) are 20 µm.

a)



b)



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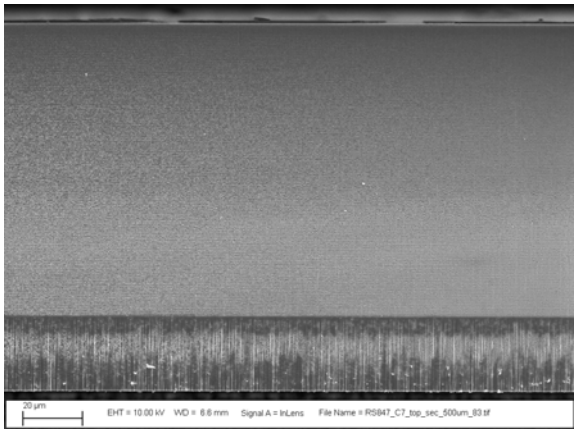

Figure 5: Scanning electron microscope (SEM) images of sidewall roughness for trench widths a) 50 µm, b) 100 µm, and c) 500 µm. The scale bars represent 20 µm in all of the images.

At all trench widths, the sidewalls of the device layer shows two distinct regions: an upper one that exhibits the scalloping surface texture typical of DRIE processes [6, 17-20] and a lower region with vertically oriented curtaining structure [20]. For some of the trench widths like the 50 µm (Fig. 5a) and 100 µm (Fig. 5b) a band appears in the scalloping region some distance above the start of the curtaining region. The 500 µm trench width image in Fig. 5c reveals the upper

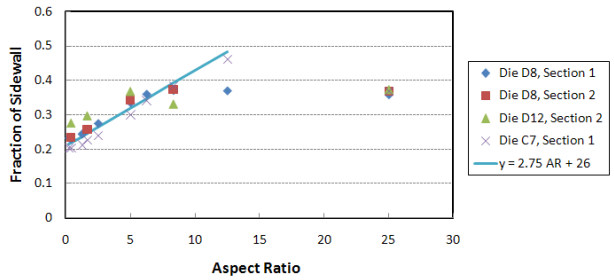

Figure 6: Height of the curtaining region at the bottom of the sidewall divided by the total etched height as a function of the trench aspect ratio. All of the samples cleared the trench for aspect ratios of 6.25 and below. Die C7, Section 1 is the only one that cleared the trench for aspect ratios of 8.3 and 12.5, and its data continuing to follow the trendline for those aspect ratios.

scalloping region and transition to the lower curtaining region especially well.

The SEM images in Figs. 4 and 5 show that the height at which the transition to the curtaining texture occurs decreases with increasing trench width. To further display the trend, the fraction of the device layer height with curtaining texture is graphed as a function of aspect ratio in Fig. 6. For aspect ratios of 6.25 and below, the fraction of the sidewall exhibiting curtaining texture increases linearly with aspect ratio. At aspect ratios above 6.25, the Die C7, Section 1 results continue to increase linearly with aspect ratio up to 12.5 but the results from the other samples whose results are plotted in Fig. 6 exhibit a more constant fraction of the sidewall that has curtaining structure. For the highest aspect ratio, 25, none of the samples etched all the way to the bottom of the device layer. Die C7, Section 1 etched to the bottom of the sidewall for aspect ratios of 8.33 and 12.5 but the other samples did not. Thus, the results show that prior to the etch reaching the bottom of the device, the fraction of the sidewall height exhibiting curtaining surface texture is around 0.36. Once the entire depth of the device layer is etched, the fraction of the sidewall surface that has curtaining increases linearly with aspect ratio.

ATOMIC FORCE MICROSCOPE (AFM) RESULTS

The sidewall surfaces were further characterized using an atomic force microscope to view the topography and quantify the roughness. 20 µm by 20 µm scans were performed at selected regions proceeding down the sidewall from the top to the bottom for two trench widths: 15 and 100 microns. Figure 7 illustrates representative results of the upper scalloping region for the 15 and 100 µm trench widths. Note that the plots are rotated. The left edge of the plot is the top part of the scan, and the scan proceeds down the sidewall moving to the right in the image. The horizontally scalloping features on the sidewall therefore appear as vertical. The scalloping of the surface is clearly visible, and the RMS roughness, R_q, values are 15.7 nm for the 15 µm trench width and 16.8 nm for the 100 µm trench width. The scalloping regions for these two trench widths

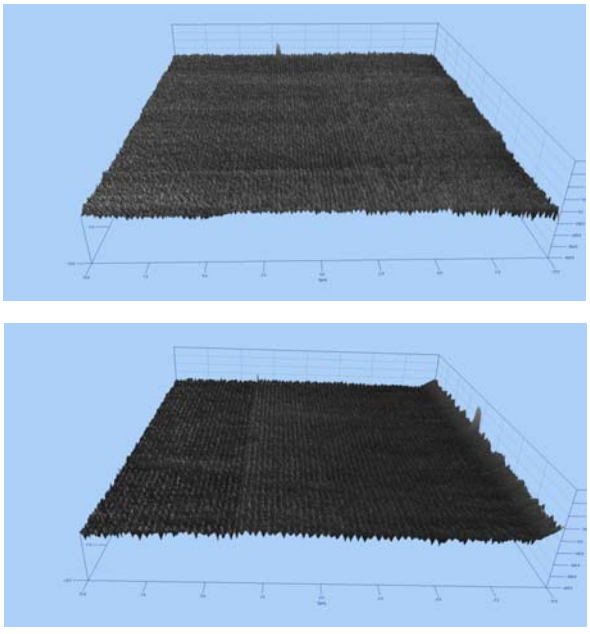

Figure 7: AFM images of a 20 μm by 20 μm scan in the upper region for two trench widths: a) 15 and b) 100 microns. The images are rotated such that the left side corresponds to top of the scan and moving to the right is proceeding down the sidewall. The scalloping of the surface is clearly visible, and the RMS roughness, R_q, values are 15.7 nm for the surface in a) and 16.8 nm for the surface in b).

appear very similar. Obtaining clean corresponding AFM images in the lower curtained regions was difficult due to the presence of particles along these portions of the sidewall which attached to the tips creating imaging artifacts. Thus, corresponding SEM images of the curtained regions for the 15 μm and 100 μm trench widths are given in Fig. 8 for comparison.

The change in the RMS surface roughness, R_q, quantified by the AFM is plotted as a function of distance down the sidewall in Fig. 10 for the 15 and 100 μm trench widths. The roughness at the top of the sidewall is similar for both trench widths. About halfway down the sidewall, the roughness increases for both trench widths. For the 15 μm trench width, the roughness remains at this higher value until the bottom of the sidewall. However, the roughness for the 100 μm trench width increases again for the bottom 25 μm and is two to three times greater than that for the 15 μm trench width. Since the fracture strength is expected to decrease with increased sidewall flaw size [8-11], it is expected the SOI structures bordered by 100 μm trench widths will have lower fracture strengths than structures bordered by 15 μm trenches due to the larger roughness.

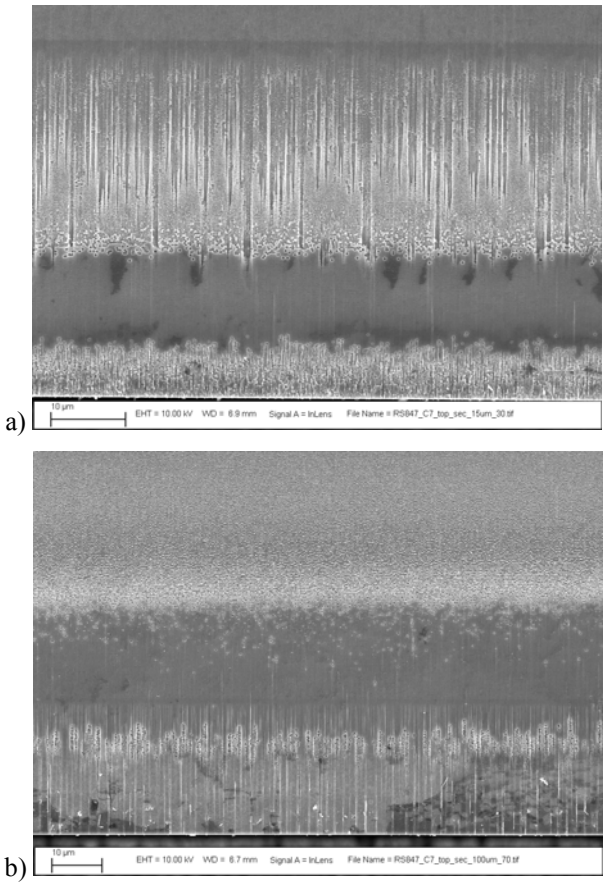

Figure 8: SEMs of the curtaining region at the bottom of the sidewall surface for trench widths of a) 15 μm and b) 100 μm. surfaces. The magnification in a) is greater than that in b) as seen by the larger 10 μm scale bar.

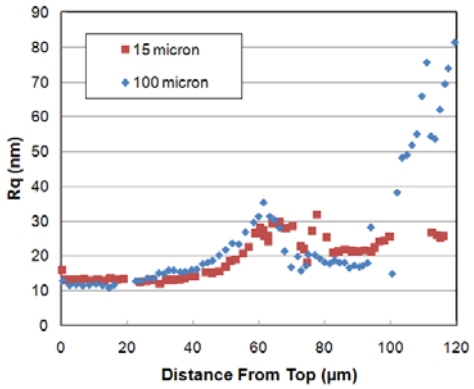

Figure 10: RMS Roughness as a function of distance from the top surface for two trench widths: 15 μm and 100 μm corresponding to aspect ratios of 8.3 and 1.25, respectively.

CONCLUSIONS

The three-step DRIE process creates silicon structures through sequential conformal polymer deposition, ion sputtering, and chemical etching. DRIE results in sidewall surface roughness which impacts subsequent mechanical characteristics like fracture strength and friction behavior. An SOI sidewall characterization die was designed and fabricated at Sandia National Laboratories containing varying trench widths from 5 μm to 500 μm for a 125 μm thick device layer corresponding to aspect ratios from 25 to 0.25. Using a scanning electron microscope (SEM), the surfaces were imaged detecting an upper region exhibiting a scalloping morphology and a rougher lower region exhibiting a curtaining morphology. The location of the die on the wafer did not produce noticeable differences in the surface characteristics. The fraction of the surface exhibiting the rougher curtaining morphology increases linearly with aspect ratio if the etch has reached the bottom of the device layer. AFM characterization for 15 μm and 100 μm trench widths indicate that the roughness increases as a function of depth along the sidewall surface. Additionally, the curtaining region for the 100 μm trench width was two to three times rougher than that for the 15 μm trench width. This suggests that the fracture strength for SOI MEMS structures neighbored by 100 μm trenches will be lower than that for those next to 15 μm trenches.

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