Si and SiGe based double top gated accumulation mode single electron transistors for quantum bits

M. S. Carroll[1], E. Nordberg[1,2], K. Eng[1], G. Ten Eyck[1], L. Tracy[1], K. Childs[1], J. Wendt[1], J. Stevens[1], M.P. Lilly[1], M. Eriksson[2]

[1]Sandia National Laboratories
[2]University of Wisconsin
Albuquerque, NM 87111, USA

Abstract:

There is significant interest in forming quantum bits (qubits) out of single electron devices for quantum information processing (QIP). Information can be encoded using properties like charge or spin. Spin is appealing because it is less strongly coupled to the solid-state environment so it is believed that the quantum state can better be preserved over longer times (i.e., that is longer decoherence times may be achieved). Long spin decoherence times would allow more complex quantum circuit computations to be completed with higher accuracy.

Recently spin qubits were demonstrated by several groups using electrostatically gated modulation doped GaAs double quantum dots (DQD) [1], which represented a significant breakthrough in the solid-state field. Although no Si spin qubit has been demonstrated to date, work on Si and SiGe based spin qubits is motivated by the observation that spin decoherence times can be significantly longer than in GaAs. Spin decoherence times in GaAs are in part limited by the random spectral diffusion of the non-zero nuclear spins of the Ga and As that couple to the electron spin through the hyperfine interaction. This effect can be greatly suppressed by using a semiconductor matrix with a near zero nuclear spin background. Near zero nuclear spin backgrounds can be engineered using Si by growing ^{28}Si enriched epitaxy.

In this talk, we will present fabrication details and electrical transport results of an accumulation mode double top gated Si metal insulator semiconductor (MIS) nanostructure, Fig 1 (a) & (b). We will describe how this single electron device structure represent a path towards forming a Si based spin qubit similar in design as that demonstrated in GaAs. Potential advantages of this novel qubit structure relative to previous approaches include the combination of: no doping (i.e., not modulation doped); variable two-dimensional electron gas (2DEG) density; CMOS compatible processes; and relatively small vertical length scales to achieve smaller dots.

A primary concern in this structure is defects at the insulator-silicon interface. The Sandia National Laboratories 0.35 µm fab line was used for critical processing steps including formation of the gate oxide to examine the utility of a standard CMOS quality oxide-silicon interface for the purpose of fabricating Si qubits. Large area metal oxide silicon (MOS) structures showed a peak mobility of 15,000 cm^2/V-s at electron densities of ~1x10^{12} cm^{-2} for an oxide thickness of 10 nm. Defect density measured using standard C-V techniques was found to be greater with decreasing oxide thickness suggesting a device design trade-off between oxide thickness and quantum dot size.

The quantum dot structure is completed using electron beam lithography and poly-silicon etch to form the depletion gates, Fig 1 (a). The accumulation gate is added by introducing a second insulating Al_2O_3 layer, deposited by atomic layer deposition, followed by an Al top gate deposition, Fig. 1 (b).

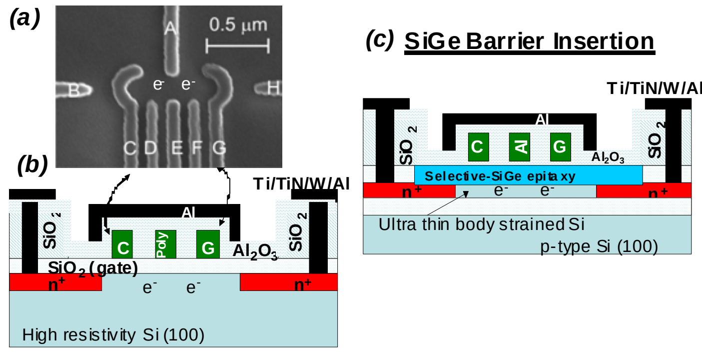

Figure 1 (a) top-view of depletion gate lay-out including point contact charge sensors on the left and right; (b) cross section of MOS-DQD structure; and (c) cross section of 2nd generation MIS-DQD structure using a SiGe barrier and ultra thin body strained silicon

Initial single electron transistor devices using SiO_2 show significant disorder in structures with relatively large critical dimensions of the order of 200-300 nm, Fig 2. This is not uncommon for large silicon structures and has been cited in the literature [2]. Although smaller structures will likely minimize the effect of disorder and well controlled small Si SETs have been demonstrated [3], the design constraints presented by disorder combined with long term concerns about effects of defects on spin decoherence time (e.g., paramagnetic centers) motivates pursuit of a 2nd generation structure that uses a compound semiconductor approach, an epitaxial SiGe barrier as shown in Fig. 2 (c). SiGe may be used as an electron barrier when combined with tensilely strained Si. The introduction of strained-Si into the double top gated device structure, however, represents additional fabrication challenges. Thermal budget is potentially constrained due to concerns related to strain relaxation. Fabrication details related to the introduction of strained silicon on insulator and SiGe barrier formation into the Sandia National Laboratories 0.35 µm fab line will also be presented.

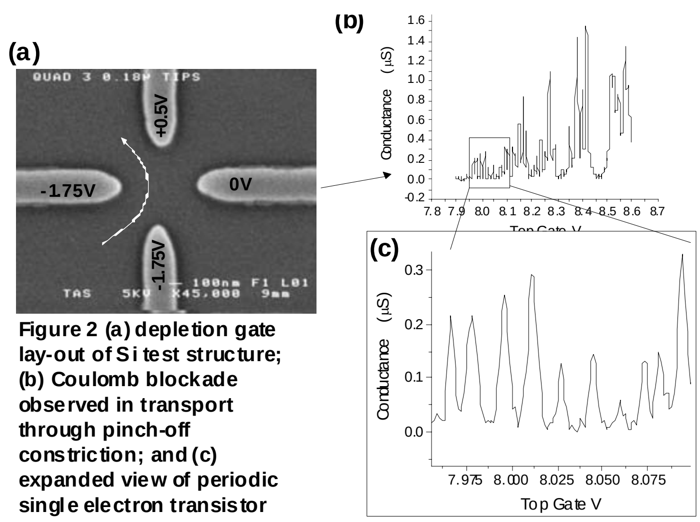

Figure 2 (a) depletion gate lay-out of Si test structure; (b) Coulomb blockade observed in transport through pinch-off constriction; and (c) expanded view of periodic single electron transistor behavior

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[1] J. Petta et al., Science 309, 2180 (2005)
[2] C. de Graff, et al. PRB 44, 9072 (1991)
[3] S. Angus, et al. Nanoletters 7, 2051 (2007)