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Self-Voting Dual-Modular-Redundancy Circuits for Single-Event-Transient Mitigation

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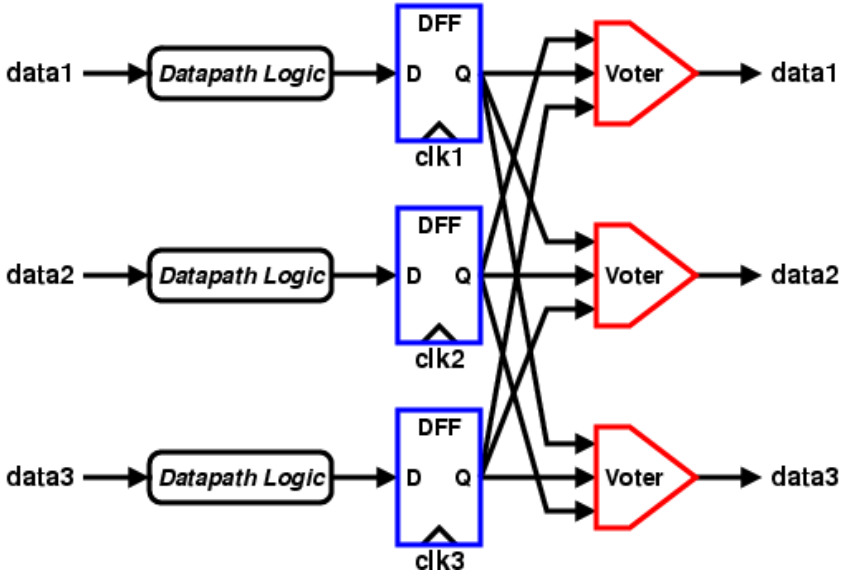
Outline

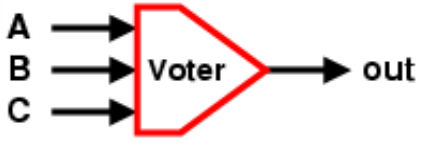
- TMR overview
- Voting circuits
- Dual-modular-redundancy (DMR) architectures
- Benchmark results

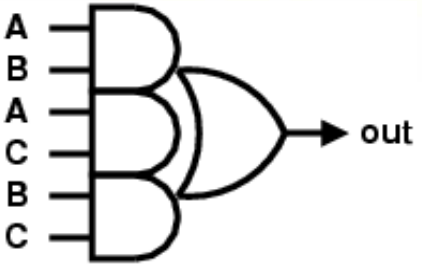
TMR Overview

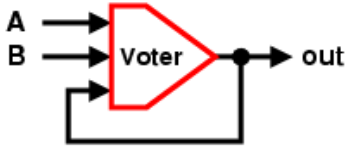


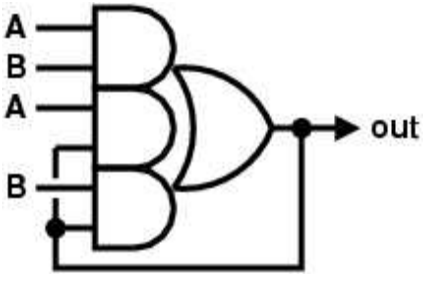
- TMR design
  - Each logic element is triplicated
  - Majority voters filter out SETs, preventing upsets
  - Clocks, resets, and voters are triplicated to avoid common-mode SET failures
  - Full TMR designs are immune to one SET, but not multiple SETs
- Large area overhead
  - 3x to 6x on typical designs

Voting and "Self-voting" Circuits









Voter feedback

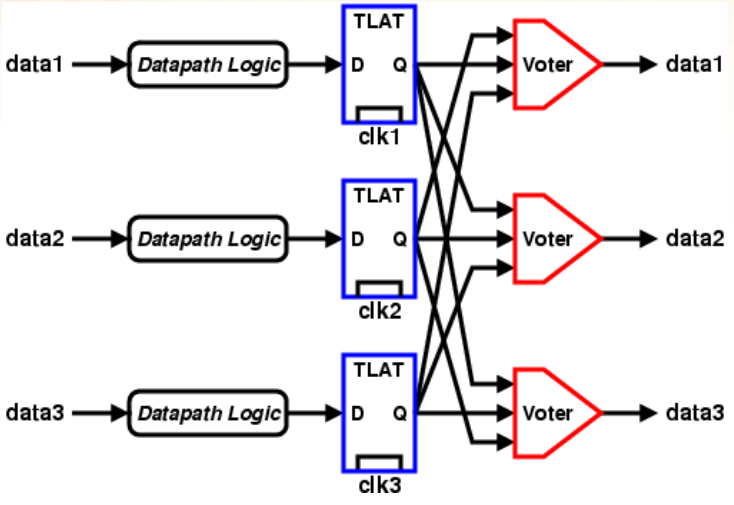
- Majority voter
  - Votes on 3 inputs
  - 2 of 3 inputs must change for output to change state
  - SET glitch on any one input will not propagate to output
- Self-voter
  - Votes on 2 inputs and current output
  - Both inputs must change for output to change state
  - SET glitch on any one input will not propagate to output
  - Numerous circuit implementations exist, including "C-elements", "Transition-And-Gates", & "Guard-Gates"
- SET inside both kinds of voters can propagate to output, but will not cause permanent SEU of voter

Self-voting Dual-Modular-Redundancy (DMR) Logic

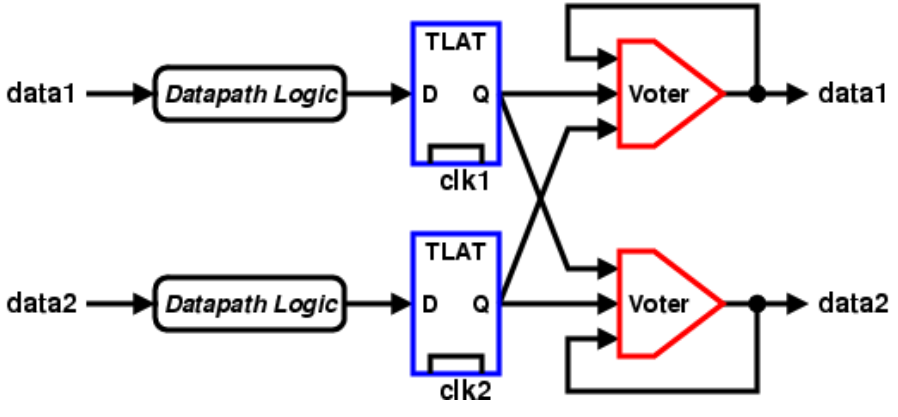
- **Goal:**
  - **Use dual-modular-redundancy (DMR) to reduce the area overhead of TMR deigns, without sacrificing SET immunity**
  - **Mitigate SETs on data inputs, clock inputs, storage cells**

- **Solution:**
  - **Self-voting circuits enable DMR logic to achieve the same level of SET protection as TMR logic**
  - **DMR designs improve area efficiency**
    - **33% for latch designs**
    - **10-24% for flip-flop designs**
  - **Marginal performance impact for "modest" designs**
    - Maximum SET-width subtracts from maximum cycle time
    - E.g., 1ns SET-width tolerance has 10% impact on 100MHz design

Latch Datapaths



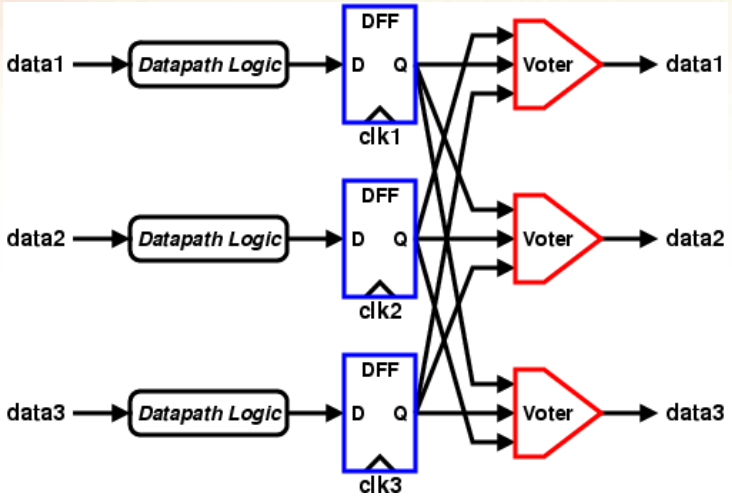
- TMR
  - Latch open: voters filter SETs
  - Latch closed: voters filter SEUs
  - Cycle time = voter + logic delay + setup



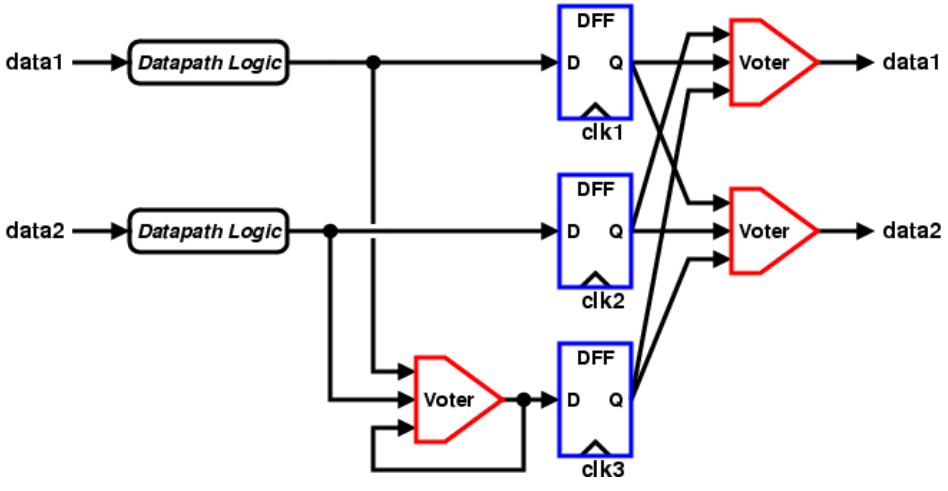
- DMR
  - Latch open: self-voters store register value and filter SETs
  - Latch closed: self-voters filter SEUs
  - Cycle time = *SET width* + voter + logic delay + setup

33% less area than TMR

Flip-Flop Datapaths



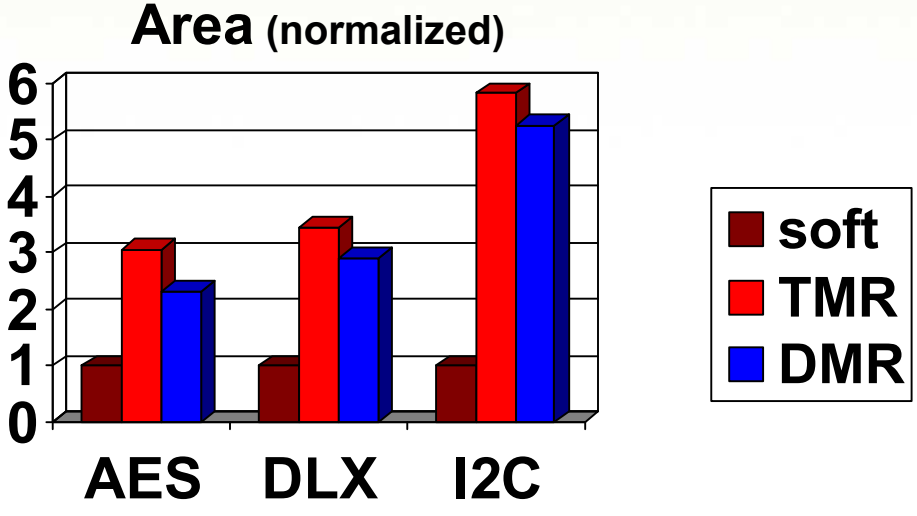
- TMR
  - 3 majority voters filter out SEUs in redundant flops
  - Cycle time = voter + logic delay + setup

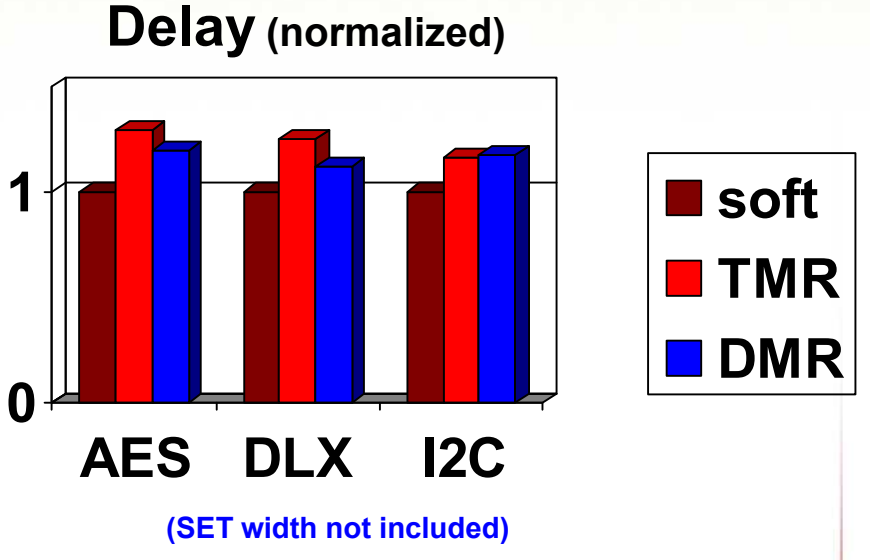


- DMR
  - 3 redundant flops required for DMR scheme (due to possibility of SET being latched on clock edge)
  - Self-voter filters out SET on any one redundant datapath and provides the 3rd redundant datapath value
  - 2 majority voters filter out SEUs in redundant flops
  - Cycle time = ***SET width*** + 2•voter + logic delay + setup

Area savings depends on % datapath logic

Benchmark DMR versus TMR (Flip-Flops)

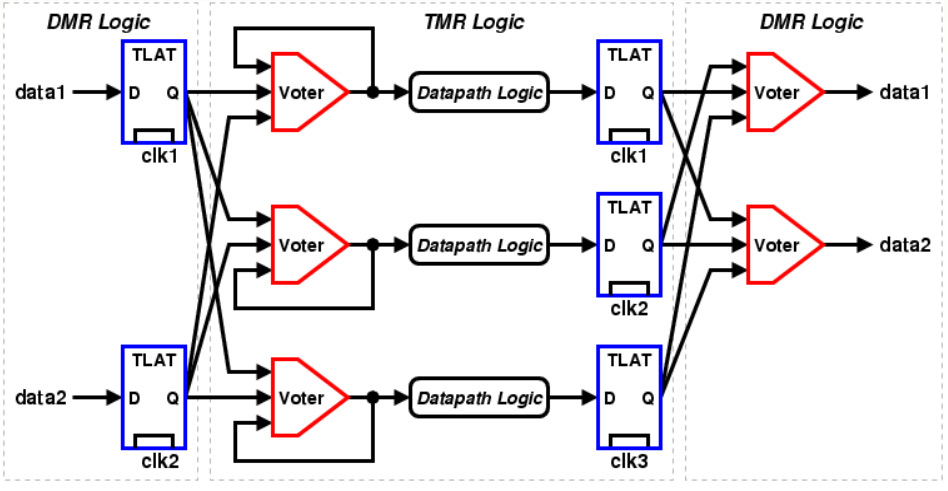


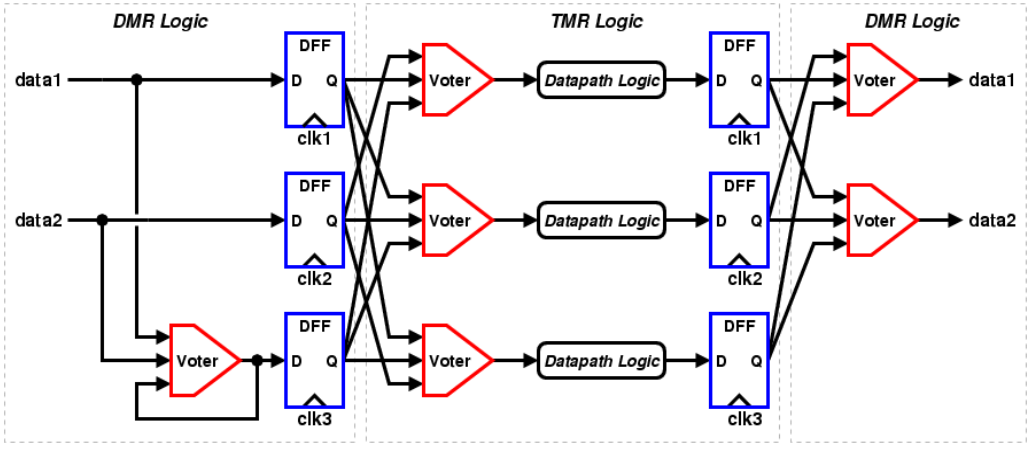


(SET width not included)

- OpenCore designs run through structured-ASIC physical synthesis
  - Clock tree, reset trees, buffer insertion, full parasitics, etc.
- DMR flip-flop designs show 10-24% lower area
- DMR logic shows no up-front speed penalty (vs. TMR)
  - Lower register fanout & less routing complexity
  - Can help offset SET-width penalty in cycle time calculation

DMR-to-TMR Conversion Logic





- No area/delay overhead to convert between DMR and TMR schemes
- Conversion occurs at register boundaries
- DMR/TMR design strategy:
  - Use TMR on critical paths to meet timing
  - Use DMR on paths with large slack to reduce area

Conclusion

- **Self-voting DMR summary**
  - **SET/SEU protection equivalent to full TMR**
    - SET protection on data & clock inputs
    - SEU protection on register storage cells
  - **Lower area overhead than TMR**
    - 33% reduction for latch designs
    - 10-24% reduction for flip-flop designs
  - **Trivial to implement**
    - No special library cells
    - Maximum SET-width tolerance is not “hard-coded” into circuit

- **Radiation testing**
  - **Self-voting DMR architecture has not been SET tested, but**
  - **Much related work has validated SET effectiveness of self-voters (i.e., C-element/Transition-And-Gate/Guard-Gate) in other datapath architectures**
    - E.g., R.L. Shuler, et. al., “The effictiveness of TAG or guard-gates in SET suppression using delay and dual-rail configurations”, IEEE Trans. Nucl. Sci., Dec. 2006.

Questions

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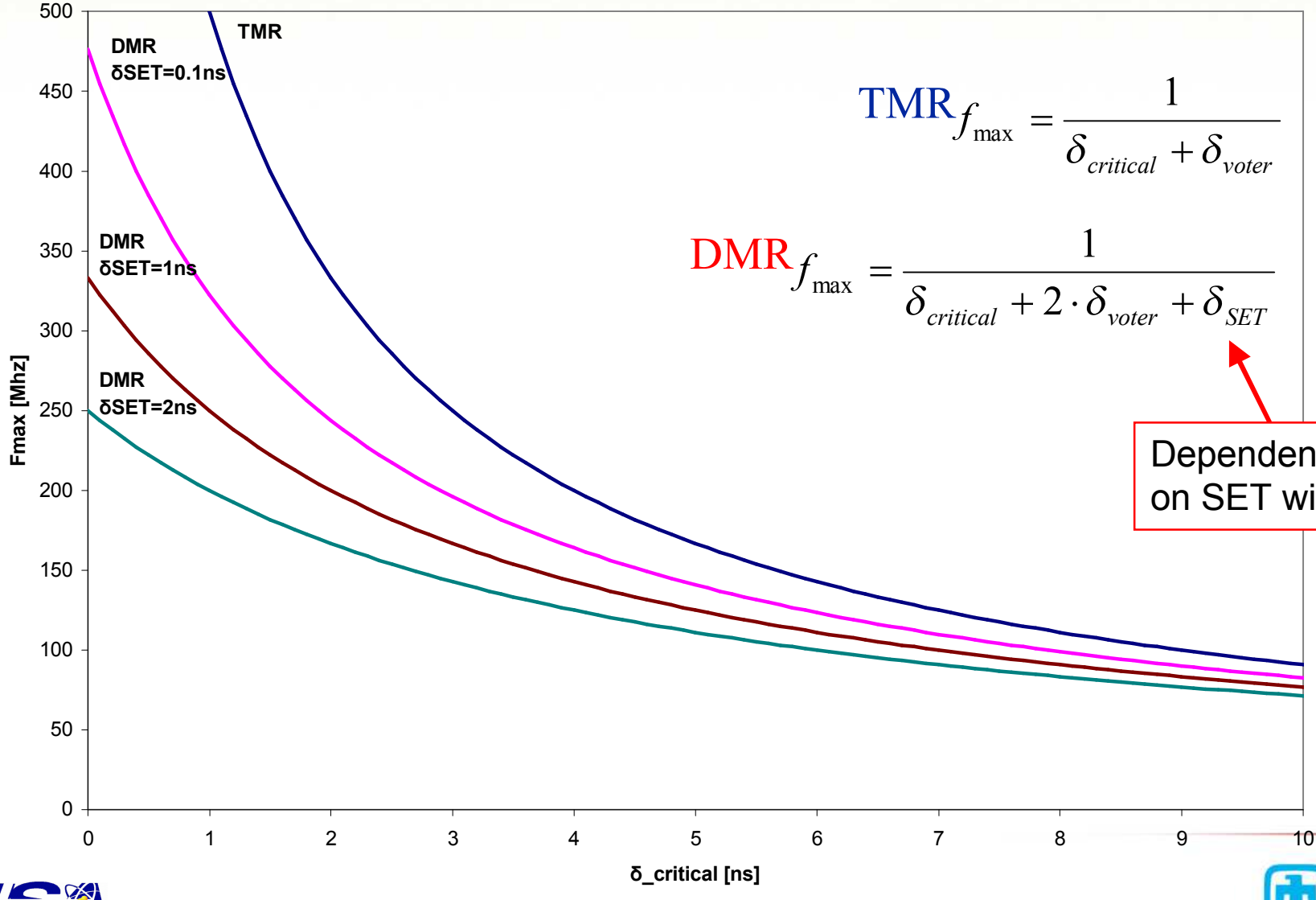
Backups

"Theoretical" DMR versus TMR Performance (Flip-Flops)

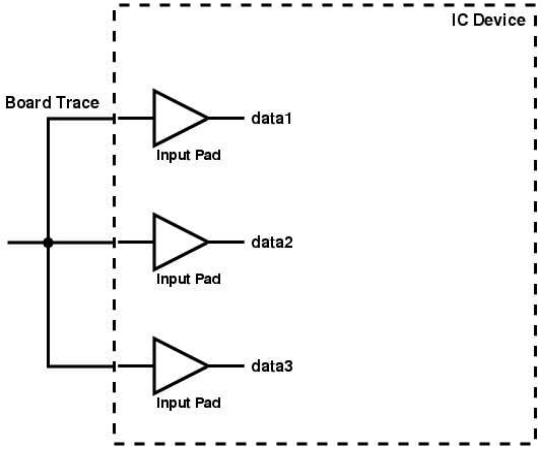


$$TMR_{f_{max}} = \frac{1}{\delta_{critical} + \delta_{voter}}$$

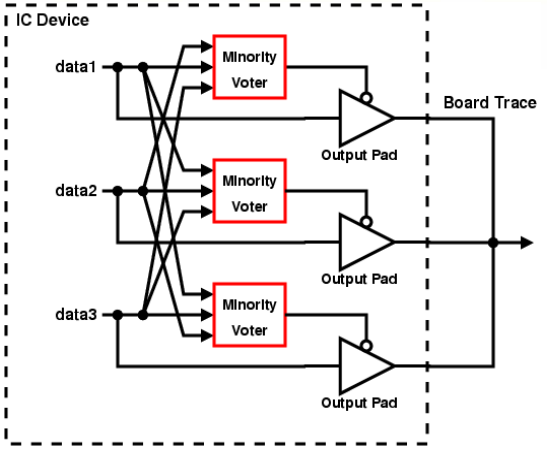
$$DMR_{f_{max}} = \frac{1}{\delta_{critical} + 2 \cdot \delta_{voter} + \delta_{SET}}$$

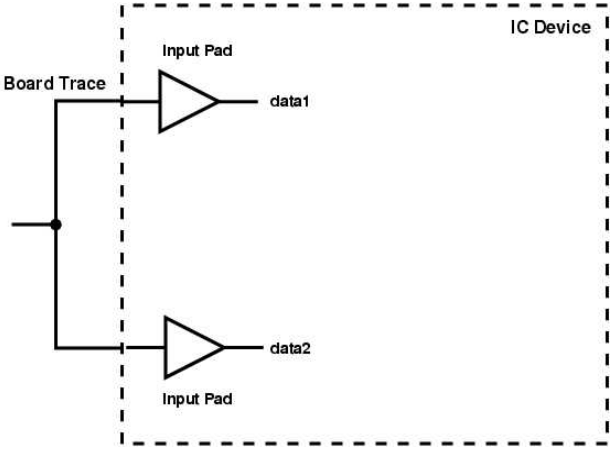
Dependence on SET width

I/O Circuits

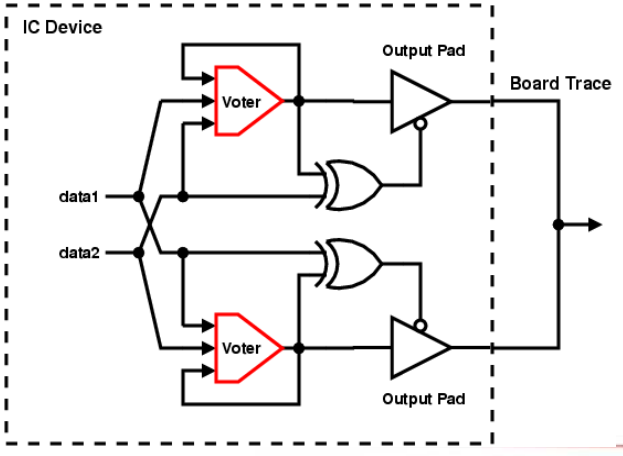


TMR I/O





DMR I/O



Background

- SET (single event transient)
  - Energetic particles striking transistor devices cause temporary voltage disturbances
  - Logic upset (SEU) can occur in registers when SET is latched on clock edge
- Rad-hard processes
  - SET immune until medium LET levels
  - Resistor feedback added for higher LET levels
- Commercial CMOS processes
  - Bulk sensitive at low LET levels
  - SOI less sensitive
  - Triple-modular-redundancy (TMR) most popular SET mitigation technique for logic circuits