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K*u*-band Six-bit RF MEMS Time Delay Network

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***Abstract*— A six-bit time delay circuit operating from DC to 18 GHz is reported. Capacitively loaded transmission lines are used to reduce the physical length of the delay elements and shrink the die size. Additionally, selection of the reference line lengths to avoid resonances allows the replacement of series-shunt switching elements with only series elements. With through-wafer transitions and a packaging seal ring, the 7 mm x 10 mm circuit demonstrates <2.8 dB of loss and 60 ps of delay with good delay flatness and accuracy through 18 GHz.**

Keywords- Microelectromechanical devices, microwave phase shifters, delay circuits, switches.

I. INTRODUCTION

Time delay circuits are critical elements for broadband electronically steerable array antennas (ESAs), where constant time delay (rather than constant phase) is essential for maintaining steering angle across large frequency ranges [1]. Radio Frequency Micro-electromechanical System (RF MEMS) switch technology offers flat time delay, low loss, and high linearity for realizing broadband time delay in ESAs. Numerous RF MEMS based phase shifters have been reported in the literature with up to six bits of delay resolution [2-6]. Our previously reported six-bit MEMS time delay circuit demonstrated delays up to 400 ps and low loss through 10 GHz, but required large die area [2]. In this work, we realize a smaller time delay circuit at higher frequency, with particular emphasis on reducing the die area and switch count of the circuit. Specific improvements made in this circuit include reducing the number of switches and die area by using series-only switches in place of series-shunt switches, reducing the length of lines internal to the time delay circuit by using LC-transmission line networks, applying a loaded transmission line delay network to the two least significant bits (LSBs), and designing the time delay to be compatible with chip-scale packaging.

II. TECHNICAL APPROACH

A. Overall Design Concept

The time delay circuit is realized using three two-bit time delay circuits cascaded in series. The four most significant bits (MSBs) of this time delay circuit use RF MEMS based single-pole four-throw (SP4T) switches to realize cascadable two-bit time delay circuits, similar to approaches reported previously [2-5]. This approach provides the best balance among loss, die size, and circuit complexity. To achieve die area miniaturization, the internal paths use LC-time delay networks rather than standard microstrip transmission lines. This allows closer routing of the transmission lines, reduces physical path length for a given electrical delay, and provides better loss balance between the delay states.

Switched line networks are impractical for small delay resolution because of the small difference in length between the transmission lines. For example, the LSB in a six-bit 16.7 GHz time delay is 0.94 ps, which requires the delay paths in a four-path, two-bit phase shifter to be 106 μm, 212 μm, and 318 μm longer than the reference path for microstrip on alumina. These small path differences require large lengths of reference line to obtain sufficient isolation between adjacent lines. Instead, the least significant two bits of this phase shifter are realized by using a loaded transmission line approach, where the delay of the transmission line is determined by a loading capacitance that is switched into and out of the circuit [7].

B. SP4T Switch

The series SP4T switch is similar to one reported earlier for time delay circuits and was designed using a similar procedure with inductance in the common path [2,3]. Additional compensating inductance was introduced into the four paths, with the 90° right angle paths made more inductive than the 30° paths to compensate for the slightly higher capacitance of the right-angle path. The SP4T switch networks were tuned to maintain an identical phase length at each path, maximize delay flatness, and demonstrate return loss better than 20 dB at the input and output port.

C. Half-wave Resonance Suppression

A key problem with switched line phase shifters is the resonance that occurs when the off-state lines are multiples of $\lambda/2$ long [6]. This resonance will couple into the signal path for any finite switch isolation and cause degradation in insertion loss, return loss, and delay flatness at the resonant frequency. Higher isolation switches will reduce but not eliminate this spurious resonance, so it is important to either damp it using shunt switches or to ensure that it is not in the band of interest. In this work, the primary band of interest was 15.2 GHz to 18.2 GHz, so the resonance can be moved with an appropriate reference path length. The selection of reference

path length is shown graphically in Figure 1 for a time delay with 15 ps steps, where the 4 time delays are plotted as a function of reference length. The forbidden delays where the off-state transmission lines are λ/2 long in-band are shown graphically by the shaded areas, and the reference path lengths that allow all delay lines to be outside of this forbidden region are bounded by the vertical dashed lines. Figure 1 shows that, for the circuit with 15 ps steps, the allowed reference lengths are in the 4-9 ps, 21-24 ps, and 35-40 ps range. The shortest allowed reference length will provide the lowest loss, shortest time delay, and in this case, the largest window, so a reference length of 5 ps between series switches was chosen. This simple analysis neglects the impact of capacitive loading due to the 5 fF switch series capacitance on the half-wave center frequency, which results in a downward shift of about 1 ps in the resonator forbidden length for the first resonance. Selecting a reference length towards the low end of the allowed lengths provides sufficient margin for this design. Repeating the analysis for the middle time delay with 3.75 ps steps shows that reference lengths up to 15 ps are allowed. In this case, a longer reference length will allow more room for delay line routing, so a reference length of 13 ps was chosen.

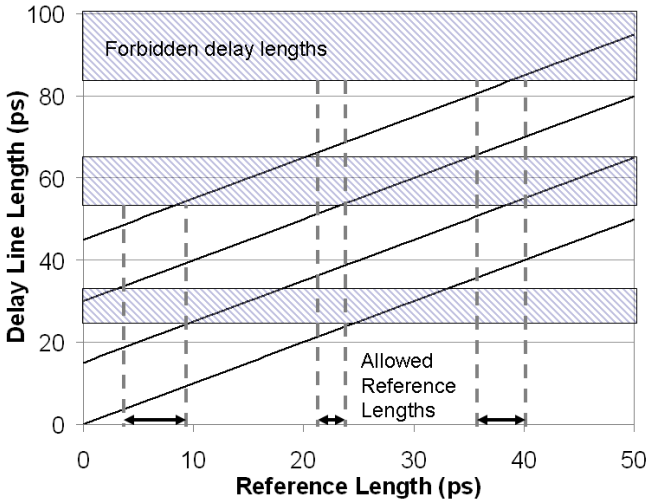

Fig. 1: Graphical analysis of reference line length for the 15 ps four-path time delay circuit. Shaded windows indicate forbidden path lengths due to in-band resonances, while the vertical lines windows indicate allowed reference lengths.

D. Switched-Line Layout Miniaturization and Loss Equalization

The reference and first delay line in each two-bit circuit were implemented using capacitively loaded high-impedance microstrip transmission lines to minimize the footprint and physical length for a given delay. Interdigitated capacitors were used to load the transmission lines because of the relatively small loading capacitance required and ease of implementation. The layout of the SP4T switch requires the outer delay lines to be about 1100 μm longer than the inner delay line, corresponding to a delay difference of 9.75 ps in straight 50 Ω lines. Because this additional delay is larger than the 3.75 ps delay steps in the medium time delay, additional delay must be built into the reference path to compensate for this difference. Using the loaded transmission lines, rather than meandering a 50 Ω line, minimizes the circuit area.

The lines were first designed using a circuit-level simulator for 50 Ω input impedance and appropriate delays, but complex interactions between the interdigitated capacitors, transmission lines, and via holes required full electromagnetic simulation. Once a general dimension was selected, the transmission line width and capacitor lengths were parameterized to obtain contour plots of return loss and delay. The time delay circuit delay line dimensions were then determined by the intersection of the best return loss and the desired delay in the width-length space. This task was performed first to define the reference length and then for the first delay length. Because the longest two paths are 50 Ω microstrip lines, the optimization of those lengths was performed simply by choosing the appropriate length. Targeted return loss was >25 dB per delay line and >18 dB for each two-bit circuit.

The measured insertion loss of the two individual two-bit switched path time delay circuits is 1 dB +/- 0.2 dB for the two circuits, which compares favorably to the simulated loss of 0.9 dB +/- 0.1 dB for each circuit.

E. Least Significant Bit Design

The loaded-line time delay circuit was designed to allow two bits of switching using two banks of capacitors, one on each side of the transmission line for each bit. The return loss goal for this two-bit circuit was 18 dB, requiring two loading capacitors for the shorter bit and three loading capacitors for the longer bit because the desired delay and return loss could not be attained with only three switches total. The reference state of this two-bit circuit is realized when all of the switches are in the up position, where the transmission line is loaded only by about 5 fF of parasitic capacitance per switch. In this case, the transmission line is slightly inductive. A bank of two switches on one side of the line is used to realize the LSB, and a bank of three switches on the opposite side are used to realize the MSB. When all of the switches are down, both delay bits are active and the line is capacitive. Because of the parasitic capacitance of the switches, the delay is not a perfect binary progression, but instead the state with both bits active will have a slightly shorter delay than the sum of the two bits. This error is much lower than the LSB time. Targeted return loss was >18 dB for this two bit circuit. The measured insertion loss of this circuit at 18 GHz is 0.5 +/- 0.2 dB, compared to the simulated loss of 0.1 +/- 0.1 dB using lossless switches.

F. Package Design

The package concept for the time delay circuit uses an alumina cap attached to the circuit using a AuSn perform. Die were designed for individual packaging to ensure quality hermetic seals. The package transition is similar to that in earlier RF MEMS surface-mount packages [8,9] but with the center trace on the bottom coplanar mount expanded to

220 µm to relax tolerances during assembly of the RF MEMS phase shifter onto the next-level board.

A small package fabricated using this transition and measured with coplanar probes demonstrated <0.25 dB insertion loss and >18 dB return loss through 20 GHz, as shown in Figure 2. The package response is slightly inductive because the feedtroughs are connected by a 75 Ω transmission line intended to imitate a closed switch.

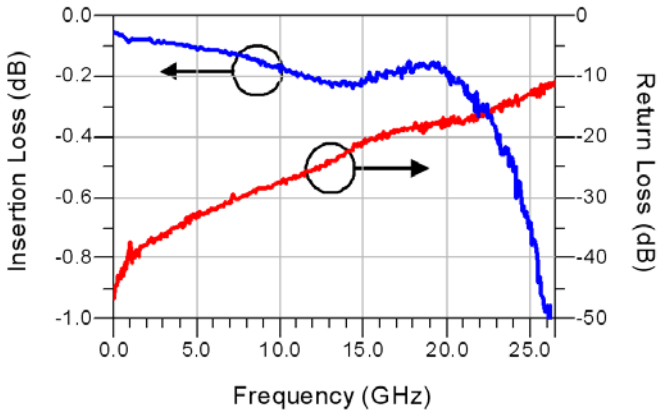

Fig. 2: Response of two back-to-back packaging transitions connected by a 75 Ω thru line.

An optical micrograph of the time delay circuit is shown in Figure 3. The circuit contains 21 RF MEMS switches, eight in each switched line time delay and five in the loaded line time delay. The circuit area is 5 mm x 8 mm, with an additional 1mm of gold seal ring extending beyond the edge of the circuit. The RF feedthroughs are at the left and right, and the thru-wafer vias for switch DC bias are at the upper and lower right of the active area.

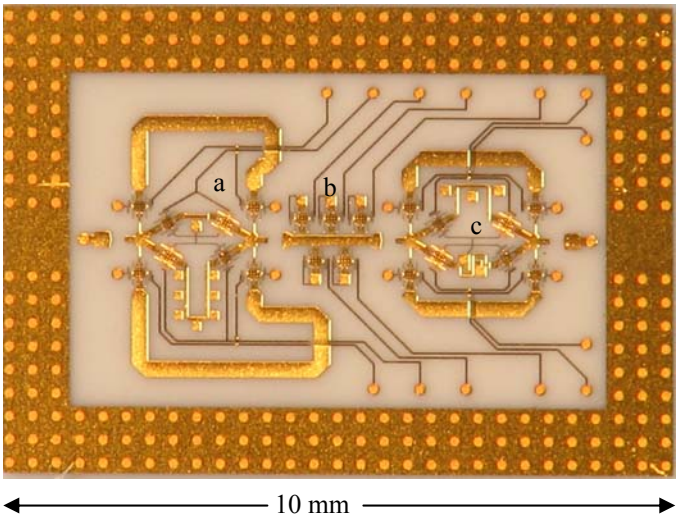

Fig 3: Optical micrograph of the six-bit time delay circuit with the individual two-bit circuits labeled: (a) long, (b) short, and (c) medium.

III. Measured Results

A. *RF MEMS Time Delay Network Fabrication*

The RF MEMS technology used in these circuits is fabricated using gold electroplating to realize the RF MEMS switch bodies and transmission lines, TaN resistors for bias routing, and CuW vias on a 250 µm thick alumina substrate. The RF MEMS switch uses gold contacts to achieve <0.2 dB loss and >30 dB isolation at 10 GHz. More details on the switch and fabrication process are provided in prior publications [2,10].

For microwave measurements, the circuit was placed into a fixture to allow direct probing on the backside contact pads. The time delay circuit was measured from 50 MHz to 20 GHz using GSG probes and an HP8510 network analyzer, calibrated at the probe tips. Forty two of the 64 possible time delay states were measured; the remaining states were not measured due to a switch that ceased operating during testing.

The measured insertion loss of the six-bit circuit, including through-wafer via transitions, ranges from 1.1 dB to 2.7 dB in the 15.2 – 18.2 GHz band of interest. There are no resonances in the 15.2 – 18.2 band, and the small resonances visible at 10 GHz and 14 GHz have negligible impact on the circuit. The return loss is > 7 dB through 18 GHz, which is a result of the large number of cascaded discontinuities in this passive circuit.

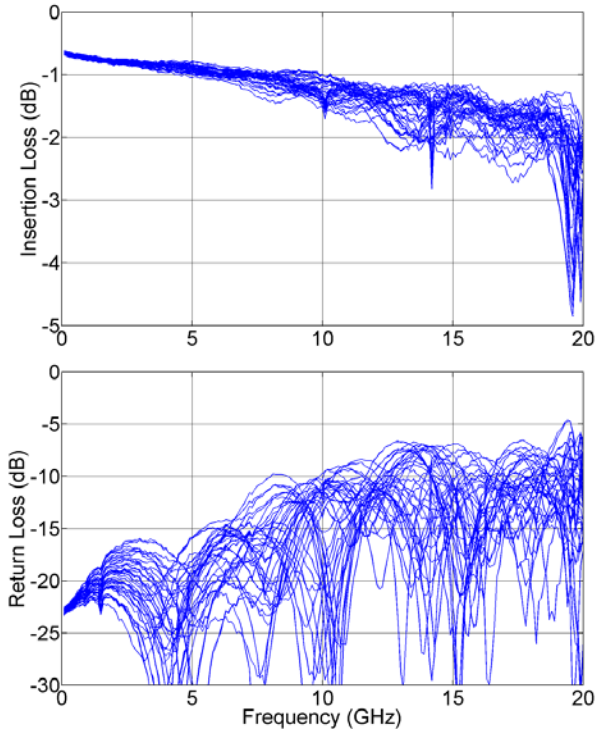

Fig. 4: Measured Insertion Loss and Return Loss of 42 states from the 6-bit circuit.

The measured phase and phase shift relative to the reference state is shown in Figure 5, and shows good phase flatness across the entire measurement band. None of the measured lines cross, indicating phase accuracy to better than one LSB.

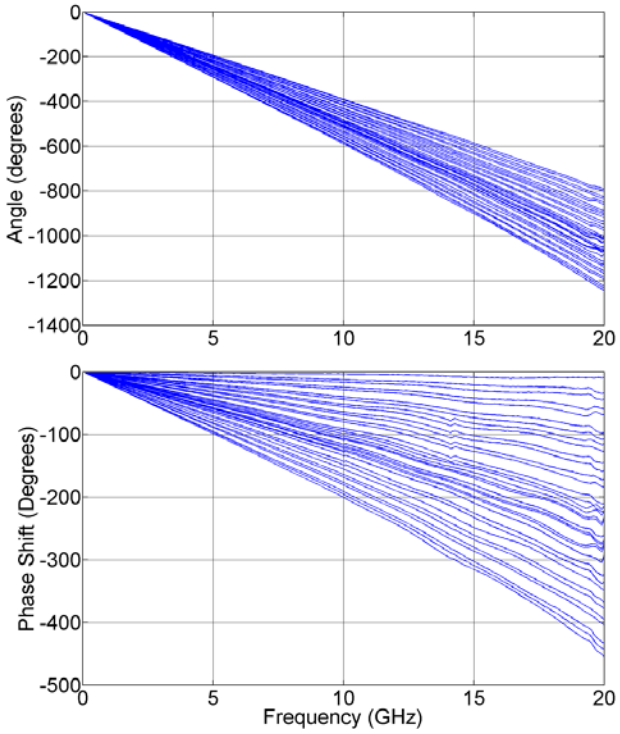

Fig 5: Phase and phase shift (relative to the reference path) for 42 states of the 6-bit time delay circuit. The gaps in the states are due to a non-functioning switch.

The measured phase at 16.7 GHz for each of the 42 measured circuit states is shown in Figure 6. The phase error for all of the measured states is smaller than the LSB of 0.94 ps. A few neighboring states have similar delays, possibly due to a stuck closed switch in the shortest time delay.

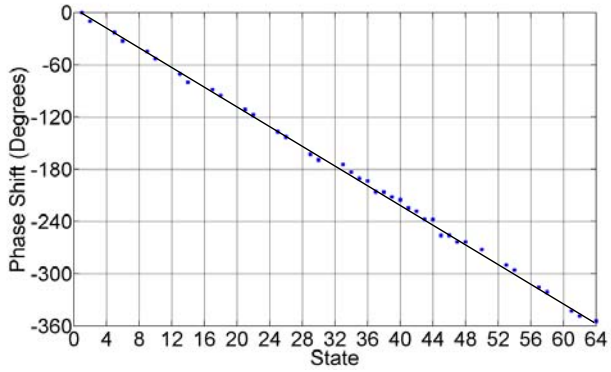

Fig 6: Phase shift at 16.7 GHz vs. circuit state for the 42 measured states of the 6-bit time delay circuit. The solid line shows the expected phase response as a function of state for comparison.

IV. Conclusion

A six-bit RF MEMS Ku-band time delay circuit has been demonstrated with <2.8 dB of insertion loss at 18 GHz. The 7mm x 10 mm circuit uses 21 RF MEMS switches and includes through-wafer transitions and a seal ring for packaging. The circuit demonstrates the use of loaded transmission lines to compensate for offset lengths, miniaturize delay lines, and balance the loss between states. Future work in packaging, improving the switch yield and reliability, and refining the return loss will allow the use of this type of RF MEMS circuits in electrically scanned array antennas.

V. Acknowledgments

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