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Growth, Fabrication, and Characterization of High-Speed 1550-nm S-SEEDs for All-Optical Logic

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We describe recent advances in the development of 1550-nm symmetric self-electrooptic effect devices (S-SEEDs). S-SEEDs are semiconductor optoelectronic devices used to implement ultrafast all-optical logic functions for optical fiber communication applications. In this paper, basic S-SEED operation is described, followed by a detailed explanation of the optimization techniques used to improve DC and high-speed performance in these long wavelength devices. Both epitaxial strain and quantum well design are shown to be important for S-SEEDs grown in the InAlGaAs quaternary material system. The device fabrication approach is outlined, and DC electrical and optical performance is discussed. Finally, we describe the high-speed optoelectronic measurements used to determine S-SEED switching characteristics. The devices described herein are the first known S-SEEDs to operate at telecommunications-compatible wavelengths and demonstrate record switching speeds with rail-to-rail switching rates faster than 6 picoseconds.

I. Introduction

Current optical fiber networks operate with single-channel bitrates as high as 40 Gb/s, and systems exceeding 100 Gb/s per channel are anticipated in the near future. The bandwidth of electronic processing systems has not kept pace with these channel rates, and data processing in these telecommunication systems is typically performed only after data has been demultiplexed down to slower, more-manageable rates. Certain applications, however, demand serial data processing at full line rates, a requirement that necessitates the use of ultrafast logic technologies. All-optical switching devices and ultrafast electronic devices are both candidates for this type of application. In this paper we describe key advances in the area of symmetric self-electooptic effect devices (S-SEEDs), one of the leading all-optical logic device candidates for high-speed data processing.

The S-SEED is a bistable all-optical logic device that can implement both NAND and NOR functions (1), enabling the creation of complex logic circuitry when multiple gates are cascaded (2). The low switching energy of an S-SEED is a key advantage for high-speed processing systems. Its compact size would enable integrated logic circuit densities of >1,000 gates/cm^2. These and other features led to extensive device optimization and system development during the previous decade, and systems with high levels of computational complexity were demonstrated (3). A notable drawback of that body of work, however, was its focus on AlGaAs-based devices that operated at 850 nm. Here, we describe the growth, fabrication, and characterization of S-SEED devices comprised

of InAlGaAs quaternary materials on InP. Section II of this paper introduces S-SEED operation, and describes the structure and epitaxial growth of long-wavelength S-SEEDs, which now operate at telecom-compatible wavelengths. Besides growth, device fabrication processes are key to achieving optimized electrical properties, and Section III describes the fabrication sequence used to create arrays of S-SEED logic gates.

High-speed operation of 1550-nm S-SEEDs has been a focus of recent work, and the devices described herein demonstrate switching at significantly faster rates than previously-reported devices. High-speed operation has been improved through the use of extremely-shallow quantum wells (ESQWs), and by electrical contacts designed for low series resistance. Switching measurements are described in Section IV, and show that the devices can switch between states in less than 6 ps. Such speeds strongly suggest suitability for 40 Gb/s operation or beyond. The paper concludes with a brief summary of the current status of 1550-nm S-SEED technology.

II. Device Operation, Design and Epitaxial Growth

S-SEED Operation

An S-SEED gate, as shown in Figure 1, is comprised of a pair of special, series-connected *p-i-n* diodes. (Each diode is known as a self-electrooptic effect device, or SEED, while the series connected pair is an S-SEED.) S-SEEDs have the useful characteristic of bistability; that is, they typically reside in one of two electrical states. When the static reverse bias V_b is applied across an S-SEED pair, these two states are roughly represented by the cases where V_b is fully dropped across a single diode's capacitance (while the other diode has essentially no bias across it). Equal optical inputs tend to reinforce this bistability, while unbalanced inputs can cause switching between states. In practice, such switching corresponds to an all-optical logic operation.

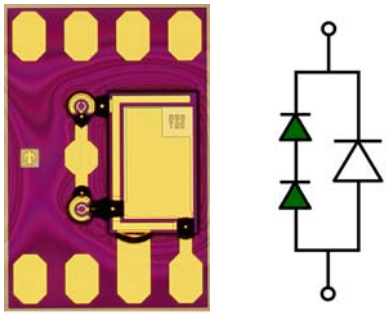

Figure 1. Fabricated S-SEED device (left) and its electrical equivalent (right). The small series-connected diodes are placed in parallel with a large diode capacitor that holds the bias constant during switching events.

As shown in Figure 2, the intrinsic region of each diode contains a multiple quantum well (MQW) region designed to interact with incident light. Switching between states occurs when optical input signals arrive normal to the plane of the S-SEED and are absorbed, generating photo-induced carriers in the MQW region of a diode. Carriers rapidly exit the diode structure and charge the other SEED, thereby toggling the S-SEED state. Hence, high-speed logic operation requires that the device be optimized much like a high-speed photodiode.

Multi-gate S-SEED logic circuits are formed by cascading optical signals from one device to the next. Cascading is achieved by optically reading out an S-SEED gate after it performs a logic operation. Read-out begins by directing an optical pulse onto the S-SEED. The pulse is reflected by the epitaxial mirror below the diode and redirected to the next gate using micro-optics described elsewhere (4). The "output signal" of the S-SEED is determined by the electrical state of the device after switching (i.e., by the voltage across the SEED's MQW region). In this step the S-SEED must operate as an efficient electroabsorption modulator.

Finally, from a system perspective it is imperative to keep power dissipation low. This is achieved primarily by minimizing device capacitance and S-SEED operating voltage. These four requirements represent the key characteristics of a good S-SEED device: high speed photoabsorption and sweep-out, strong modulation contrast, and low device capacitance, all for low operating voltages. The device cannot be designed to emphasize a single characteristic, but rather, must be optimized to achieve adequate performance in each area simultaneously. The following section details some of the design strategies used to reach this goal for InAlGaAs S-SEEDs.

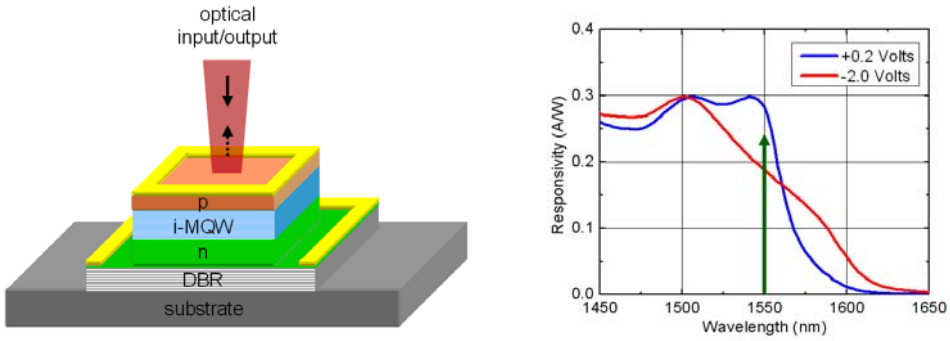

Figure 2. Cross-sectional schematic of a single SEED diode and nominal optical absorption characteristics at the two stable S-SEED operating voltages as a function of wavelength. This S-SEED is designed to operate at approximately 1550 nm. Optical signals are incident normal to the surface of the device, and modulated outputs may pass back out the top of the device after striking the integrated distributed Bragg reflector (DBR) mirror shown.

S-SEED Structure and Quantum Well Design

A schematic of the S-SEED structure is given in Figure 3. The device, grown on an InP:Fe substrate and a 5000 Å InP:Si buffer layer, consists of a 4000 Å n-doped bottom cladding layer, a 25 multiple quantum well (25-MQW) region, a 100 Å undoped top cladding layer, a 4000 Å p-doped top cladding layer, and a 200 Å p-InGaAs contact layer. The specific layer compositions are given in the figure.

As described for earlier work using AlGaAs devices (5), the use of extremely shallow quantum wells is advantageous for high-speed, low-voltage S-SEED operation. The low barriers of ESQWs provide only minimal electronic confinement, so even low electric fields cause photo-generated carriers to escape rapidly from the wells. This rapid sweep-

out leads to fast, low-power S-SEEDs. ESQWs simultaneously reduce the ionization energy of confined excitons, thereby reducing the voltage required to effectively modulate light. The Al fraction between the barrier and well layers differs by only 7% in the designs used here, while the In and As fractions remain constant throughout the MQW region.

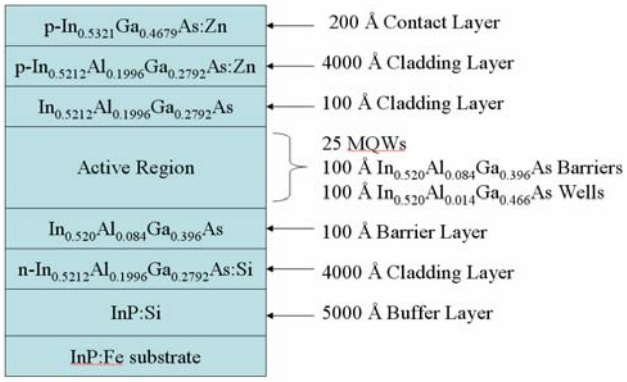

Figure 3. Layer structure of a 25-MQW S-SEED. This test structure lacks the DBR typically found below the InP:Si buffer layer, but allows complete characterization of the MQW design.

The effect of strain is significant in the InAlGaAs material system, and modeling has shown that it can be used to improve S-SEED device performance if applied correctly. Figure 4 summarizes the influence of strain on S-SEED performance. As shown in Figure 4 (left), the degree of biaxial strain (or equivalently, In mole fraction) alters the energy (wavelength) of light-hole and heavy-hole excitons. While the light and heavy holes are normally split at the lattice-matched condition, compressive strain further separates the two and leads to a device with poor optical modulation. The appropriate amount of tensile strain causes a superposition of light- and heavy-hole excitons, inducing the largest-possible optical modulation contrast. Note that once superposition is achieved, it is a simple matter of altering the Ga/Al ratio to shift the operating point to the appropriate wavelength – 1550 nm in our case.

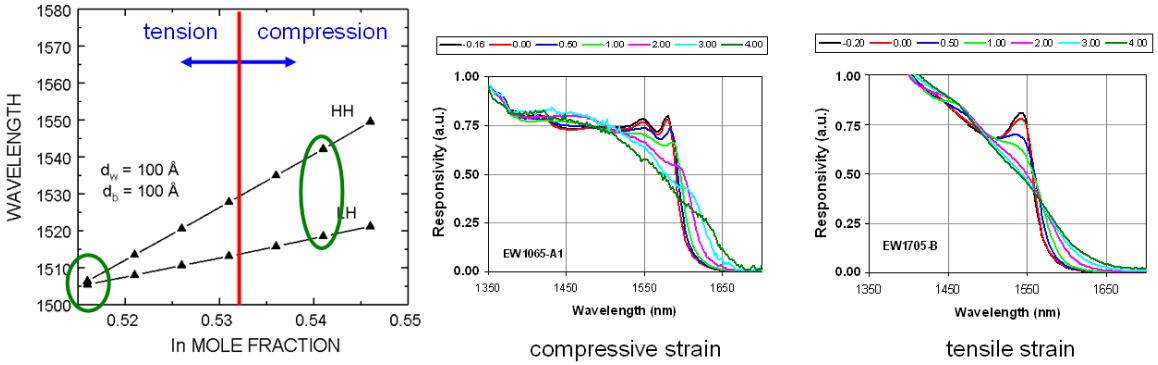

Figure 4. Effects of strain on S-SEED performance. Modeling of the conduction and valence band energy levels shows that biaxial strain alters the light- and heavy-hole transitions differently (left). Compressive strain leads to a device with separated excitons (middle), while tensile strain can achieve a condition wherein both transitions overlap and yield enhanced optical absorption (right).

The epitaxial structures described above have been grown by molecular beam epitaxy (MBE) and by metal-organic chemical vapor deposition (MOCVD). Both approaches have yielded devices with good optical absorption and contrast and with similar high-speed switching characteristics.

Distributed Bragg Reflector Design and Growth

System-level operation of an S-SEED circuit requires light to be cascaded from one S-SEED to the next. For top-illuminated, surface-normal optical devices, cascading is aided by an integrated mirror situated under the SEED diodes as shown in Figure 2. This mirror is a DBR epitaxial structure that achieves an optical reflectivity ≥80% at the operating wavelength using a stack of quarter-wave layers of alternating high and low refractive indices. DBRs have been grown using both InAlGaAs/InAlAs and InAlGaAs/InP stacks, on MOCVD and MBE platforms, respectively. Precise wavelength control was achieved using careful growth rates monitoring, and by *in-situ* optical reflectance measurements with feedback during growth. Figure 5 shows a representative post-growth optical reflectivity spectrum for one of these DBRs. In some cases, the mirrors were taken from the reactor before the S-SEED structure was grown on top. Hence, the DBR surfaces were generally terminated with a quarter-wavelength layer of InP rather than InAlGaAs to provide a relatively oxide-free surface for the regrowth. Because InP is the low-index layer in this DBR, the reflectance spectrum has a dip rather than a peak at the center of the mirror stopband.

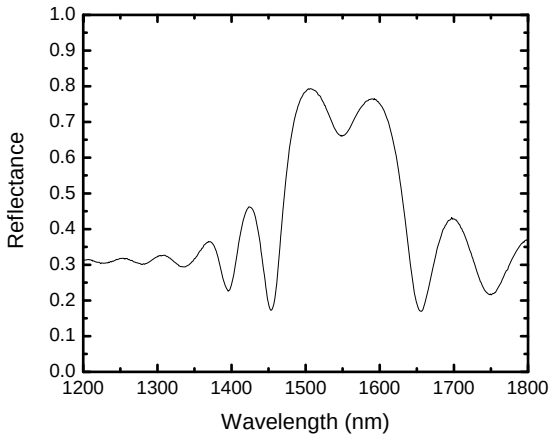

Figure 5. Reflectance spectrum of a typical InAlGaAs/InP DBR without S-SEED device epitaxy. (The S-SEED layers shown in Figure 3 are generally grown above the DBR, but their asymmetric absorption would prevent an accurate measurement of reflectivity.)

III. S-SEED Fabrication

S-SEED devices are created from the epitaxy using conventional fabrication processes and cleanroom equipment. A typical process sequence consumes a quarter of a 2-inch InP wafer, creating arrays of hundreds of S-SEEDs. Since current system-level testing requires only a few devices at a time, a large portion of the mask set is also devoted to test structures that characterize the performance of the epitaxy and the fabrication process.

The full processing sequence for S-SEED devices is relatively straightforward. After AuBe top metal deposition and liftoff for p-type ohmic contacts, a non-selective 1:4:45 H_3PO_4:H_2O_2:H_2O wet etch is used to create diode mesas. This etch extends into the n-type contact layer, and leaves behind SEEDs with diameters of about 25 μm. A lower n-type ohmic contact is deposited, followed by an HBr-based isolation etch that isolates individual devices on the undoped DBR/semi-insulating substrate. A passivation layer of PECVD silicon nitride is then blanket-deposited and selectively removed from metalized areas. Generally, the thickness of the SiN corresponds to one quarter-wave at 1550 nm, which creates an antireflection coating for incident light. In some cases we remove the passivation layer from the S-SEED aperture and use the partially-reflective top surface to provide resonant cavity absorption enhancement. Finally, photoresist bridges are patterned and hardbaked, and a final metallization is used to create wirebonding pads and to interconnect the different mesa levels. Figure 6 shows a fully processed S-SEED.

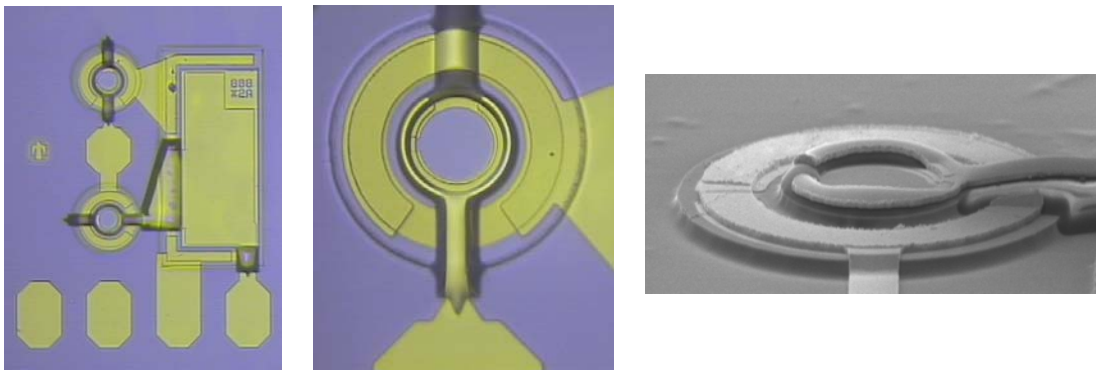

Figure 6. Optical micrograph of a fabricated S-SEED device (left). The optical aperture of a single SEED diode is roughly 18 μm in diameter for the 25 μm upper mesa shown here (middle). A scanning electron micrograph shows the wet etch profile and resist bridge used to contact the upper mesa (right).

IV. Device Characterization

DC Measurements

All processed S-SEED wafers are characterized both electrically and optically. Typical electrical measurements include full testing (i.e., I-V, V-I, reverse leakage) of single diodes and S-SEED gates. Test structures on the mask set are also helpful in characterizing contact integrity and background doping levels, using TLM and CV measurements, respectively. After electrical testing has verified initial wafer quality, optical testing can be used to investigate the performance of new S-SEED wafer designs.

Optical photoresponse is a simple and effective measurement that can determine the relative performance of an S-SEED wafer. Figure 7 shows the photocurrent generated by an S-SEED at various applied biases as a function of input wavelength. The optimized MQW region leads to the superposition of light- and heavy-hole excitons, as described earlier. Also shown in the figure is the modulation contrast as a function of wavelength and bias, referenced to zero volts. This set of curves essentially describes the ability of the S-SEED to operate as a modulator at the zero bias and high bias operating points, with 30% to 40% contrast at 2V to 4V achieved by the optimized design.

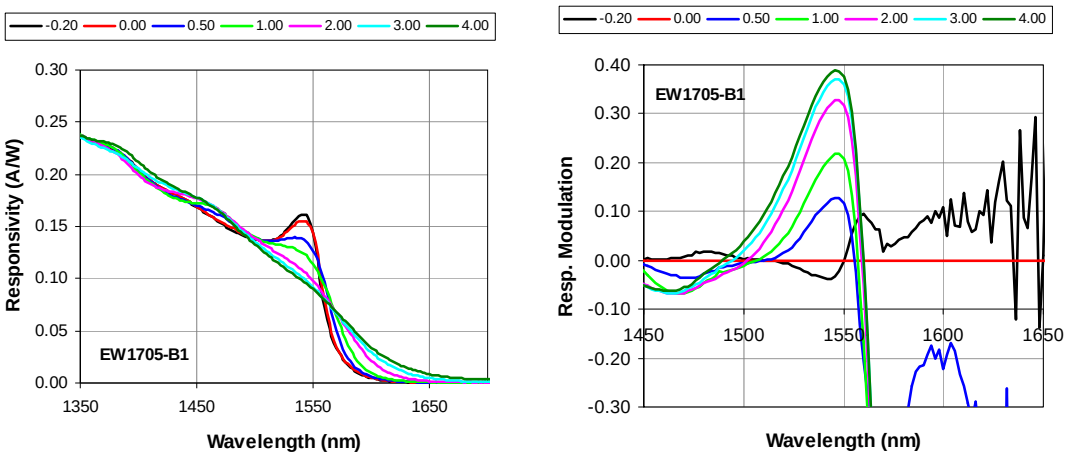

Figure 7. Optical responsivity (photocurrent) versus wavelength (right), measured at various reverse bias voltages (see legend). The strong absorption peak results from a superposition of light and heavy hole excitons, and corresponds to the operating wavelength of the device. Also shown is the calculated optical modulation compared to the zero volt absorption (left).

RF Switching Measurements

Previous measurements at Sandia demonstrated that optimized S-SEEDs operating at 860 nm were capable of optically-induced switching on the picosecond timescale (6). A transition time of 7 ps was measured for those AlGaAs-based devices. Here, we employed similar measurement techniques to determine the switching speed of 1550-nm S-SEEDs.

In order to completely characterize S-SEED switching, we used a combination of measurement techniques: optical pump-probe characterization, to provide high-speed measurements, and electrical probing, to monitor switching at low speeds. Because electrical probing adds a large capacitive load to the device under test, this method could not be employed to characterize true switching speeds. However, a custom high-speed active probe was assembled to minimize device loading (its capacitance is less than 1 pF) and provided a measurement bandwidth of ~1.5 GHz. Figure 8 shows an electrical measurement of S-SEED switching with this probe. As seen in the image, the active probe was used to monitor the voltage on the center node of the S-SEED. The oscilloscope trace shows that full rail-to-rail switching has been achieved, even in the presence of parasitic loading.

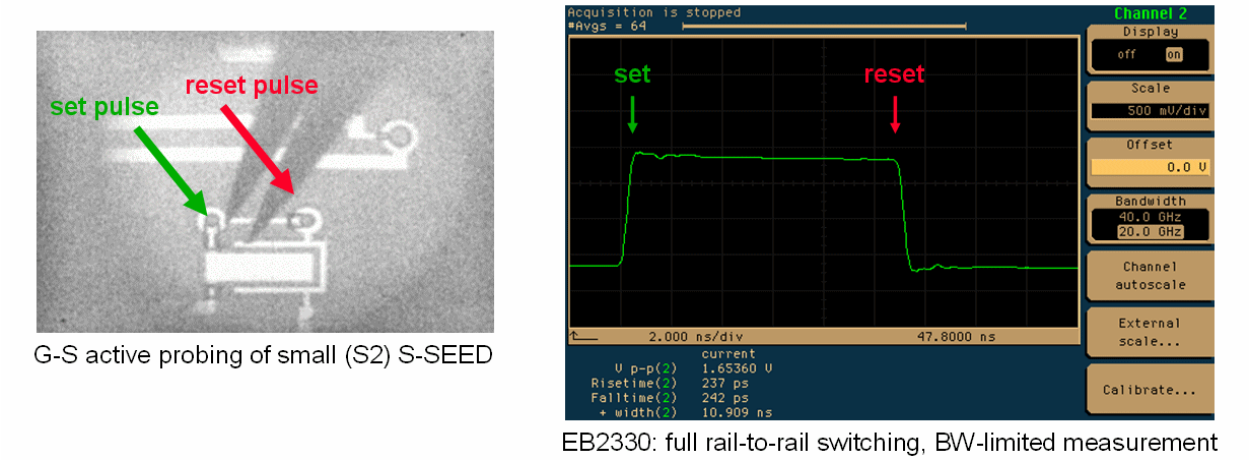

Figure 8. Electrical monitoring of S-SEED switching using an active, low-capacitance, ground-signal probe. (The InGaAs CCD used for imaging is capable of viewing the 1550-nm input beams but leads to the grainy photo.) The voltage on the S-SEED center node is displayed in the oscilloscope trace, demonstrating full rail-to-rail switching with a 1-V bias. Transition times are bandwidth-limited by the measurement apparatus.

Using the pump-probe setup shown in Figure 9, the switching speed of InAlGaAs S-SEED devices was investigated. Optical switching at 1550 nm was measured with a 20% – 80% transition time of 5.5 ps, as shown in Figure 10. This promising high-speed switching result demonstrates that our 1550-nm InAlGaAs-based S-SEED devices have the potential to operate beyond 40 GHz in an integrated optical logic circuit.

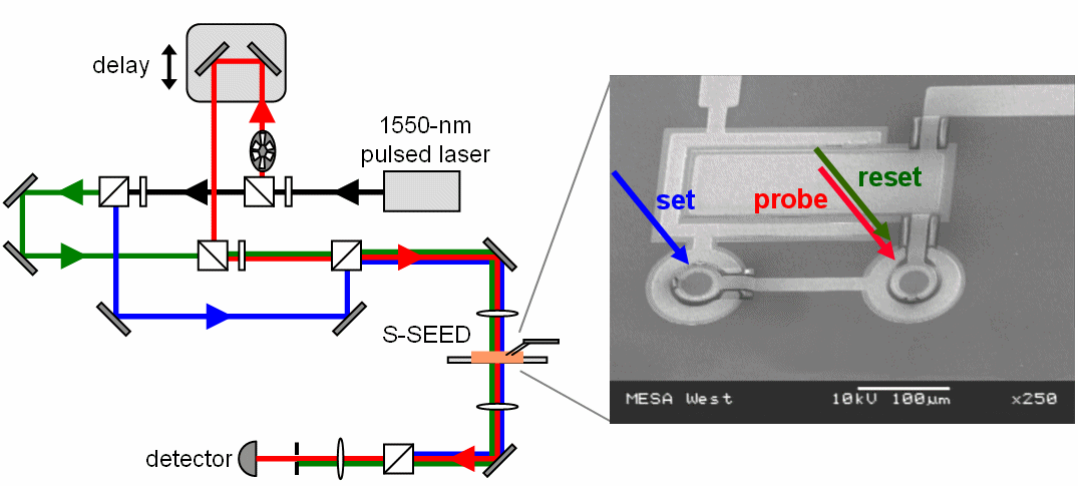

Figure 9. Optical pump-probe setup to measure switching for a 1550-nm S-SEED device. The set and reset beams toggle the device state at the laser repetition rate. A delay stage enables optical interrogation of the device state by a probe beam, which maps out the transition with picosecond resolution.

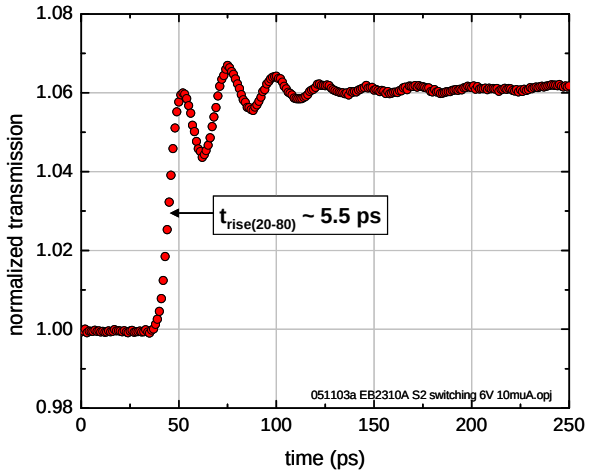

Figure 10. Optical pump-probe measurement of a 1550-nm S-SEED device, demonstrating switching of logic states with a transition time of 5.5 ps. The transition is accompanied by ringing due to the diode capacitance and wiring inductance, which yield an LC frequency of approximately 40 GHz. Experimental parameters: 25-μm mesas, 6-V applied bias, pump energy ~2.5 pJ.

V. Technology Summary

1550-nm S-SEEDs have been designed and fabricated in the InAlGaAs material system. Strain engineering has been used to improve modulation contrast by altering the valence band structure and superpose the light- and heavy-hole excitonic absorption energies. Extremely shallow quantum wells have been employed to reduce carrier sweep-out times and to lower operating voltages. High-speed optical pump-probe testing of individual S-SEEDs shows that switching between logic states occurs with transition times below 6 ps, suggesting suitability for logic operation beyond 40 GHz.

While this paper has focused on the design, fabrication and characterization of a single S-SEED gate, integrated multi-gate systems will require the ability to precisely route and focus optical beams between S-SEEDs. We are currently investigating the use of micro-optic arrays for S-SEED interconnection, an approach that can achieve systems of moderate logical complexity with a compact, chip-scale footprint (4). By appropriately packaging optoelectronic gates with micro-optic interconnects, S-SEED technology may prove to be a scalable solution for future ultrafast optical data processing applications.

Acknowledgments

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