

Limits to Silicon Modulator Bandwidth and Power Consumption

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Outline

Exascale Computing: Challenges Ahead

Modulator Bandwidth and Power Consumption

Bandpass Switches

Adiabatic Microring Resonators

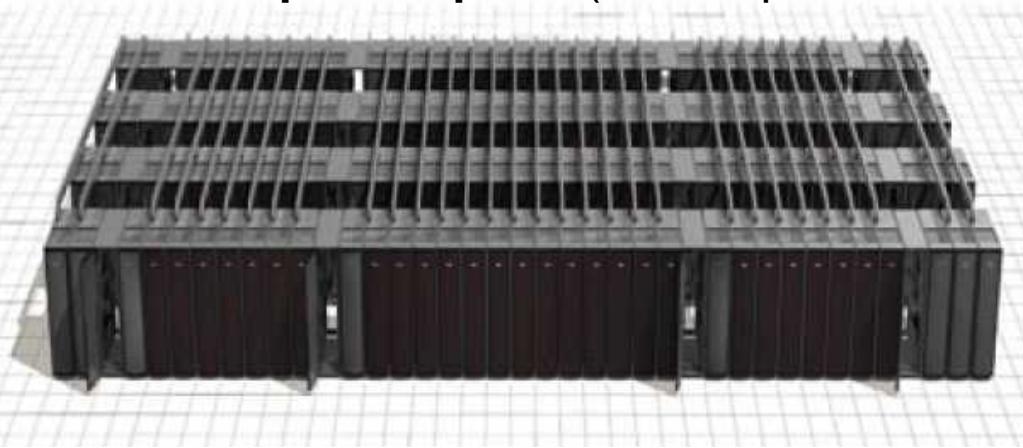


Motivation: Power / Bandwidth in Supercomputers

"Based on current trends, by 2011 data center energy consumption will nearly double again, requiring the equivalent of 25 power plants. The world's data centers, according to recent study from McKinsey & Company, could well surpass the airline industry as a greenhouse gas polluter by 2020."

Quote from "Demand for Data Puts Engineers in Spotlight," New York Times, June 17, 2008

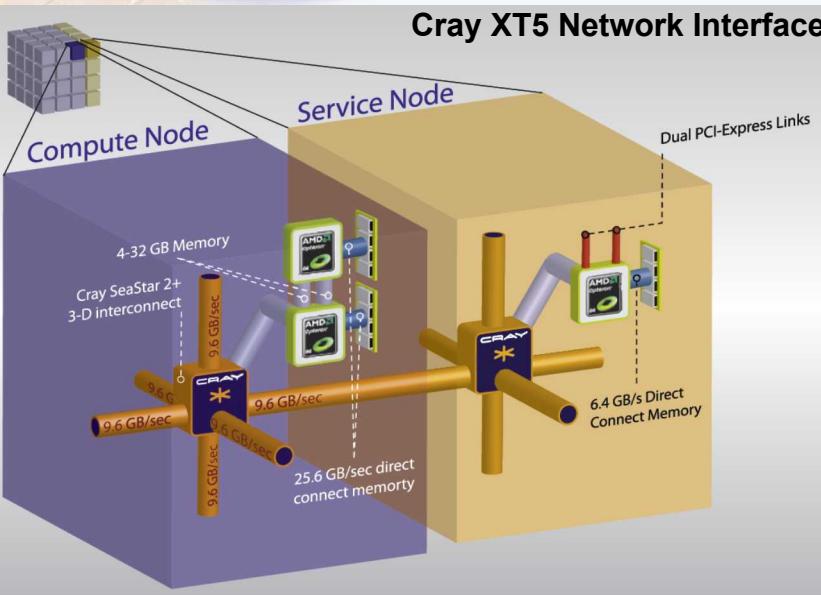
Sandia's Red Storm Supercomputer (26,569 processor cores, ~3.5MW power)



- Question:** Now at 1PFLOPs, what does it take to get to 1-ExaFLOPs?
- Power:** Hoover Dam provides ~1GW . . . what will future supercomputers need?
- Bandwidth:** To scale real-world application performance, communications must scale with compute performance (i.e. bytes/FLOP ~ 1)



Interconnect Requirements for Super-Computers



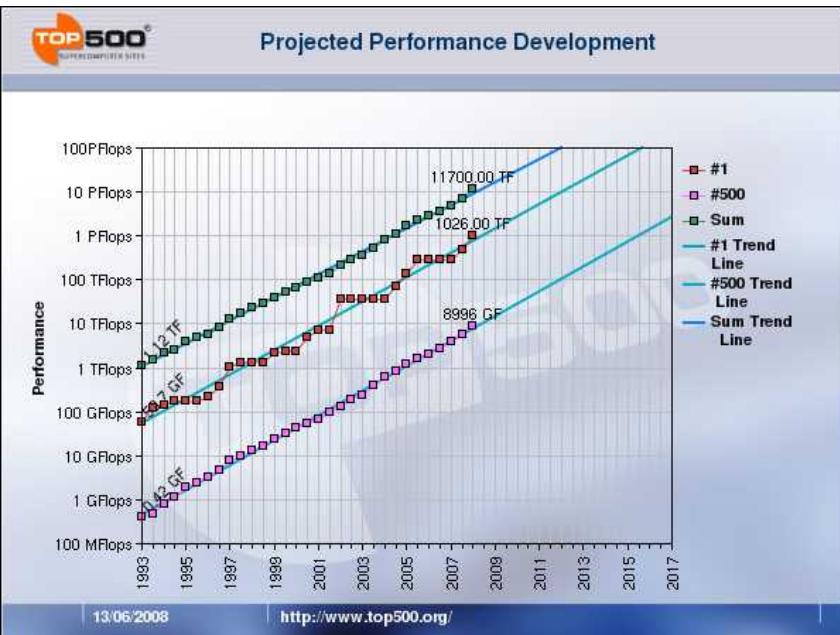
Today (2008)

- ❑ **BW/node:** $6 \times 9.6\text{GB/s} + 6.4\text{GB/s} \rightarrow 0.512\text{Tb/s/node}$
- ❑ **BW/core:** 0.512Tb/s ($\sim 1 \text{ Byte/FLOP}$ orig.)
– now BW/core is $\sim 128\text{Gb/s}$
- ❑ Top machines achieve $\sim 1\text{PFLOPs}$ peak
- ❑ $\sim 20\%$ power is used for network comm.

Future (2018)

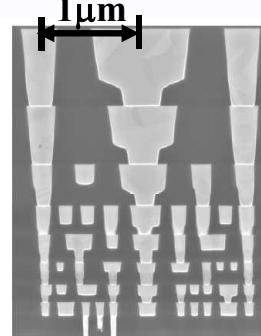
- ❑ Expected to reach 1-ExaFLOPs
- ❑ ITRS projects we will reach 17nm node
- ❑ Cores/chip > 100 , conservatively
- ❑ $100\text{cores/chip} \times 0.51\text{Tb/s/core} = 51\text{Tb/s/chip}$

Can the bandwidth requirements be achieved with electrical signaling at reasonable power levels?



Can Electronics meet BW Requirements?

IBM 65nm Process Metal

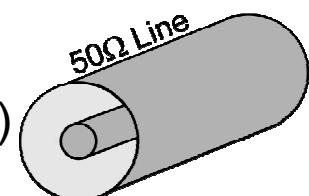


Intrachip Electrical: Charged Lines

- Energy/Bit: $CV_0^2/4 \rightarrow \sim 0.5 \text{pJ/bit/cm}$ (25W for 50Tb/s)
- Bandwidth: Achieve $\sim 1 \text{Gb/s}/1 \mu\text{m} \rightarrow 10 \text{Tb/s/cm/layer} \rightarrow 5 \text{ layers}$
- Conclusion: On-chip electrical signaling is troublesome in 2018

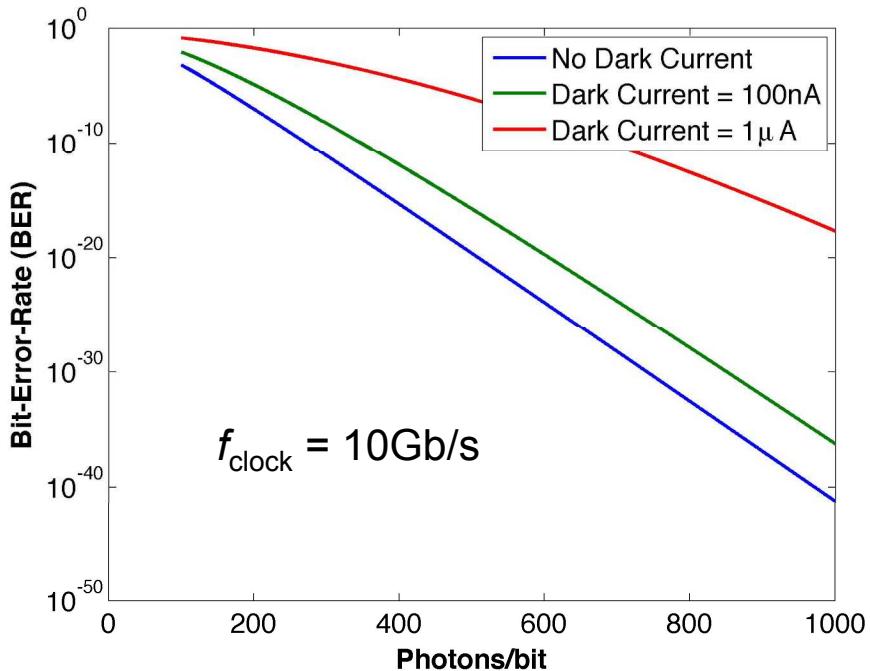
Interchip Electrical: Transmission Lines

- Energy/Bit: $\tau V_0^2/2Z_0 \rightarrow \sim 10 \text{pJ/bit}$ (50Ω line, 1ns pulse, 1-Volt signal)
 - Chip Comm. Power: $50 \text{Tb/s} \times 10 \text{pJ/bit} \rightarrow 500 \text{W/chip}$
 - System Comm. Power: 1-ExaFLOPs $\rightarrow 1.6 \text{GW Communications Power}$
- Bandwidth
 - Board: 100Gb/s/cm/layer 50 layers $\rightarrow 50 \text{Tb/s}$
 - Pins-to-board: $10 \text{Gb/s/pin} \rightarrow 5000 \text{ pins/chip} \rightarrow 50 \text{Tb/s}$
 - Inter-Rack: 5000 wires/chip, 500-chips/rack $\rightarrow 2.5 \text{M wires/rack}$
- Conclusion: Logistically, off-chip electrical signaling becomes impossible



Receiver Power for Optical Communications

Bit-Error Rate (Fundamental)



Results Based Shot, Johnson, and Dark Current Noise

- ❑ Require Dark Current $< 100nA$
- ❑ 1000 Photons/Bit is sufficient
- ❑ Figure 10dB loss, 10% E-O efficiency, still only 15fJ/bit

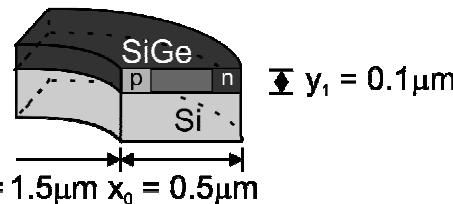
Capacitance (Technological)

Required Voltage: $V = Q/C_T$

- ❑ $C_T = C_g + C_d$, so capacitance can be dominated gate or photo-detector

Photodetector Capacitance

$$\square C_d = \epsilon A/d \approx 12\epsilon_0 (2\pi \cdot 2 \cdot 0.1) \cdot 10^{-6} / 0.5 \\ \approx 0.27 \text{ fF}$$



Gate Capacitance

- ❑ ITRS-HP Roadmap $C_g \sim 0.5fF/\mu m$

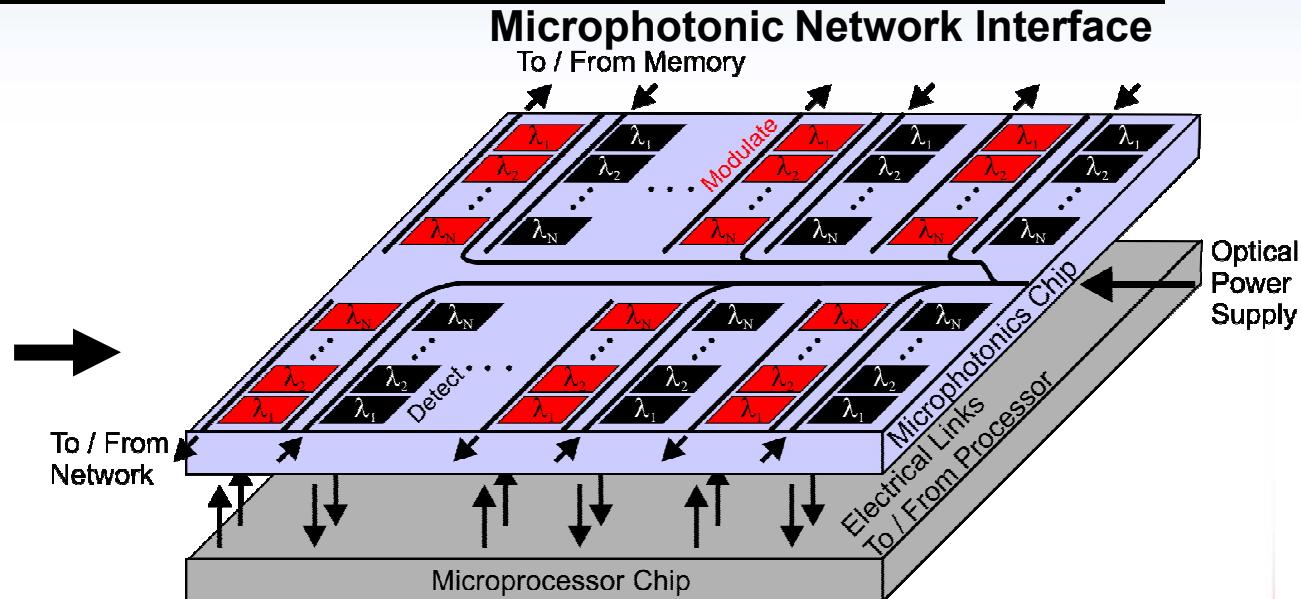
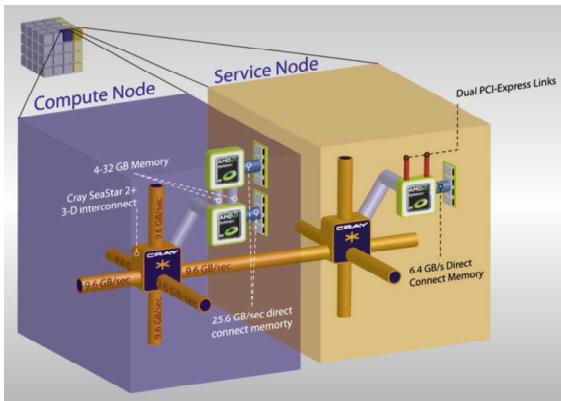
Initial Conclusion

- ❑ 0.3fF corresponds to ~ 2000 photons required or $\sim 0.3fJ/bit$ at the receiver
- ❑ Even with 20dB penalty $\sim 30fJ/bit$



What about an Optical Network Interface?

Electrical Network Interface



Optical Communications (Tightly Integrated with CMOS)

Energy/Bit = $h\nu V_0 C / (\eta q)$ (achieve $<100\text{fJ/bit} \rightarrow <16\text{MW @exascale}$)

- Receiver: $<1\text{fJ/bit}$ required to flip a gate (Miller, 1989)
- Modulator: Limited by capacitance (70fJ/bit power budget)

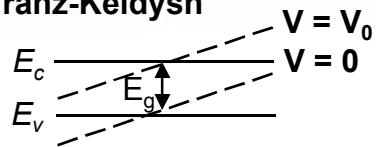
Bandwidth

- Line bandwidth: $>1\text{-Tb/s}$ (10Gb/s @100 λ 's), 50GHz spacings \rightarrow **5THz (40nm)**
- Bandwidth (on-chip): $> 200\text{Gb/s}/\mu\text{m} \rightarrow$ **1Tb/s on a 5um pitch**
- Bandwidth (off-chip) $> \sim 10\text{Tb/s/mm}$ (**5mm $\rightarrow 50\text{Tb/s, 25k fibers/rack}$**)
- Routing of data could be O-E-O or in the optical domain . . .

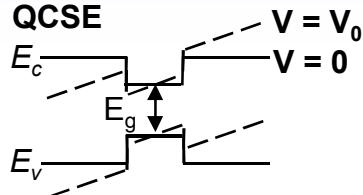
Possible Effects in Si/Ge Systems

Ge: Band-Edge Effects (Electro-Absorption $\Delta\alpha$)

Franz-Keldysh

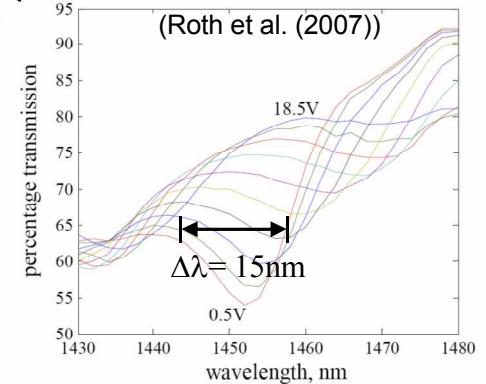


QCSE



- Franz-Keldysh (Liu et al. *NP*, July 2008)
- Quantum Confined Stark (Roth et al. *OE*, April 2007)
- Advantage:** Strong effect \rightarrow small, low power devices (Liu claims 50fJ/bit)
- Disadvantages:** \rightarrow Limited Optical Bandwidth ($\Delta\lambda = 10\text{nm-to-}15\text{nm}$)
Limited Contrast ($\Delta\alpha/\alpha \sim 3$), Intricate Fabrication

Quantum Confined Stark Effect

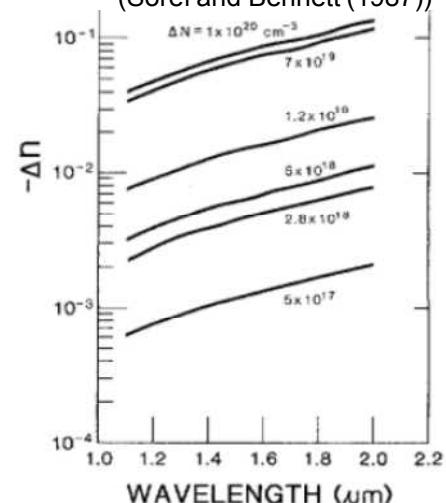


Si: Free-Carrier Effect (Electro-Refraction Δn)

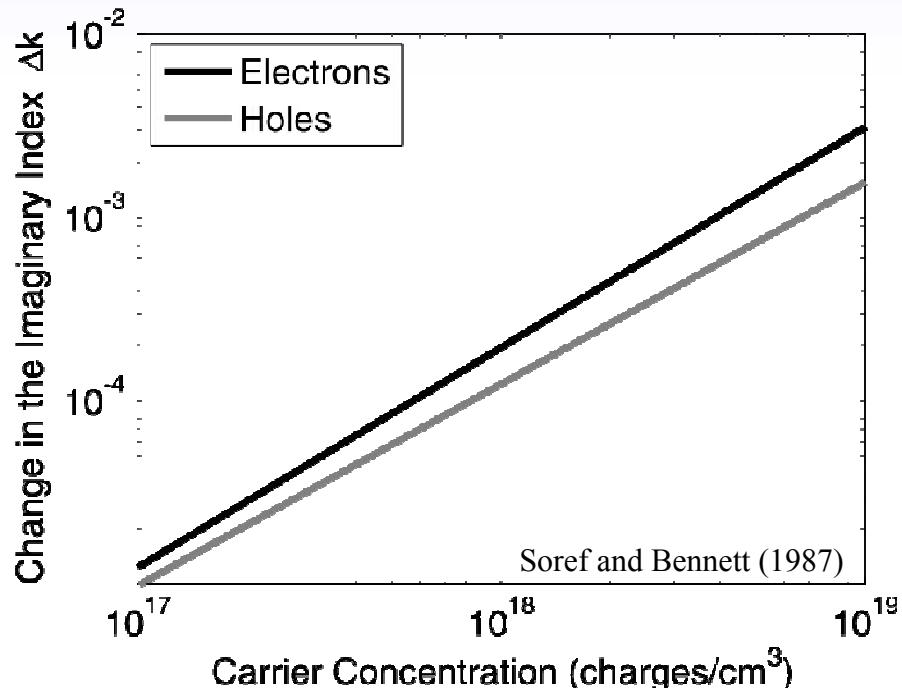
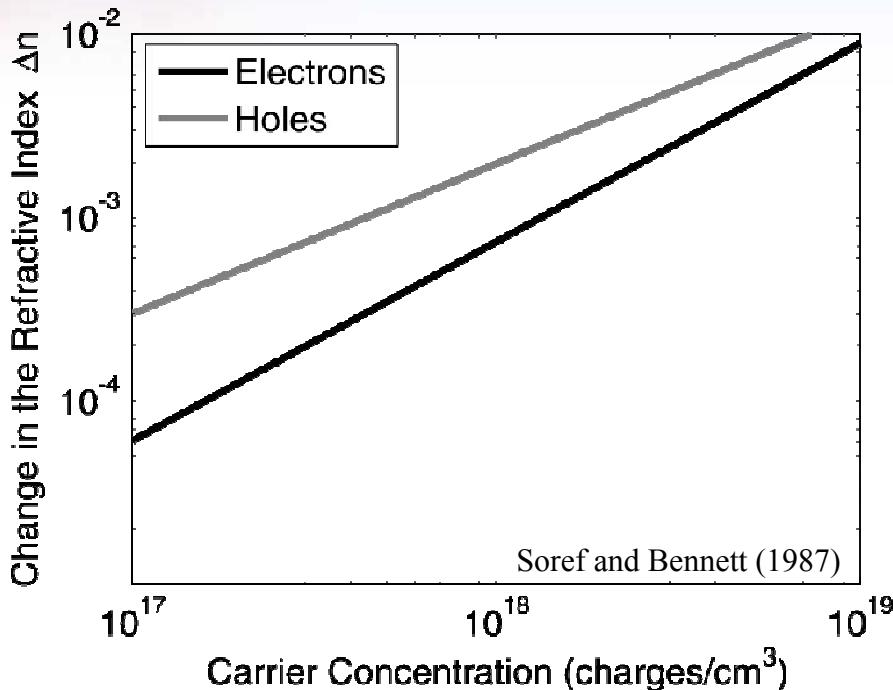
- Advantages:** Broadband effect ($\Delta\lambda \gg 100\text{nm}$),
easy CMOS implementation
- Disadvantages:** Weaker effect \rightarrow
need resonance for low energy/bit,
but already have thousands of
resonators on-chip

Free-Carrier Effect

(Soref and Bennett (1987))



Magnitude of the Free-Carrier Effect

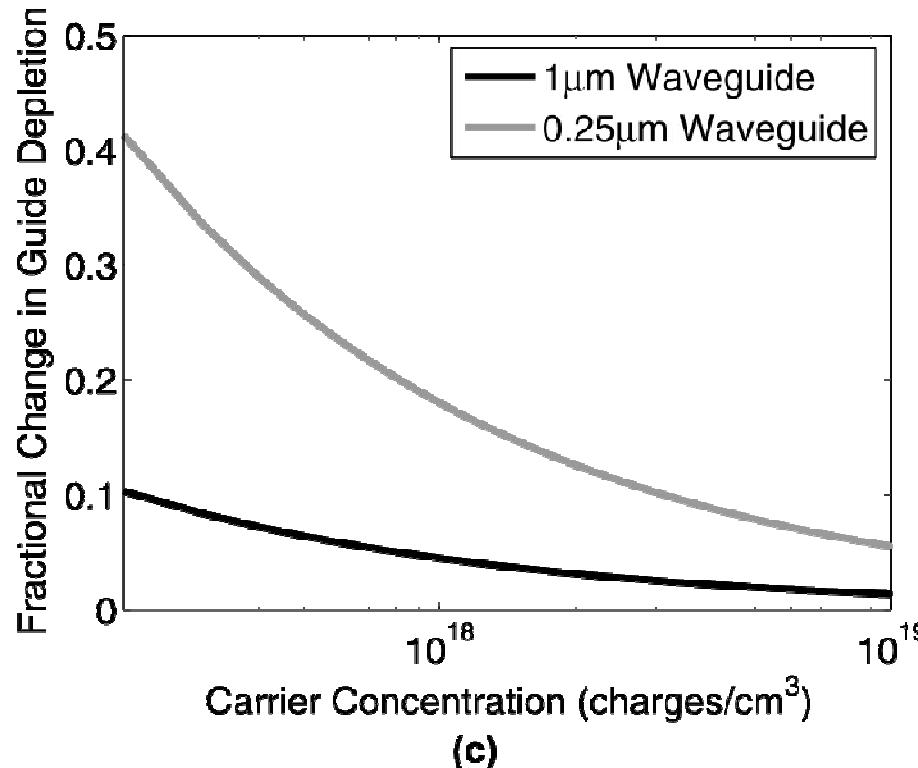
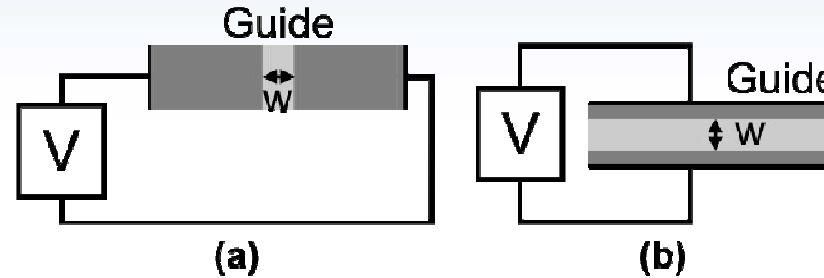


Important Points

- ❑ Effect is small
- ❑ Larger real change in index than imaginary
- ❑ Holes impact real part of the index more than electrons
- ❑ Holes induce less loss than electrons



Geometry Considerations (Depletion Approach)



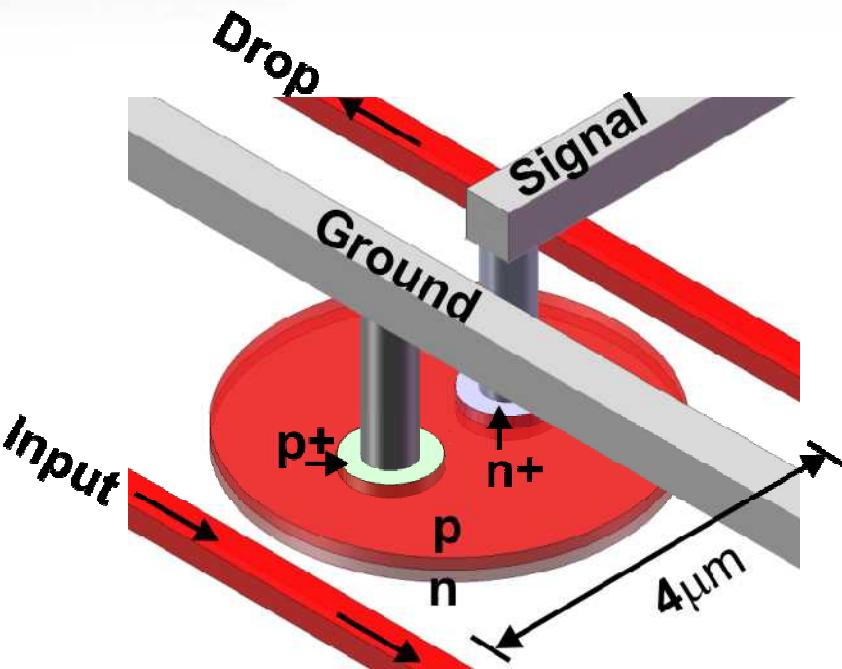
Important to Take Maximal Advantage of a Small Effect:

Since, waveguides are wide and thin for fabrication reasons, vertical junctions provide a greater overlap with depletion region

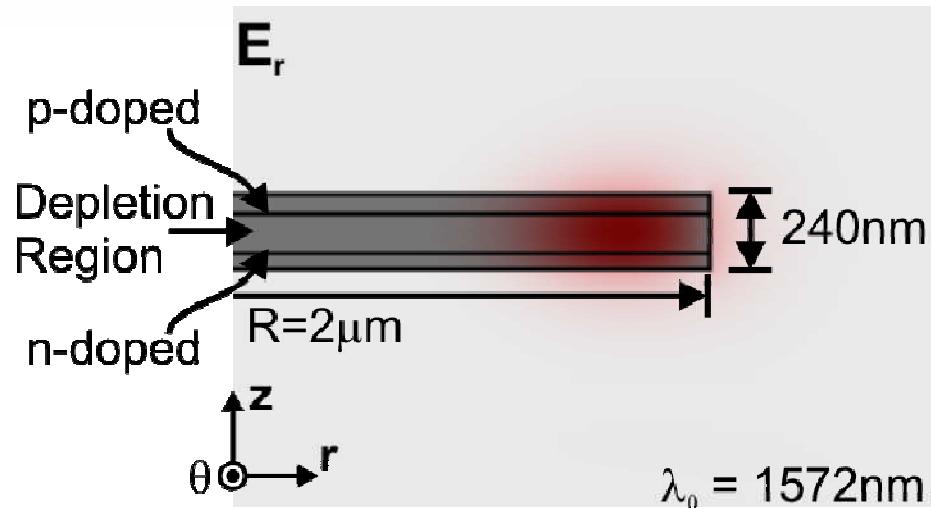


Microdisk Modulators: A Vertical P-N Junction

Vertical P-N Junction



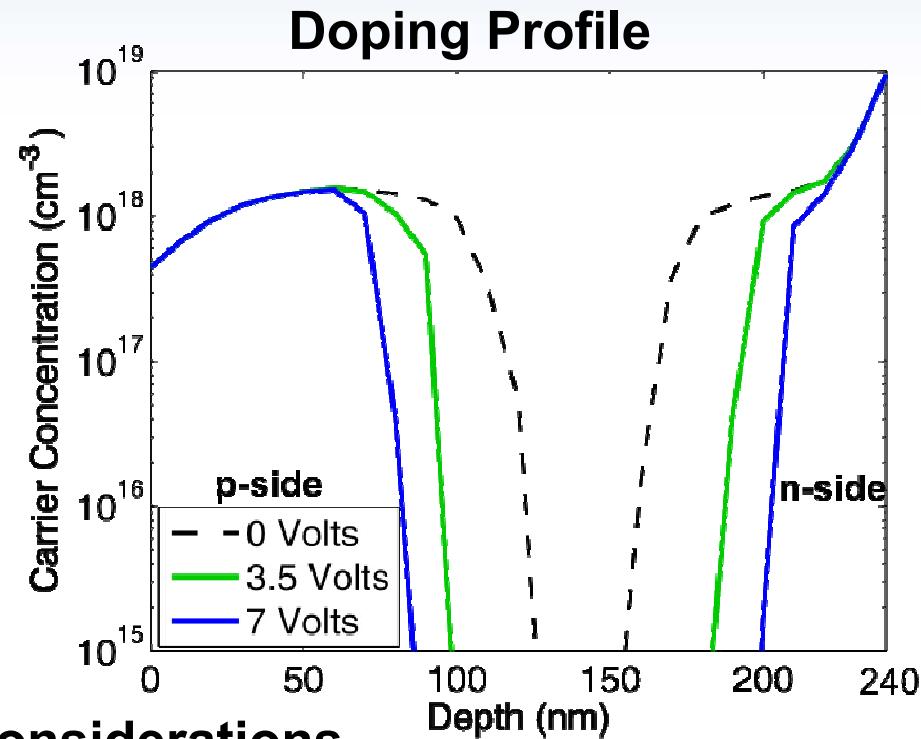
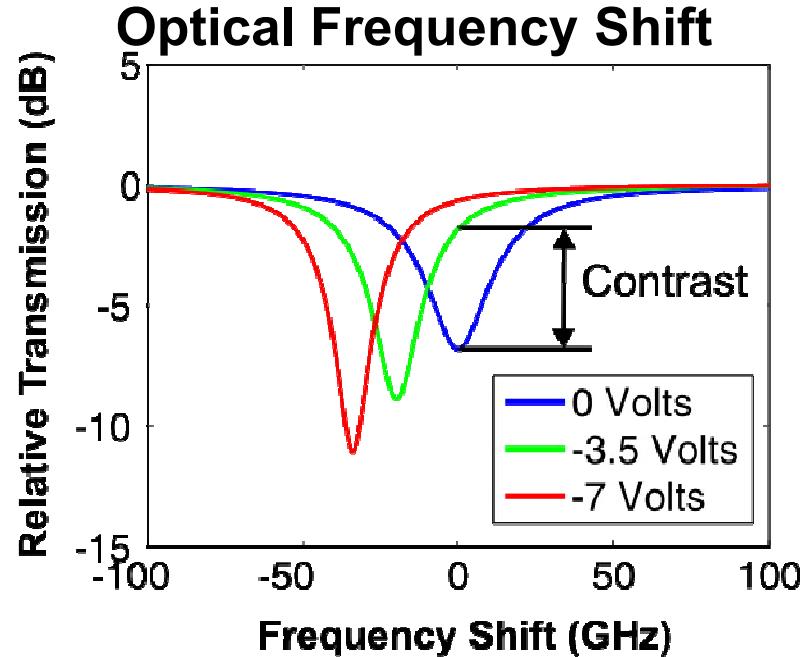
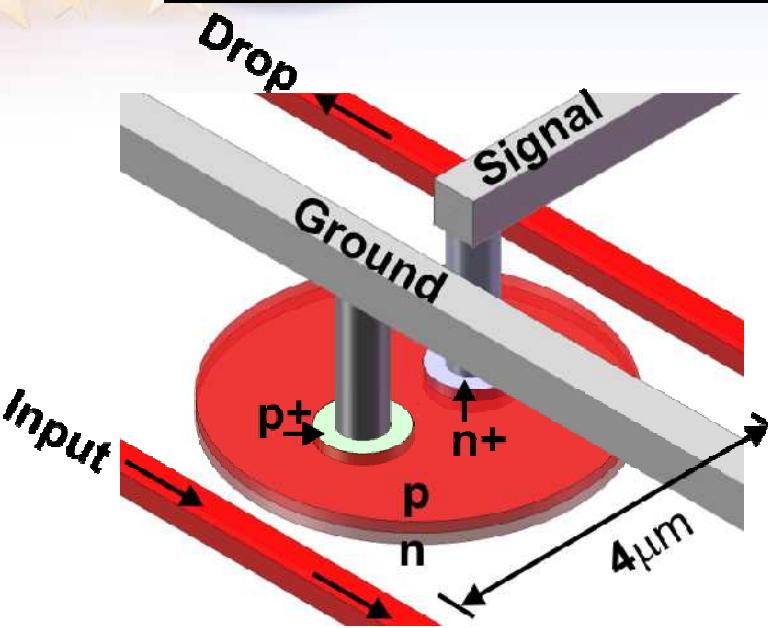
TE₁₁ Cylindrical Mode



Advantages of a Vertical P-N Junction Modulator

- Vertical P-N junction enables tighter confinement and large modal overlap
- Devices as small as $R = 1.5 \mu\text{m}$ are possible
- Huge Free-Spectral-Range ($> 9 \text{ THz}$ possible w/ $R=1.5 \mu\text{m}$)
- Smaller devices, no pre-emphasis → faster / lower power

Anticipated Optical Response



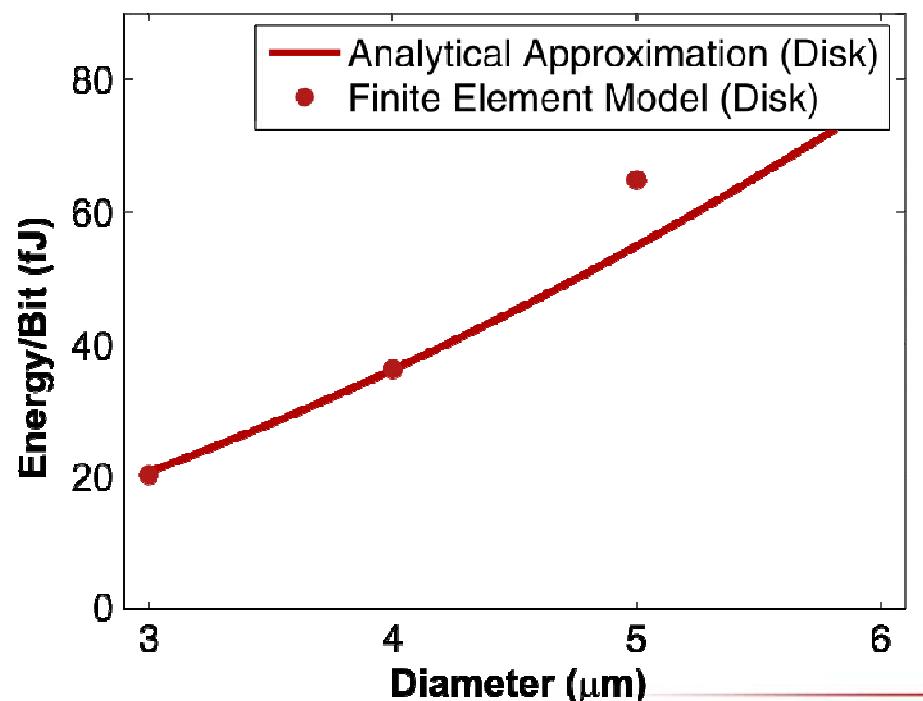
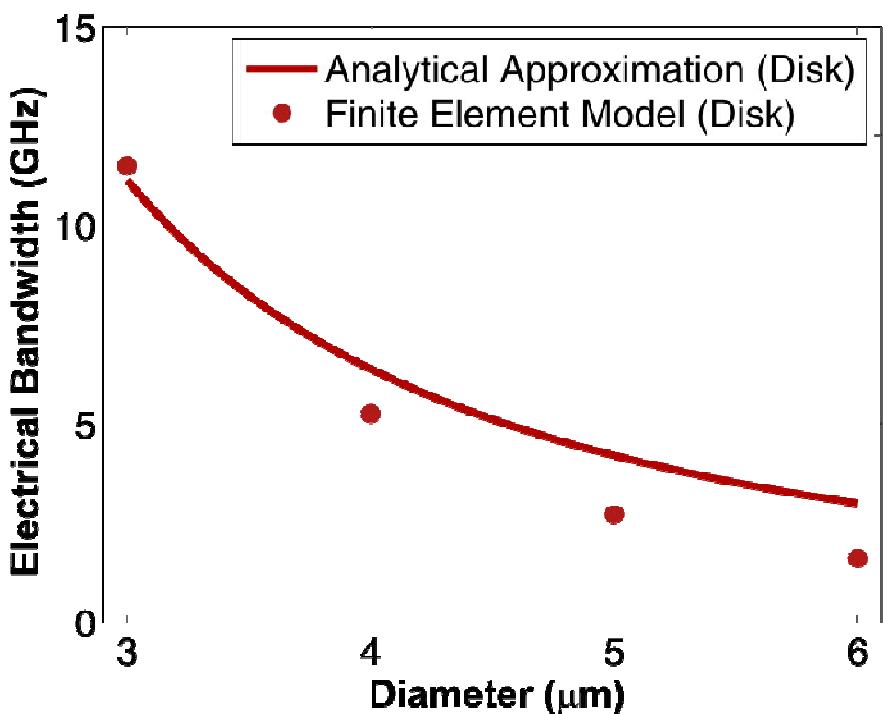
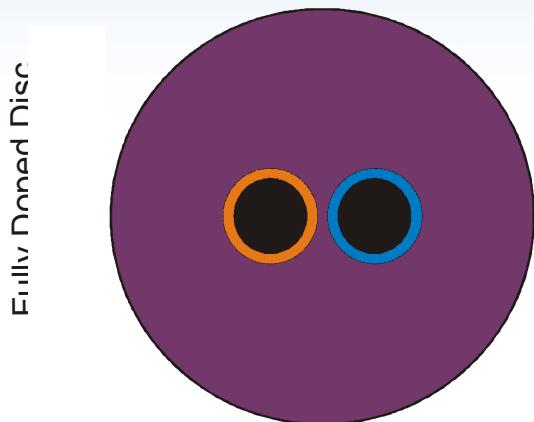
Considerations

- Depletion goes as square-root of doping, but index change is ~ linear with doping, so higher-doping \Rightarrow a larger change
- Higher doping levels also induce loss, limiting Q and contrast, but chosen Q must also be sufficiently low for a given BW

Simple Disk: Bandwidth and Energy/Bit

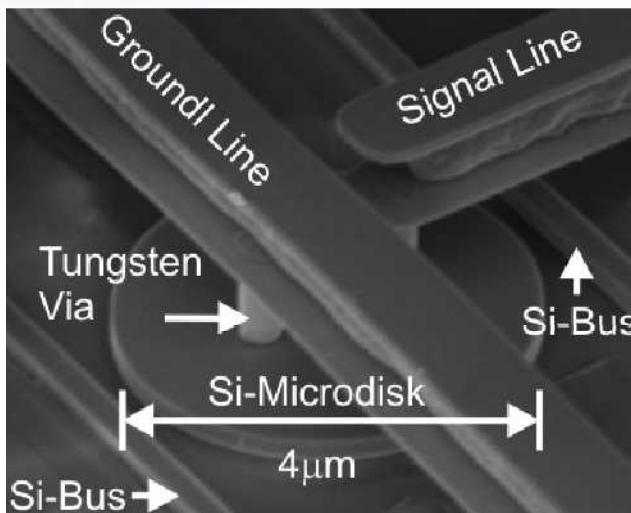
Modeling Results

- **Bandwidth:** >5GHz possible at 4 μm diameter
- **Energy/Bit:** ~20fJ/bit possible at 3 μm diameter (2.5V) and can be reduced by going to higher-Q rings and slower modulation speeds . . . but . . . thermal control

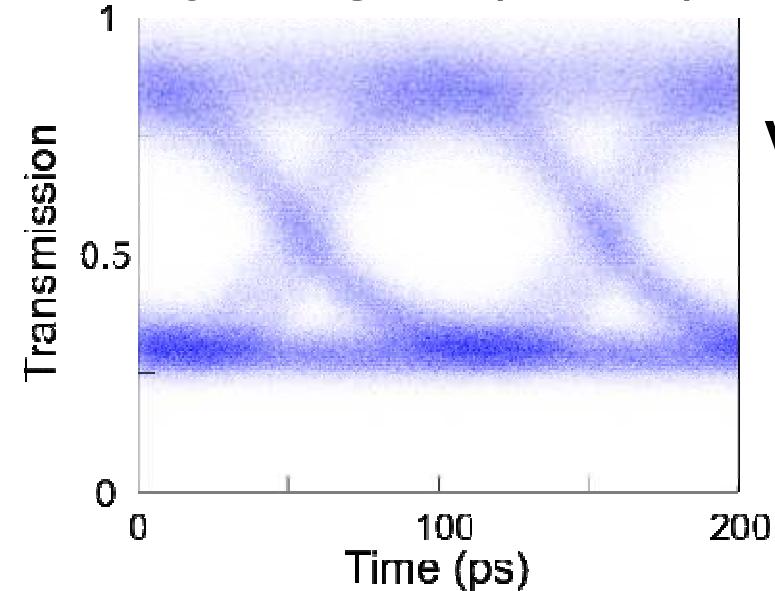


Microdisk Modulator Demonstration

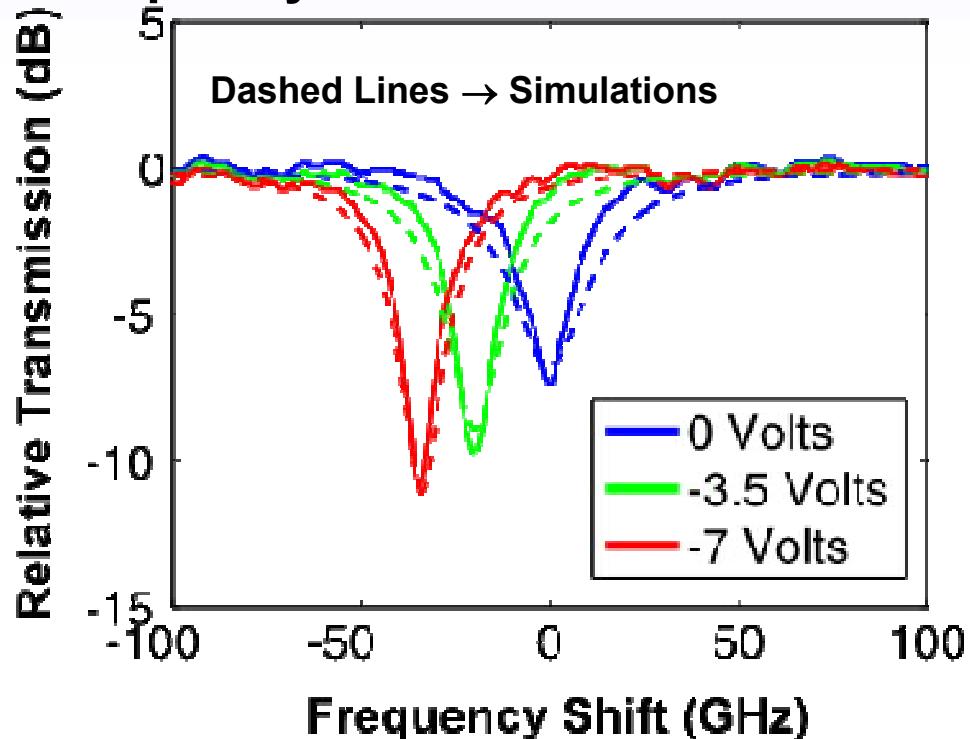
SEM of the Microdisk



Eye Diagram (10Gb/s)



Frequency Shift vs. Reverse Bias



Vertical Junction Reverse-Biased Results

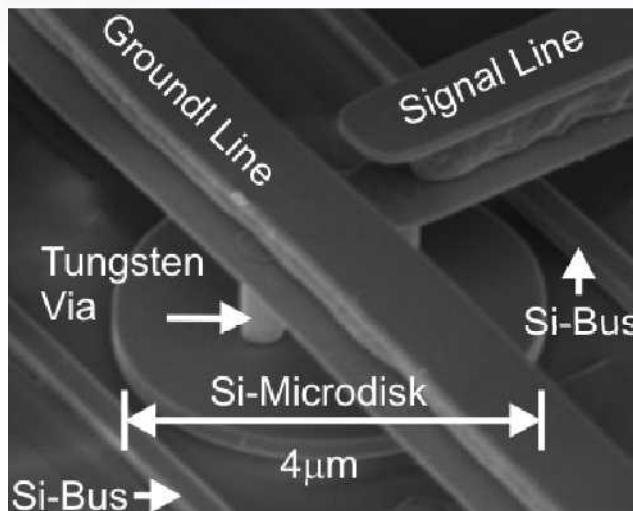
- 35-GHz freq. shift demo'ed, >70-GHz possible
- Achieved a $\text{BER} < 10^{-12}$ at 10Gb/s
- First resonant modulator with CMOS compatible drive (1.8V incident, ~3.5V due to reflection)

*Note: 2.5V/3.3V are avail. CMOS voltages @90nm

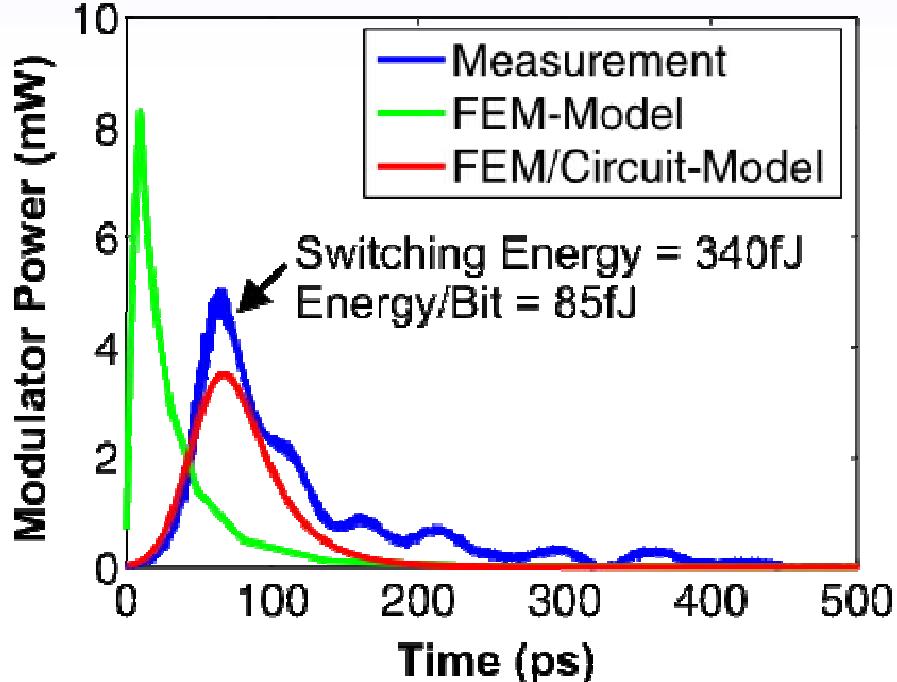


Power Efficiency Measurement (energy/bit)

SEM of the Microdisk



TDR Measurement vs. Simulations



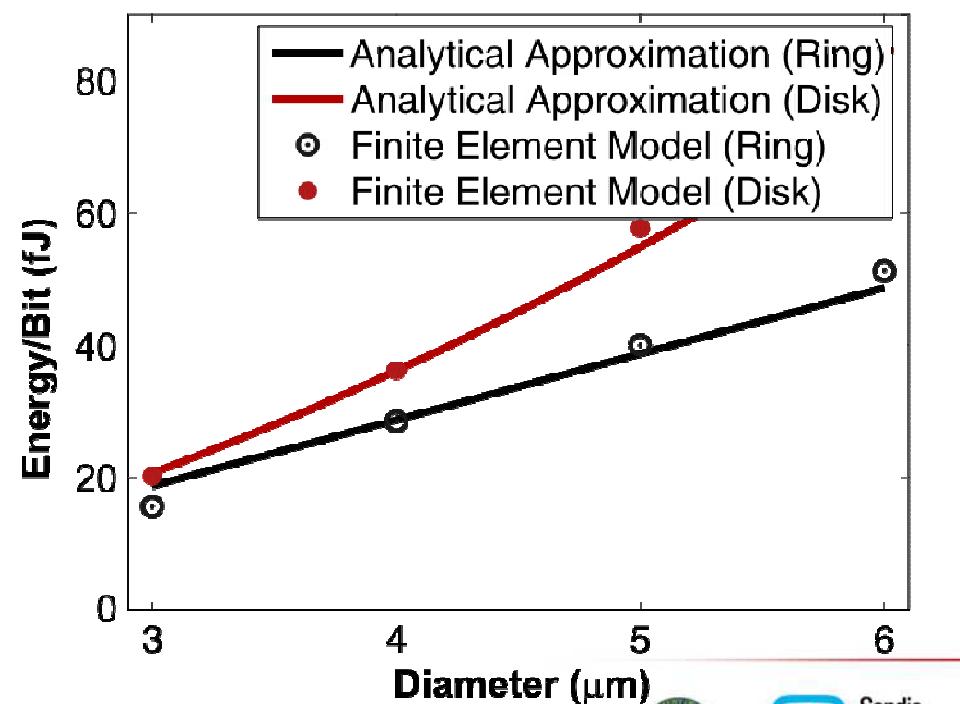
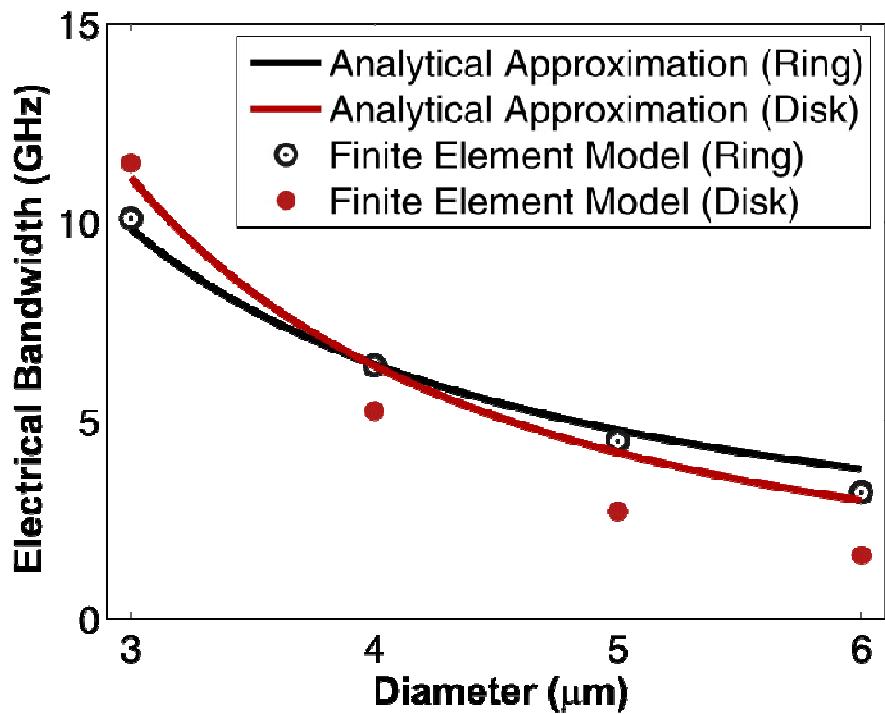
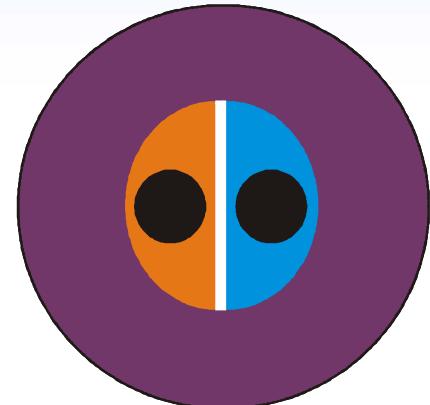
Time Domain Reflectometry Measurement Results (@3.5V)

- ❑ Depletion-based approach dissipates essentially no static power
- ❑ Switching Energy = 340fJ
- ❑ PRBS Energy/Bit = Switching Energy/4 = 85fJ (**100X less than electrical**)
- ❑ New designs indicate ~10fJ/bit is possible

Can We Do Any Better?

Modeling Results

- **Bandwidth:** Reduces capacitance, increases resistance
- **Energy/Bit:** Reduced capacitance lowers energy/bit
- **Conclusions:** Do a little better . . . mostly on energy/bit
perhaps even more intricate doping schemes are necessary
. . . perhaps higher-Q devices





Quick Review of Modulators

Modulators

- ❑ **Potential:** Replacement for electrical interconnects with >100X increase in bandwidth density and >100X reduction in energy/bit. At exascale we would be looking at 16MW of communication power instead of 1.6GW of communications power.
- ❑ **Demonstration:** Smallest, highest speed (10Gb/s), lowest energy/bit (85fJ), and lowest voltage (3.5V) resonant silicon modulators
- ❑ **Future Work:** Improved doping profiles to reach 20fJ/bit and higher bandwidths, thermal control, and terabit/s links . . .

So, What Else?

- ❑ Try coupling some disks together . . .

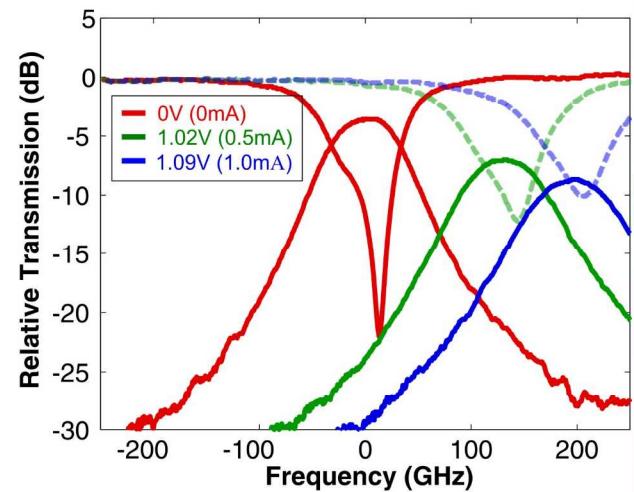
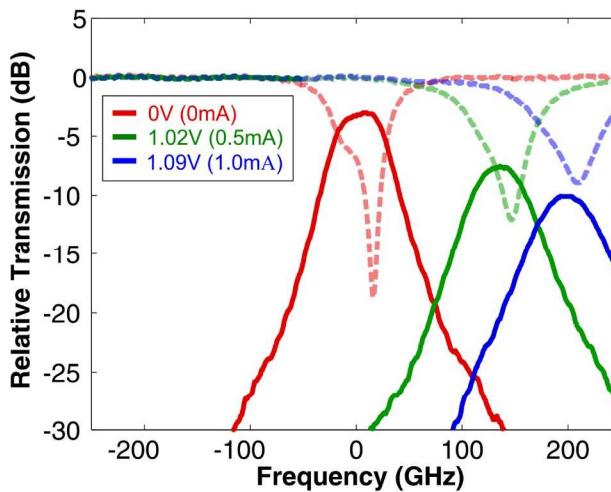
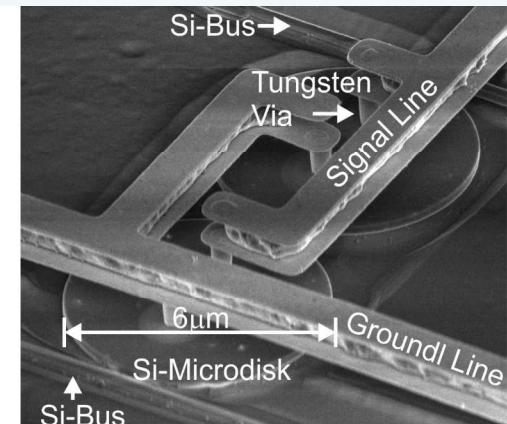
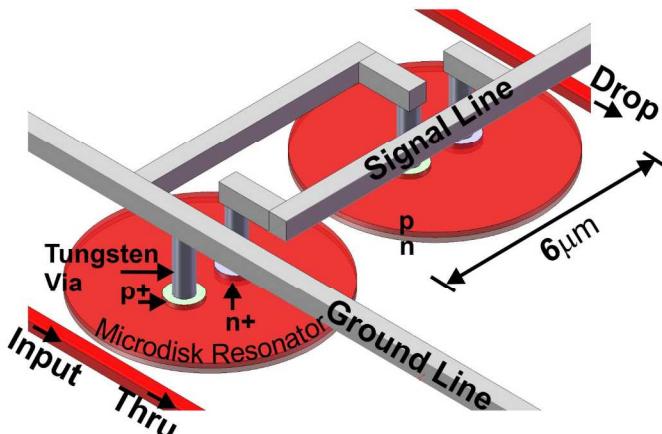


Sandia
National
Laboratories

Reconfigurable Networks: Bandpass Switch

Demonstration

- 1st demonstration of high-speed, electrically active, silicon bandpass switches
- Completely shift resonator bandpass out of the channel

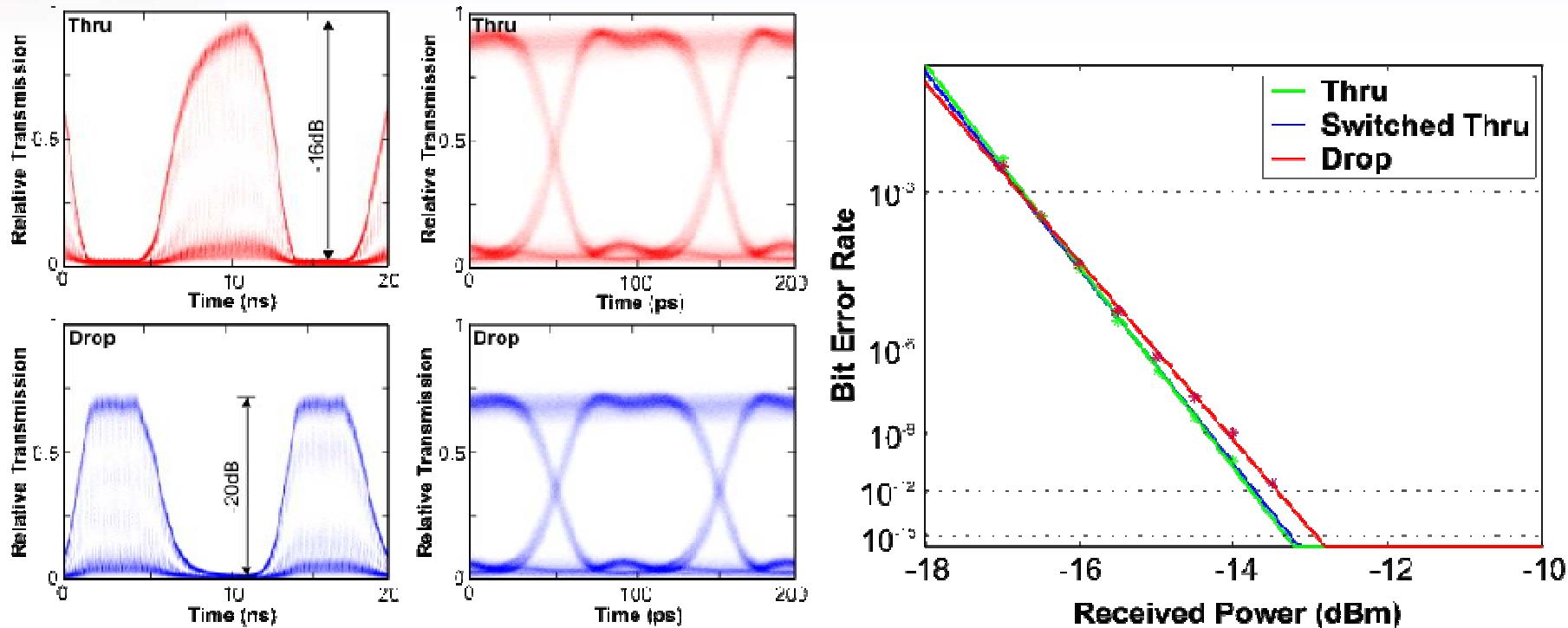


Benefits

- Potential for ultralow power switching in the optical domain (to avoid OEO conversions)

M. R. Watts et al., OFC Postdeadline Presentation (Feb. 2008)

Data Routing with Bandpass Switch

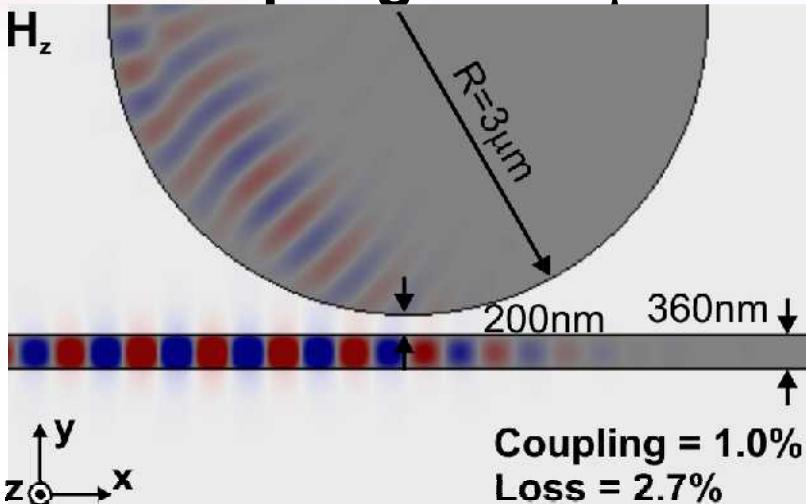


Switch Results

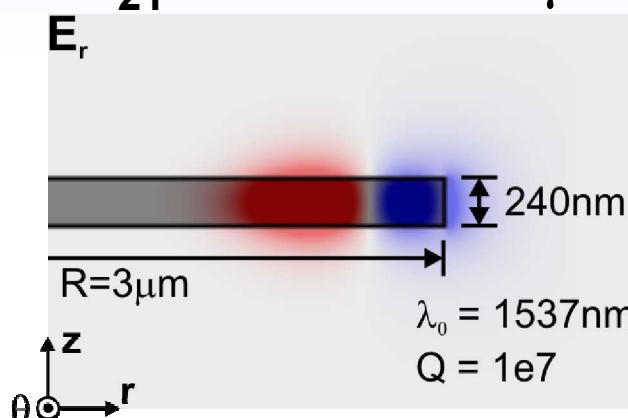
- Data switched error-free ($BER < 10^{-12}$) with little power with ~ 2 ns rise time
- Power penalty measured to be < 0.4 dB in Drop Port and < 0.1 dB in Thru Port
- Driven with ~ 0.6 V (~ 1 V due to reflection), so CMOS compatible
- Still, there are some problems with microdisks . . .

Problem 1: Coupling Losses

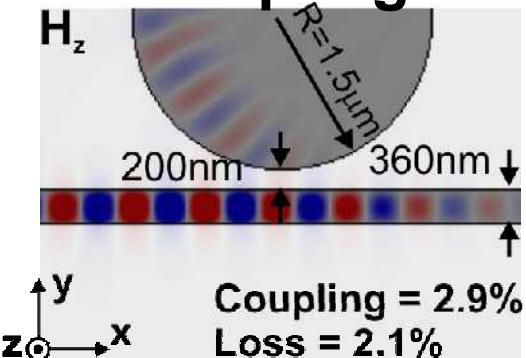
TE Coupling: $R = 3\mu\text{m}$



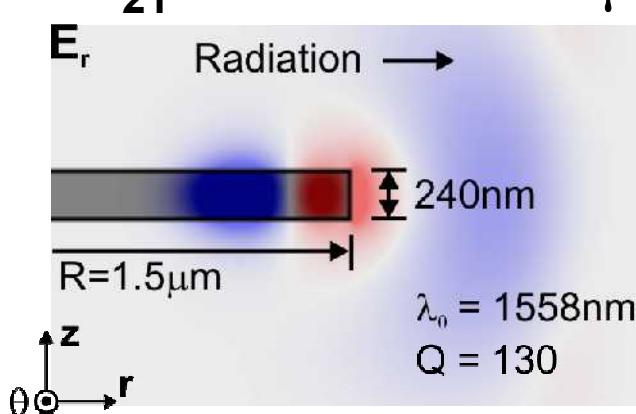
TE₂₁ Mode: $R = 3\mu\text{m}$



TE Coupling: $R = 1.5\mu\text{m}$



TE₂₁ Mode: $R = 1.5\mu\text{m}$



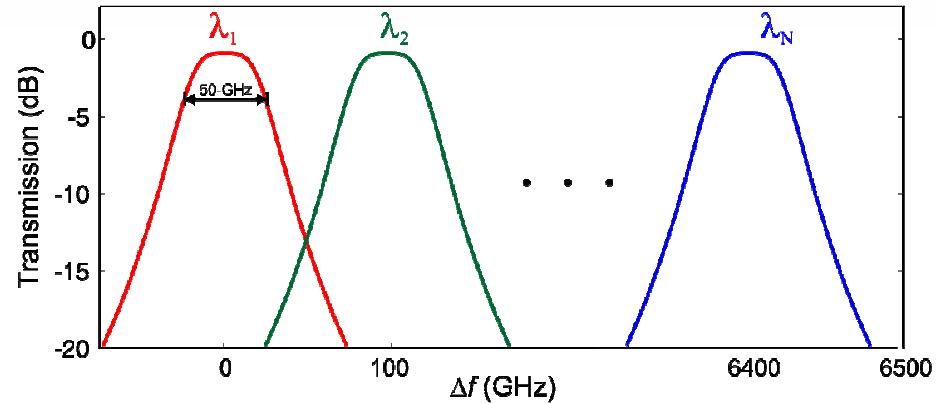
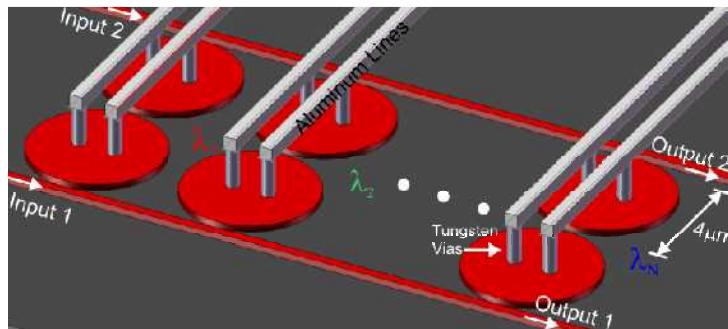
Important Considerations

- Smaller disk \Rightarrow Lower coupling loss? Why?
- Secondary mode can be cut-off, but requires very small disks

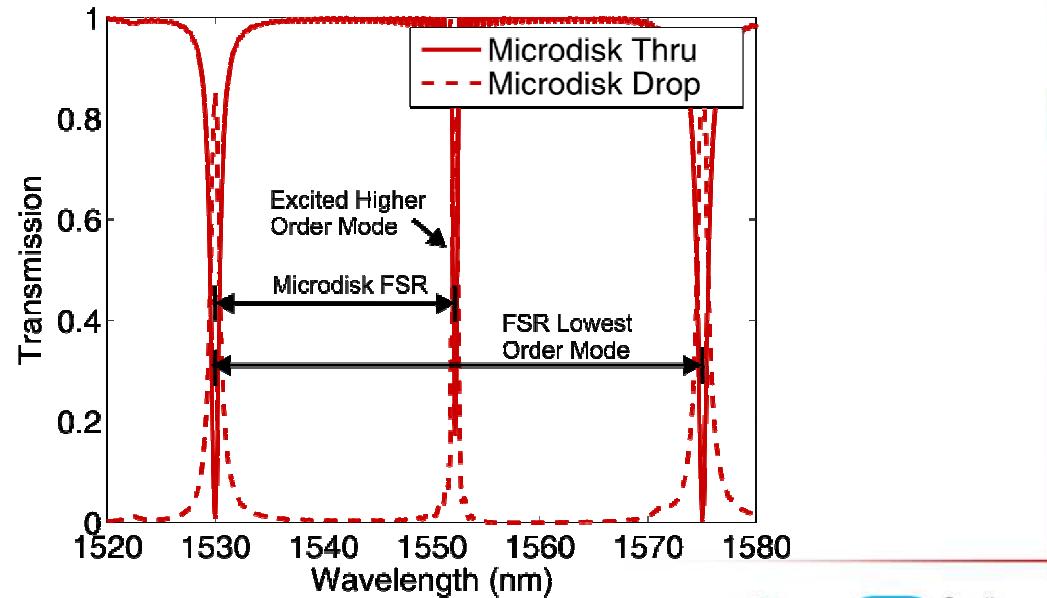
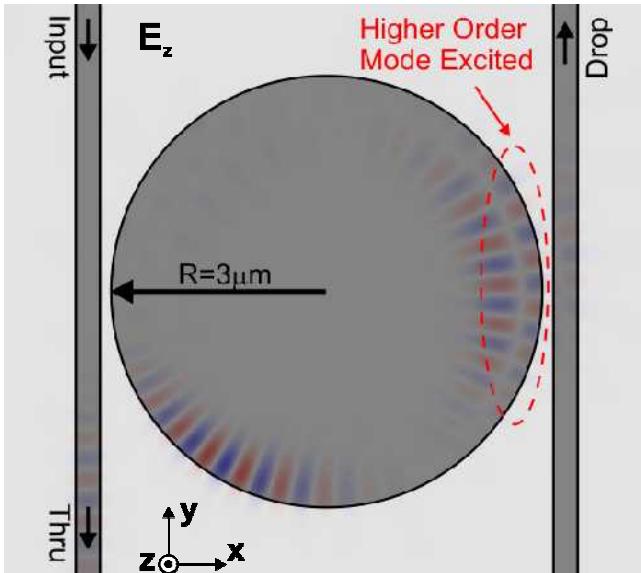


Problem 2: Limited Free-Spectral Range

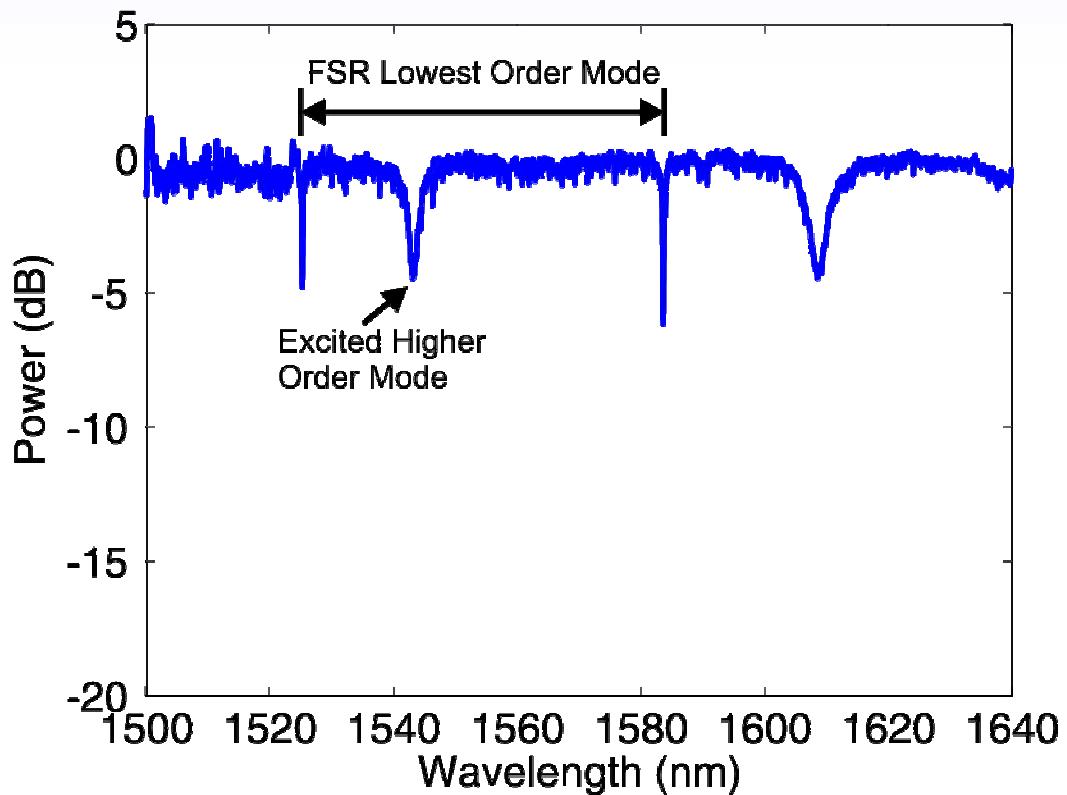
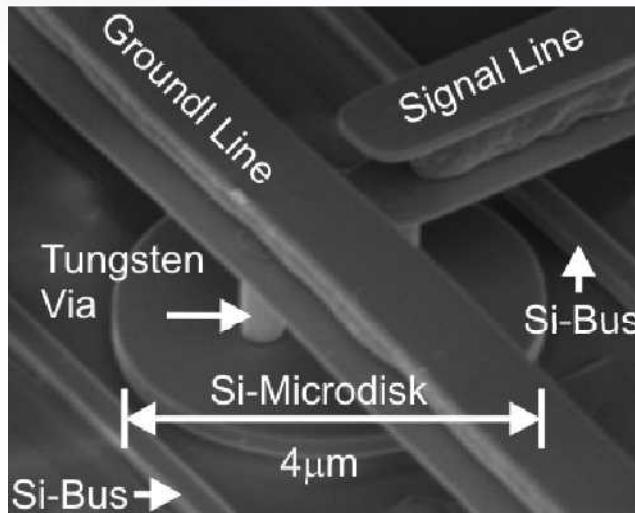
Goal: Large channel count, large bandwidth \rightarrow Large FSR



Problem: Microdisks propagate multiple spatial modes, corrupting FSR



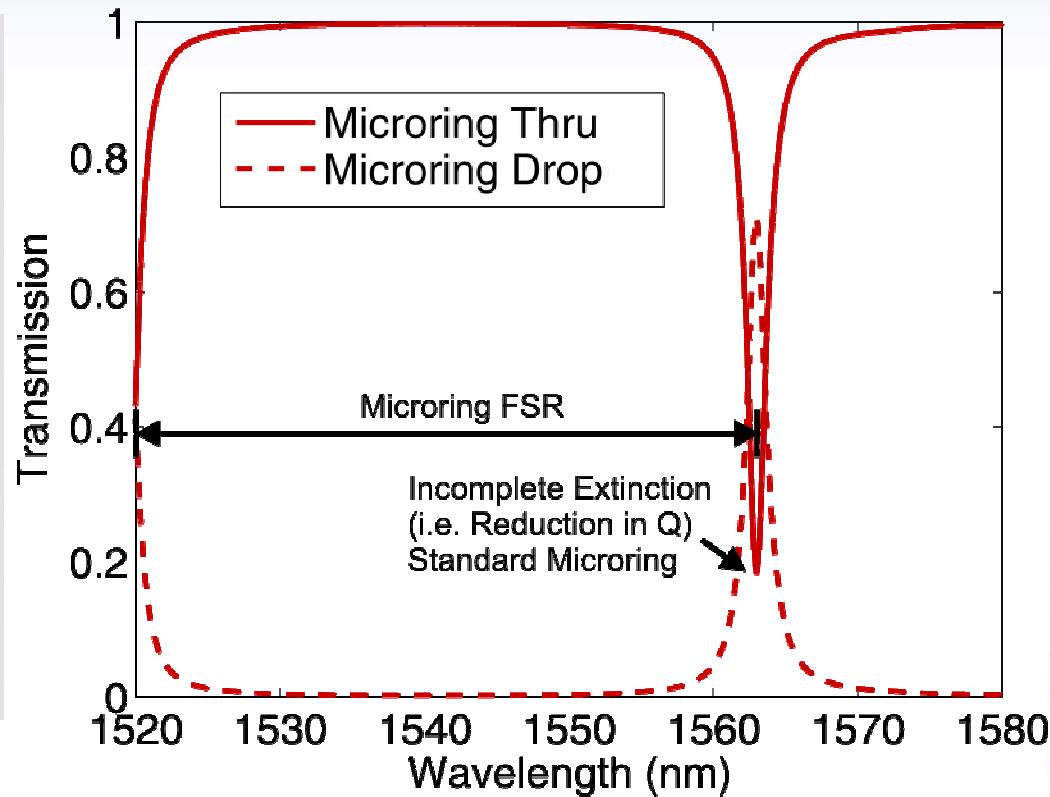
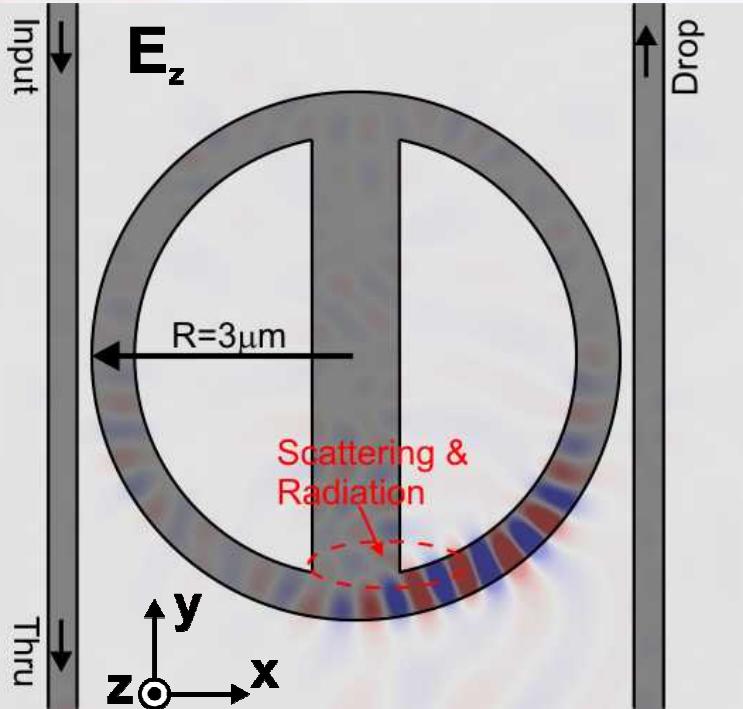
Experimentally Observed Microdisk FSR



Results

- As expected, microdisk propagates higher order modes corrupting FSR and limiting the available line bandwidth
- Can be fixed with a microring, but how do you make electrical contact?

What about Directly Contacting a Microring?



Results

- Microrings enable a recovery of the full Free Spectral Range
- However, the contact leads to scattering and a reduction in Q
- Can we modify the ring geometry to enable contact without loss?

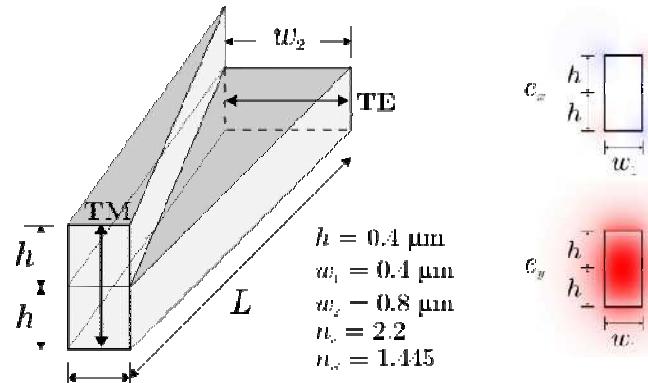
So Let's Consider Mode-Evolution

Thought: Mode-evolution is commonly used to transform modes

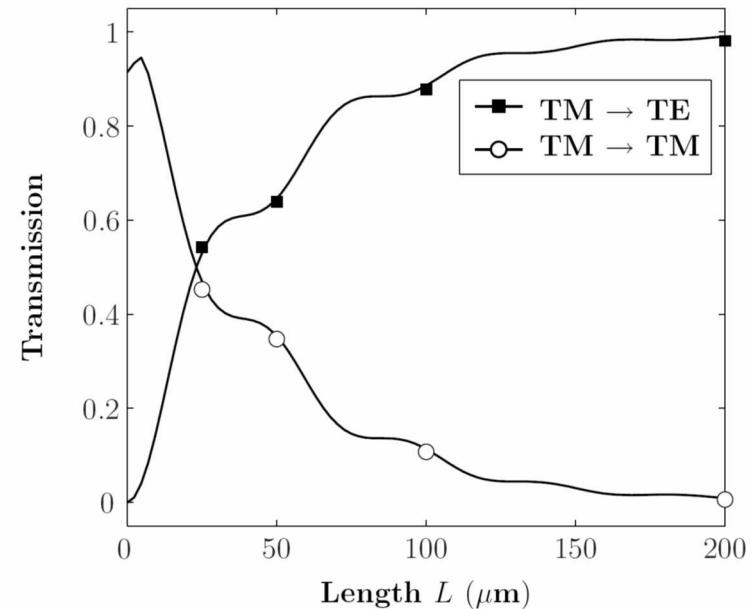
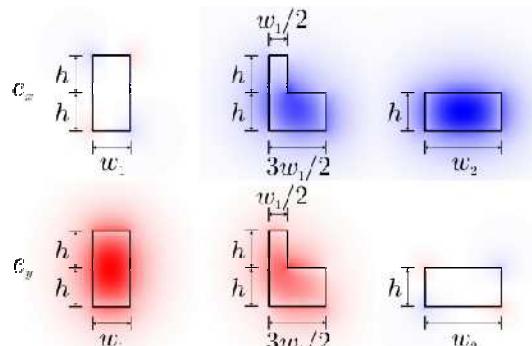
Principle: Slow perturbations ($\Delta\beta/\kappa \gg 1$) do not result in coupled power

$$P(L) \propto \left| \frac{\kappa}{\Delta\beta} \right|^2 [1 - \cos(\Delta\beta L)]$$

An Example: A Polarization Rotator



M. R. Watts and H. A. Haus, **30**, *Optics Letters*, 2005



So, what if we introduce an adiabatic taper into a microring to enable a contact without inducing radiation?

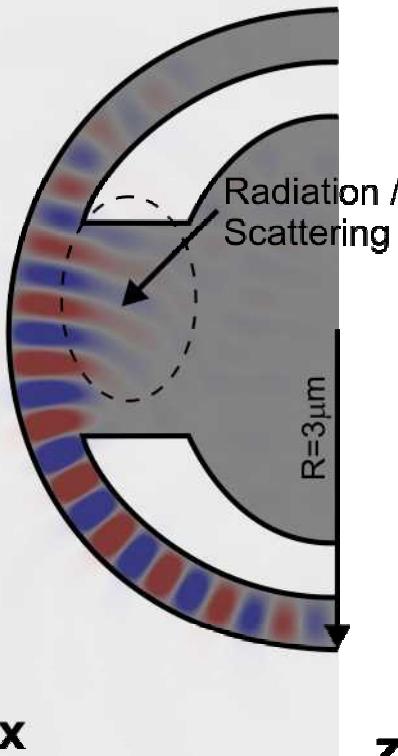


Simple Contact vs. Adiabatic Bend

Simple Contact

Transmission = 64%
Loss = 36%

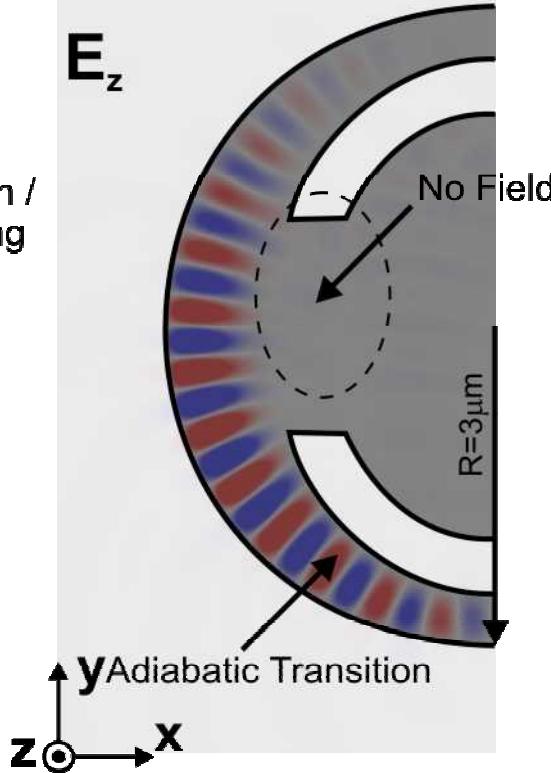
E_z



Adiabatic Bend

Transmission = 99.9%
Loss = 0.1%

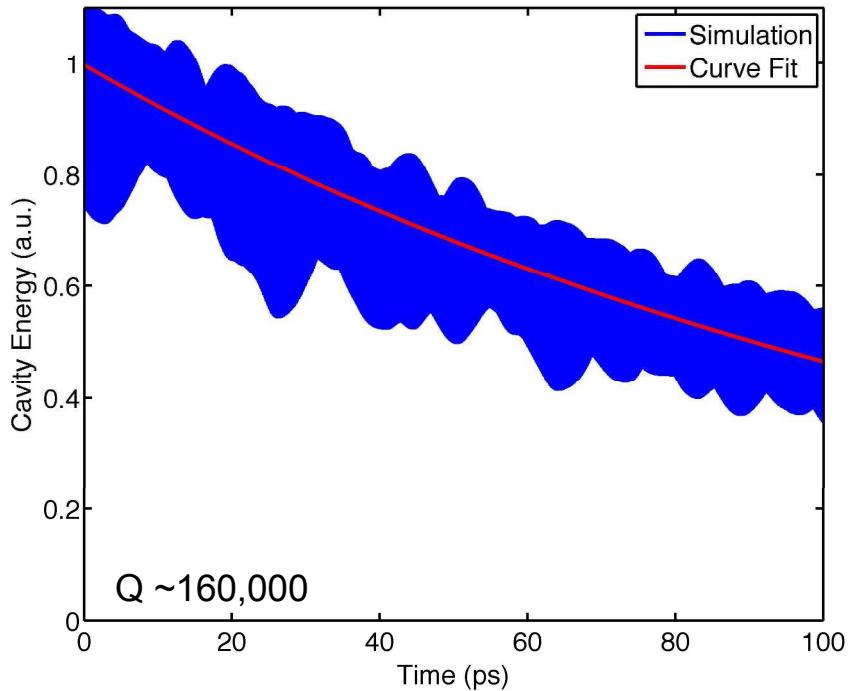
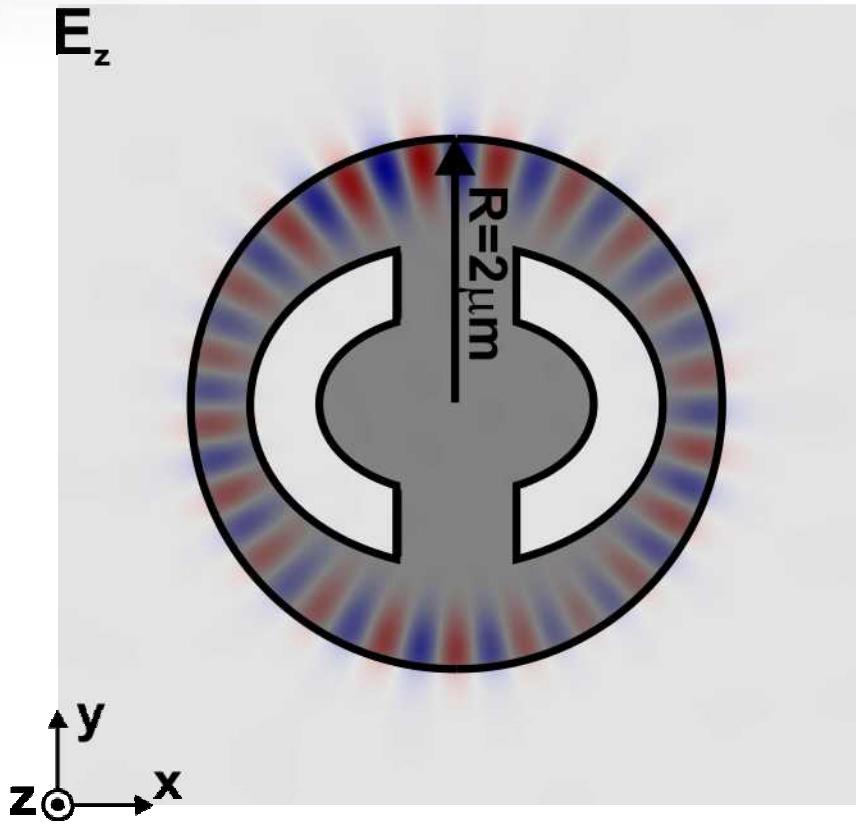
E_z



Results

- Adiabatic bend reduces losses from 36% to 0.1%
- Loss of 0.1% enables a Q exceeding 10^4
- Further optimization should enable lower losses
- Surprising how rapidly "adiabatic" transition is made (enabled by large difference in propagation rates between modes)

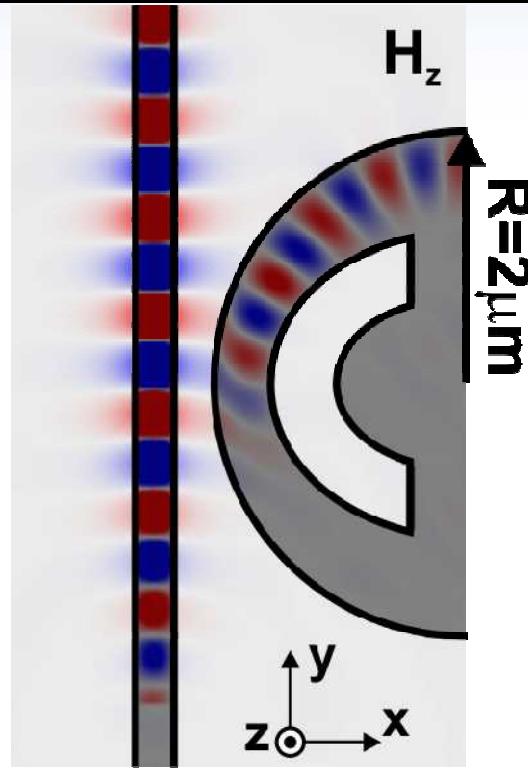
Adiabatic Microring-Resonator Q



Results

- Internal Q's exceeding 10^5 are possible in small adiabatic microrings
- Q's exceeding 10^6 are likely by iterating on designs

Coupling Losses: Essentially Eliminated



Coupling = 1.5%
Loss = 0.16%

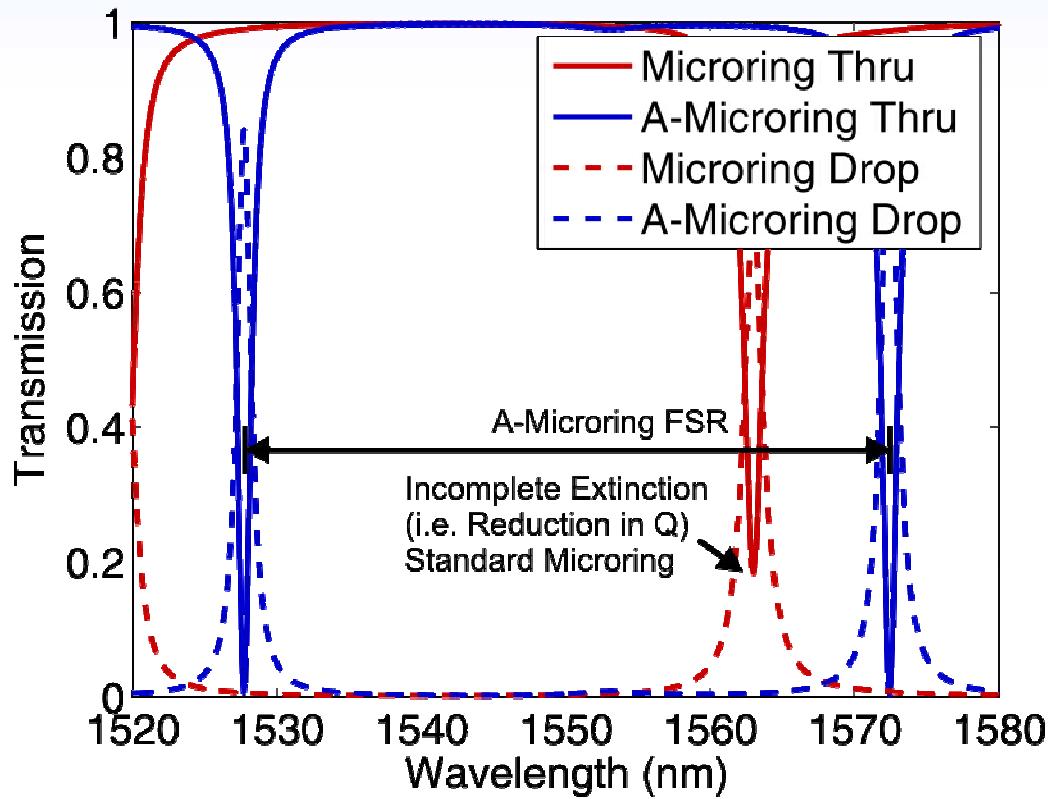
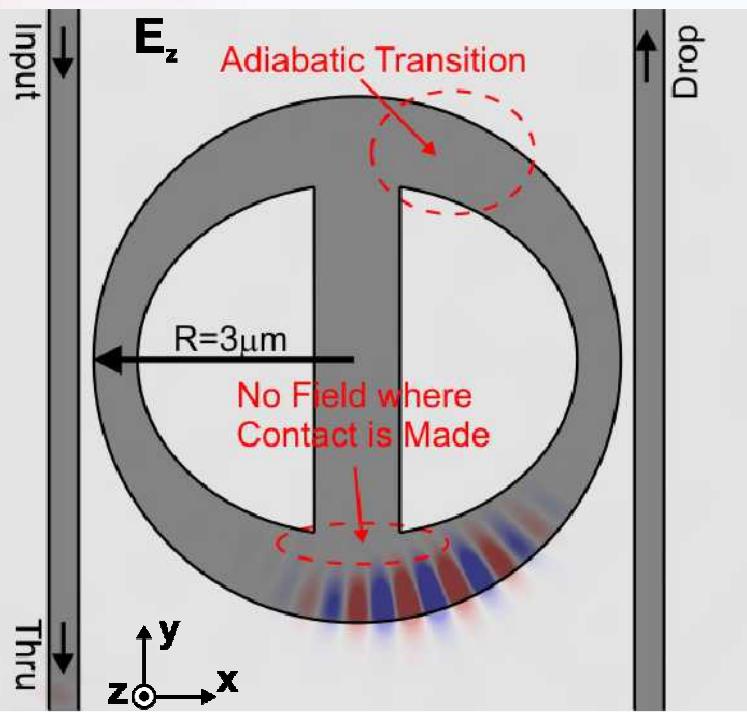
Approach / Results

- Higher order modes are eliminated in coupling region \rightarrow lossless coupling
- Narrower bus than ring waveguide used to mode-match / suppress coupling to lossy supermodes with the structure*,**

*M. R. Watts, PhD MIT Thesis (2005)

M.A. Popović et al., Opt. Lett., **31, pp. 2571-2573 (2006)

Free Spectral Range: Fully Recovered

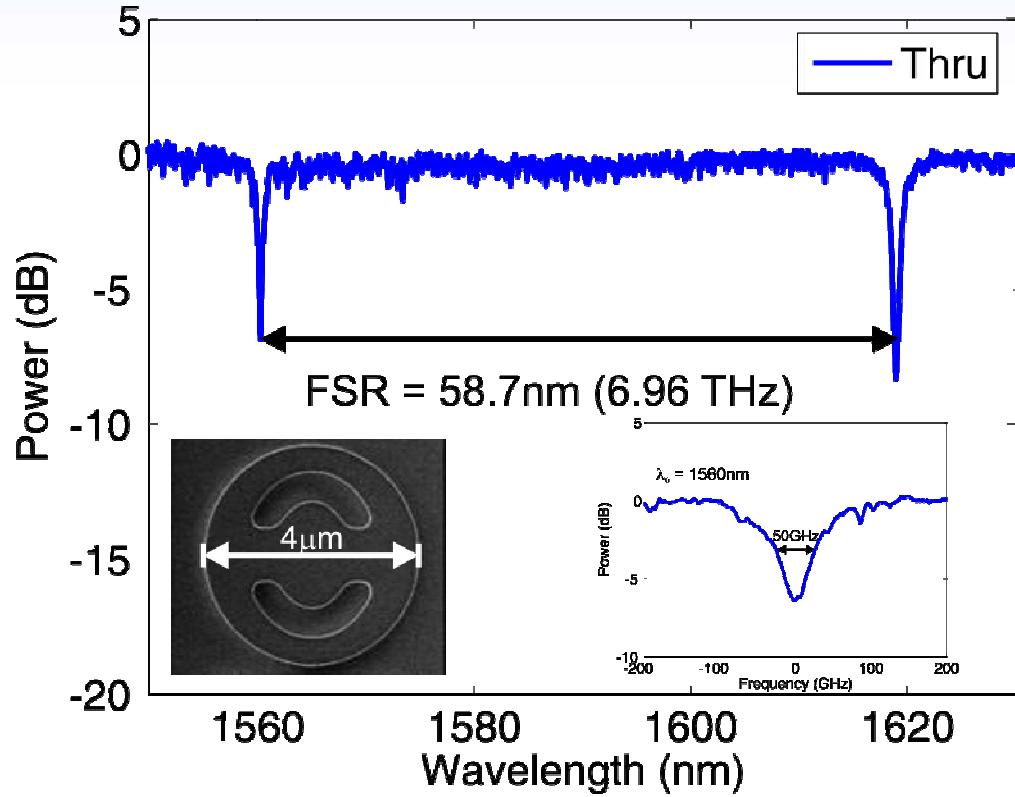
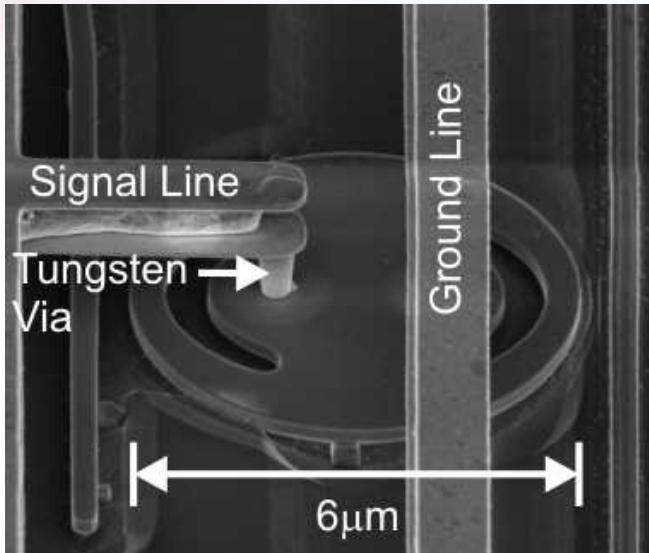


Results

- Adiabatic microrings enable a recovery of the full Free Spectral Range without inducing scattering and loss



Adiabatic Microring: Experimental Results



Results

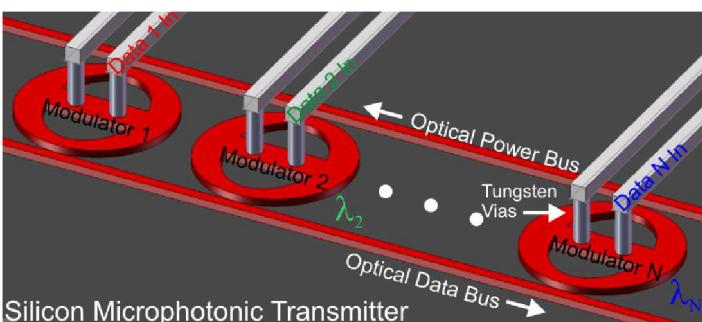
- Uncorrected 6.96THz Free-Spectral-Range
- Eliminated higher order modes without significant loss ($Q_{ext} \sim 4000$)
- Slight reduction in Q due to fabrication bias (i.e. loss of ~ 100 nm)
- Electrically active, 4 μm rings currently have insufficient Q, 6 μm rings have high-Q, testing now . . .

Summary and Future Outlook

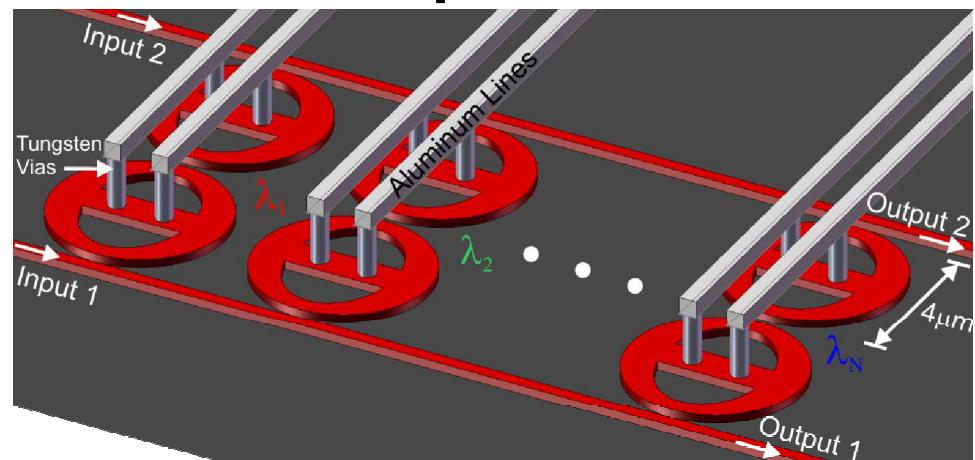
Modulators

- Demonstrated error-free, 10Gb/s NRZ data transmission (no pre-emphasis)
- Communications efficiency of 85fJ/bit (**100X less than electrical interchip**)
- Path to ~10fJ/bit with <2.5V drive is highly probable . . . enabling 1-Tb/s @10mW

1×N Silicon Modulators



1×N Bandpass Switches



Bandpass Switches

- First demonstrated electrically active high-speed (~2ns) silicon bandpass switch
- Can be driven with ~1V drive
- Did not require any post-fabrication trimming

Challenges Ahead

- Temperature control, fabrication tolerances, dense integration



Acknowledgements

FDTD Code: Christina Manolatou

Cylindrical Modesolver: Milos Popovic

Funding: Sandia LDRD and DARPA MTO (M. Haney and J. Shah)



Energy/Bit in a Capacitive Modulator

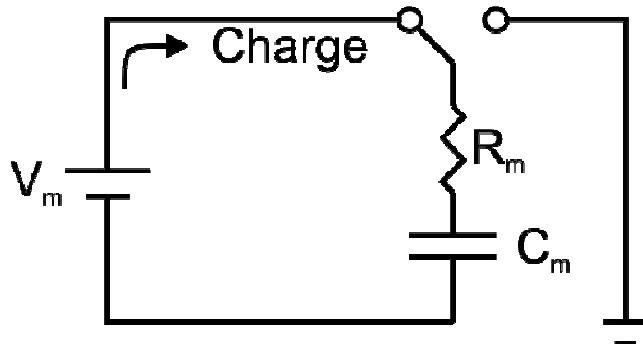
Definition: Energy / Bit = $\frac{1}{BR \cdot T} \int_0^T P(t) dt$, where BR = Bit Rate

Total Bits

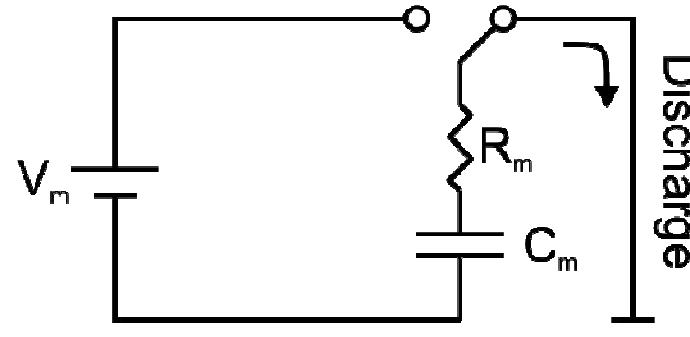
Energy

0-to-1 Transition

1-to-0 Transition



CV^2 Energy Supplied
($CV^2/2$ Dissipated, $CV^2/2$ Stored)



0 Energy Supplied
($CV^2/2$ Dissipated)

- Switching Energy:** $E_s = CV^2$ ($CV^2/2$ dissipated, $CV^2/2$ stored)
- Clocking Energy/"Bit":** $CV^2/2$ (because 0-1-0-1-0-1, etc.)
- $$E(\text{energy/bit}|0) = P(0-1|0\text{-state}) * \text{energy}_{\text{diss}}(0-1) + P(0-0|0\text{-state}) * \text{energy}_{\text{diss}}(0-0)$$
$$= 0.5 * CV^2/2 + 0.5 * 0 = CV^2/4$$
- $$E(\text{energy/bit}|1) = P(1-0|1\text{-state}) * \text{energy}_{\text{diss}}(1-0) + P(1-1|1\text{-state}) * \text{energy}_{\text{diss}}(1-1)$$
$$= 0.5 * CV^2/2 + 0.5 * 0 = CV^2/4$$
- PRBS E(energy/bit)** = $P(0) * E(\text{energy/bit}|0) + P(1) * E(\text{energy/bit}|1) = CV^2/4$

