SAND2009-1612C

Low Disorder Si MOSFET Dots for Quantum Computation

APS March Meeting 2009

Eric Nordberg, Lisa Tracy, Greg Ten Eyck, Kevin Eng, Harold Stalford, Kent Childs, Jeff Stevens, Robert Grubbs, Mike Lilly, Mark Eriksson, Malcolm Carroll

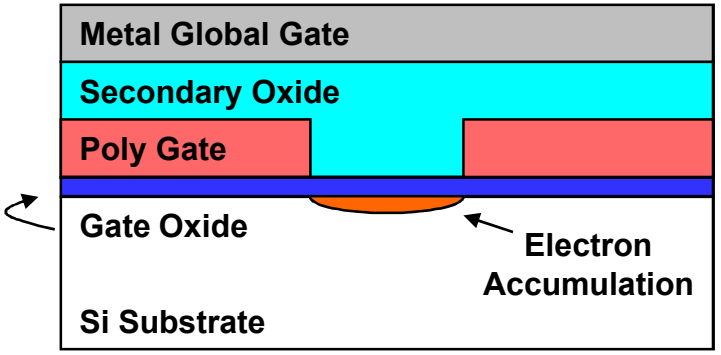
- Goal:
  - Coupled Few-Electron Quantum Dots in a Silicon/Silicon Dioxide Inversion Layer

- This Talk:
  - Process Characterization
  - Disorder Observation and Mitigation
  - Nanostructure Characterization

Quantum Dot Spin Qubits in Si

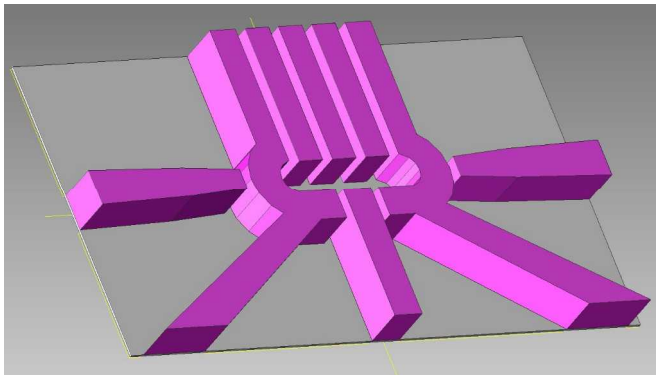
Advantages Si Material:

- Low spin-orbit coupling
- High percentage Si^{28} reduces nuclear spin coupling



Advantages of the MOS System:

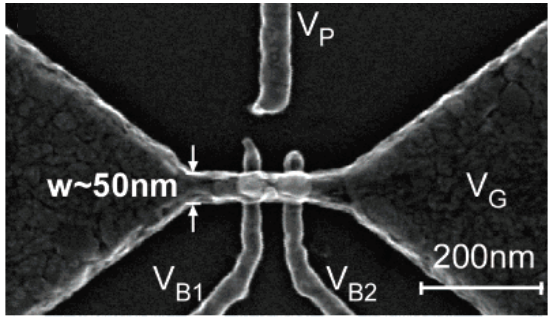
- Tunable Densities
- Scaling advantage due to gate proximity to electrons
- No δ-dopants required for transport
- Readily CMOS compatible



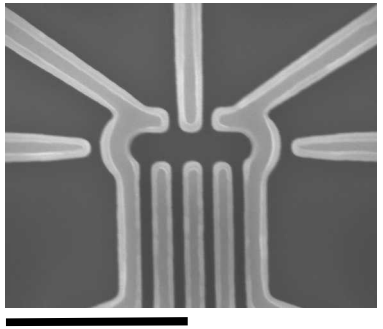
Coulomb Blockade in MOS Structures

	Mobility	Feature Size	Dot Size	Result
Angus et al.	**~5000 $cm^2/V\ s$**	**~30nm**	**~50nm**	**Stable Coulomb blockade**
H. W. Liu et. al.	**-**	**~50nm**	**12nm**	**Coulomb blockade, Pauli blockade**
De Graaf et al.	**5000 $cm^2/V\ s$**	**~200nm**	**<150nm**	**Disorder Dot**

- Smaller dot reports appear less affected by disorder
- Recent results are stable & show single electron characteristics (Pauli blockade)
- Target: Repeat successes of GaAs structures



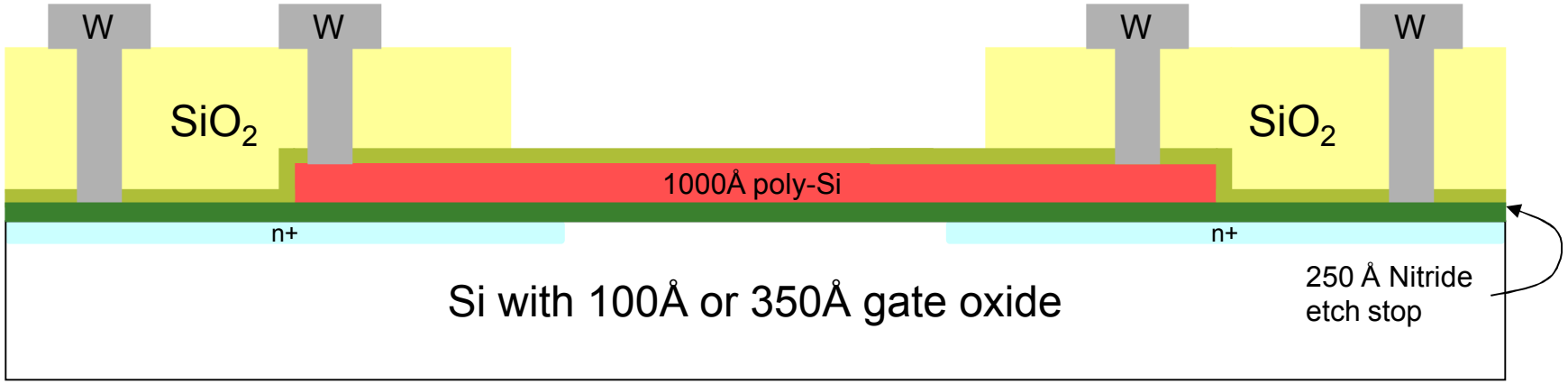
*Angus, et al. Nanoletters **7**, 2051 (2007)*

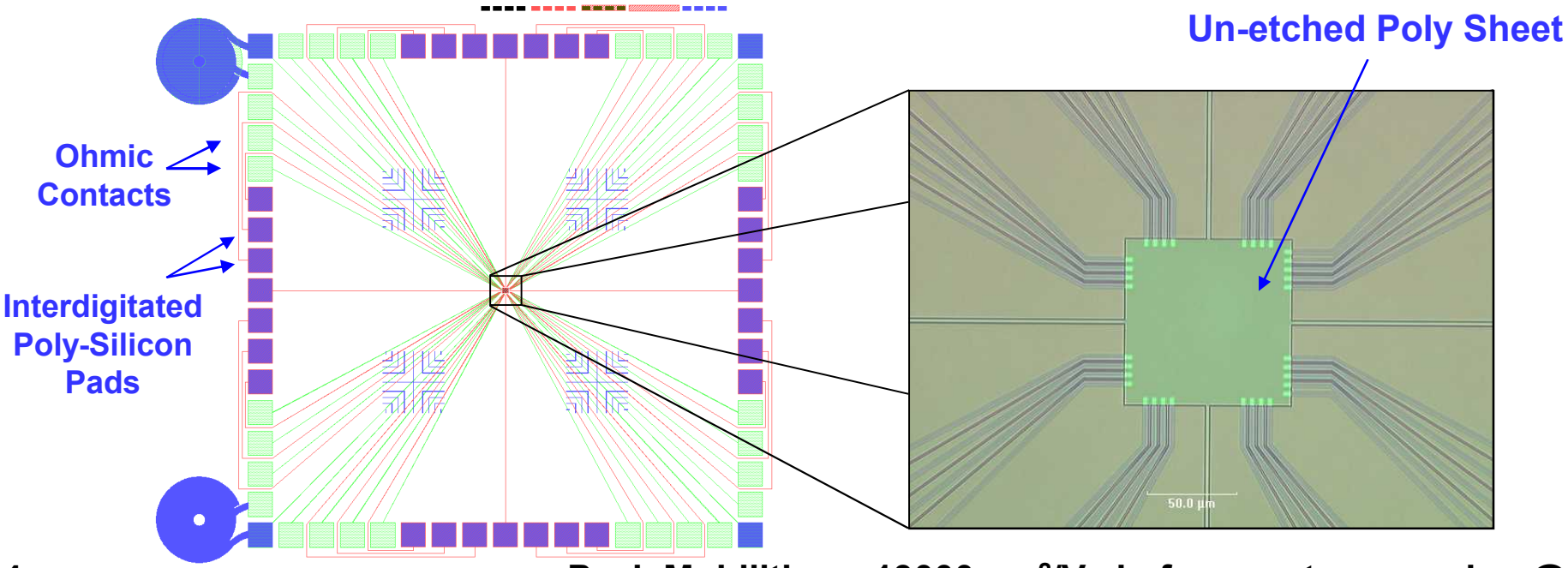


*H.W. Liu et al. PRB **77**, 073310 (2008)*

*C. De Graaf, et al. PRB **44**, 9072 (1991)*

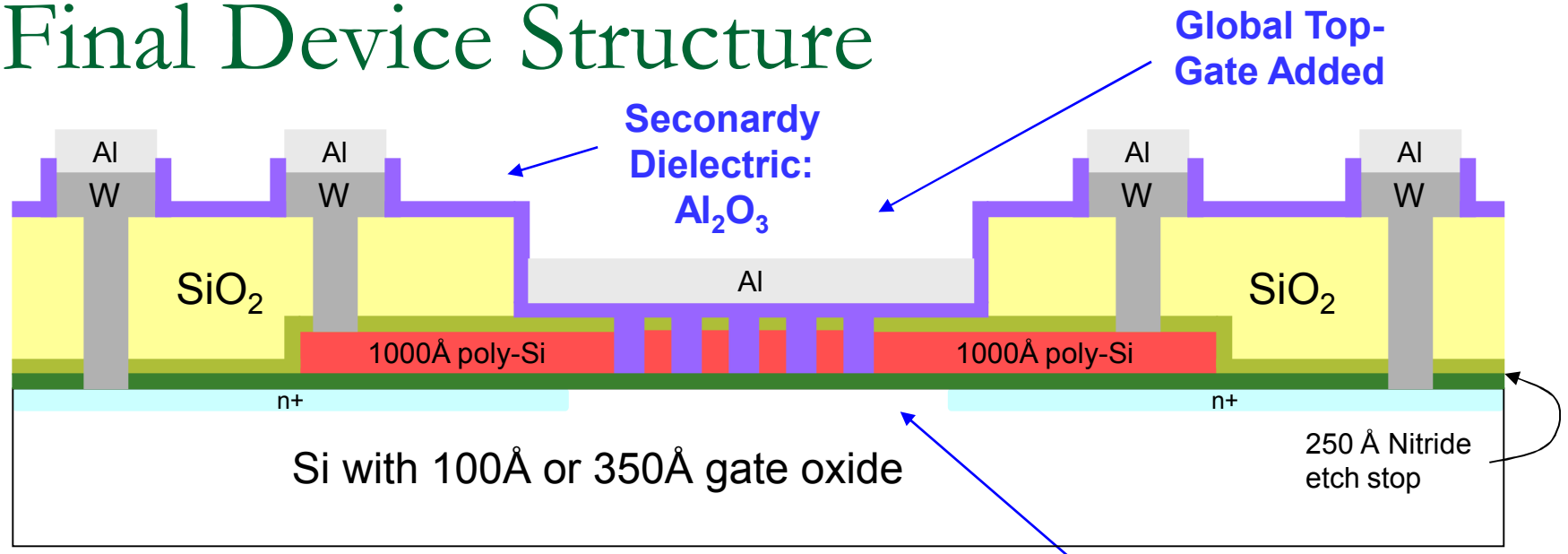
Initial Device Structure



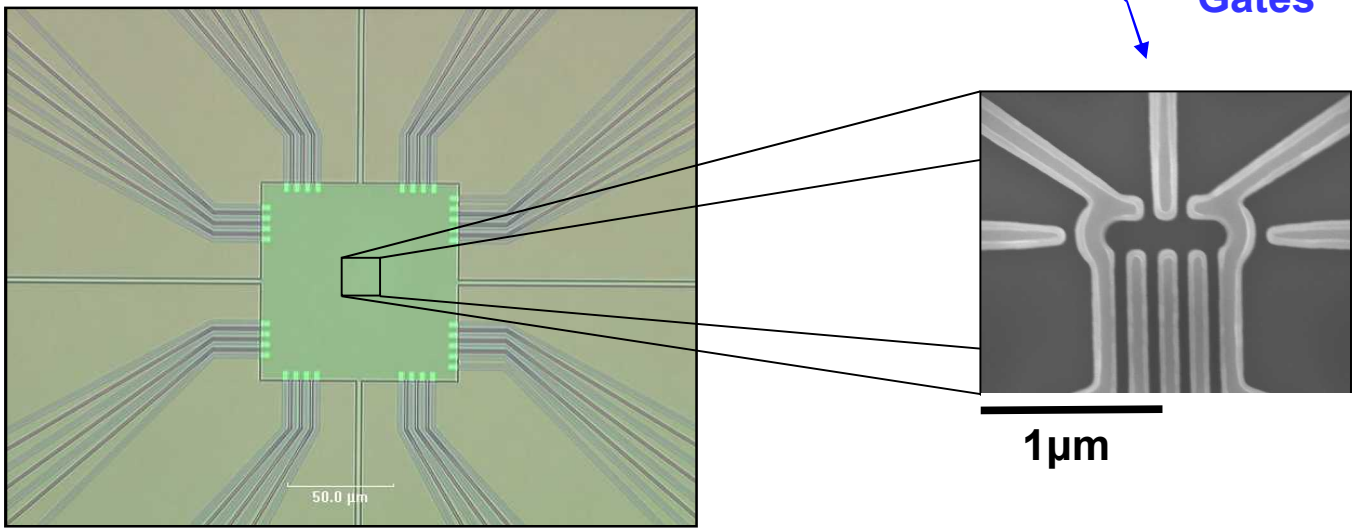


Peak Mobilities ~ 13000 cm^2/Vs before post processing @4K

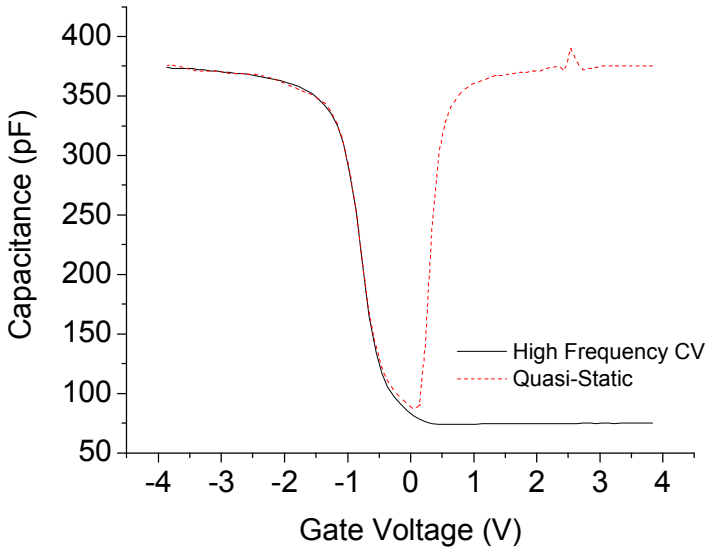
Final Device Structure

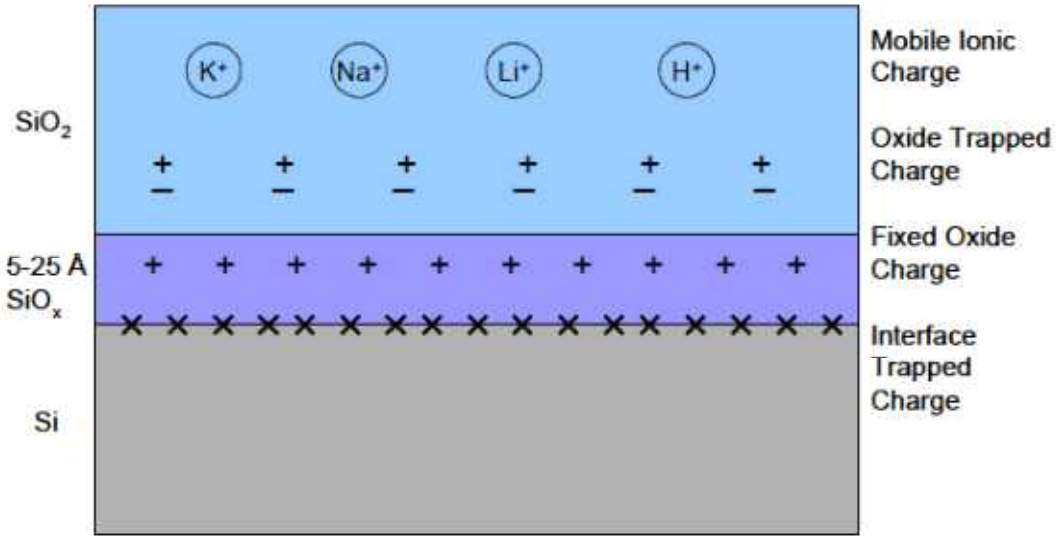


Etched poly-Gates



CV Measurements





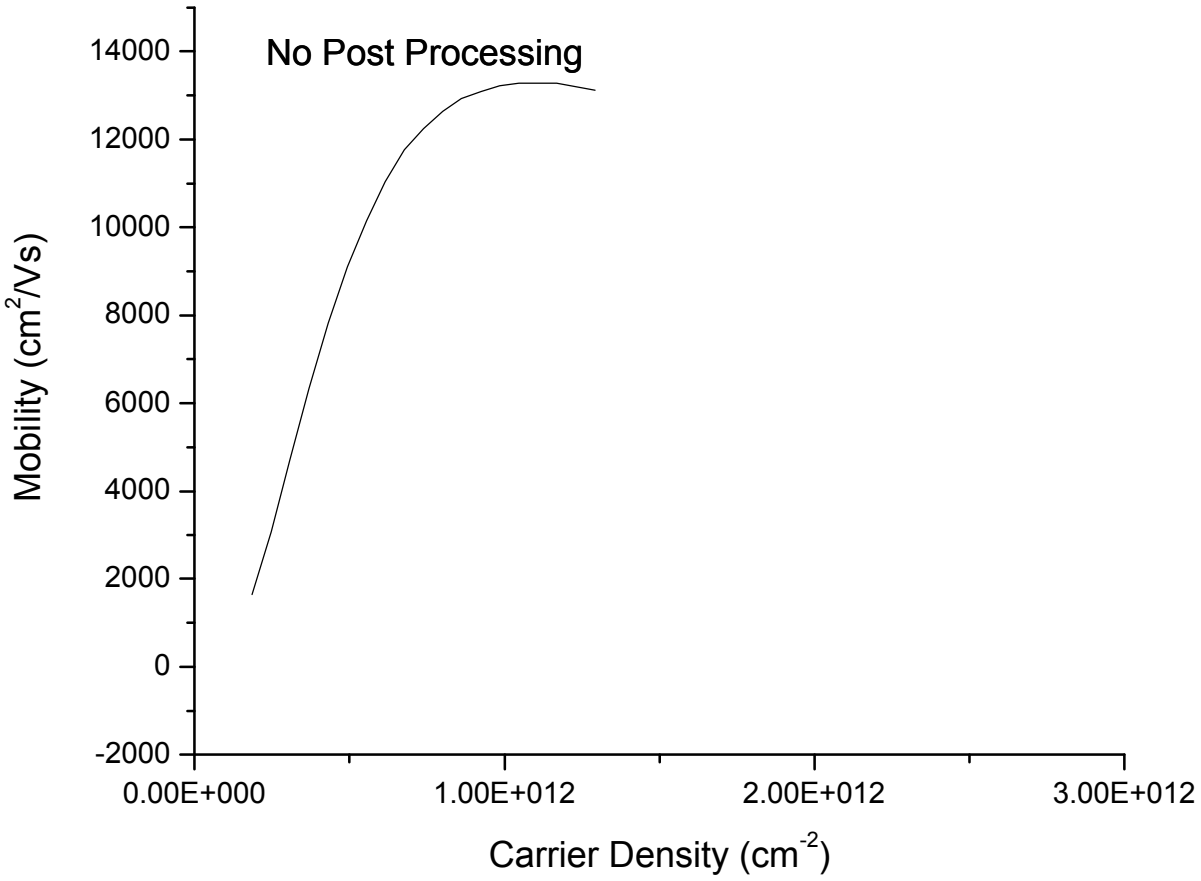
Values for 35nm Gate Oxide, and electron beam evaporation:

D_{it}=2.39E+10 $cm^{-2}eV^{-1}$

Q_{calc}=6.58E+10 cm^{-2}

Process Step	Effect on D_{IT}	Effect on Q_{calc}
Poly silicon Etch	No Effect	Increases negative charge to -4E+11
30nm of ALD Al_2O_3	Lower by 25-50%	Increases negative charge to ~ -1E+11
Thermal Evaporation	Lower by 25-50%	No Effect

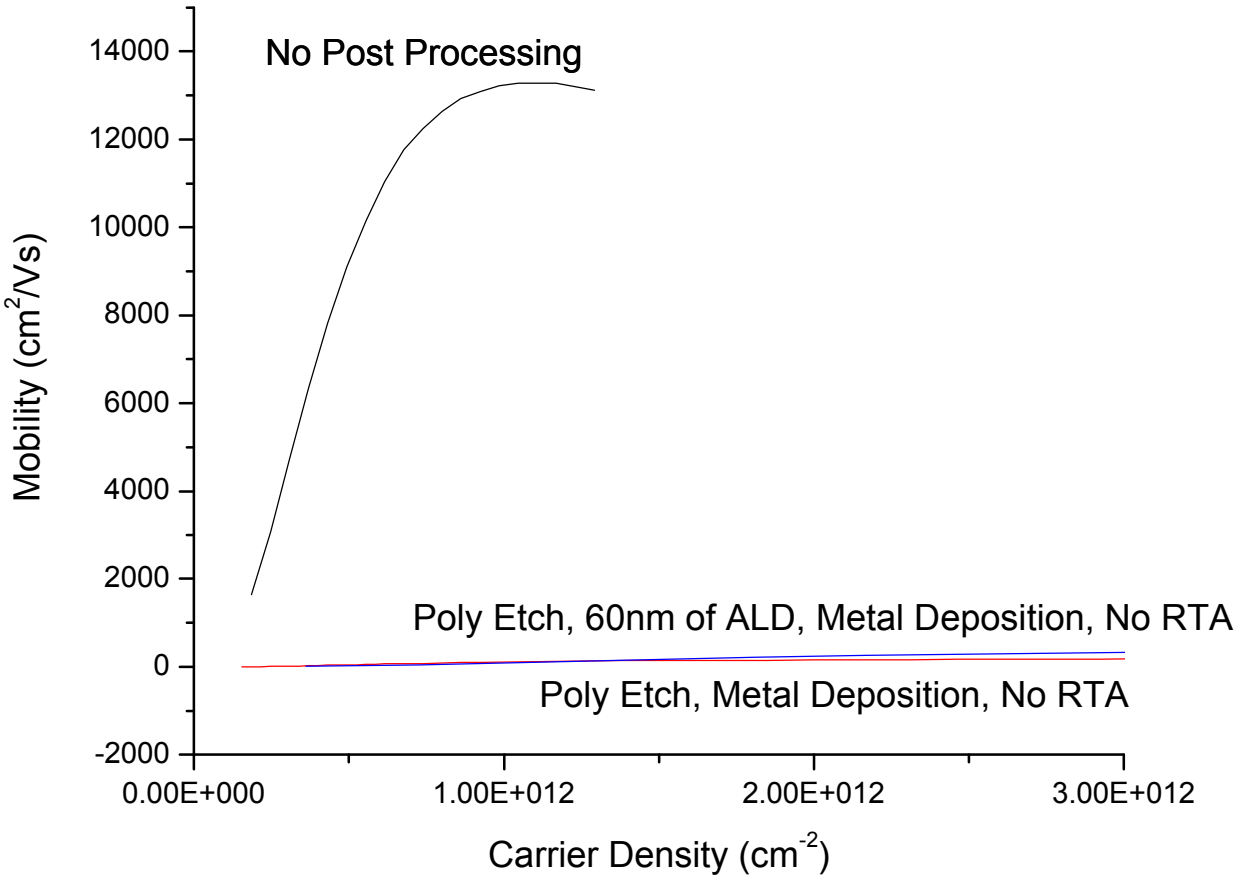
Sources of Disorder Inducing Process Damage



Process Steps Examined:

- Electron Beam Lithography
- Poly Silicon Plasma Etch
- Dielectric Atomic Layer Deposition (ALD)
- Metal Evaporation
- Forming Gas Rapid Thermal Anneal

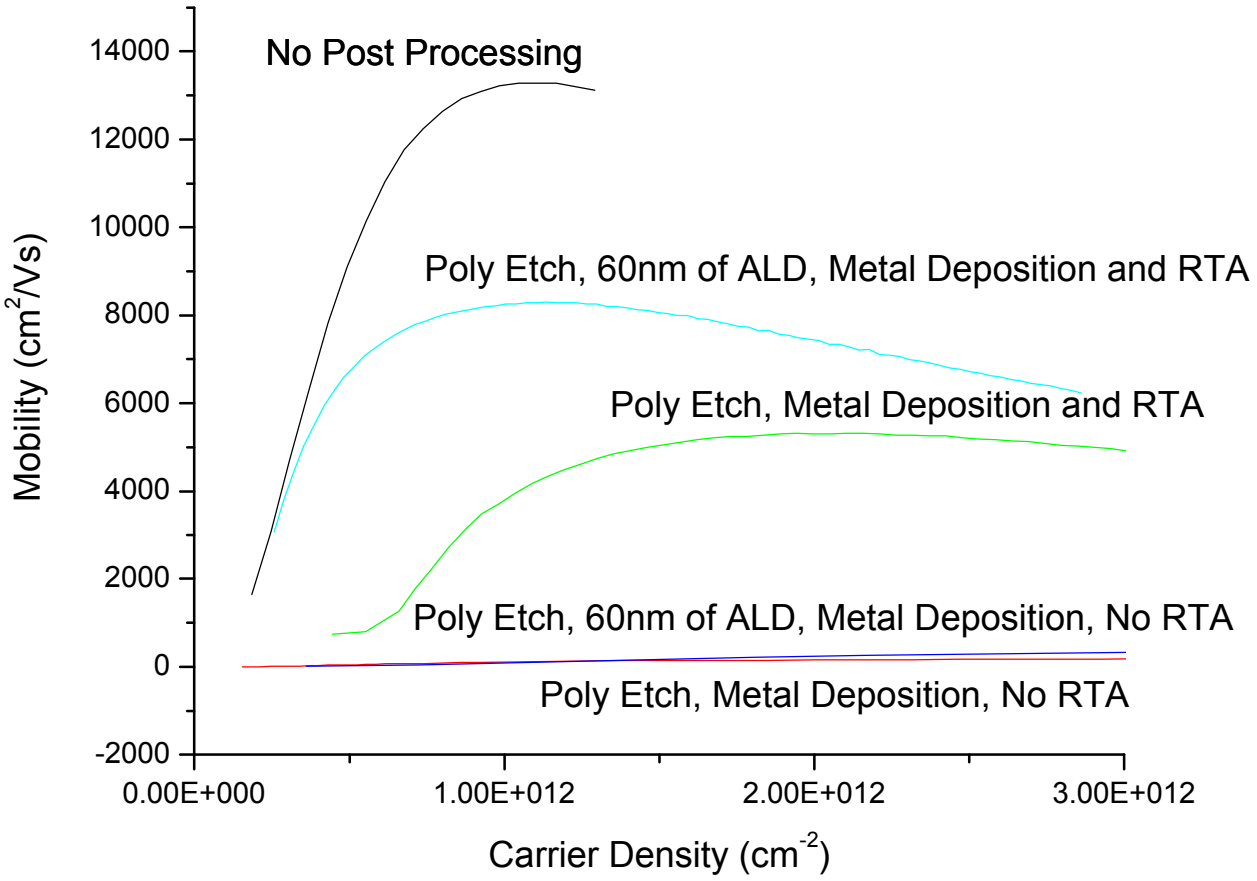
Sources of Disorder Inducing Process Damage



Process Steps Examined:

- Electron Beam Lithography
- Poly Silicon Plasma Etch
- Dielectric Atomic Layer Deposition (ALD)
- Metal Evaporation
- Forming Gas Rapid Thermal Anneal

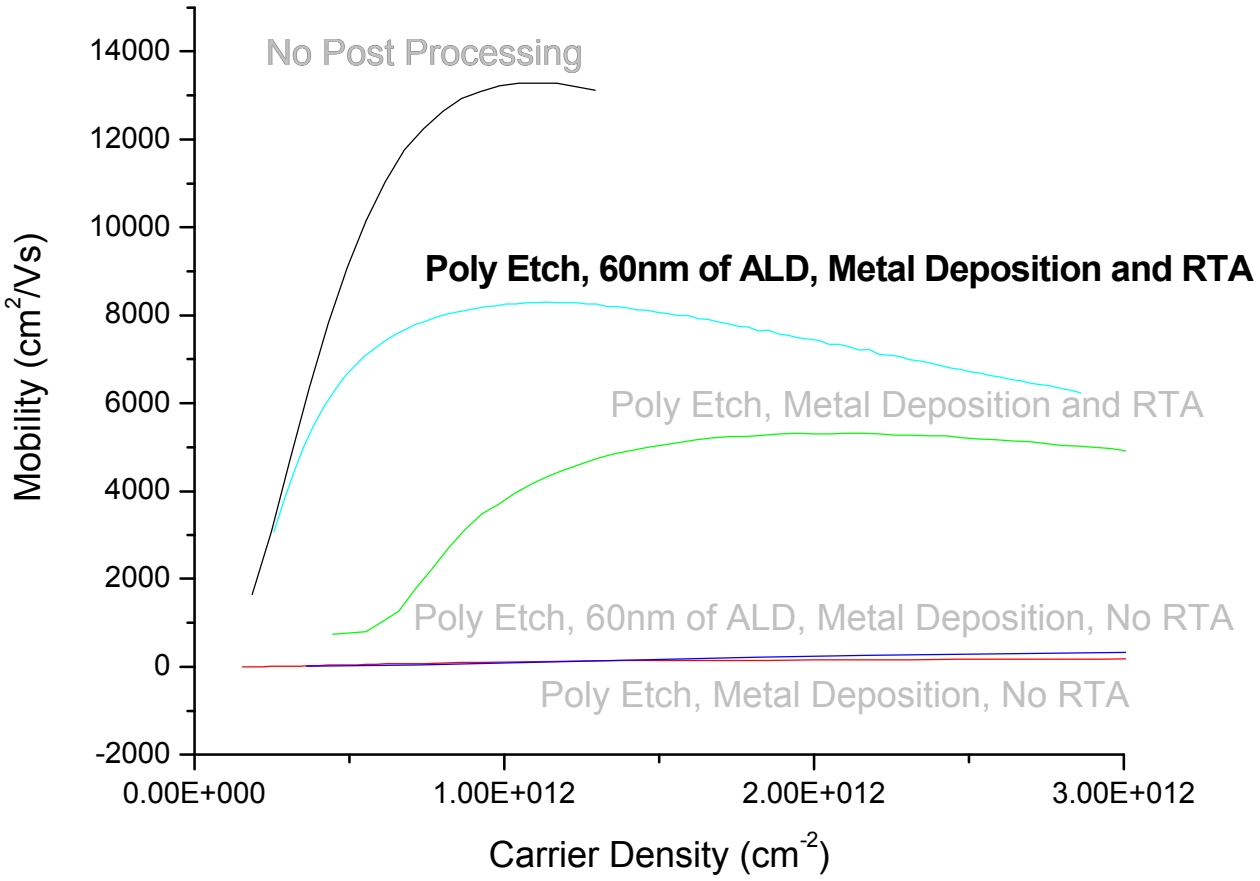
Sources of Disorder Inducing Process Damage



Process Steps Examined:

- Electron Beam Lithography
- Poly Silicon Plasma Etch
- Dielectric Atomic Layer Deposition (ALD)
- Metal Evaporation
- Forming Gas Rapid Thermal Anneal

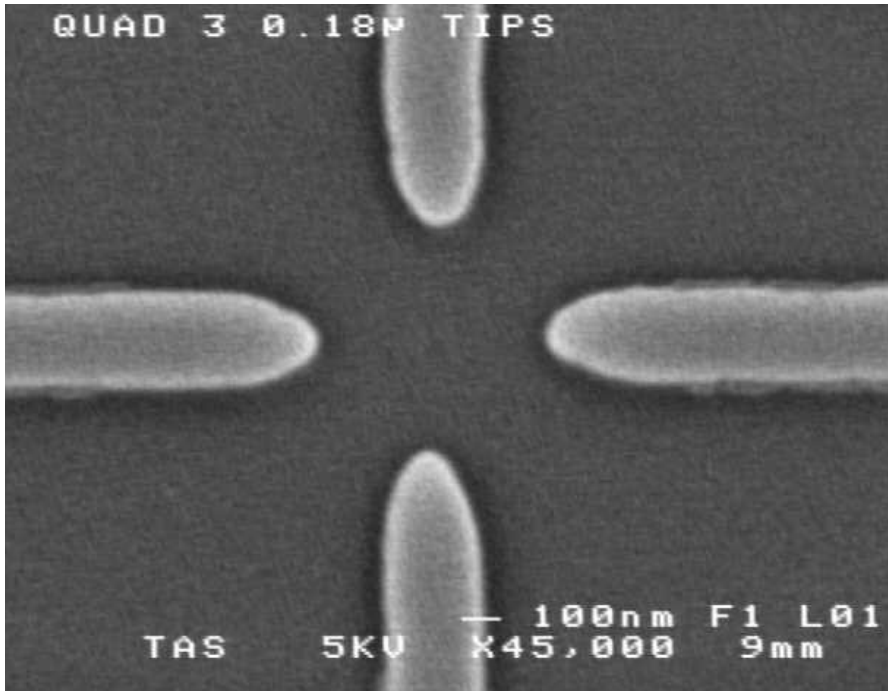
Sources of Disorder Inducing Process Damage

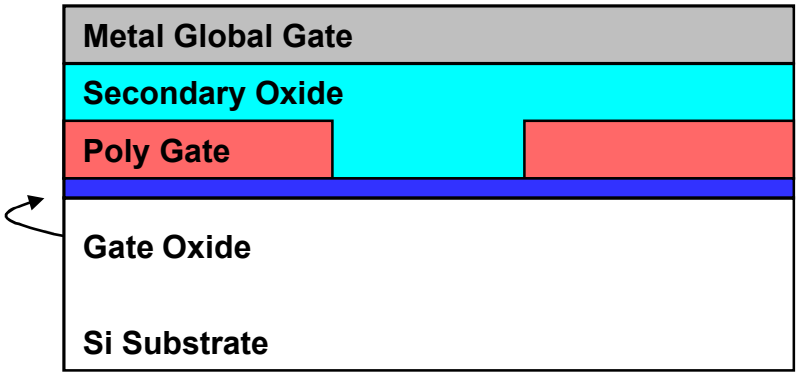


Process Steps Examined:

- Electron Beam Lithography
- Poly Silicon Plasma Etch
- Dielectric Atomic Layer Deposition (ALD)
- Metal Evaporation
- Forming Gas Rapid Thermal Anneal

Device Operation

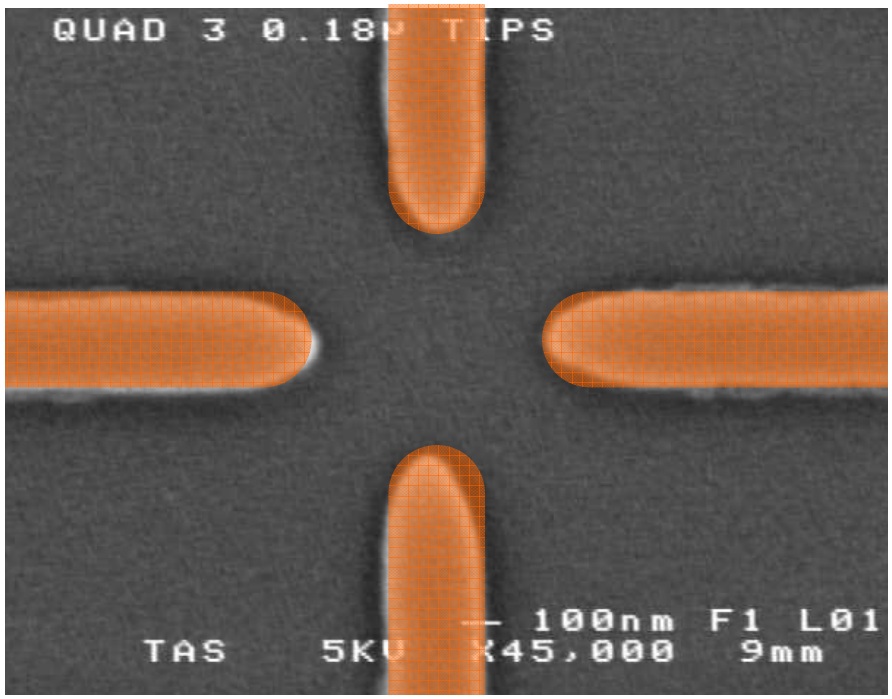




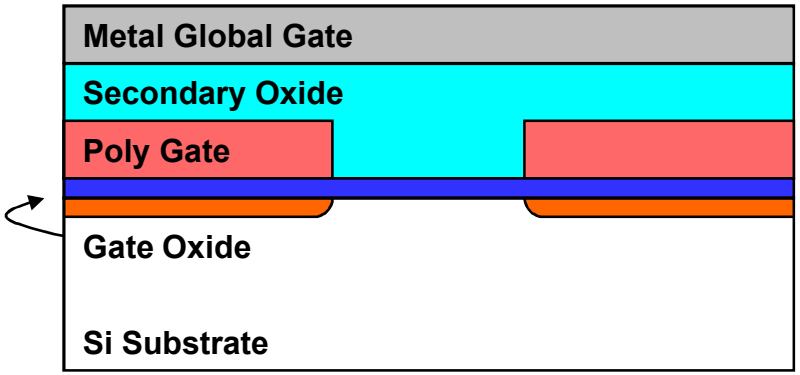
Polysilicon gates can be used for either accumulation or depletion in addition to the global accumulation gate

*G.M. Jones et al. PRL **89**, 073106 (2006)*

Device Operation

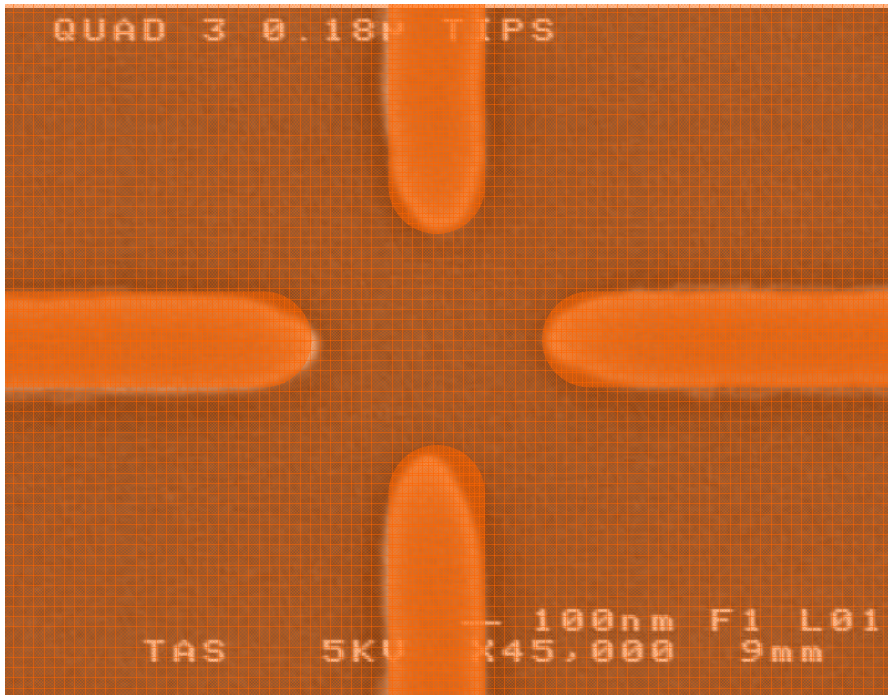


Polysilicon gates accumulating

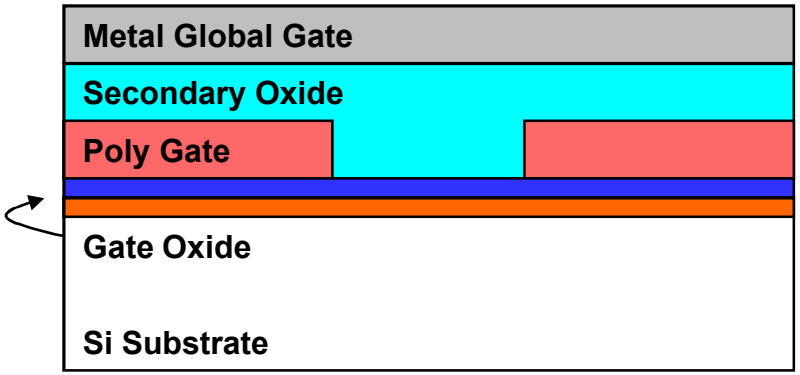


Polysilicon gates can be used for either accumulation or depletion in addition to the global accumulation gate

Device Operation

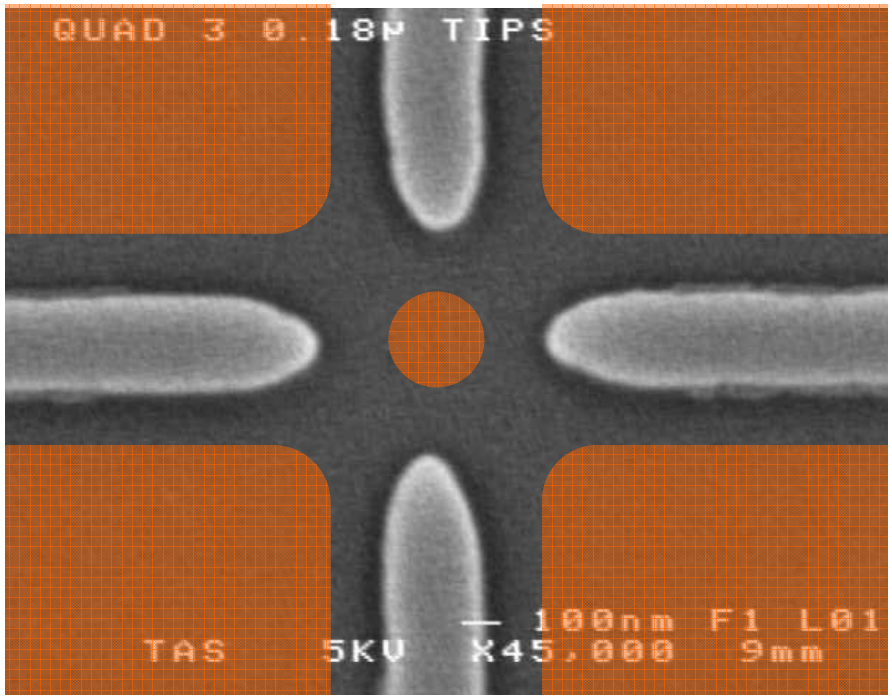


Both global top gate, and polysilicon gates accumulating

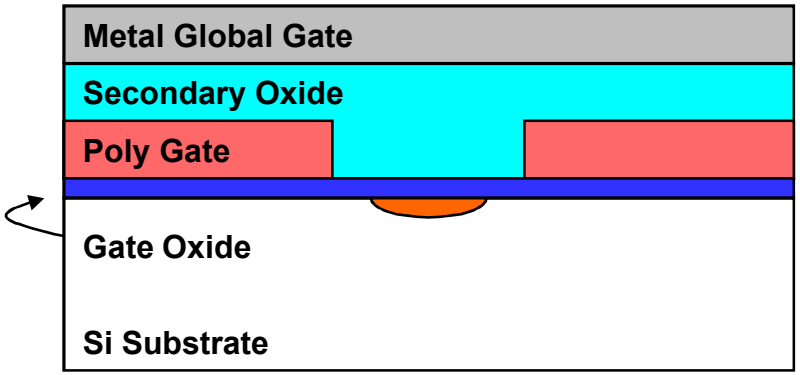


Polysilicon gates can be used for either accumulation or depletion in addition to the global accumulation gate

Device Operation



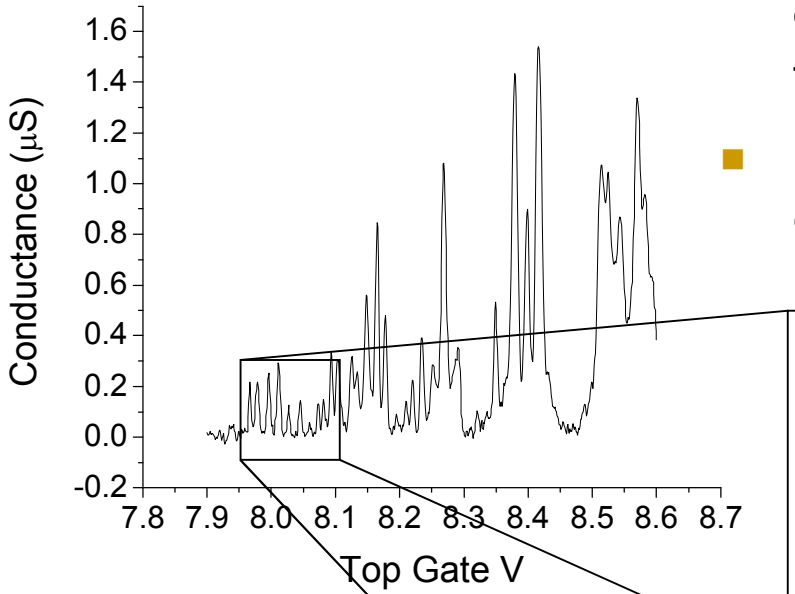
Global top gate accumulating, polysilicon gates depleting to form a quantum dot.

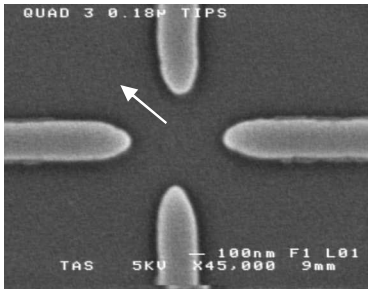


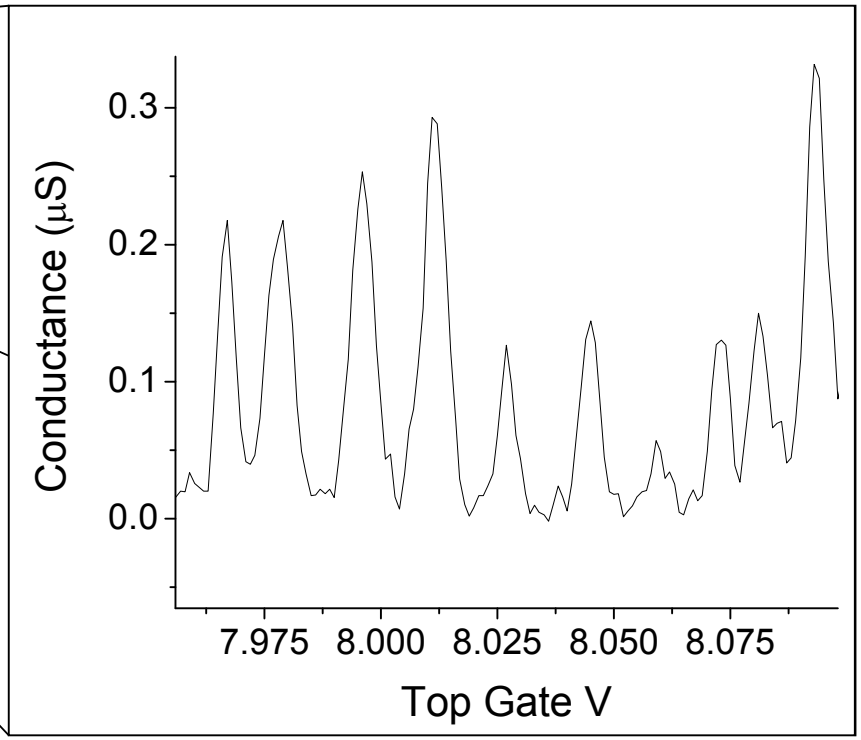
Polysilicon gates can be used for either accumulation or depletion in addition to the global accumulation gate

Disorder Dot

- Peak spacing corresponds to a dot diameter of ~65nm, fitting well within the lithographic constriction
- Longer period oscillations would correspond to a 25nm diameter

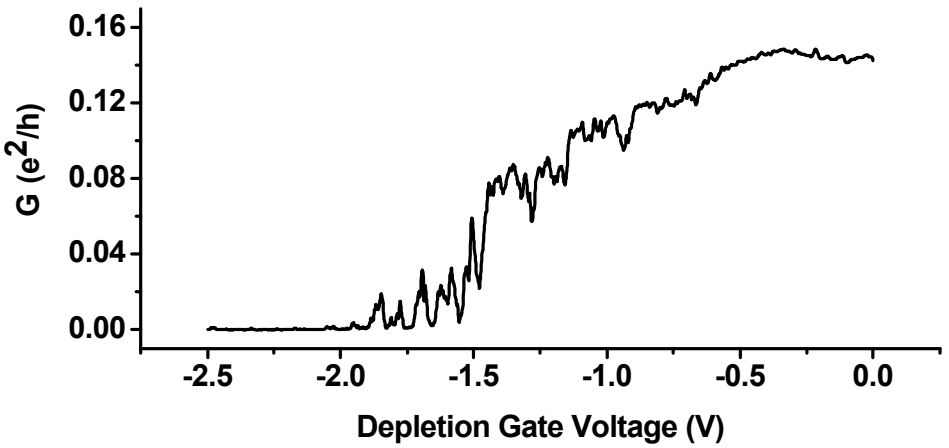


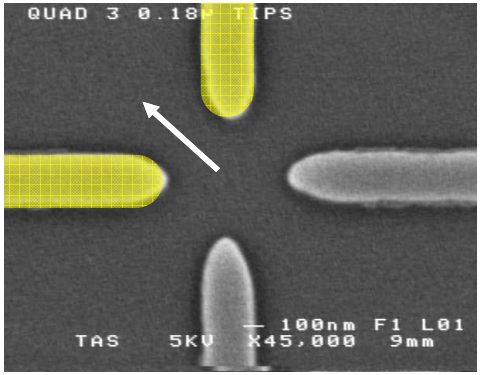




Process Induced Disorder

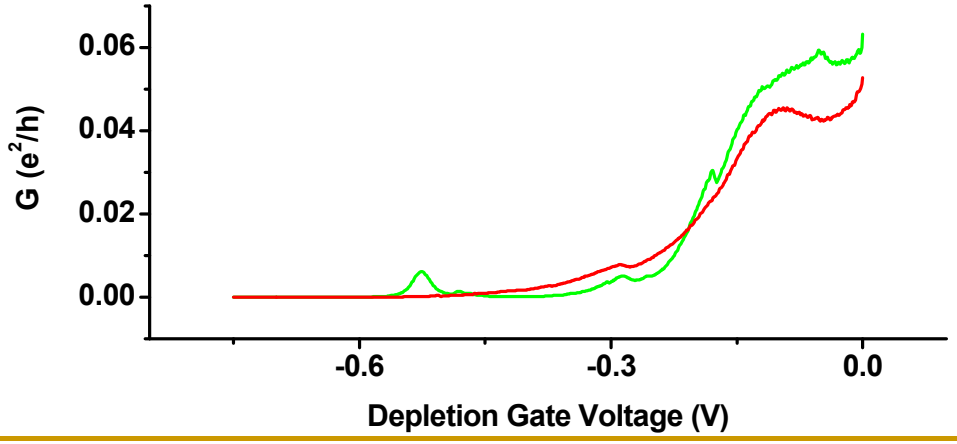
Disorder Dominated Conduction

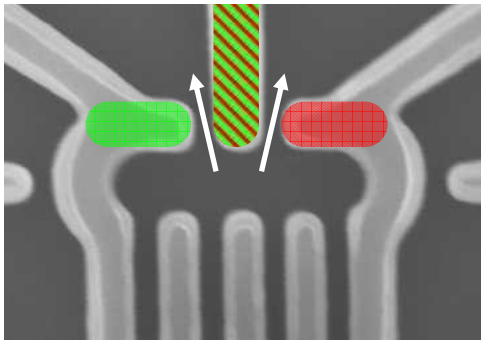




Top Gate Voltage: 8V

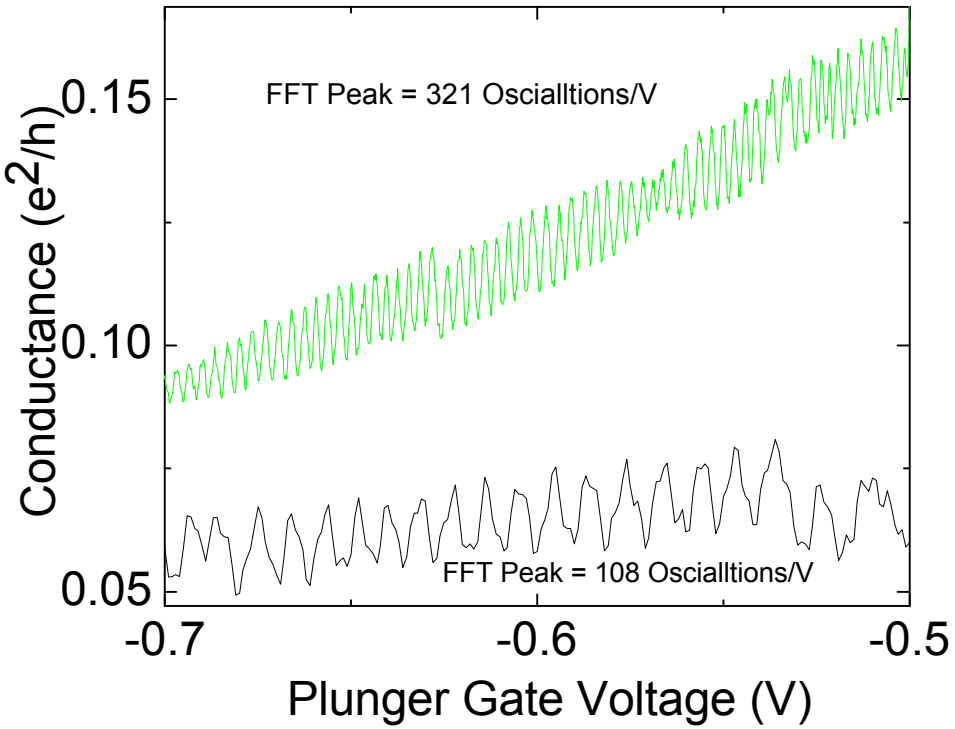
Constriction Dominated Conduction

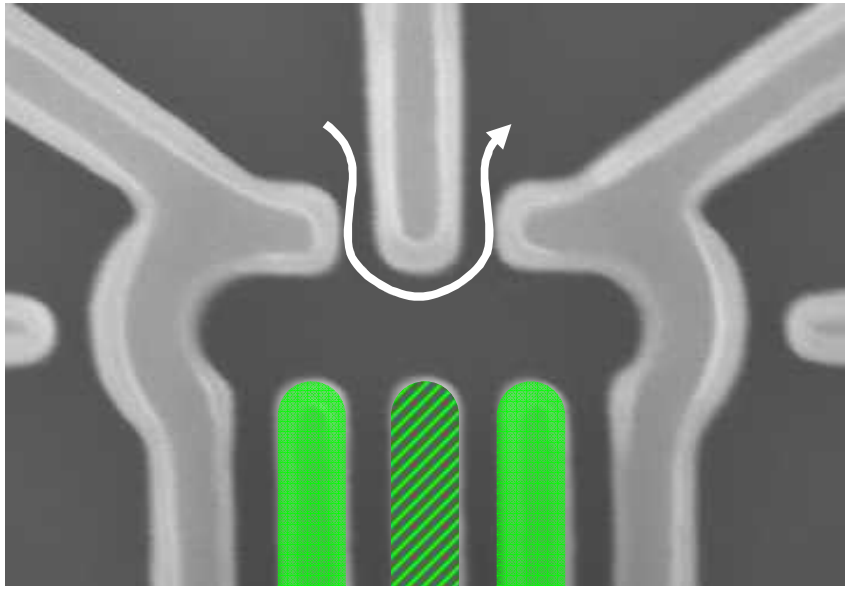




Top Gate Voltage: 20V

Lithographically Induced Coulomb Blockade

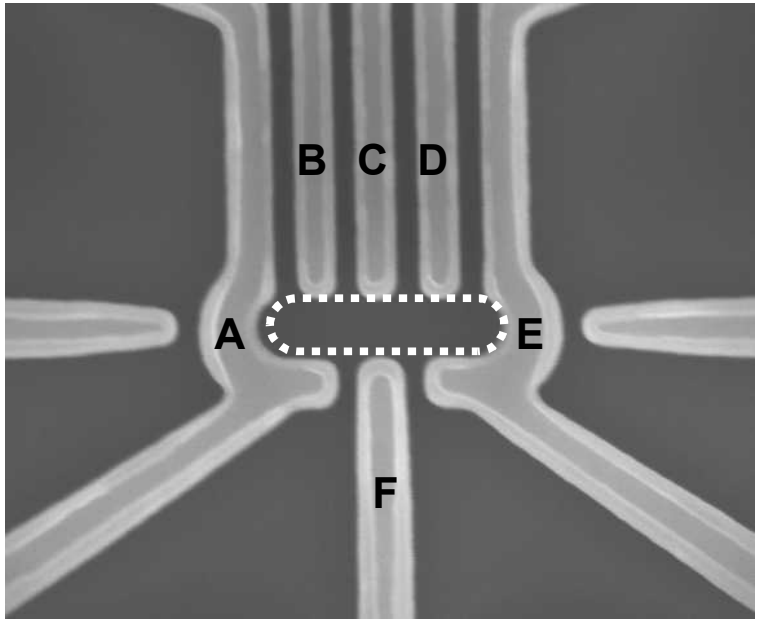


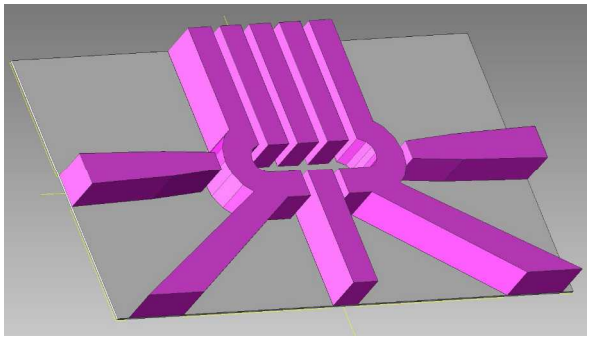


- Using different gate combinations produce different oscillation frequencies
- These oscillation frequencies lead to physically reasonable capacitances between the gate or gates and a dot within the center region

Capacitances: Measured and Calculated

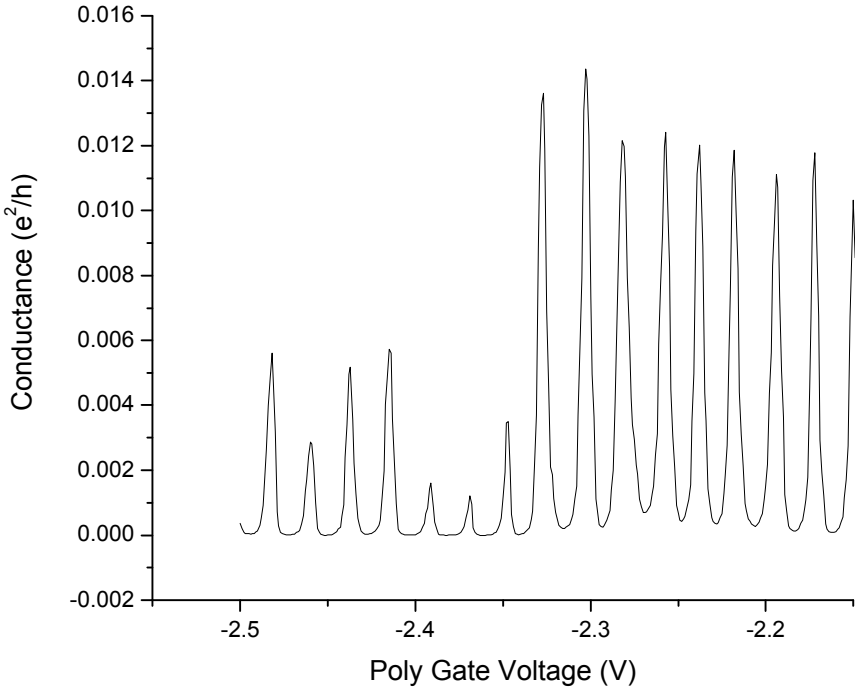
Gate	Model	Measured
A	36.0aF	48.1aF
B	17.0aF	14.1aF
C	17.0aF	17.3aF
D	17.0aF	14.7aF
E	36.0aF	48.1aF
F	15.0aF	20.8aF

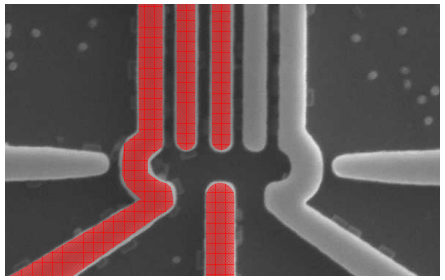


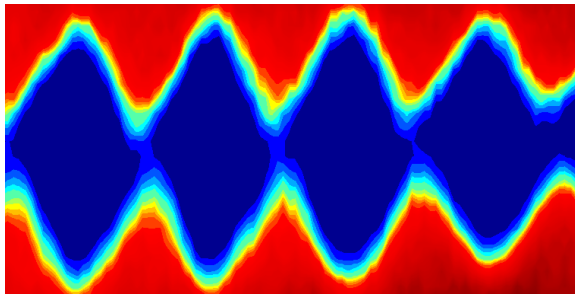


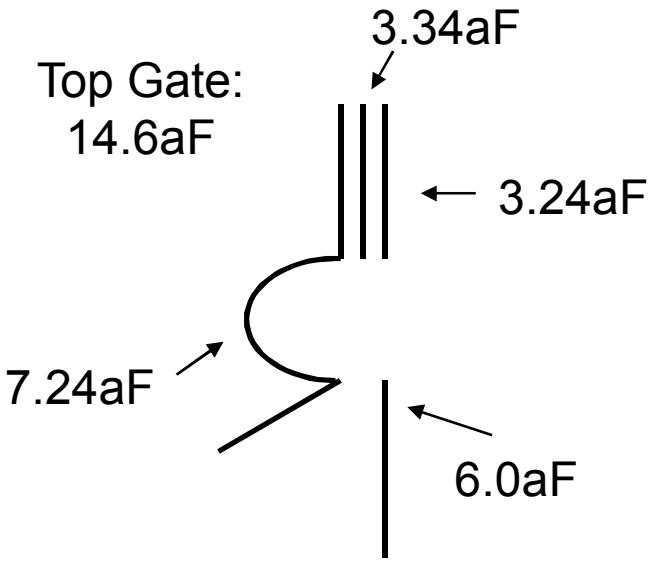
- Calculated capacitances compare favorably in trend and magnitude with those extracted directly from transport data

Stable, Repeatable Coulomb Blockade









Summary

- Double top gate MOS quantum confined structures produced with SNL Si fab facility and additional “back-end” processing
  - Stable, repeatable Coulomb blockade peaks observed within designed structure despite
- Critical processing steps have been identified and evaluated for potential damage to the prospective device
  - Thermal metal evaporations and forming gas anneals clearly improve studied figures of merit
- Future direction: More suitable geometries, and implementation of more disorder mitigation strategies