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# Trap-Related Parametric Shifts under DC Bias and Switched Operation Life Stress in Power AlGaN/GaN HEMTs

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***Abstract*— This paper reports on trap-related shifts of the transfer curve and threshold voltage of power AlGaN/GaN HEMTs under switched bias operating life and reverse and forward DC bias stress. Opposite polarity threshold voltage shifts at room temperature under operating life and reverse bias stress conditions can be explained by means of drain current transient measurements under reverse bias stress conditions. A proposed model to explain the trapping/de-trapping behavior under different stress conditions is described and highlights the critical role of the electric field. Experimental evidence of the importance of the role of the electric field is seen in reduced parametric shift by improving the field plate design.**

***Keywords- AlGaN/GaN; Power HEMT; reliability; field plate; trapping***

## I. INTRODUCTION

Wide-bandgap-based power devices such as AlGaN/GaN High Electron Mobility Transistors (HEMTs) are expected to lead future roadmaps of energy-efficient electronics due to superior intrinsic material properties when compared to incumbent Si power devices. Commercialization efforts to bring GaN-based power devices to market have recently increased to address the diminishing return-on-investment of Si power devices, which are considered to be arriving at a relatively mature stage of performance. These Si-based devices include the workhorses of power ICs, namely the lateral Reduced Surface Electric Field (RESURF) LDMOST [1], as well as the discrete Vertical Super-Junction DMOST [2].

High electron mobility that can reach up to 2000 $cm^2/Vs$ and large critical electric field (~3 MV/cm) that is an order of magnitude higher than Si translates into superior performance for GaN devices. In addition, the wide-bandgap property of GaN ($E_G \approx 3.4$ eV) is expected to enable operation at higher temperatures, and hence opens the possibility of inserting these devices into harsh-environment applications.

For example, in automotive applications the development of GaN-based power devices is consistent with efforts directed at fleet electrification to reduce $CO_2$ emissions and system-level cost, and to increase vehicle range. On the other hand, barriers to wide market adoption still persist, which include the lack of a compelling cost structure, lack of low-defect epitaxial material, and lack of high-quality dielectrics and dielectric/semiconductor interfaces. These factors all lag behind those of their Si-based counterparts, with the latter issues giving rise to stability and reliability degradation challenges in AlGaN/GaN power HEMTs.

Work done to understand the degradation mechanisms in GaN-based HEMTs during accelerated reliability testing and during in-circuit operation are emerging, with the number of publications in the field of GaN reliability on the rise [3]. Chief among the reported degradation mechanisms are the inverse piezoelectric effect [4], time-dependent-dielectric-breakdown of the gate stack [5], hot-carrier degradation during the semi-on/semi-off transition [6], and dynamic on-state resistance degradation [7].

In this paper we report on mechanisms responsible for parametric shifts, specifically transfer curve and threshold voltage ($V_T$) shifts. We use short-time DC reverse-bias electrical stress measurements to explain the differences in behavior between longer DC reverse-bias stress and room-temperature operating life stress, where the device operates as a switch in a boost converter circuit. We present a mathematical model that highlights the role of the electric field, and demonstrate that an improved field plate design can mitigate the observed parametric shifts.

## II. DEVICE STRUCTURE

Power AlGaN/GaN HEMTs fabricated on MOCVD-grown GaN-on-Si substrates were evaluated (Fig. 1). The fabrication process flow and device optimization were described in [8]. The device features a recessed-gate structure that was implemented using a combination of fluorine ion treatment and a two-step atomic layer etching process.

Because of the large area needed for high current carrying capability, an insulating gate consisting of $Al_2O_3$ was grown by atomic layer deposition to reduce the gate leakage current. The device utilized a PECVD silicon nitride passivation layer to terminate the AlGaN surface in the drift and gate-to-source access regions.

Except where otherwise stated in the paper, the device features a 3-step field plate design that is comprised of one gate-connected field plate and two source-connected field plates extending over the drift region between the gate and the drain. The 3-step field plate is used to arrive at an electric field distribution that is characterized by a saw-tooth type of distribution. This is more favorable than the triangular field distribution that is common in devices with no field plates, but is less favorable than a flat electric distribution that could be

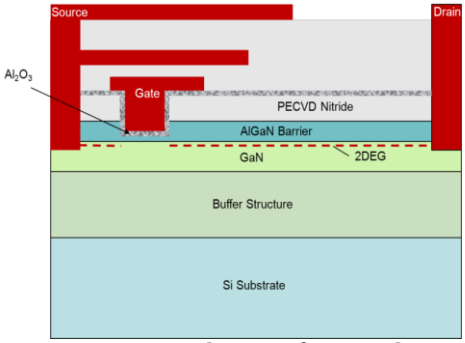



**Fig. 1.** 2-D cross-sectional view of HRL AlGaN/GaN power HEMT [8].

possible using a more advanced field-shaping technique (e.g. a slanted field plate).

## III. Experimental Results

### A. Test Setup

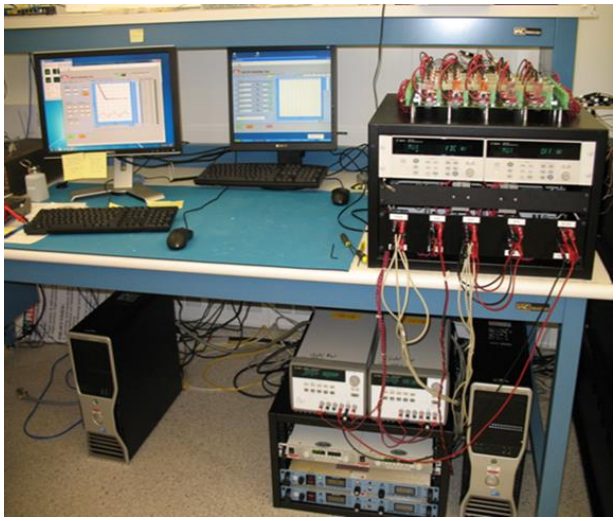
Room- and High-Temperature Reverse Bias (RTRB and HTRB) and Room- and High-Temperature Operating Life (RTOL and HTOL) measurements were carried out on the power HEMTs to assess the stability and reliability of HRL's GaN-on-Si technology. The setups of the RTRB/HTRB and RTOL/HTOL test stations are shown in Figs. 2a and 2b respectively. Special attention was given to the design of the test boards to reduce parasitic components. In particular, emphasis was placed on reducing parasitic inductances in order to suppress gate and drain current transients that can significantly increase voltage spikes and impact reliability data.

For the operating life tests, TO-257-packaged devices were inserted in multiple boost converter circuits designed in-house to reproduce device stress conditions encountered in typical power management switching applications. Key device parameters such as $V_T$, on-state resistance $R_{on}$, and gate and drain leakage currents were measured at predetermined time intervals and were plotted versus stress time. A monitor device, which was not subjected to any electrical stress, had the key device parameters measured at the time intervals to detect any drifts in the test setup or the ambient environment. There was a typical delay time of a few minutes (not exceeding 10 minutes) between the end of a stress interval and the acquisition of the transfer curve and extraction of key device parameters.

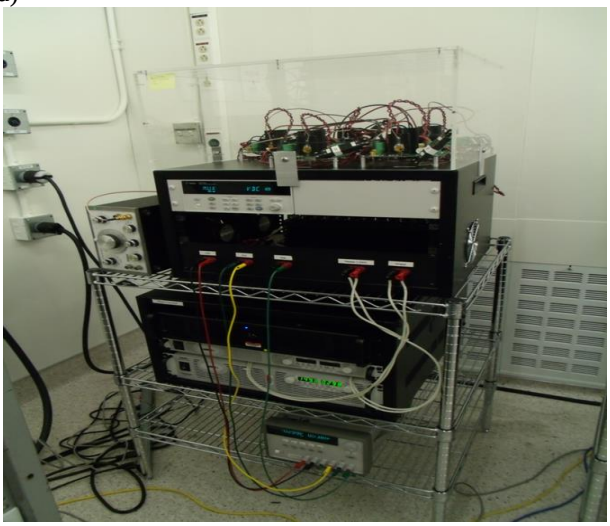
### B. RTOL and HTOL Results

Fig. 3 shows the HEMT transfer curves before and after stress for one of the five devices that were subjected to RTOL stress in a boost converter operating at 100 kHz with a duty cycle of 50% and an output voltage of 200V. An almost parallel shift in the positive direction of the transfer curve, and a corresponding positive shift in $V_T$, can be seen.

The shifts in $V_T$ versus RTOL stress time for all five stressed devices as well as the monitor device are shown in Fig. 4, and indicate a consistent qualitative behavior for all stressed devices. The positive shift in the transfer curve is attributed to a dominant electron trapping mechanism in the gate stack, which at room temperature dominates possible de-trapping events that



(a)



(b)

**Fig. 2.** (a) RTRB/HTRB test station and (b) RTOL/HTOL (boost converter) test station.

accumulate during the on-state, off-state, and semi-on/semi-off transition states of the switching cycle seen by the device. The positive shift saturates and a value between 0.4 and 0.7 V during the 1032 hours duration of the RTOL stress.

The positive shift in the transfer curve results in a 15% degradation in $R_{on}$, as shown in Fig. 5, which was evaluated at the same positive $V_G$ = 2.5V as was the pre-stress case. The parallel and positive shift in the transfer curve and the reduced gate voltage swing after stress are responsible for $R_{on}$ degradation, i.e. it will take a larger gate voltage to arrive at the pre-stress value of $R_{on}$.

The normalized gate leakage current during RTOL stress is shown in Fig. 6 and exhibits a falling trend with stress time during the initial 300 hours of stress for the majority of the devices (with the exception of DUT #4).

Fig. 7 shows the $V_T$ shifts during HTOL testing carried out at 125°C. The behavior is markedly different from the RTOL results. The positive shift in $V_T$ was not observed in the initial stage of the stress (up to 4 hours, denoted as region 1 in Fig. 7);

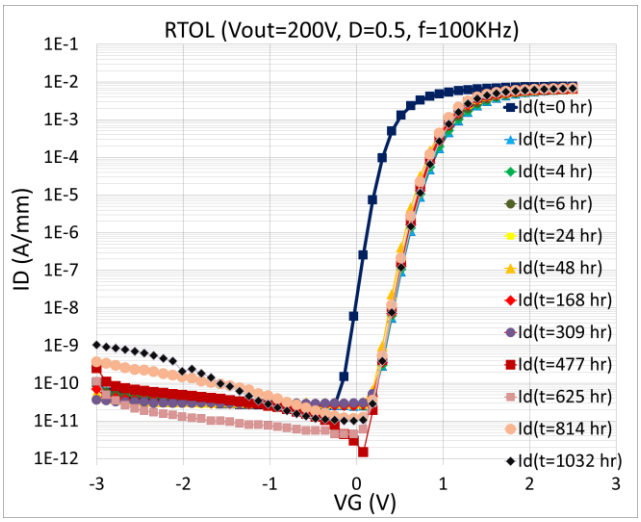



**Fig. 3.** Transfer curves before (dark blue) and at indicated stages of RTOL stress. The positive shift is indicative of electron trapping.

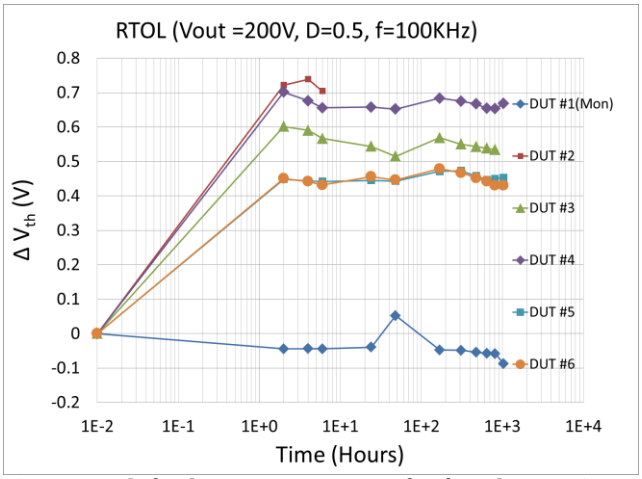



**Fig. 4.** $V_T$ shifts during RTOL stress for five devices ($V_T$ is evaluated at 10 μA/mm). The positive shift is indicative of electron trapping.

instead, a smaller negative shift attributed to electron de-trapping is observed, with a magnitude between 0.15 and 0.2 V. This saturates and continues to exhibit a saturation behavior up to at least 48 hours of stress time (region 2). The saturation behavior in region 2 must be due to a competing trapping process that cancels out the de-trapping process which dominates in region 1.

The saturation region is then followed by a positive shift attributed to the dominance of the trapping mechanism (region 3). That this behavior was not observed in RTOL is indicative of the presence of competing temperature-dependent electron trapping and de-trapping mechanisms. While these results are not completely understood at the present time, the concept of a reversal from one trapping/de-trapping process to an opposite de-trapping/trapping process is discussed later in the paper.

The electron trapping mechanism becomes dominant starting at roughly 48 hours (region 3) but could have started to be dominant anywhere between 24 hours and 48 hours (time

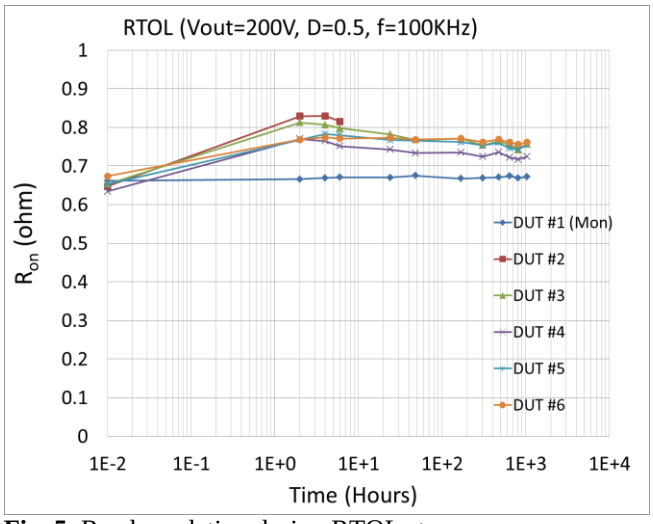



**Fig. 5.** $R_{on}$ degradation during RTOL stress.

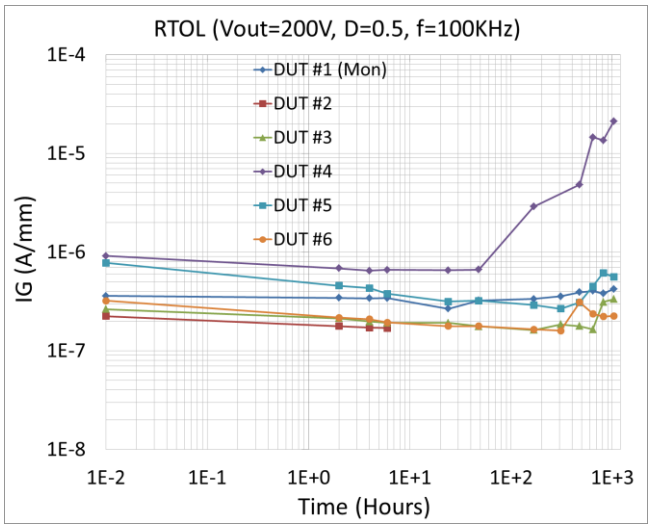



**Fig. 6.** Gate leakage current during RTOL stress.

resolution limited). A second region of saturation (region 4) is observed with the final $V_T$ shift stabilizing between zero and 0.2 V. HTOL did not impact the on-state resistance, which was ~ 0.7 Ω over the entire stress time, as shown in Fig. 8.

### *C. RTRB, HTRB, and DC Bias Stress Results*

A DC reverse-bias stress, where the device is turned off by applying $V_G < V_T$ and coupled with a high positive drain voltage, causes a negative shift in the transfer curve and a corresponding negative shift in $V_T$. The negative $V_T$ shift is shown in Fig. 9, where five devices were subjected to RTRB stress with $V_G$ = -3 V and $V_D$ = 200 V for 1675 hours (results for an un-stressed control device are also shown). While a saturation behavior followed by a small reversal in the direction of the shift is observed, the net shift observed over the total duration of the stress is in the negative direction. The negative shift in $V_T$ and in the transfer curves are attributed to de-trapping of electrons in the AlGaN barrier during reverse bias stress when the stress time is sufficiently long. In this context, "sufficiently long" refers to a period greater than about

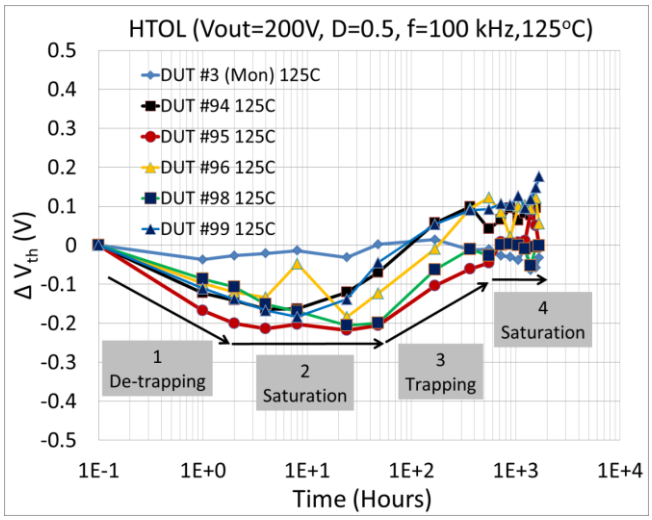



**Fig. 7.** $V_T$ shifts during HTOL stress. Both electron de-trapping and trapping are active at high temperature.

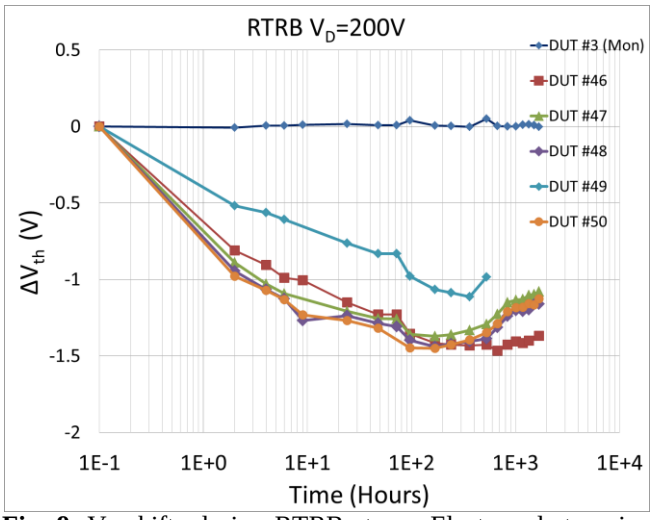



**Fig. 9.** $V_T$ shifts during RTRB stress. Electron de-trapping dominates.

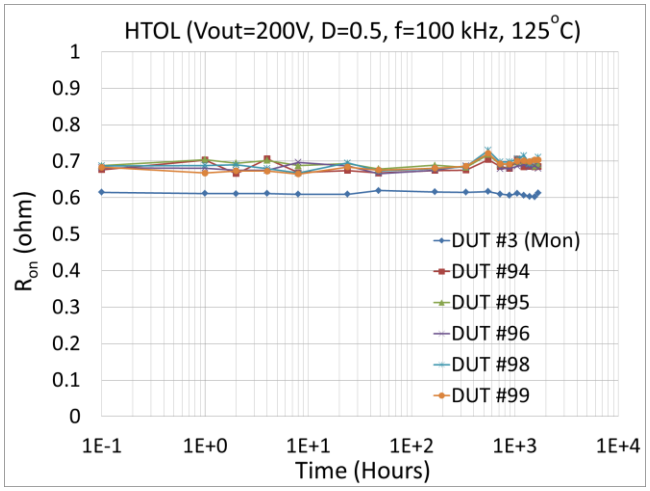



**Fig. 8.** $R_{on}$ degradation during HTOL stress.

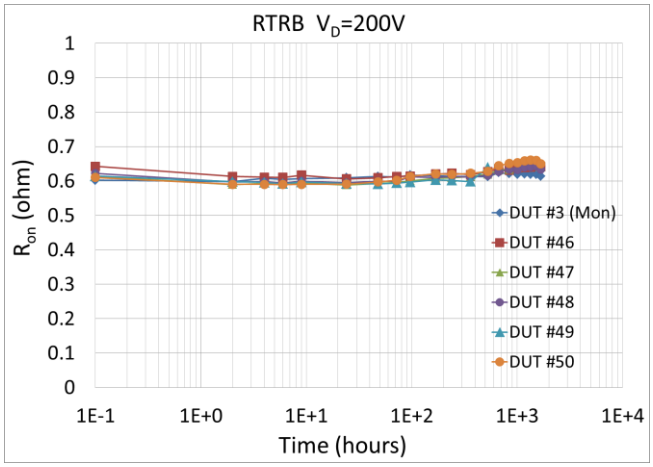



**Fig. 10.** $R_{on}$ degradation during RTRB stress.

1 s. During DC stress measurements on the order of a fraction of a second we did not observe the negative shifts, as explained below. The negative $V_T$ shifts for the five devices ranged between -1.1 and -1.4 V at the end of the 1675 hours of RTRB stress. The on-state resistance ($R_{on}$) versus time is shown in Fig. 10, and indicates small changes correlated with the changes in $V_T$.

The negative shift due to RTRB stress is not permanent and is recoverable with temperature, as depicted in Fig. 11. The two devices that recovered at 110°C and 150°C showed complete recovery within the 340 hours of the high-temperature storage life test while devices recovered at room temperature and at 75°C showed only partial recovery. The direction of the recovery in $V_T$ (positive shift) is consistent with electron trapping, indicating that the increased recovery at high temperature is consistent with the presence of an energy barrier limiting the trapping rate.

The model emerging here postulates that the presence of an energy barrier to electron trapping, as evident from the enhancement of trapping at higher temperature during recovery under storage life tests. This model is enforced by observing the parametric shifts in HTRB tests at 125°C in which a smaller *negative* shift (compared to RTRB) in the transfer curve and in $V_T$ are seen, as shown in Fig. 12. The reduced shifts are attributed to an increase in the competing but non-dominant trapping process. Positive shifts in the transfer curve and in $V_T$ were also observed under DC forward gate-bias stress ($V_G$ = 2.5 V, $V_D$ = 0.1 V) at room temperature for up to 3 hours (Fig. 13). The positive shift indicates that in forward gate-bias stress, electron trapping is predominant. Further, the shift exhibits a saturation behavior.

The positive shift in the transfer curve due to RTOL can be explained by conducting short-time transient tests under reverse-bias conditions and capturing the drain current transients over relatively short periods of time, which is described in detail in [10]. The anticipated increase in drain transient current due to electron de-trapping was not observed, at least for the initial period of the stress; instead, a drop in the drain current was obtained under room temperature, as shown in Fig. 14a. The reverse bias test ($V_G$ = -7 V, $V_D$ = 50 V) was repeated for periods of 200, 400 and 800 ms, and after each interval of the transfer curve was acquired (Fig. 14b).

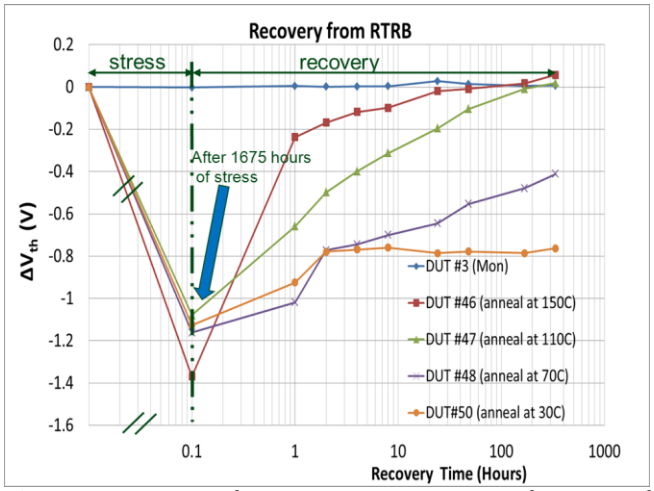



**Fig. 11.** Recovery from RTRB stress as a function of temperature. For the first part of the curve up to 1675 hours (which shows the magnitude of the $V_T$ shift due to RTRB stress), the x-axis is not drawn to scale.

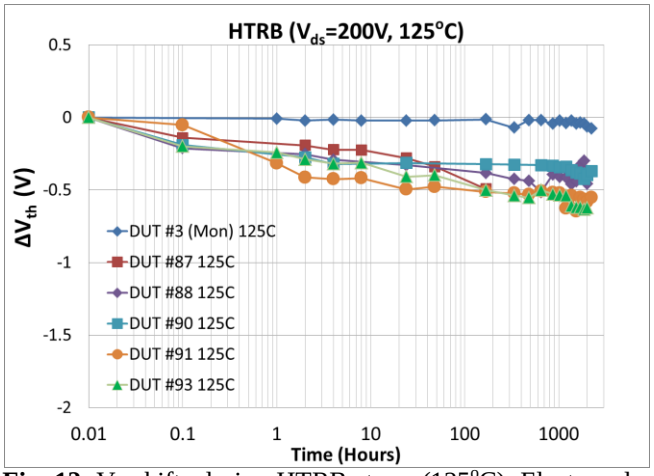



**Fig. 12.** $V_T$ shifts during HTRB stress (125°C). Electron de-trapping dominates, but is compensated by a trapping process at high temperature.

The following observations are consistent with carrier trapping during the initial period of the stress: First, the drain currents are falling with time during all three stress intervals; and second, the transfer curve taken after the 200 ms stress had a positive shift, and the curve taken after 400 ms the stress had a further positive shift. For the 800 ms stress, while the current is still showing an overall falling trajectory, the onset of a saturation behavior is apparent. This conclusion is supported by two observations: First, the onset of a negative shift in the transfer curve (red curve in Fig. 14b) with respect to the post 200 ms and 400 ms curves. Second, the leakage current following the 800 ms stress is larger than that following the 200 ms and 400 ms curves, but still smaller than that for the pre-stress curve. For a longer duration stress of 1.2 s (Fig. 15a), the de-trapping mechanism starts to dominate and the drain current starts increasing. Finally, for a stress duration of 40 s, carrier de-trapping causes a net negative shift in the transfer curve (blue curve in Fig. 15b). This is similar to the negative shifts that are encountered following both RTRB and HTRB

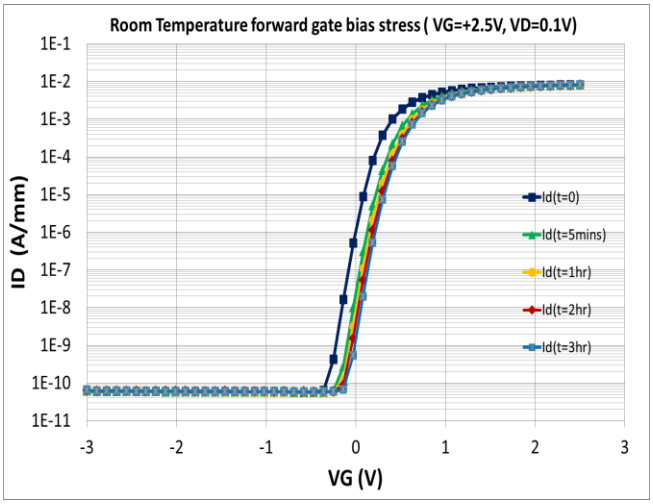



**Fig. 13.** Transfer curve shift due to DC forward gate bias stress at room temperature. Electron trapping dominates.

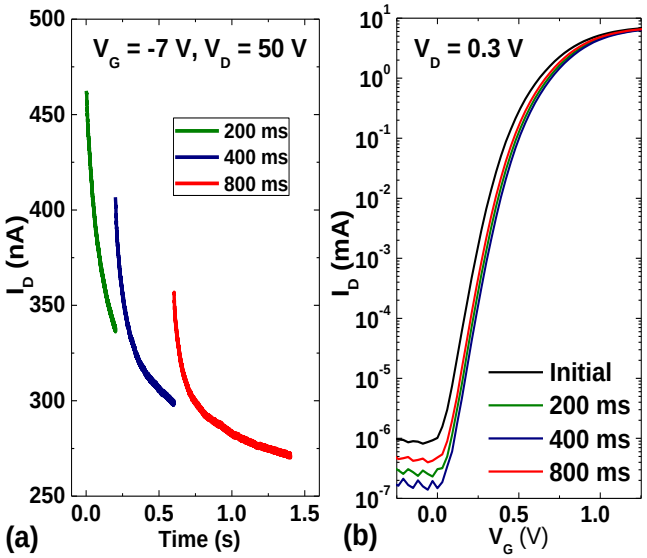



**Fig. 14.** (a) Drain current transients during RTRB stress. (b) Transfer curves measured after 200, 400 and 800 ms of RTRB stress. A saturation in electron trapping is observed.

stress, where the first post-stress characterization curves were captured typically after at least one hour of stress had elapsed. Further, the short-time drain current transients explain experimentally why operating life tests at room temperature show only positive shifts in the transfer curves, since devices experiencing RTOL stress spend very short periods of time (on the order of μs) under reverse bias.

### *D. Trap Energy Evaluation*

Trap energy is usually evaluated by observing emission from the trap over a range of temperatures, which requires a stress condition that initially fills the traps. Since, as shown above, blocking bias conditions result in electron de-trapping except at very short times, stress conditions with $V_G < V_T$ and $V_D = 0$ were used for this purpose. These conditions result in electron trapping [10], similar to what is observed following the stress conditions of Fig. 13. Following stress, de-trapping

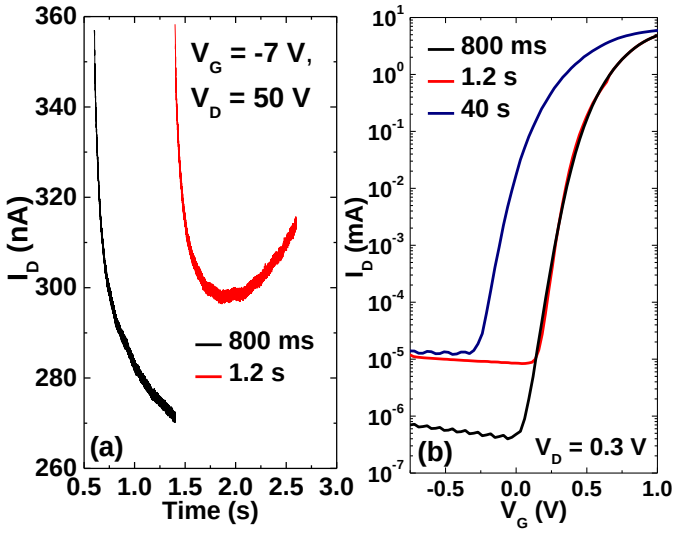



**Fig. 15.** (a) Drain current transients during 800 ms and 1.2 s RTRB stresses. (b) Transfer curves following 800 ms, 1.2 s, and 40 s RTRB stresses. A transition from electron trapping to de-trapping occurs.

experiments were performed at elevated temperatures to extract the trap energy. However, the recovery transients at elevated temperatures did not fit a single exponential, indicating the presence of multiple time constant components. Such transients have been observed previously [11-12] and can be analyzed by considering the derivative at time t = 0. The transient may be written as a sum of exponentially decaying terms:

$$I_D(t) = I_\infty + \sum_i a_i exp\left(\frac{-t}{\tau_i}\right) \quad (1a)$$

$$\left.\frac{dI_D}{dt}\right|_{t=0} = -\sum_i \frac{a_i}{\tau_i} \quad (1b)$$

Thus, for comparable amplitudes, the smallest time constant will dominate the derivative at t = 0. Assuming a single time constant $\tau_n$ dominates and that this time constant corresponds to electron emission from the trap, the trap energy $E_T$ was evaluated according to the standard expression [9]:

$$\tau_n T^2 = \frac{1}{\sigma_n \gamma_n} exp\left(\frac{E_T}{kT}\right) \quad (2)$$

where $\sigma_n$ is the capture cross-section, $\gamma_n$ is a constant proportional to the electron effective mass, k is Boltzmann's constant, and T is the temperature in degrees Kelvin. The approximate time constants were evaluated in this manner over a range of temperatures (Fig. 16), and a trap energy of $E_T \approx 0.6$ eV was extracted (inset of Fig. 16). This value has been previously observed by many different groups on AlGaN/GaN HEMTs of various designs [11].

## IV. Proposed Model

Data reported recently in [10] concluded that the primary $V_T$ shift is consistent with electron trapping and de-trapping in the AlGaN layer under the gate and that the changes in the drain leakage current are likely related to an energy barrier in the gate stack. In addition, the recoverable nature of the change in leakage current also suggests that it is not due to generation of permanent defects. There is also a consistent correlation between the direction of the $V_T$ shift and the corresponding changes in the leakage current. Overall, the time-dependent changes in $V_T$ are consistent with a short initial trapping phase followed by a longer de-trapping phase.

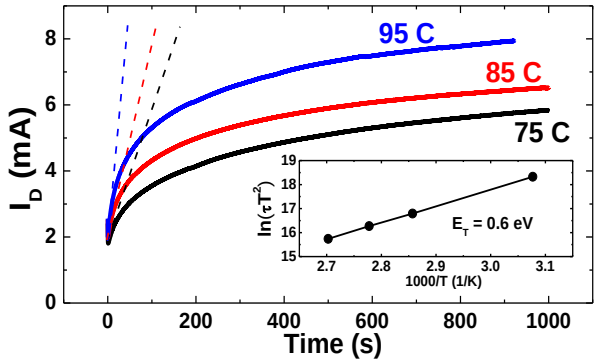



**Fig. 16.** Drain current transients following stress ($V_G$ = -9 V, $V_D$ = 0), measured at high temperatures. The dashed lines in illustrate the fit to the slope at t = 0. A trap energy of $E_T \approx$ 0.6 eV is extracted (inset).

The proposed model is based on the concept of field-enhanced emission through barrier lowering and phonon-assisted tunneling (Fig. 17) [13]. The basic idea is that electrons are initially injected into the AlGaN in the gate stack (this may be due to tunneling from the gate electrode under high electric field), become trapped, and lead to the short-term positive $V_T$ shift. The corresponding leakage current reduction is correlated, but may not be directly due to electron trapping in the AlGaN – e.g. it may be due to trapping elsewhere in or near the gate stack, which may impact the barrier height and/or tunneling rate at the gate metal contact. Depending on the specific distribution of the trapped electrons and the boundary conditions, the electric field may become sufficiently large within the AlGaN to induce emission of the trapped electrons. This de-trapping results in the long-term negative $V_T$ shift and leakage current increase. The proposed process is complex, depending sensitively on the energy barriers for capture and emission (and thus the specific deep levels present), the temperature, and the geometry of the device (including the compositions and thicknesses of the various constituent layers, the field plate structure, etc.) In the following, we attempt to mathematically demonstrate the plausibility of this model.

We have constructed a simple model in one spatial dimension linking the time- and position-dependent electric potential $\varphi(t,x)$ and the density of trapped electrons $n_T(t,x)$. They are coupled via the Poisson equation with the filled traps as the source of charge:

$$\frac{\partial^2 \varphi(t,x)}{\partial x^2} = \frac{q n_T(t,x)}{\varepsilon} \quad (3)$$

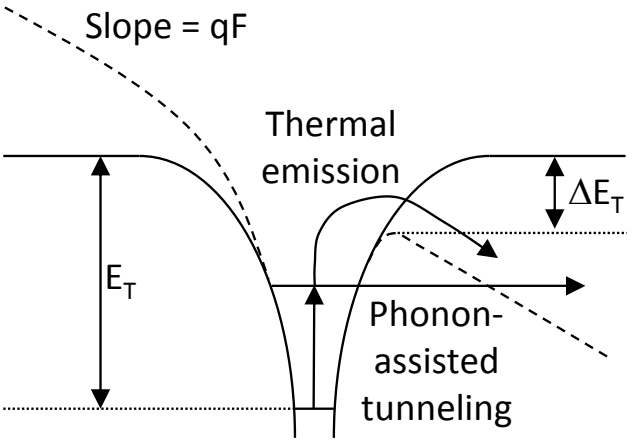



**Fig. 17.** Schematic illustration of enhanced emission from a deep-level trap due to a high electric field. Both thermal emission and phonon-assisted tunneling are considered. Solid lines show the trap's potential well at zero field, and dashed lines show the well as modified by the electric field F. $E_T$ is the zero-field well depth and $\Delta E_T$ is the field-induced barrier lowering.

Further, a rate equation governs the time-dependent trap occupancy [9]:

$$\frac{dn_T}{dt} = c_n(N_T - n_T)n - e_n n_T \tag{4}$$

In Eqn. 4, $c_n = \sigma_n v_{th}$ is the capture (i.e. trapping) coefficient (equal to the product of the capture cross-section $\sigma_n$ and the thermal velocity $v_{th}$), $N_T$ is the total (assumed uniform) trap density, n is the available electron density, and $e_n$ is the emission (i.e. de-trapping) rate. In a bulk material the available electron density would simply be the free electron density; however, consistent with the experimental data presented above, here we assume that this density is limited by transport over a barrier of energy $E_B$. This can be accounted for by using the following equation for the available electron density:

$$n = n_0 exp\left(\frac{-E_B}{kT}\right) \tag{5}$$

As noted above, the emission rate $e_n$ is modeled considering a Coulombic trap potential impacted by both field-enhanced thermal emission and phonon-assisted tunneling [13]:

$$e_n = e_{n0}\left\{exp\left(\frac{\Delta E_T}{kT}\right) + \int_{\Delta E_T/kT}^{E_T/kT} exp\left[z - \left(\frac{z}{z_0}\right)^{3/2}\left(1 - \left(\frac{\Delta E_T}{zkT}\right)^{5/3}\right)\right]dz\right\} \tag{6}$$

The zero-field emission rate is [9]:

$$e_{n0} = \sigma_n \gamma_n T^2 exp\left(\frac{-E_T}{kT}\right) \tag{7}$$

Further, the field-induced barrier lowering is [13]:

$$\Delta E_T = q\sqrt{\frac{q|F|}{\pi\varepsilon}} \tag{8}$$

In Eqn. 8, F is the electric field ($F = -d\varphi/dx$). Finally, the integral in Eqn. 6 is also dependent on the electric field through $z_0$ [13]:

$$z_0^{-3/2} = \frac{8\pi\sqrt{m_n(kT)^3}}{3qh|F|} \tag{9}$$

In Eqn. 9, we used $m_n = 0.2\ m_0$ for the electron effective mass. Note that Eqns. 8 and 9 both depend only on the magnitude of the electric field, not its direction. It is evident that in addition to the coupling between $\varphi$ and $n_T$ through the Poisson equation (Eqn. 3), these two quantities are also coupled through the rate equation for $n_T$ (Eqn. 4), since it is dependent upon the derivative of the potential (i.e. the electric field) through Eqns. 6, 8, and 9.

A MATLAB simulation was written to solve Eqns. 3 through 9 numerically. A uniform density of $N_T = 10^{15}$ cm$^{-3}$ was assumed, with 80% of the traps filled at t = 0. A slab of material of length L = 10 μm was considered, with boundary conditions of zero field at x = 0 and zero potential at x = L. The initial condition for the potential was a quadratic function of position, consistent with the boundary conditions and the initial uniform density of trapped electrons. Various values of the temperature T, the trap energy $E_T$, and the capture barrier energy $E_B$ were evaluated; the results of a simulation with T = 300 K, $E_T$ = 0.6 eV, and $E_B$ = 0.4 eV are shown in Fig. 18, where $n_T(t,x)$ is plotted vs. time and position. At time t = 0, 80% of all traps are uniformly filled such that $n_T(0,x) = 8\times10^{14}$ cm$^{-3}$. As time advances, near x = 0 (where the boundary condition is zero field) trapping dominates, whereas near x = L (where the boundary condition is zero potential) de-trapping dominates. The specific behavior is sensitive to the chosen values of $E_T$ and $E_B$, as shown in Fig. 19. Fig. 19a plots the trapped electron density at the mid-point of the material (x = L/2) calculated for $E_T$ = 0.6 eV for various values of the capture barrier energy $E_B$. It is seen that for a small $E_B$, electron trapping dominates (which is physically intuitive, as the trapping rate is faster for a smaller $E_B$), whereas for large $E_B$ electron de-trapping dominates. Appropriate balancing of the two energies results in a transition from trapping to de-trapping, as illustrated in Fig. 19b. Further, adjustment of the magnitudes of the two energies simultaneously alters the prominence of the transition peak as well as the time at which it occurs (fig. 19c). This simple model demonstrates that a transition from trapping to de-trapping is physically plausible.

Of course, the behavior observed experimentally will depend on detail of the geometry of the real device and the exact location of trapping, which is not captured in the simple 1-D model and requires the use of 2-D finite-element simulations. One possible scenario is that electrons are initially trapped in the AlGaN in the gate stack and/or in the region underneath the gate field plate. This will tend to raise the conduction band edge in this region, leading to significant band bending (and hence a large electric field) near the drain side edge of the gate and at the edge of the gate field plate. This high electric field, induced by the initial trapping, will in turn lead to a higher de-trapping rate from the traps in the vicinity of the channel, as described by our model.

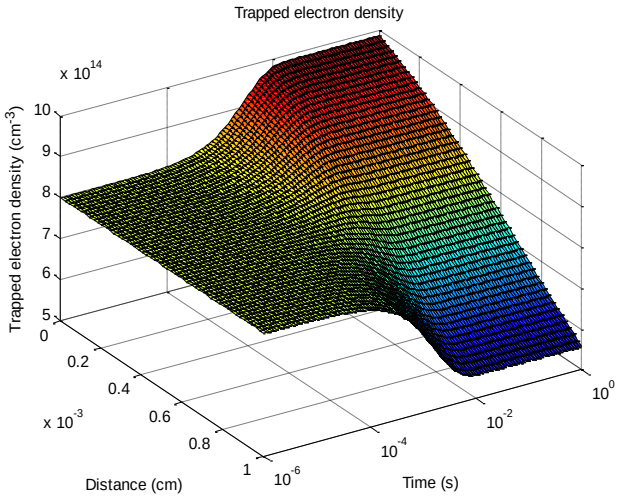



**Fig. 18.** Surface plot of trapped electron density $n_T(t,x)$ calculated at 300 K using the 1-D model described in the text, using $E_T$ = 0.6 eV and $E_B$ = 0.4 eV. Both trapping and de-trapping are observed.

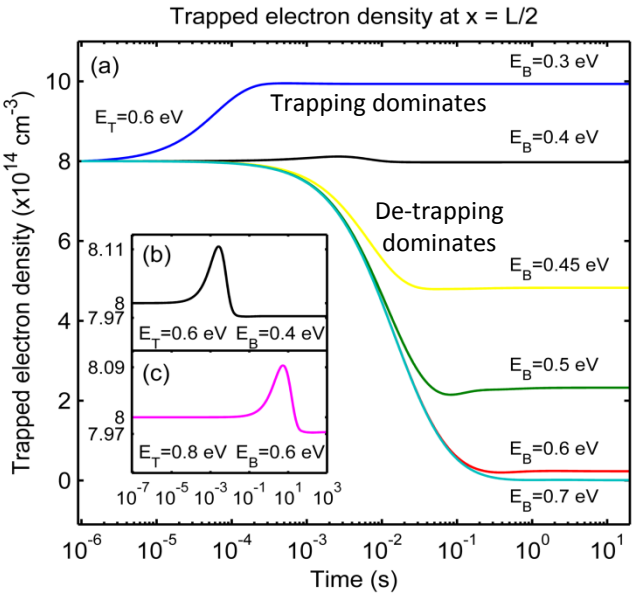



**Fig. 19**. (a) Plots of $n_T(t,L/2)$ calculated using the 1-D model at 300 K with the trap energy fixed at $E_T$ = 0.6 eV with various values of the capture barrier energy $E_B$. The dominance of trapping vs. de-trapping depends on the relative values of $E_T$ and $E_B$. (b) Expanded view of trapped electron density plotted vs. time for $E_T$ = 0.6 eV and $E_B$ = 0.4 eV, illustrating transition from trapping to de-trapping. (c) Expanded view of trapped electron density plotted vs. time for $E_T$ = 0.8 eV and $E_B$ = =0.6 eV, illustrating the dependence of the transition time on $E_T$ and $E_B$.

TCAD simulations in [10] showed that the maximum field under reverse bias occurs in the AlGaN layer at the drain side edge of the gate. The field is of sufficient magnitude (~ 1 MV/cm) to induce de-trapping of electrons, as outlined in the model described above. Full time-dependent TCAD simulations are in progress and will be presented in a future paper.

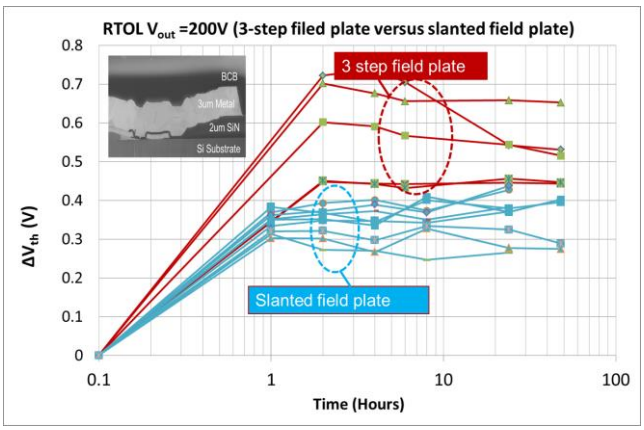



**Fig. 20.** $V_T$ shift comparison between devices with 3-step field plate design and devices with slanted field plate design.

The electric field profile in the AlGaN barrier and GaN channel layer, as well as the field plate design, can therefore play an important role in mitigating parametric shifts seen under operating life stress. The problem of moderating electric fields at the drain side edge of the gate is in principle similar to that of mitigating hot carrier injection in short-channel silicon devices. Indeed, designs with slanted field plates have achieved a noticeable reduction in the positive $V_T$ shift under operating life tests, as shown in Fig. 20.

## V. Conclusion

In this paper we have reported shifts of the transfer curve and of $V_T$ under different stress conditions for AlGaN/GaN power switching HEMTs. Positive shifts observed under room temperature operating life stress are consistent with an initial electron trapping behavior under reverse bias stress, as seen by the decay of drain current transients during the initial period of the stress. A saturation of the drain current transient decay, followed by an increase in the current at longer times under reverse bias stress, is consistent with both room- and high-temperature reverse bias stress in which a negative shift in the transfer curve and in $V_T$ is observed. The saturation and reversal of the drain current transients are indicative of sequential capture and emission mechanisms, with a transition between the two opposite mechanisms resulting from the evolving electrostatic potential distribution. The simultaneous numerical solution of the Poisson equation and the electron capture/emission rate equation described on our 1-D model demonstrates that the trap density and energy, capture barrier energy, and temperature, can cause a transition from trapping to de-trapping is possible on a time scale of the same order of magnitude as that seen in our experimental transient current measurements. RTOL data comparing $V_T$ for a 3-step field plate and a slanted field plate highlights the importance of electric field shaping techniques to suppress parametric shifts resulting from electrical stress.

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