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Interstitial Monitoring Technologies

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ABSTRACT

When developing new hardware for a computer system, bus monitors are invaluable for testing compliance and troubleshooting problems. Bus monitors can be purchased for other common system busses such as the Peripheral Component Interconnect (PCI) bus and the Universal Serial Bus (USB). However, the project team did not find any commercial bus analyzers for the Low Pin Count (LPC) bus. This report will provide a short overview of the LPC interface.

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INTRODUCTION

When developing new hardware for a computer system, bus monitors are invaluable for testing compliance and troubleshooting problems. Bus monitors can be purchased for other common system busses such as the Peripheral Component Interconnect (PCI) bus and the Universal Serial Bus (USB). However, the project team did not find any commercial bus analyzers for the Low Pin Count (LPC) bus. This report will provide a short overview of the LPC interface, as specified in [1].

THE LOW PIN COUNT (LPC) INTERFACE

This portion of the report is intended as an overview of the LPC interface as defined in [1]. The electrical domain details will be left to the full specification [1]. In addition, the specific bit patterns defined for each symbol will not be listed unless there is a reason to do so.

Signals with a # following their name are "active low" signals.

The LPC interface includes both required and optional signals. The required signals must be implemented by all LPC hosts and peripherals. Optional signals might not be implemented on many hosts or peripherals. This effort focused only on the required signals of the LPC interface.

The LPC required signals are

- LAD[3:0]
- LFRAME#
- LRESET#
- LCLK

LPC Required Signal Descriptions

LAD[3:0]

This bidirectional, four bit bus carries the address, data, and other information transmitted between the host and peripherals on the LPC bus during the course of an LPC bus cycle.

LFRAME#

LFRAME# is used by the host to signal the start of a new LPC cycle to all the peripherals on the LPC bus. LFRAME# is also used to terminate broken cycles.

LRESET#

LRESET# is the reset signal for the LPC host and peripherals. LRESET# is the same as the PCI reset signal.

LCLK

LCLK is the 33 MHz clock from the PCI bus.

Symbols

During an LPC bus cycle, the values on LAD[3:0] take on different meanings in the protocol. Each of these meaning is given a symbolic name.

START

There are three categories of LPC cycles

- Memory, I/O, and DMA
- Firmware
- Bus Mastered Memory and I/O

The start of an LPC cycle is identified by the LFRAME# signal being asserted (going low). The value on LAD[3:0] when LFRAME# is negated (goes high) is used as the START field. The value of the START field determines which of the three categories the LPC cycle is going to be.

CYCTYPE_DIR

For memory, I/O, and DMA cycles, the CYCTYPE_DIR field is the value on LAD[3:0] during the single clock cycle following the START field. This field distinguishes the type of the cycle (memory, I/O, or DMA) and the direction of the cycle (a read or a write).

ADDR

The ADDR field occupies eight clock cycles and is composed of a 32 bit memory address that is transferred most significant nibble first across LAD[3:0]. The ADDR field is used during memory cycles.

IO_ADDR

The IO_ADDR field occupies four clock cycles and is composed of a 16 bit I/O address that is transferred most significant nibble first across LAD[3:0]. The IO_ADDR field is used during I/O cycles.

IDSEL

The IDSEL field occupies one clock cycle and indicates which firmware device is being selected during firmware access cycles.

MADDR

The MADDR field occupies seven clock cycles and is composed of a 28 bit address that is transferred most significant nibble first across LAD[3:0]. MADDR is used during firmware access cycles. Together, IDSEL and MADDR can alternately be viewed as a 32 bit address.

CHANNEL

The CHANNEL field occupies one clock cycle during a DMA cycle and notifies the peripherals which DMA channel has been granted.

SIZE

The SIZE field occupies one clock cycle and indicates how many bytes of data will be transferred during the DMA cycle.

MSIZE

The MSIZE field occupies one clock cycle and indicates how many bytes of data will be transferred during the firmware access cycle.

DATA
Each DATA field occupies two clock cycles and is composed of a single byte of data that is transferred least significant nibble first across LAD[3:0].

TAR (Turn-Around)
The TAR field occupies two clock cycles. During the first clock cycle, the device currently driving the bus will drive LAD[3:0] to b"1111". During the second clock cycle, the driving device will stop driving the bus so that the other device it is communicating with can begin driving the bus. Weak pull-up resistors on the bus keep LAD[3:0] at b"1111" during the second clock cycle.

SYNC
The SYNC field occupies at least once clock cycle to indicate that synchronization was achieved without error, and may occupy additional clock cycles to insert wait states if needed. There are two types of wait states: short waits and long waits. Short waits can last a maximum of eight clock cycles. Long waits do not have a defined maximum number of clock cycles.

Cycle Types
This section describes the sequences of symbols that constitute the valid LPC bus cycles. Symbols or sequences of symbols that can occur multiple times during an LPC cycle are followed by a set containing the number of times that they can occur. For example, if the DATA symbol can occur consecutively one, two, or four times, it will be written as DATA{1,2,4}. Similarily, the sequence (SYNC + DATA){1,2} would indicate that either of "SYNC + DATA" or "SYNC + DATA + SYNC + DATA" are valid sequences that could occur at that position.

To keep each cycle type readable, a preamble is defined for each cycle type that includes the START symbol and any address and size symbols. Both the read and write variants of each cycle type begin with the same preamble.

During normal cycles, the host controls the preamble. During bus master cycles, the host drives a START code to identify it as a bus master cycle, and then turns control of the bus over to a peripheral that drives the rest of the preamble to identify the cycle type, direction, address, and size.

BLUE_NORMAL = Host drives the bus. *RED_ITALIC* = Peripheral drives the bus.

Memory Read/Write
Read sizes supported: 1 byte
Write sizes supported: 1 byte

```
MEM_PREAMBLE := START + CYCTYPE_DIR + ADDR
MEM_R := MEM_PREAMBLE + TAR + SYNC + DATA + TAR
MEM_W := MEM_PREAMBLE + DATA + TAR + SYNC + TAR
```

I/O Read/Write
Read sizes supported: 1 byte
Write sizes supported: 1 byte

```
IO_PREAMBLE := START + CYCTYPE_DIR + IO_ADDR
IO_R := IO_PREAMBLE + TAR + SYNC + DATA + TAR
IO_W := IO_PREAMBLE + DATA + TAR + SYNC + TAR
```

DMA Read/Write

Read sizes supported: 1, 2, 4 bytes
Write sizes supported: 1, 2, 4 bytes

```
DMA_PREAMBLE := START + CYCTYPE_DIR + CHANNEL + SIZE
DMA_R := DMA_PREAMBLE + (DATA + TAR + SYNC + TAR){1,2,4}
DMA_W := DMA_PREAMBLE + TAR + (SYNC + DATA){1,2,4} + TAR
```

Firmware Memory Read/Write

Read sizes supported: 1, 2, 4, 16, 128 bytes
Write sizes supported: 1, 2, 4 bytes

```
FIRMWARE_PREAMBLE := START + IDSEL + MADDR + MSIZE
FIRMWARE_R := FIRMWARE_PREAMBLE + TAR + SYNC + DATA{1,2,4,16,128} + TAR
FIRMWARE_W := FIRMWARE_PREAMBLE + DATA{1,2,4} + TAR + SYNC + TAR
```

Bus Master Memory Read/Write

Read sizes supported: 1, 2, 4 bytes
Write sizes supported: 1, 2, 4 bytes

```
BM_MEM_PREAMBLE := START + TAR + CYCTYPE_DIR + ADDR + SIZE
BM_MEM_R := BM_MEM_PREAMBLE + TAR + SYNC + DATA{1,2,4} + TAR
BM_MEM_W := BM_MEM_PREAMBLE + DATA{1,2,4} + TAR + SYNC + TAR
```

Bus Master I/O Read/Write

Read sizes supported: 1, 2, 4 bytes
Write sizes supported: 1, 2, 4 bytes

```
BM_IO_PREAMBLE := START + TAR + CYCTYPE_DIR + IO_ADDR + SIZE
BM_IO_R := BM_IO_PREAMBLE + TAR + SYNC + DATA{1,2,4} + TAR
BM_IO_W := BM_IO_PREAMBLE + DATA{1,2,4} + TAR + SYNC + TAR
```

CONCLUSION

This report provided a high level overview of the Low Pin Count (LPC) interface.

REFERENCES

[1] Intel® Low Pin Count (LPC) Interface Specification, August 2002, Revision 1.1: http://www.intel.com/design/chipsets/industry/25128901.pdf

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