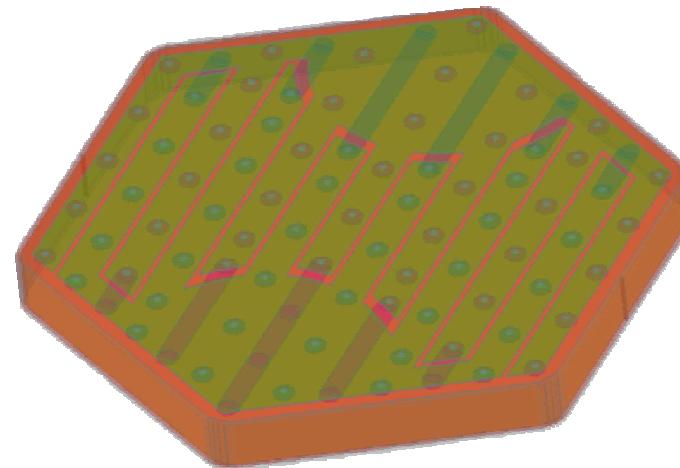
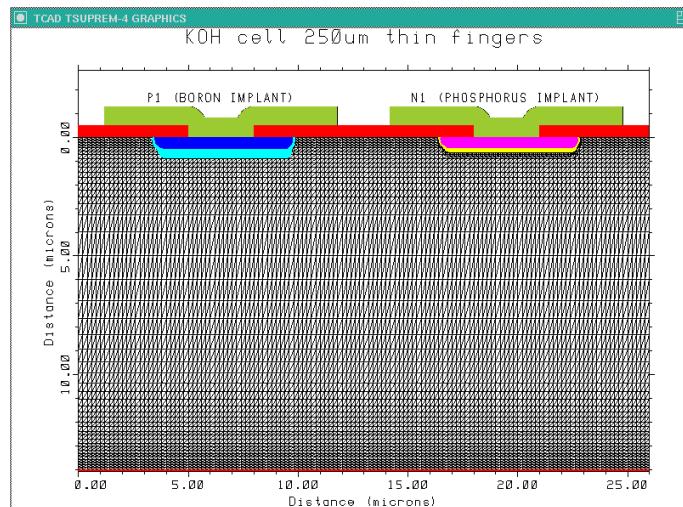


# Thin Crystalline Silicon Photovoltaics Simulations

## Sandia National Labs

**Jose Luis Cruz-Campa, Tammy Pluym, Paul Resnick, Ralph Young, Peggy Clews, Murat Okandan, Robert Grubbs, and Gregory N. Nielson**



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11.40 AM session Wednesday, November 4, 2009



# Background

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- Thin and small form factor photovoltaics could reduce the cost and improve the efficiency at the cell, module, and system levels [1,2]
- Back contact cell designs avoid grid shading and allow coplanar interconnection [3]. If textured, they are more tolerant to non-uniform and off normal cell illuminations [4]
- Diffusion length, surface recombination velocity, depth and concentration of the junction are crucial for back contact solar cells [5]
- Simulation work has been done up to dimensions of 100um in thickness and side dimensions of 400um. [3]

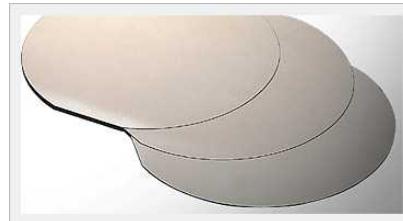
1. Gregory N. Nielson, Murat Okandan, Paul Resnick, Jose L. Cruz-Campa, Tammy Pluym, Peggy J. Clews, Elizabeth Steenbergen, Vipin P. Gupta "Microscale C-Si (C)PV Cells For Low-cost Power", presented at *IEEE PVSC*, Philadelphia, 2009
2. Nielson, G. N.; Okandan, M; Resnick. P. J.; Cruz-Campa, J. L.; Clews, P; Wanlass, M.; Sweatt, W. C.; Steenbergen, E.; Gupta, V. P., "Microscale PV Cells For Concentrated PV Applications", presented at the *EUPVSEC*, Germany, 2009
3. David D. Smith, "Review of Back Contact Silicon Solar Cells for low-cost Application", *SAND99-2025C Sandia National Laboratories*, Albuquerque, NM
4. William P. Mulligan, Akira Terao, David D. Smith, Pierre J. Verlinden, and Richard M. Swanson, "Development of chip-size silicon solar cells", *Conference record on the 28<sup>th</sup> IEEE photovoltaic Specialist conference*, pp 158-163, 2000
5. J.C. Pla , M.J.L. Tamasi, C.G. Bolzi, G.L. Venier, J.C. Duraan, "Short circuit current vs. cell thickness in solar cells under rear illumination: a direct evaluation of the diffusion length", *Solid-State Electronics* 44 (2000) 719-724

# Cost vs. Efficiency

## Current process



Full wafer  
300 $\mu$ m  
thick cells



Lift-off

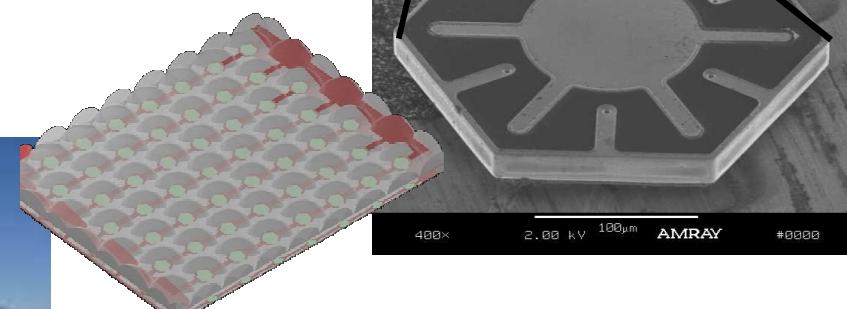
Sub  
millimeter  
14 $\mu$ m  
thick cells



## Our process



250 $\mu$ m  
wide cells

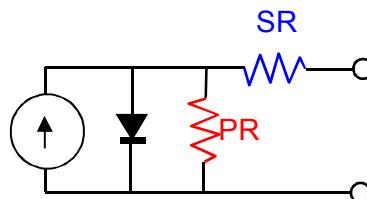


12% efficient  
modules

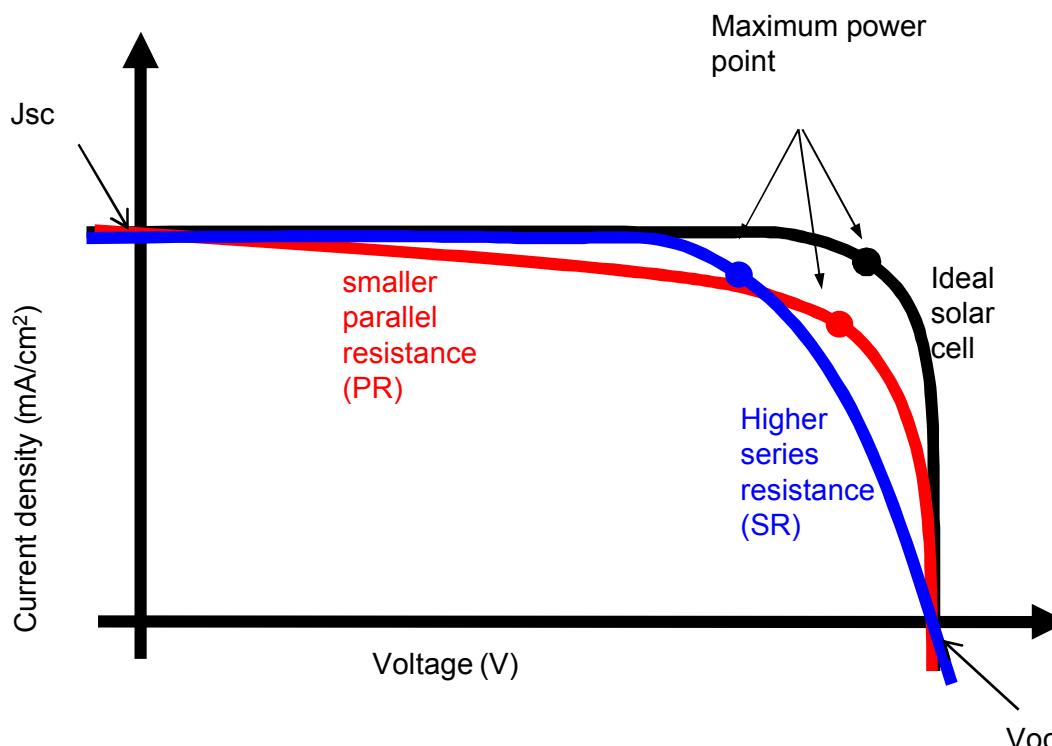


Inexpensive 22%  
efficient modules

# IV Characteristics



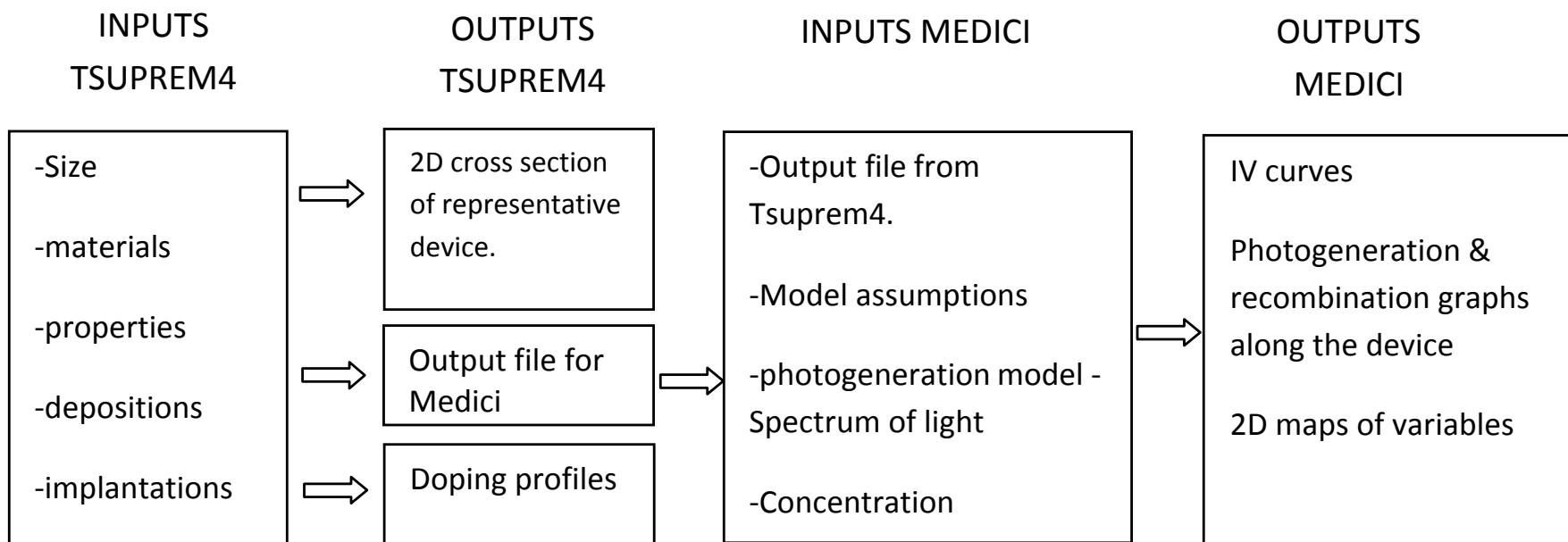
Equivalent circuit  
of a solar cell



J-V curve

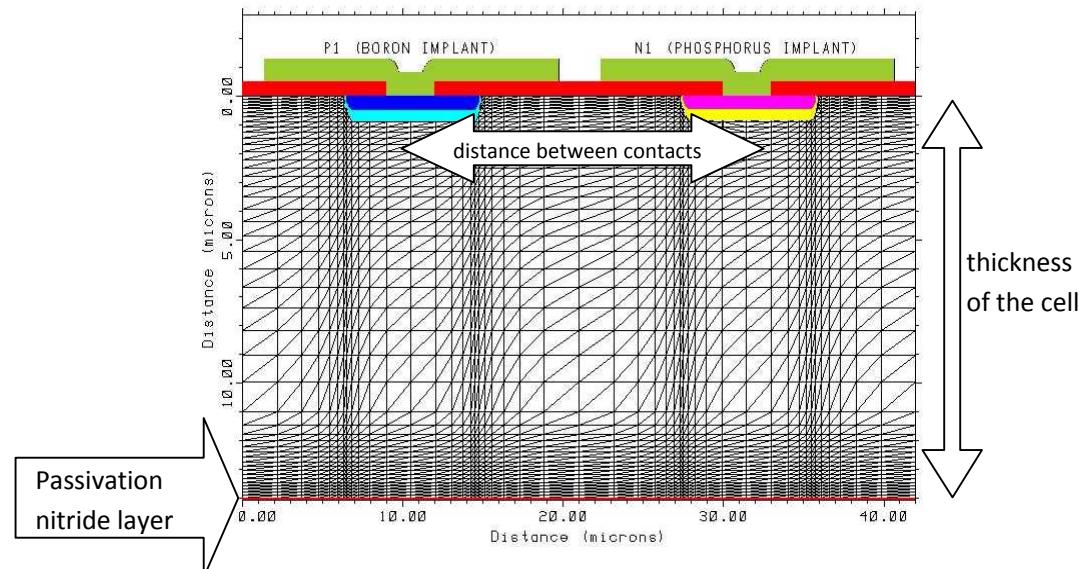
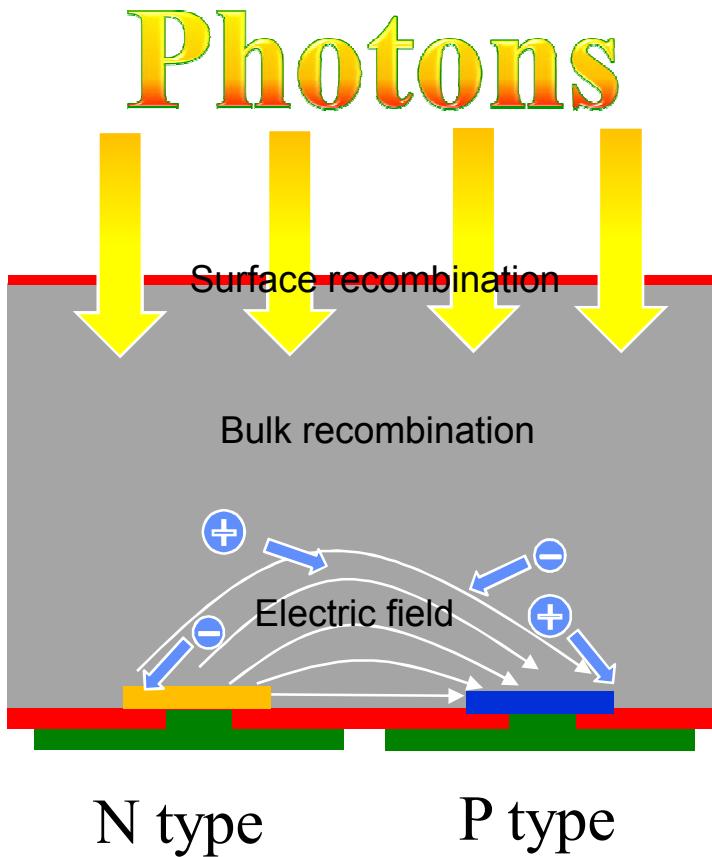
# Simulation On Devices

Purpose: see overall benefit and  
optimize design through  
simulations



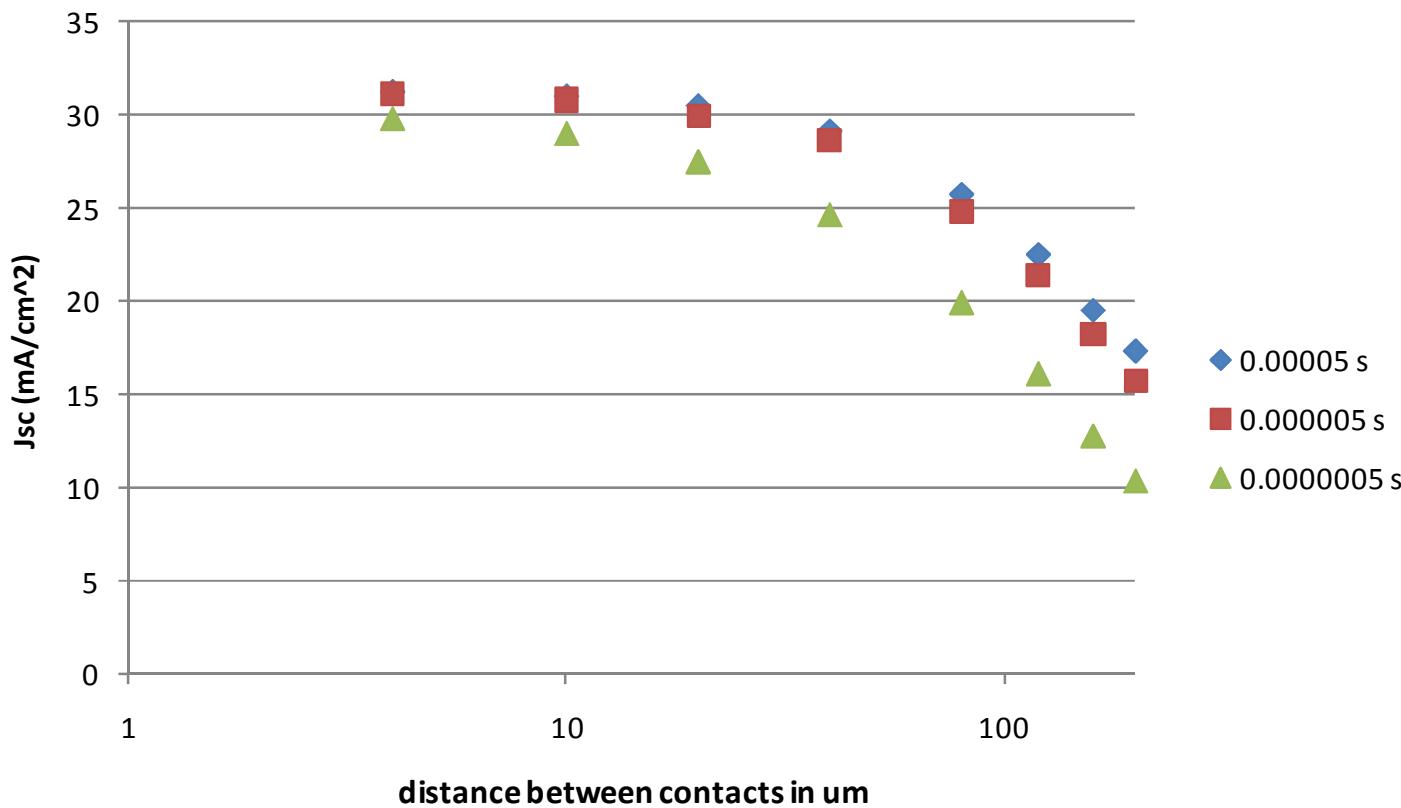
# 2D Device Simulations

- Simulation 1: effects of distance between contacts for different carrier lifetimes.
- Simulation 2: effects of thickness for different surface recombination velocities.



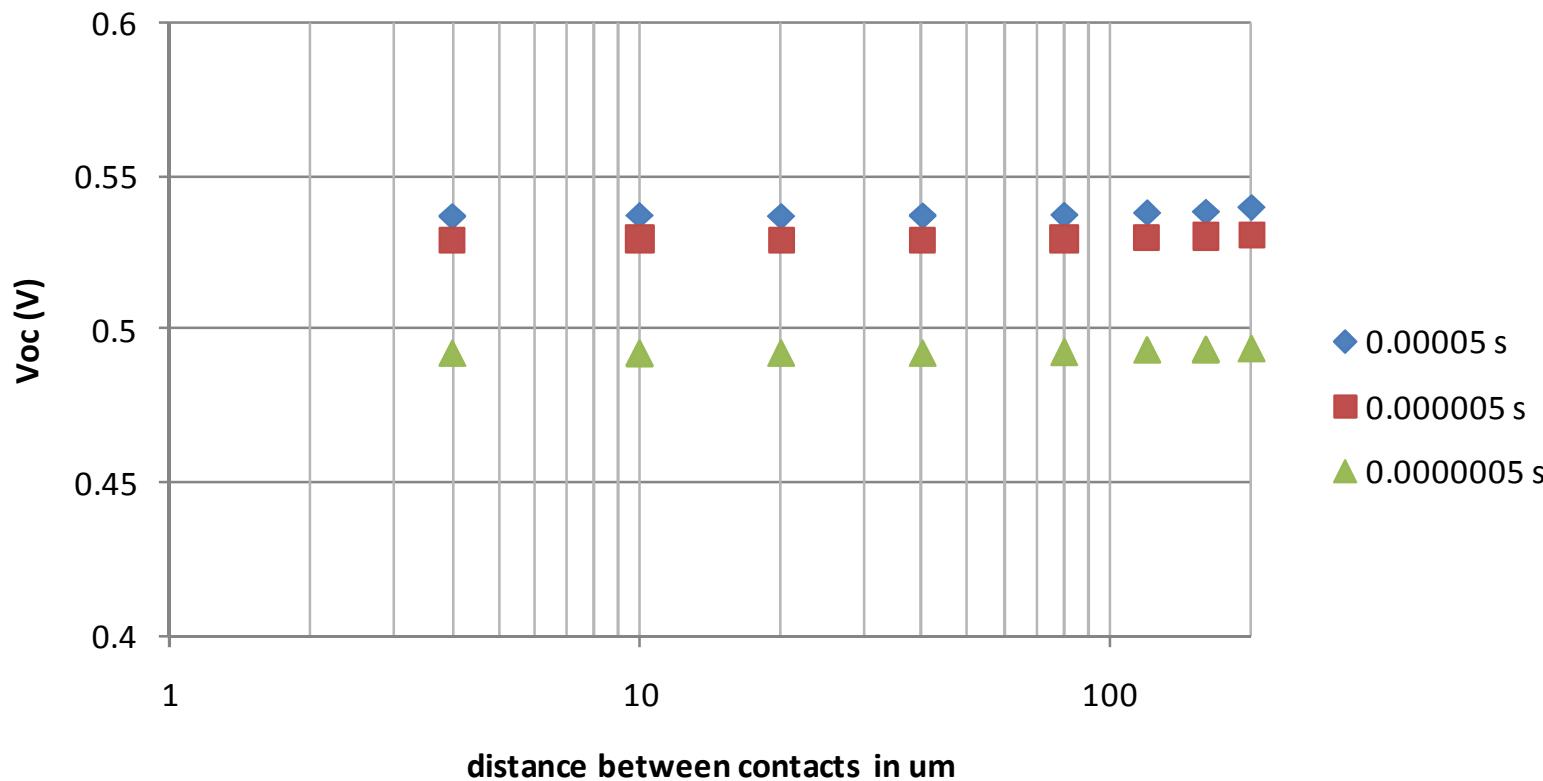
# Simulated Current Density

Current density vs. distance between contacts  
for different carrier lifetimes (14 um thick cell)



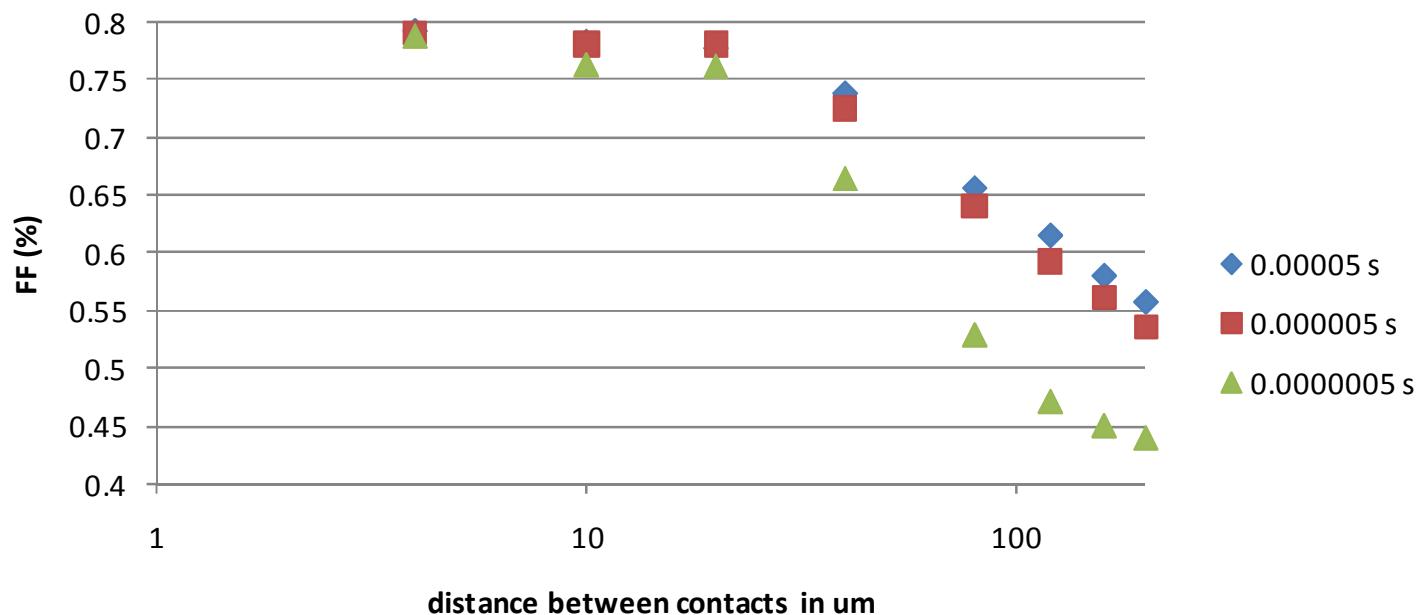
# Simulated Open Circuit Voltage

Voc vs. distance between contacts for different carrier lifetimes (14 um thick cell)

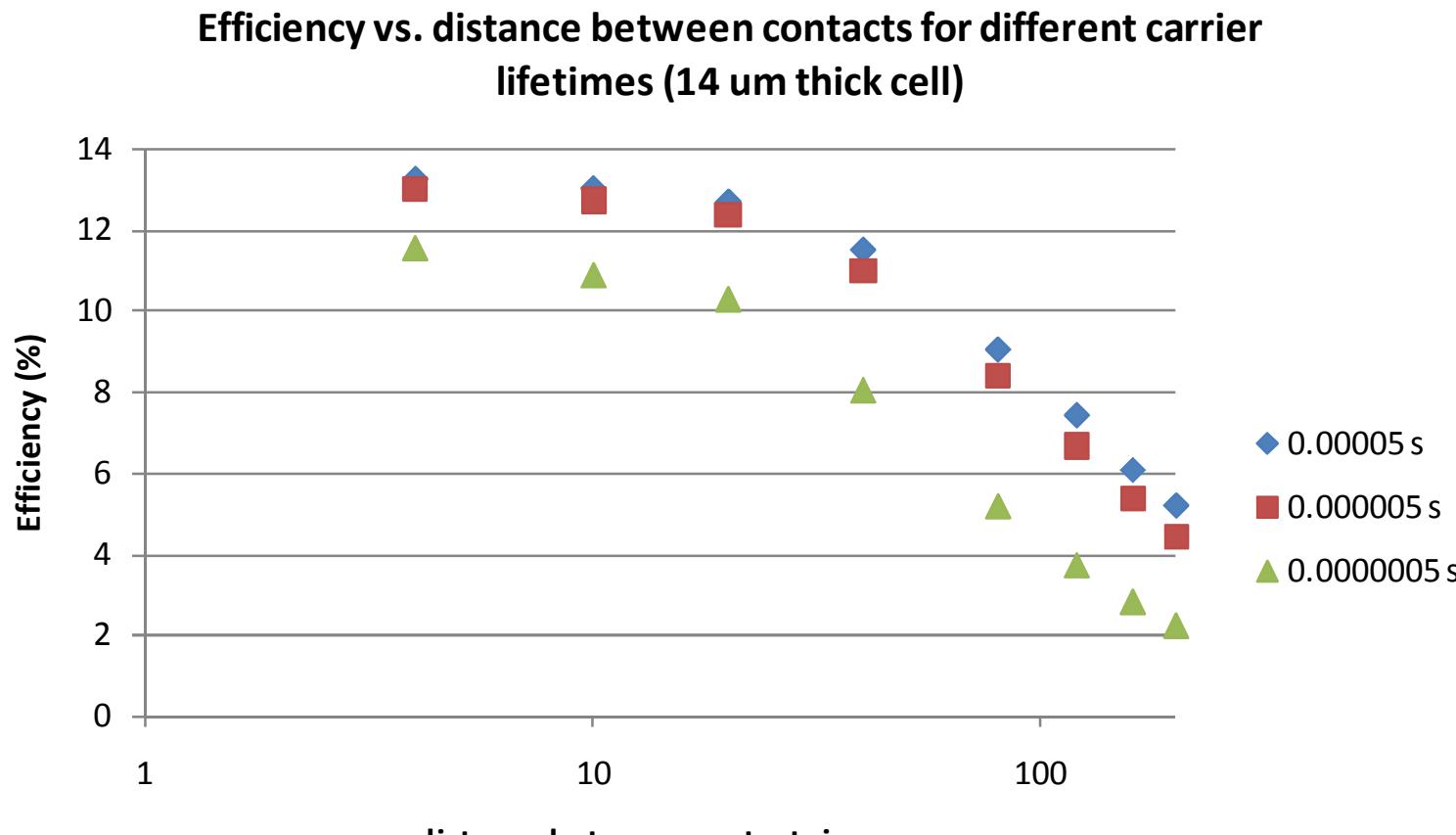


# Simulated Fill Factor

**Fill factor vs. distance between contacts for different carrier lifetimes (14 um thick cell)**

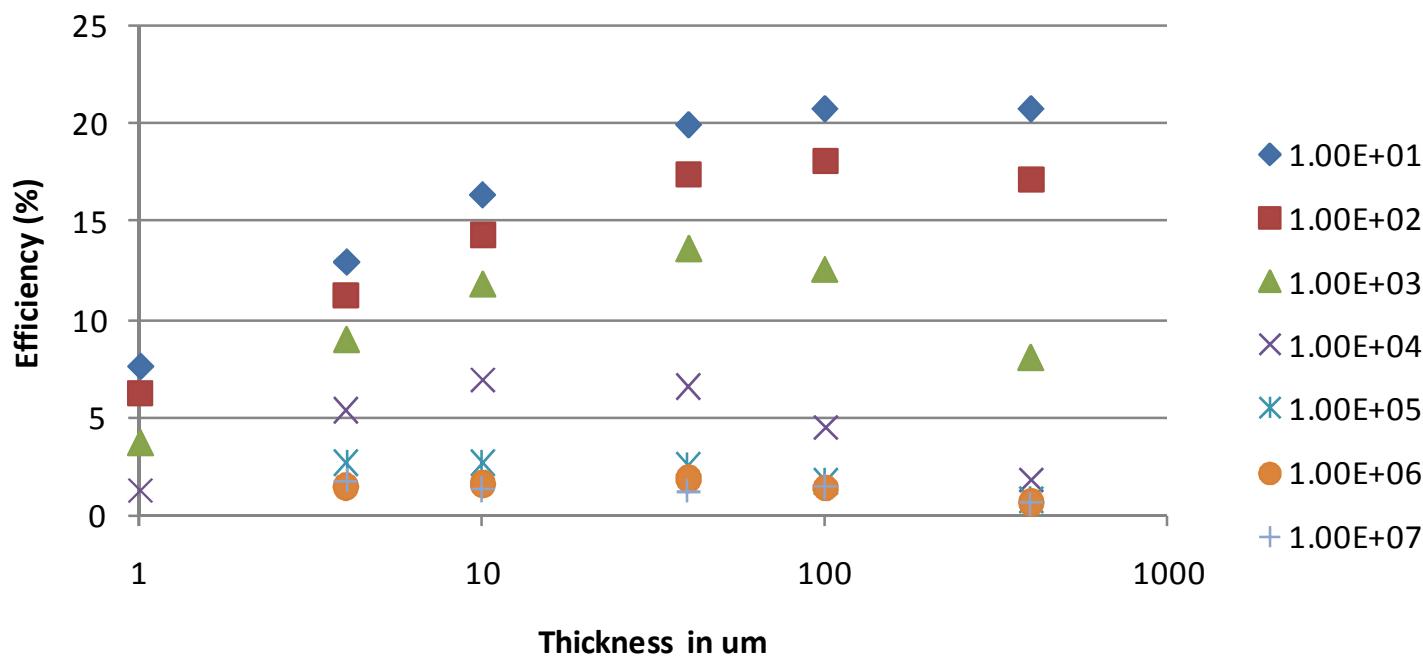


# Simulated Efficiency Vs. Distance



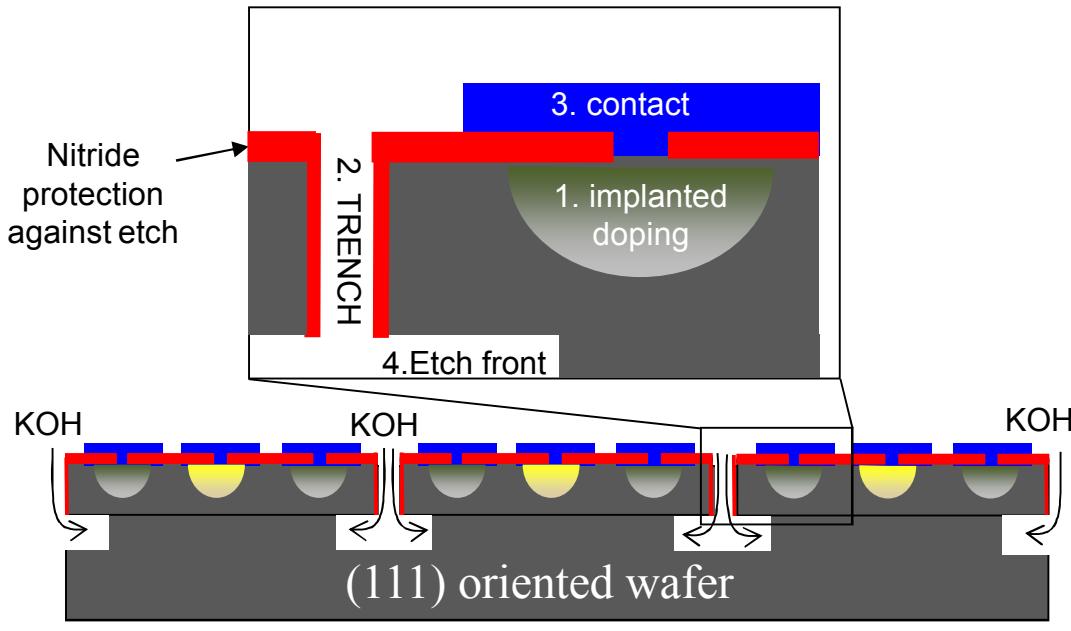
# Simulated Efficiency Vs. Thickness

## Efficiency vs. thickness for different surface recombination velocities



# Process: Reusable Wafer

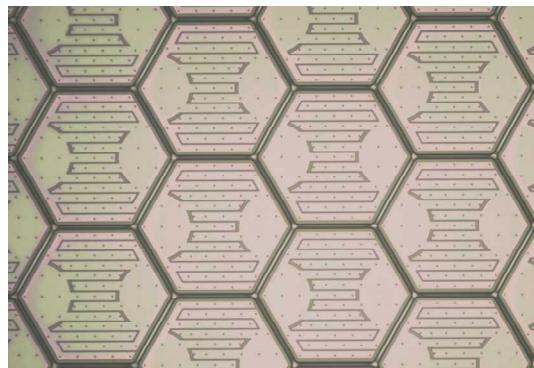
1. Boron and phosphorus implantations in a 111 oriented wafer and drive in step.
2. Trench to define the sides and depth of the cell coated with nitride.
3. Secondary etch creates the windows for the contacts. Another deeper etch is made to create an access point to the KOH chemistry.
4. Wafer is submerged in a KOH chemistry to detach the cells from the wafers.



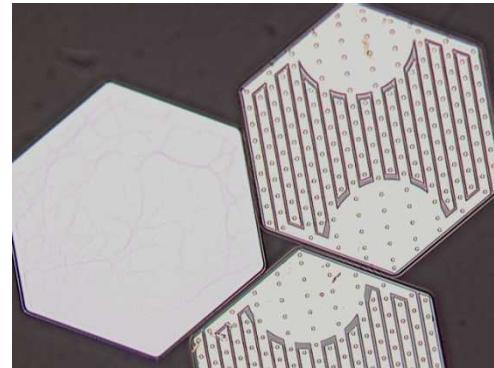
(111) Si wafer KOH Release

*Potassium Hydroxide enters in the gaps. The KOH will not etch either the plane parallel to the surface of the wafer nor the material enclosed by nitride. After some minutes, the whole cell will be detached from the substrate.*

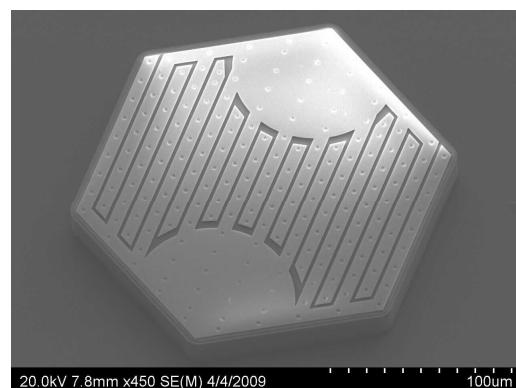
# Experimental Results...



Cells attached  
to the wafer

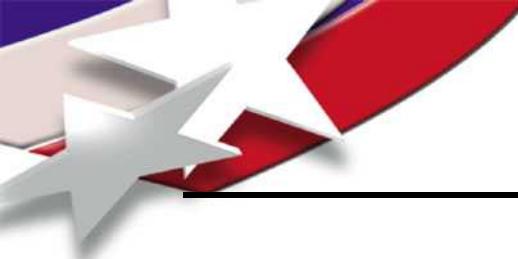


Released cells

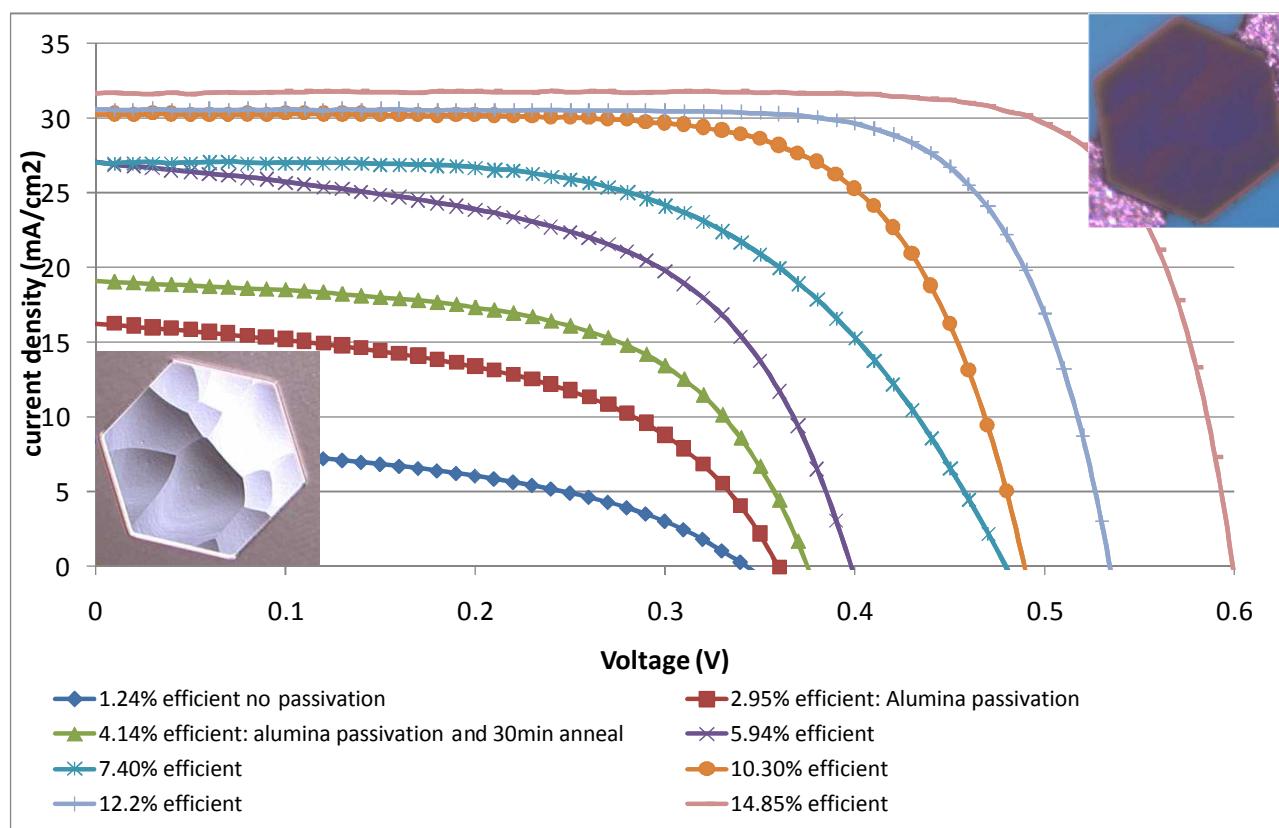


SEM of released cell

# Progress in passivation

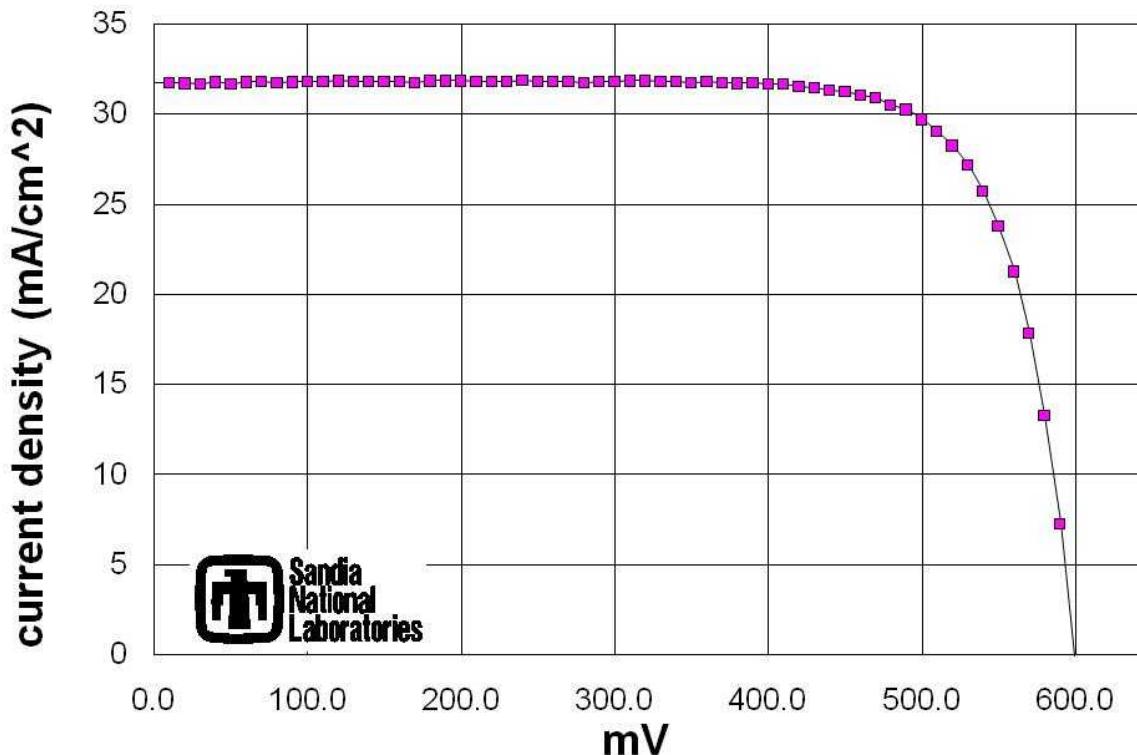


Before AR  
coat and  
passivation



After AR  
coat and  
passivation

# High Efficiency Cell





# Conclusions

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- Simulations demonstrate that really thin substrates < 20um are capable of absorbing a large fraction of the incoming light.
- Thin cell won't perform well if distance between contacts is too large (>100um); making the contacts close together in a thin structure collects carries more efficiently.
- Bulk recombination affects efficiency but becomes less important as the collection sites are closer together. This approach could use inexpensive, low quality silicon.
- The performance of the cell depends on the thickness of the wafer but thinner cells will use the material more efficiently.
- Surface passivation is crucial in these devices and depending on the quality of the passivation the same device could have efficiencies from 1% to 15%.