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Effects of Moisture on Radiation-Induced Degradation in CMOS SOI Transistors

M. R. Shaneyfelt, J. R. Schwank, P. E. Dodd, T. A. Hill, S. M. Dalton, and S. E. Swanson

Sandia National Laboratories, P.O. Box 5800, Albuquerque, NM 87185-1083

35 WORD ABSTRACT:

The effects of moisture on radiation-induced charge buildup in oxides of a 0.35-μm SOI technology are explored. The results are compared to previously published results on MOS technologies fabricated in the 1980s.

Corresponding (and Presenting) Author:

Marty Shaneyfelt, Sandia National Laboratories, P.O. Box 5800, Albuquerque, NM 87185-1083 (USA), phone: (505) 844-6137, fax: (505) 844-2991, email: shaneymr@sandia.gov

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I. INTRODUCTION

Previous work has explored the effects of moisture exposure on radiation-induced degradation of both MOS transistors and ICs fabricated in older technologies (e.g., vintage mid-1980s with gate lengths of 2 μm and larger) [1-3]. Results of these works have shown some impact of moisture exposure on radiation hardness and have suggested that moisture-related aging effects can be important for electronic systems in radiation environments. For example, for transistors exposed to moisture (water vapor) at elevated temperatures before irradiation, the magnitudes of n-channel gate oxide voltage shifts post-irradiation were larger than those of transistors not exposed to moisture [1,3]. For these transistors, it was also shown that the magnitude of the degradation was dependent on the transistor gate channel length; the magnitude of degradation increased with decreasing channel length. This result suggests that the degradation was associated with a diffusion-limited process, i.e., the longer the time and the shorter the distance H_2O has to diffuse, the bigger the effect. This of course raises concerns about how much degradation might be observed in advanced technologies with much shorter channel lengths. Previous work also showed extremely large gate oxide voltage shifts for p-channel transistors exposed to moisture pre-irradiation [3]. These p-channel voltage shifts are large enough to lead to enhanced parametric degradation and lower the functional failure dose of ICs. Large increases in radiation-induced charge buildup in parasitic field oxides were also observed in devices exposed to moisture [3].

In this work, we explore the effects of moisture exposure on radiation-induced charge buildup in oxides of a more advanced 0.35-μm SOI IC technology. Transistors were exposed to water vapor using highly accelerated stress tests (HAST) and then their radiation response was characterized.

II. EXPERIMENTAL DETAILS

The transistors used for this work were fabricated at Sandia National Laboratories in the CMOS7 silicon-on-insulator (SOI) technology. The gate length of transistors in this technology is nominally 0.35 μm. However, for this work, transistors with gate lengths from 0.35 to 10 μm were examined. This technology uses the BUSFET transistor to mitigate the effects of radiation-induced charge buildup in the SOI buried oxide on transistor performance [4]. To examine the effects of moisture exposure on radiation-induced charge buildup in the buried oxide, special non-BUSFET transistors were also fabricated. With these special non-BUSFET structures, at high total dose levels, transistor degradation can occur due to radiation-induced charge buildup in the gate and field oxides, and in the SOI buried oxide. To determine the effects of moisture exposure on radiation-induced charge buildup in gate oxides, the threshold voltage shifts in p-channel transistors were monitored (charge buildup in the field and buried oxide to not impact the IV characteristics of p-channel transistors). To determine the effects of moisture exposure on radiation-induced charge buildup in parasitic field oxides, n-channel BUSFET transistor leakage current, I_{DS}, at a gate-to-source voltage, V_{GS}, of zero volts was monitored. Using the BUSFET transistors eliminated any potential for radiation-induced charge buildup in the buried oxide from impacting I_{DS} @ V_{GS} = 0 V. To determine the effects of moisture exposure on radiation-induced charge buildup in the buried oxide, the back-gate transistor voltage shift was monitored. The back-gate transistor consists of the silicon wafer (back gate) and the source and drain of the top gate transistor.

All transistors were characterized at the wafer level on transistors from the same wafer using standard I-V charge separation techniques before and after HAST exposure and irradiation. The HAST exposures were performed at 85% relative humidity, at a temperature of 130°C, and for times up to 3 weeks. The 1-week HAST exposures are consistent with times specified by JEDEC Standard No: 22-A100 for HAST exposure of plastic encapsulated microcircuits. The HAST exposures were performed at the wafer level. The 3-week HAST exposures are presently being conducted and results will be reported in the full paper. To characterize the radiation response as a function of total dose, transistors were irradiated at the wafer level using an ARACOR Model 4100 Semiconductor X-ray Irradiator. All

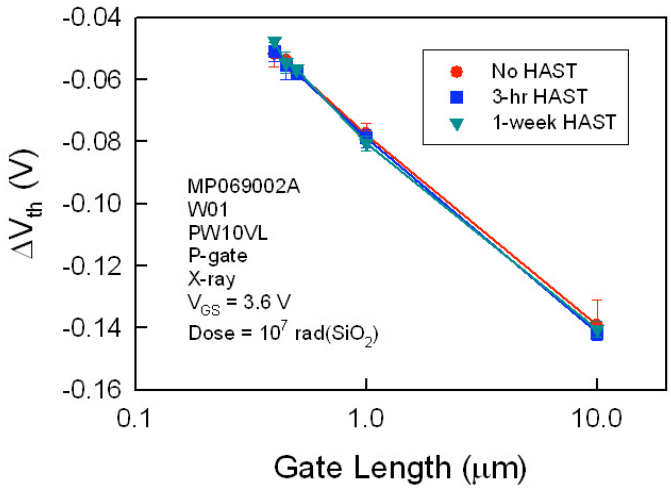

Figure 1: Threshold voltage shift versus gate length for p-channel transistors irradiated to 10^7 rad(SiO_2) with V_{GS} = 3.6 V for transistors not exposed to HAST and for transistors exposed to HAST for 3 hours or 1 week.

irradiations were performed at room temperature. A dose rate of 1667 rad(SiO_2) was used for the x-ray irradiations. The data points shown in the figures are the averages and maximum and minimum values for the transistors evaluated.

III. Experimental Result

Figure 1 is a plot of the threshold voltage shift, ΔV_{th}, of p-channel transistors after irradiation to a total dose of 10 Mrad(SiO_2) with V_{GS} = 3.6 V (source and drain grounded) for transistor gate lengths from 0.4 to 10 μm. Data are shown for transistors that were not exposed to HAST and for transistors exposed to HAST for 3 hours and for 1 week. For p-channel transistors, radiation-induced charge buildup in parasitic field oxides and in the buried oxide is not important and the threshold voltage shift is due entirely to radiation-induced charge buildup in the gate oxides. Although the amount of threshold voltage shift varies with gate length as might be expected [5,6], there is no observable difference in the amount of threshold voltage shift for the transistors not exposed to HAST or for the transistors exposed to HAST for times of 3 hours or 1 week. These data are considerably different than that observed previously in older technologies [3]. For similar HAST conditions, HAST exposure led to very large threshold voltage shifts for the older p-channel transistors [3].

Figure 2 is a plot of I_{DS} @ V_{GS} = 0 V for n-channel BUSFET transistors versus total dose irradiated with V_{GS} = 0 V. As mentioned above, increases in I_{DS} @ V_{GS} = 0 V are due to radiation-induced charge buildup in parasitic field oxides for these transistors and radiation conditions. Data are shown for transistors that were not exposed to HAST and for transistors exposed to HAST for 3 hours, 1 day, and 1 week. As is normally observed, I_{DS} @ V_{GS} = 0 V increases with total dose due to a buildup of radiation-induced oxide-trapped charge in parasitic field oxides. At very high total dose levels, I_{DS} @ V_{GS} = 0 V appears to saturate or decrease with total dose as the radiation-induced buildup of interface traps becomes significant compared to the amount of radiation-induced oxide-trapped charge buildup. However, within experimental uncertainty, HAST exposure has no significant impact on I_{DS} @ V_{GS} = 0 V at

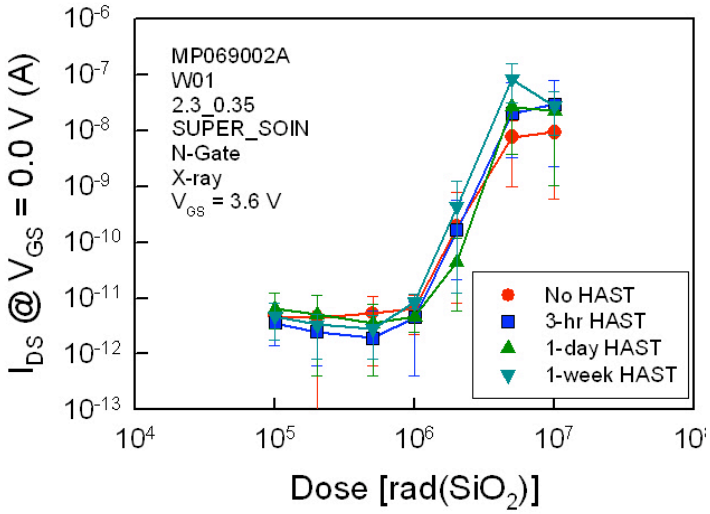

Figure 2: I_{DS} @ V_{GS} = 0 V versus total dose for n-channel transistors irradiated to 10^7 rad(SiO_2) with V_{GS} = 3.6 V for transistors not exposed to HAST and for transistors exposed to HAST for 3 hours, 1 day, or 1 week.

any total dose level. These data suggest that HAST exposure does not significantly affect the amount of radiation-induced buildup of oxide-trapped charge or interface-trap charge in parasitic field oxides. Similar to that for radiation-induced charge buildup in gate oxides, these results are contrary to previous results obtained on much older technologies [3].

Figure 3 is a plot of the back-gate threshold voltage shift, $\Delta V_{th\text{-}bg}$, for n-channel transistors irradiated with a source and drain voltage of 3.6 V and with V_{GS} = 0 V versus total dose. These bias conditions (typical of that for a pass-gate transistor) have been determined to be worst case for radiation-induced charge buildup in buried oxides [7,8]. Data are shown for transistors that were not exposed to HAST and for transistors exposed to HAST for 3 hours, 1 day, and 1 week. As mentioned above, increases in $\Delta V_{th\text{-}bg}$ are due to radiation-induced charge buildup in the buried oxide. Within experimental uncertainty, there is no difference in the radiation-induced charge buildup in the buried oxide for transistors that were not exposed to HAST and for transistors exposed to HAST. Previous work on older technologies did not investigate the effects of moisture exposure on radiation-induced charge buildup in SOI buried oxides. Hence, these are the first results for the effects of moisture exposure on radiation-induced charge buildup in SOI buried oxides.

IV. Discussion

The results of Figures 1-3 show no observable effects of moisture-related aging on radiation hardness. These results are in contrast to those of previous work performed on older technologies [1-3]. The mechanisms for the differences in this work and in previous work are under investigation. One possible reason for these differences could be associated with the final chip passivation layers used. Unlike the Sandia devices examined in the previous work, which used doped glasses as the final passivation layer, the SOI transistors examined in this work used a nitride final passivation layer. It is well known that nitride passivation layers are excellent barriers to moisture diffusion and are commonly used for devices packaged in plastic packages [9]. However, this explanation is not consistent with previous data taken on OKI p-channel transistors from a 2-μm commercial technology fabricated in the mid 1980s that also used a nitride passivation layer [3]. For the OKI transistors, moisture exposure degraded the radiation response of the transistors. In this case, it was speculated that moisture most likely diffused through surface regions not covered by nitride [3]. In addition to the final passivation layer, several other process differences could lead to differences on the effects of moisture on radiation hardness between this SOI technology and the technologies fabricated in the 1980s. These include the use of different implant materials (e.g., arsenic) and thicker overlayers (the SOI technology has five levels of metallization vs. one layer of metallization used for the 1980s technologies). For example, the different implant materials could affect the diffusion of impurities into gate oxides and subsequently the buildup of radiation-induced oxide traps as suggested in Ref. [3]. Thicker overlayers will increase the distance H_2O has to diffuse to reach the gate oxides and hence, substantially longer moisture exposure times might be required

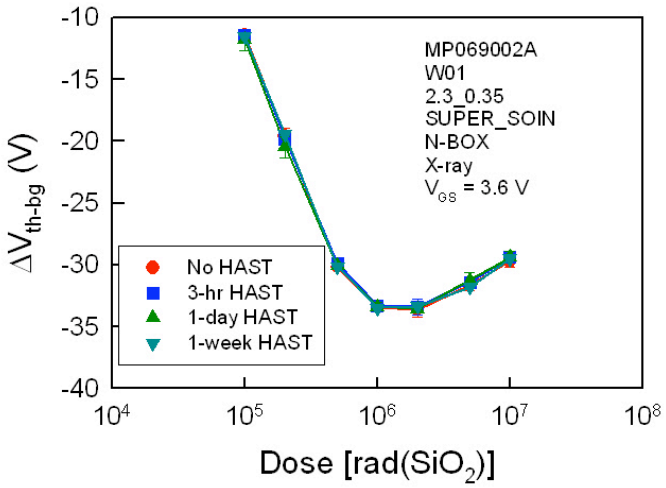

Figure 3: $V_{th\text{-}bg}$ versus total dose for n-channel transistors irradiated to 10^7 rad(SiO_2) with the source and drain at 3.6 V and V_{GS} = 0 V for transistors not exposed to HAST and for transistors exposed to HAST for 3 hours, 1 day, or 1 week.

to observe similar effects. More work needs to be performed to establish the mechanisms for the observed differences in the older and newer technologies and to determine if other new technologies might be impacted by moisture exposure and thus, may be susceptible to aging effects.

V. SUMMARY

Both n- and p-channel SOI transistors were exposed to moisture prior to irradiation. The results show no observable effects of moisture-related aging on radiation hardness, in contrast with previously published results on bulk MOS technologies fabricated in the 1980s [1-3]. This suggests that the process technology used to fabricate the more advanced SOI technology has reduced or eliminated the effects of moisture on radiation hardness. While only one technology (the SOI technology) was examined as representative of a new technology in this work, whether or not moisture exposure has an impact on the radiation hardness of other present day SOI and bulk CMOS technologies is not known. In any case, our SOI technology results indicate that not all advanced technologies are necessarily susceptible to significant long-term radiation-induced aging effects related to moisture exposures.

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