SAND2009-6083C

DARPA/OSD Trusted Foundry Circuit Designers Workshop

Sandia's Trusted Foundry Experience

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Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND2009-0357P

Sandia National Laboratories

Topics

- Sandia and Microsystems Technology and Science Center
- Trusted Foundry Design Experience and Examples
- Trusted Foundry Program Feedback

Sandia National Laboratories and Microsystems Technology and Science Center Overview

Sandia National Laboratories

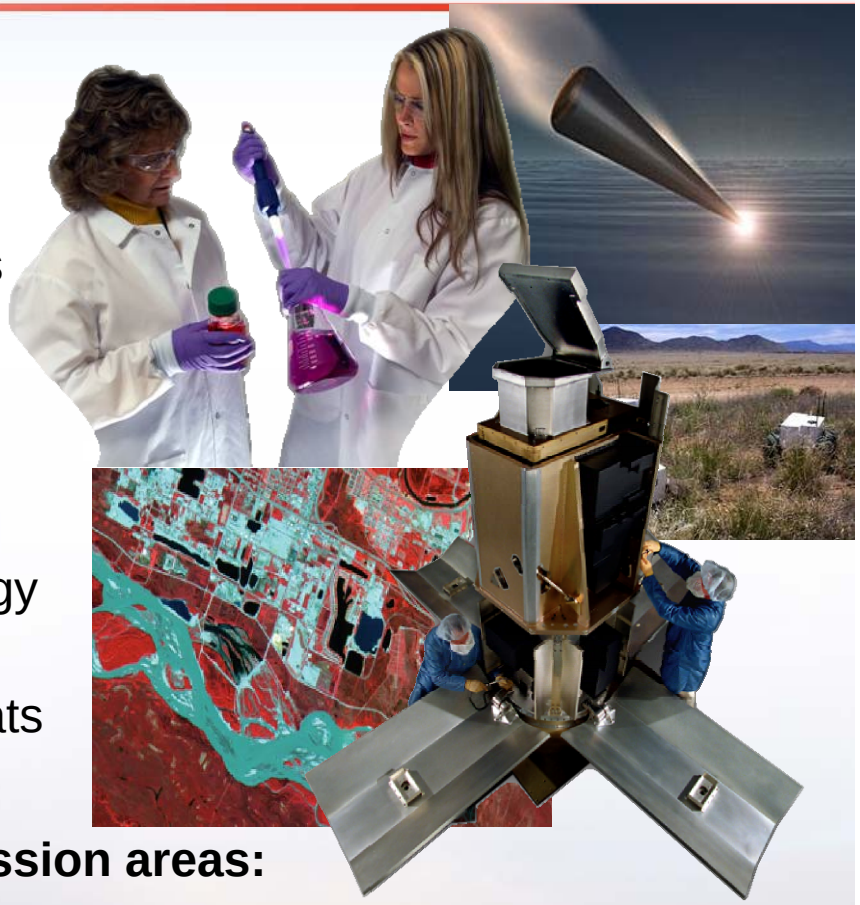
Our Business: National Security

- **Core purpose**
  - to help our nation secure a peaceful and free world through technology
- **Highest goal**
  - to become the laboratory that the United States turns to first for technology solutions to the most challenging problems that threaten peace and freedom for our nation and the globe

Sandia National Laboratories

Technologies for National Security

- **We develop technologies to:**
  - Sustain, modernize and protect our nuclear arsenal
  - Prevent the spread of weapons of mass destruction
  - Provide new capabilities to our armed forces
  - Protect our national infrastructures
  - Ensure the stability of our nation's energy and water supplies.
  - Defend our nation against terrorist threats



- **In four primary mission areas:**
  - Nuclear Weapons
  - Defense Systems & Assessments
  - Energy, Resources & Nonproliferation
  - Homeland Security and Defense

Sandia's Administration

- AT&T: 1949–1993
- Martin Marietta: 1993–1995
- Lockheed Martin: 1995–Present

Government-Owned Contractor-Operated (GOCO)

Federally Funded Research & Development Center (FFRDC)

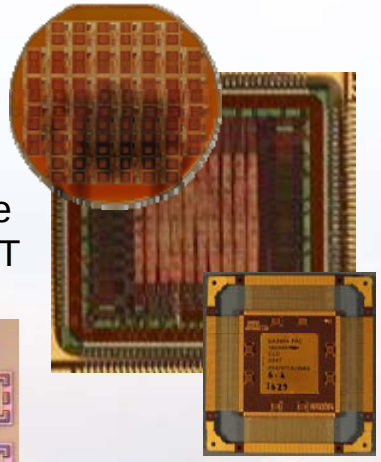
Microsystems Technology and Science Center provides micro products & leading edge R&D

Our customer base includes:

Intelligence Community

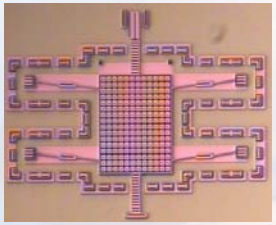
Our product deliveries include:

Neutron-immune QASPR III-V HBT Transistors



AF&S Controller
(No bid from commercial suppliers)

NUDET Sensors for satellite payloads
(2000:1 size reduction)



MEMS Shock Sensor

MicroChemLab-based Sensor systems

Our Unique R&D Capabilities Transform Concepts to Products

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IBM Trusted Foundry Design Experience & Examples

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Sandia was one of the 1st users of the IBM Trusted Foundry and is a heavy user

- **Sandia was one of the 1st users of the IBM Trusted Foundry**
  - Helped IBM and TAPO define process for using IBM Trusted Foundry
  - One of the heaviest government users fabricating several integrated circuits via Trusted Access Program Office (TAPO) at several process nodes (180nm down to 65nm CMOS; 250nm and 180nm SiGe)
  - Driver behind IBM getting on-shore embedded non-volatile memory (Flash)
- **Sandia IBM Trusted Foundry Tapeout History**
  - FY07 Tapeouts
    - 6 at IBM CMOS8RF, 130nm technology
    - 1 at IBM CMOS9LP, 90nm technology
  - FY08 Tapeouts
    - 7 at IBM CMOS8RF, 130nm technology
    - 1 at IBM CMOS9LP, 90nm technology
  - FY09 Tapeouts
    - 4 at IBM CMOS8RF, 130nm technology
    - 4 at IBM CMOS9LP/SF, 90nm technology
    - 1 at IBM CMOS10SF, 65nm technology
  - FY10 Projected Tapeouts
    - 3 at IBM CMOS8RF, 130nm technology
    - 3 at IBM CMOS9LP/SF, 90nm technology
    - 1 at IBM CMOS10SF, 65nm technology
    - 1 at IBM CMOS12SOI, 45nm technology

TAPO

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IBM

Key Data Processor

- ***Program Description***

  The Key Data Processor is a generic System-On-a-Chip processor system that is designed to securely host the cryptographic algorithms that ensure the integrity, availability and confidentiality of the Military GPS for the Selective Availability Anti-Spoofing Module (SAASM).

- ***Program Goal***

  The KDP goal is to provide a secure, NSA-certified Hard Cell solution for integration into a single-chip SAASM or other security applications. The KDP design can host a wide variety of field-programmable application software packages.

- ***Program Sponsor***
  - *Department of Defense*

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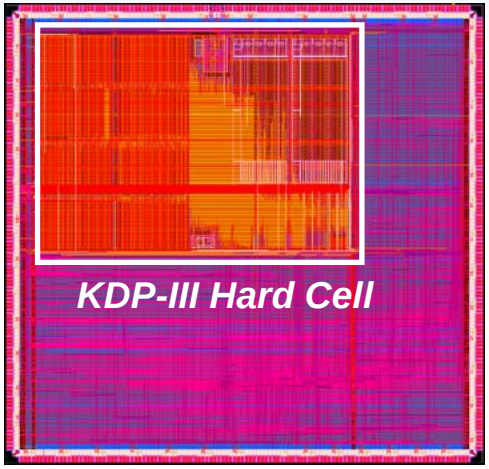
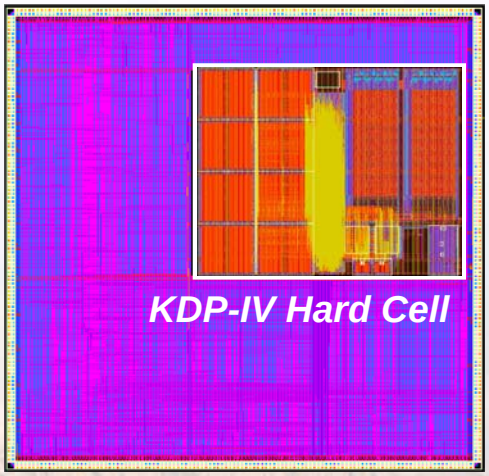
KDP-III and KDP-IV Test Chips

- **Project Features**

	KDP-III	KDP-IV
IBM Process:	CMOS 8RF	CMOS 9LP
Feature size:	130 nm	90 nm
Design size:	24.8 mm^2	19.4 mm^2
Operating conditions:	-55ºC to 125ºC 1.5V ±10%	-55ºC to 125ºC 1.5V ±10%
Gate count:	3.6M	7.2M
Power:	62-200 mA	20-80 mA
Frequency:	48 MHz	48 MHz
Package:	388 PBGA	388 PBGA



KDP-III Instance Test Chip



KDP-IV Instance Test Chip

Bottlecap Program

- ***Program Description***

  Develop and fabricate a set of test characterization vehicles (TCVs) in the IBM 130nm technology (8RF) that

  - *allows for the assessment of the basic technology elements and*
  - allows for the characterization of the reliability and repeatability of measured electrical parameters.

- ***Program Goal***

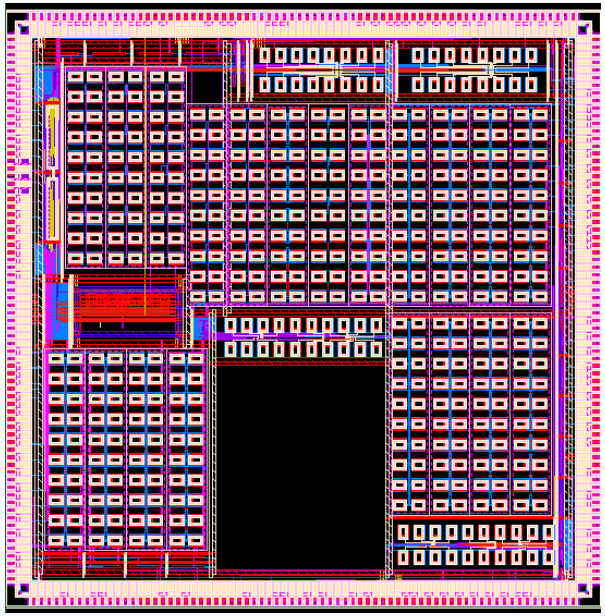
  Enable the trusted design community to develop better assessment methods in the following areas of interest:

  - Fundamental device responses to various stimulus.
  - Device behavior in various circuit topologies including those that typically apply to amplifier gain-bandwidth and basic gate response.

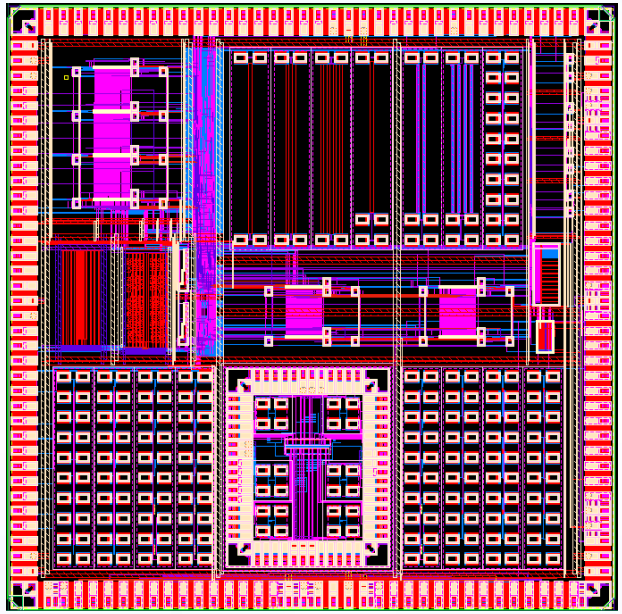
- ***Program Sponsor***

  - *Department of Defense*

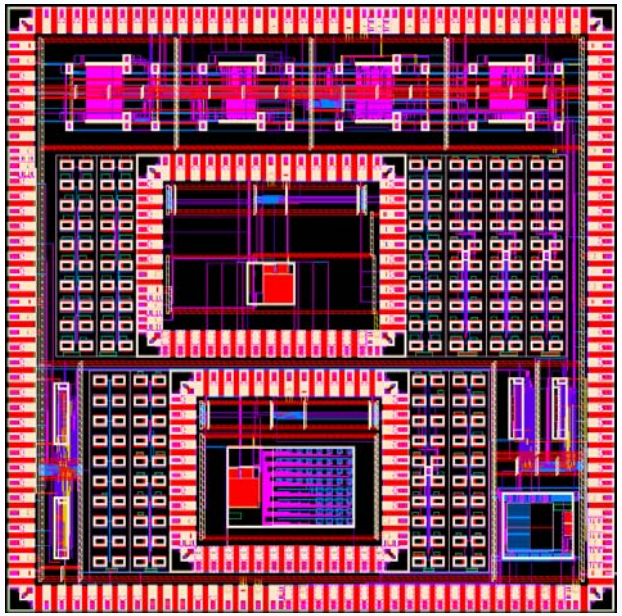
Bottlecap Testchips



- **BCTC1**
  - 8RF09B
  - Artisan RA1SHD, 16k x 8
  - EFUSE, 128 bits
  - Basic analog functions
  - Basic digital functions



- **BCTC2**
  - 8RF09C
  - Artisan RA1SHD, 16k x 8
  - Custom SRAM, 128 x 8
  - Voltage amplifiers
    - High power
    - High bandwidth
  - 3.3V combinatorial logic



- **BCTC3**
  - 8RF09D
  - Mature analog circuits with digital control
    - EFUSE, 128 bits
    - RF oscillators
    - Analog to digital converters
    - Voltage comparators

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Silicon MicroPhotonic Backplane

- ***Program Description***

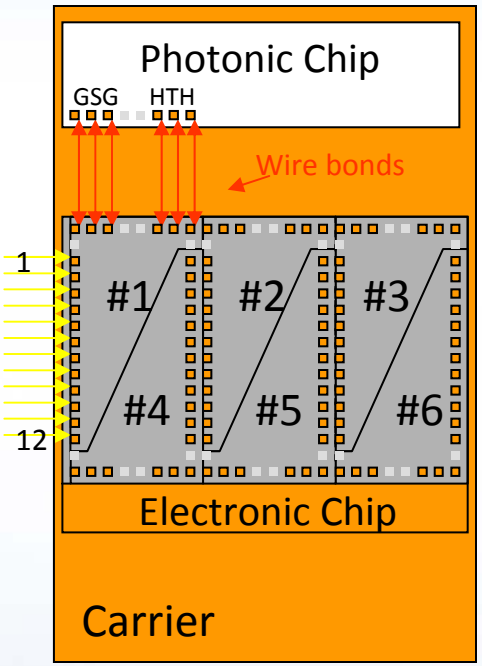
  Research and development program to provide high speed optical modulator driver and temperature sensing and control circuits for silicon photonic interconnects. Applications include communications from FPAs as well as intra-computer communications

- ***Program Goal***

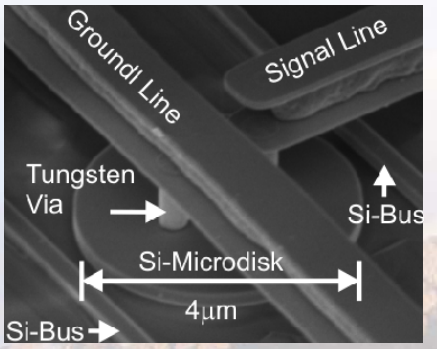
  The goal of the program is to demonstrate the integration of high speed optical modulator driver and temperature sensing and control circuits with low-energy silicon photonic optical modulators. The photonic interconnect has the potential to drastically reduce the power dissipation for high speed interconnections within digital systems.

- ***Program Sponsor***
  - *Internal Laboratory Directed Research and Development Program*
  - *DARPA*

MircoPhotonic Prototype Control Chip



- Drive electronics designed to drive two versions of a microphotonic modulator at 10 Gb/s. Psuedo-random bit-stream generator integrated with various versions of the drive electronics.
- Temperature control design is an analog control loop using multiple amplifiers to control the temperature of the modulator. Control loop uses feedback from a sensor to accurately control the temperature of the modulator.
- Process: IBM 90nm Process (CMOS9SF)
- Supplies: 1.2V and 3.3V Core, with 3.3v I/O

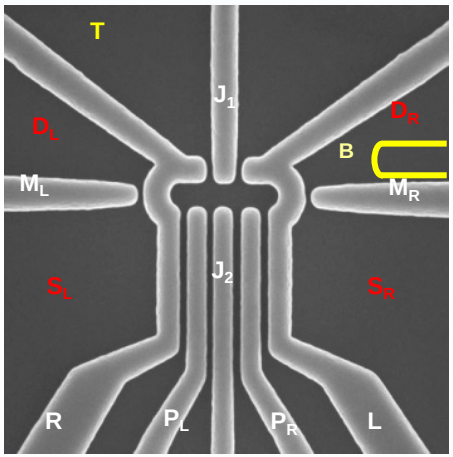


- Microphotonic modulators (shown on left) were developed in Sandia's trusted foundry
  - 0.35um custom process

Quantum Information Science & Technology (QIST) Grand Challenge

- ***Program Description***

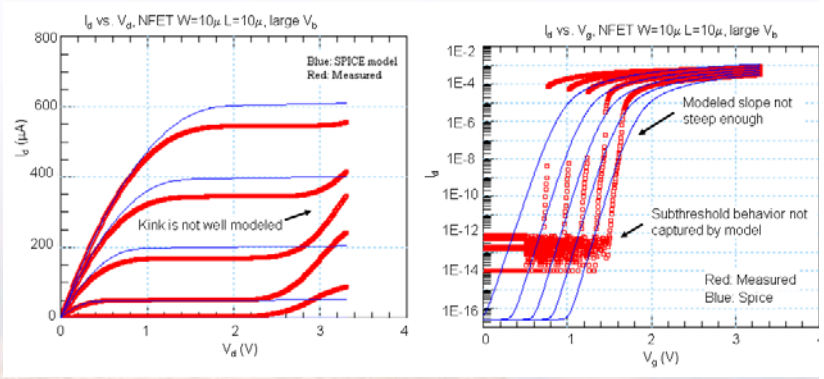
  A mutli-pronged research and development effort to develop a single silicon double quantum dot depletion qubit (Si DQD qubit) as well as design a logical qubit.



- ***Program Goal***

  Develop architectures, modeling, and cryogenic electronics to support Si DQD qubit effort.

  - Evaluate advanced process nodes at cryogenic temperatures (4K & 100mK).
  - Design control circuits to operate at cryogenic temperatures in support of physics experiments.



- ***Program Sponsor***
  - *Internal Laboratory Directed Research and Development Program*
  - *Department of Defense*

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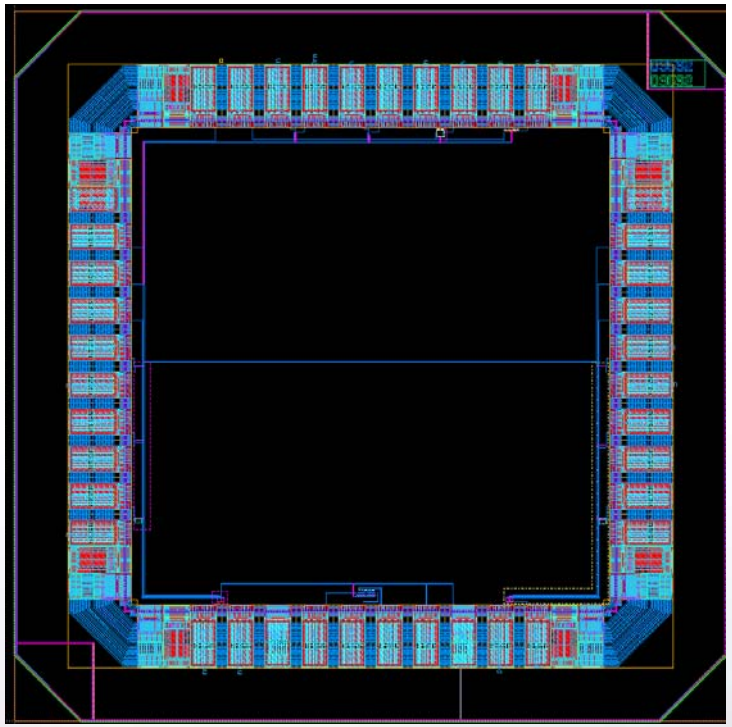
QIST Prototype Chip

- **Transistors for characterization at 4K and 100mK**
  - Nmos & Pmos devices
  - Nmos 0 threshold devices
- **Current Amplifier to assist with quantum state read-out.**
  - Gain: 125
  - MHz bandwidth
  - Amplify very small signals (10's-100's pA)
- **IBM Process:**
  - 65nm tapeout (10SF)
  - 45nm tapeout planned in May 2010.
- **IP: Aragio Wirebond Pads**
- **Status: Awaiting parts for test and evaluation**
- **Devices also fabricated at Sandia's Trusted Foundry**
  - Devices tested at 4K



Focal Plane Array Grand Challenge (FPAGC)

- ***Program Description***

  A research & development effort to develop new focal plane array architectures, and the key enabling technologies, to provide very high pixel count focal plane arrays characteristic of full framing imagers, with the speed, efficient data reduction, and power efficiency of event-driven designs.

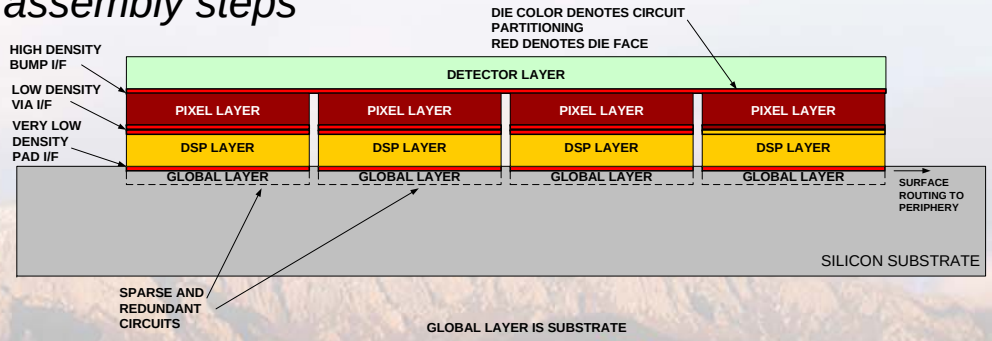
- ***Program Goal***

  The FPAGC goal is to prove the necessary components and technology to build a modular, 4-side abuttable, 3D stacked design.

  - *A 2D testchip to prove circuit architecture and performance*
  - *A 3D testchip to prove process and assembly steps*

- ***Program Sponsor***

  - *Laboratory Directed Research and Development Program*
  - *Department of Defense*



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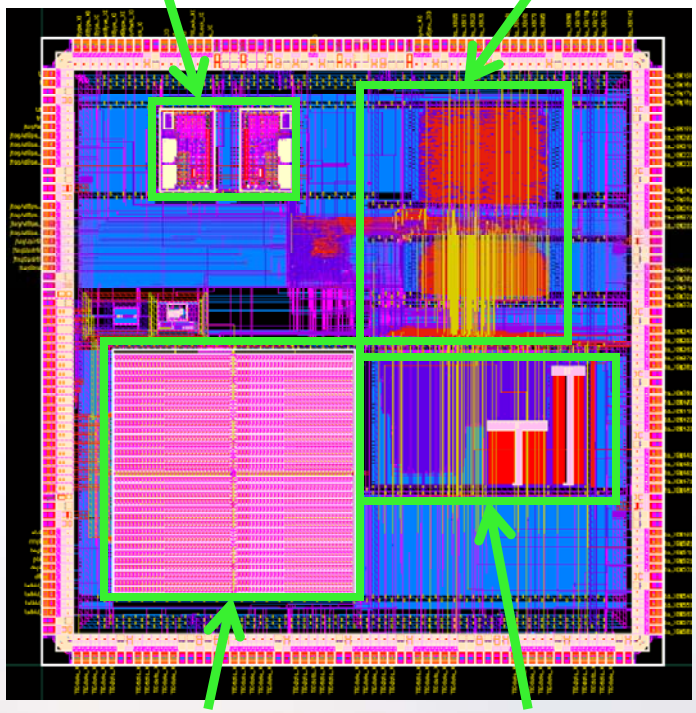
FPAGC 2D Testchip

- **Project Features**

	FPGAC Testchip
IBM Process:	CMOS 8RF
Feature size:	130 nm
Design size:	25 mm^2
Operating Conditions:	-55ºC to 125ºC 1.5V, 2.5V, 3.3V
Pixel count:	64 x 64
Frequency:	56.32 MHz, 112.64 MHz, 174.08 MHz



IBM Trusted Foundry and TAPO Feedback

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TAPO IBM Trusted Foundry Program Positive Feedback

- Ease of access to modern process nodes has been extremely beneficial.
- Customer was pleased with design validation and accessibility to advanced process nodes
- Extensive use of IP was very beneficial in the success of this program. PLL's, Memories, Standard Cells, IO
- My experience is they are willing to help out and find answers to my problems. Overall it has been a very positive experience
- We've taped out 9 KDP test designs and 3 additional instance test designs through TAPO in support of the KDP program. TAPO has been very responsive to our inquiries and willing to work with us to meet our schedule and need dates."
- TAPO has been very supportive in obtaining required IP…and providing additional MPW runs to support our program need dates.

TAPO IBM Trusted Foundry Program
Areas for Improvement

- CMOS9SF design manual had significantly more errors than other comparable manuals (e.g. IBM 130nm)
- Better communication regarding when wafers are expected back, including informing riders of delays
- However, the RTM (Release To Manufacturing) cycle time is often much longer than anticipated, delaying silicon availability. More frequent updates in RTM targets would be helpful.

End