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Impact of Gate Stack on the Stability of Normally-Off AlGaN/GaN Power Switching HEMTs

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***Abstract* – We have examined the response of AlGaN/GaN power switching HEMTs to electrical bias stress. Three different gate stack structures were studied. In devices containing a ~ 5 nm thick AlGaN layer in the gate stack, both positive and negative shifts in the threshold voltage were observed following high blocking voltage stress, consistent with a short initial period of electron trapping followed by a longer period of de-trapping. Correlated changes in reverse bias leakage current were also observed, although this also occurred in devices containing only residual AlGaN in the gate stack. The data have been explained by a field-enhanced emission model in which an electron trapping to de-trapping transition occurs. The exact nature of the transition is found to be sensitive to a variety of parameters including trap energy, geometry, and initial and boundary conditions.**

Keywords – AlGaN/GaN HEMT, power switching, reliability, electron trapping, gate stack, field plate

I. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) have recently seen widespread progress as a key device for the next generation of high-voltage power electronics [1-2]. Power devices require normally-off operation with low gate leakage current for safety and for compatibility with standard gate drive designs in power converters. The conflicting requirements of high on-state current and low gate leakage current requires significant design considerations in the gate stack architecture and processing.

Carrier trapping and de-trapping are prominent limiting factors of AlGaN/GaN HEMT performance and reliability [3-5]. In this study, the location and nature of deep level traps are analyzed by subjecting HEMTs employing different gate stack structures to electrical stress. We have observed complex time- and structure-dependent behavior, suggesting a strong coupling between the properties of the deep levels and the electric field profile in the device. A mathematical model for field-induced barrier lowering is shown to be a plausible explanation for the observed behavior.

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II. HEMT Structure and Processing

Three different device types with variations in gate stack processing were used in the experiments. In all cases, the devices were fabricated on Silicon (111) substrates at HRL Laboratories. All devices employ one gate field plate and two source-connected field plates, as shown in [6]. Device type A has a ~5 nm Al_2O_3 gate oxide deposited under the gate stack, whereas device types B and C are Schottky-gated. In all devices the gates are recessed by atomic layer etching to achieve normally-off operation; the remaining thickness of AlGaN under the gate is indicated in Table I. All devices used deep-acceptor compensation to achieve semi-insulating GaN buffer layers to limit leakage current.

Device Type	Gate Oxide	Gate Stack AlGaN
A	Yes	Present (t ~ 5 nm)
B	No	Residual (t < 1 nm)
C	No	Present (t ~ 5 nm)

Table I. Summary of recessed-gate normally-off AlGaN/GaN HEMT types studied in this work.

III. Threshold Voltage Shift and Change in Leakage Current Following Blocking-Mode Stress

Fig. 1a shows the I_D-V_{GS} characteristics for a device of type A measured at V_{DS} = 5 V a few seconds after being sequentially stressed at different bias conditions for 20 minutes each. These curves, and all other curves presented herein, are representative of a sampling of devices of the particular type stressed at the specified conditions. An off-state gate bias (V_{GS} = -7 V, V_{DS} = 0 V) produces a *positive* threshold voltage (V_T) shift, consistent with an increase in trapped electron density in the gate stack. This is accompanied by a decrease in drain leakage current. On changing the stress to conditions consistent with blocking voltage operation in a power circuit (V_{GS} = -7 V, V_{DS} = 50 or 100 V) V_T shifts in a *negative* direction, consistent with a decrease in trapped electron density in the gate stack. This shift is accompanied by an increase in the drain leakage current. Significantly, the changes in drain leakage current are reflected in the gate current, not the source current, which is suggestive of variation in a potential barrier in the gate stack.

Fig. 1b (measured for a different device of type A) shows that the negative shift in V_T is not completely recoverable at room temperature. Although biasing the device at V_{GS} = -11 V with V_{DS} = 0 V for 20 minutes appears to partially recover the device (which is consistent with the positive V_T shift observed in Fig. 1), subsequently leaving the device sitting unbiased for

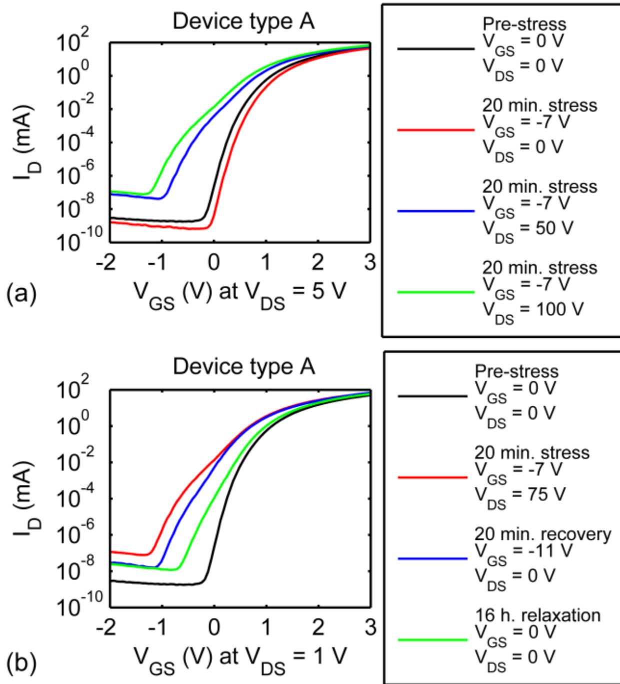

Fig. 1. (a) Post-stress I_D-V_{GS} characteristics for device type A measured at V_{DS} = 5 V. The threshold voltage shifts in the positive direction following off-state bias conditions. However, for blocking voltage conditions there is a prominent V_T shift in the negative direction. (b) Post-stress and recovery I_D-V_{GS} characteristics for device type A from measured at V_{DS} = 1 V. Following the negative shift under blocking voltage conditions, the device partially recovers when stressed at V_{GS} = -11 V, V_{DS} = 0 V for 20 minutes. Allowing the partially-recovered device to sit unbiased for 16 hours results in a shift back towards the post-stress characteristics.

16 hours causes the characteristics to shift back in the direction of the post-stress curves. The latter observation is consistent with thermal emission of trapped electrons.

I_D-V_{GS} characteristics following blocking-voltage operation for 20 minutes for device types B and C are shown in Fig. 2. For device type B, the drain leakage current under negative gate bias conditions increases in a manner similar to device type A, but the threshold voltage shift is clearly absent. Conversely, device type C exhibits both a negative V_T shift and an increase in drain leakage current, similar to device type A. A post-stress "hump" is present in oxide-gated device type A but is not present in device types B or C, suggesting that this feature may be related to charge trapping in the gate oxide. The shift in V_T seen in device types A and C and absent in device type B strongly suggests that *the primary negative shift in V_T after blocking voltage stress is related to the thin AlGaN layer under the gate.* Assuming that the hole density in the device is negligible, a negative V_T shift can only occur due to electron de-trapping in the gate stack region. An estimate of the density of traps required to produce the ~ -0.5 V shift in V_T observed for device type C in Fig. 2 can be made using the simple relation $q \cdot \Delta N = C \cdot \Delta V$ with $C = \varepsilon/t \approx 8.6\times10^{-13}$ F/cm^2 for a 5-nm-thick AlGaN barrier; this calculation yields $\Delta N \approx 4.5\times10^{12}$ cm^{-2}.

Since the change in drain leakage current is present in all device types and is reflected in the gate current, it is most likely related to the lowering or narrowing of an energy barrier in the gate stack. *For the device types with appreciable AlGaN in the gate stack, the observed shifts in V_T directly correlate with changes in leakage current: a positive V_T shift is accompanied by a decrease in leakage current, while a negative V_T shift is accompanied by an increase in leakage current.*

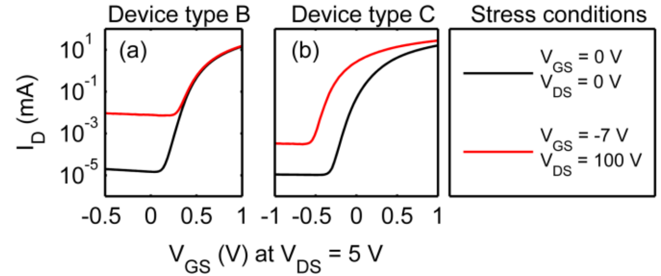

Fig. 2. (a) I_D-V_{GS} characteristics for device type B shows minimal V_T shift and a prominent increase in reverse leakage current following a 20 minute stress. (b) I_D-V_{GS} characteristics for device type C show a negative V_T shift and a less pronounced increase in reverse leakage current after a 20 minute stress, similar to device type A.

Although device type A shows a negative V_T shift following DC blocking voltage stress, a *positive* V_T shift was seen following Room-Temperature Operating Life (RTOL) stress in actual switching bias operation in a boost converter containing devices of the same type. However, in a boost converter the devices are subjected to repeated, short-duration, blocking-voltage stresses, as well as on-state stress. The boost converter results are reported elsewhere [7]. To understand this apparent discrepancy a series of short-duration (0.2, 0.4, 0.8, and 1.2 s) stresses were sequentially performed (Fig. 3). The drain current transients during the 0.2, 0.4, 0.8, and 1.2 s intervals are shown in Fig. 3a for a bias condition of V_{GS} = -7 V and V_{DS} = 50 V. After each short stress, a gate-sweep characterization curve was measured using V_{DS} = 0.3 V (Fig. 3b). In contrast to the 20-minute stress for which a *negative* shift in V_T is observed, for the short-duration stresses *positive* V_T shifts are observed. Note that the drain current following each experiment partially recovers following characterization. It is seen that during the first 0.2 and 0.4 s blocking voltage stress periods, the drain leakage current decreases during stress. The positive V_T shifts in the I_D-V_{GS} curves recorded at the end of both of these stress periods are correlated with the reduced leakage current, and are consistent with trapping of electrons. *Further, this positive V_T shift at short times is consistent with our observations of the HEMT behavior following RTOL switching operation in the boost converter.* Conversely, towards the end of the 0.8 s transient period the decrease in drain leakage current slows, commensurate with a transition to an increase in leakage current (compare the green and red curves in Fig. 3b). The drain current transient during an additional 1.2 s of stress clearly reverses direction and a further increase in drain leakage current is observed in the post-stress gate sweep (blue curve in Fig. 3b). Finally, following a much longer blocking-voltage stress of 40 s, the negative shift in the threshold voltage is clearly seen (magenta curve in Fig. 3b). Thus, again assuming that holes can be neglected, *our experiments show that at short times, electron trapping dominates, while at long times this is reversed and electron de-trapping dominates.* This resolves the apparent discrepancy between the 20-minute DC blocking-voltage stress experiments and the RTOL switching stress in the boost converter: in the boost converter, since the blocking-voltage stress is applied for

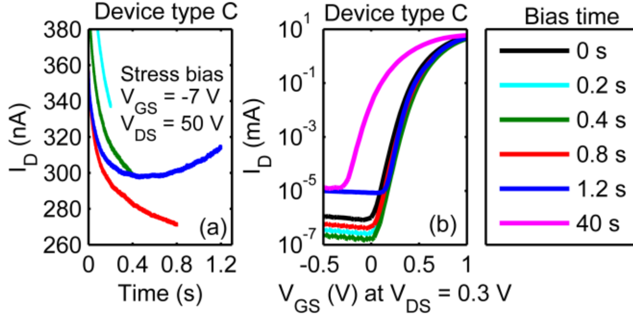

Fig. 3. (a) Drain current transients during successive blocking voltage stresses of durations 0.2, 0.4, 0.8, and 1.2 s for device C. The 1.2 s stress curve reveals a reversal in the transient. (b) I_D-V_{GS} curves measured after each stress period show a transition from positive to negative V_T shift with increasing stress time. The reversal in the drain current transient marks the onset of a sharp increase in reverse leakage, followed by a negative V_T shift (40 s curve).

only a short period of time, there is insufficient time for the electron trapping to de-trapping transition to occur. Thus, only the short-time positive V_T shift occurs during each switching cycle, resulting in a net positive V_T shift at the end of the boost converter operating period.

Under room temperature operation, the negative V_T shift does not recover within a reasonable period of time (hours to days). However, when annealing experiments are performed at elevated temperature, the negative shift can be recovered, and the recovery rate increases with increasing temperature. Details of this recovery are presented in [7]. Since the negative shift is consistent with electron de-trapping, this recovery must be due to electron trapping, indicating that *an energy barrier limits electron trapping in the device*. This may be the same barrier responsible for the observed changes in the leakage current. The presence of an energy barrier is consistent with the behavior reported by Joh et al., in which a barrier energy of $E_B \approx 0.7$ eV was observed for electron trapping [8]. Indeed, our High-Temperature Operating Life (HTOL) experiments on the boost converter show a complex, non-monotonic dependence of degradation on time and temperature, suggesting that competing trapping and de-trapping mechanisms are active, all of which are temperature dependent.

IV. Proposed De-trapping Model

For the data presented herein, the primary V_T shift is consistent with electron trapping and de-trapping in the AlGaN layer under the gate, since this is the only feature that is present in device types A and C but not in device type B. Further, changes in the drain leakage current are likely related to an energy barrier in the gate stack, since such changes are observed in all three device types, and these changes are reflected in the gate current rather than the source current. The time-dependent changes in V_T are consistent with a short initial electron trapping phase followed by a longer de-trapping phase. All observed effects are at least partially thermally recoverable and thus are probably not due to generation of permanent defects. Observed parametric shifts also show behavior consistent with energy barriers for both capture and emission. The latter has been evaluated experimentally for device type A and is consistent with the commonly-reported 0.6 eV activation energy [7]. Here, we propose a possible mechanism in which an initial electron trapping phase is followed by a second de-trapping phase, consistent with the experimental data and with the structure of the device. Our model is based on the concept of field-enhanced emission from a Coulombic trap potential well via barrier lowering and phonon-assisted tunneling [9]. The basic idea is that electrons are initially injected into the AlGaN in the gate stack (this may be due to tunneling from the gate electrode under high electric field), become trapped, and lead to the short-term positive V_T shift. The corresponding leakage current reduction is correlated with electron trapping in the AlGaN. However, since the leakage current is also observed in device type B, it may not be directly due to the electron trapping – e.g., it may be due to trapping elsewhere in or near the gate stack, which may impact the barrier height and/or width at the metal gate contact. Depending on the specific distribution of the trapped electrons and the boundary conditions (which are influenced by the field plate structure), the electric field may become quite large (~ 1 MV/cm) within the AlGaN and GaN layers, which will subsequently lead to emission of the trapped electrons. This de-trapping in turn results in the long-term negative V_T shift and leakage current increase. Clearly, the proposed process is quite complex and depends sensitively on the energy barriers for capture and emission, the temperature, and the composition and geometry of the device.

Our model consists of the Poisson equation coupled with the rate equation for capture and emission of electrons, the latter of which incorporates the aforementioned field-enhanced emission mechanisms [7]. To demonstrate the plausibility of the model, a MATLAB simulation was written to numerically solve the model for specific cases. Consistent with recent reports of deep-level defect concentrations in AlGaN [10], a uniform density of $N_T = 10^{15}$ cm^{-3} was assumed, with 80% of the traps initially filled at t = 0. A slab of material of length L = 10 μm was considered, with boundary conditions of zero field at x = 0 and zero potential at x = L. The initial condition for the potential was a quadratic function of position, consistent with the boundary conditions and the initial uniform density of

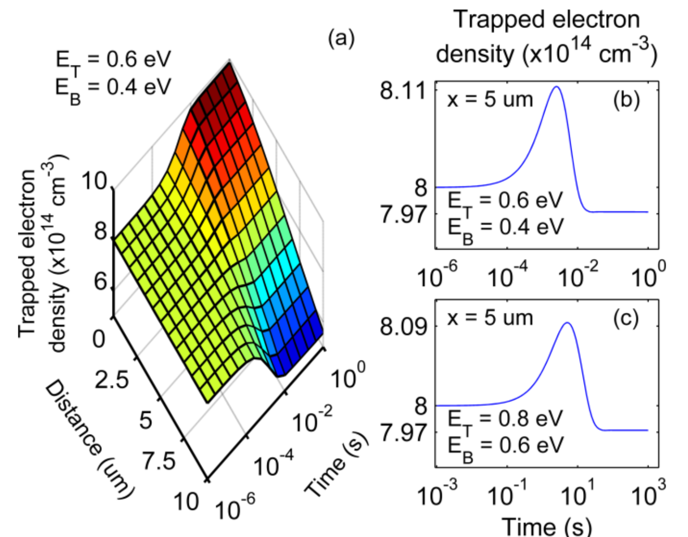

Fig. 4. (a) Trapped electron density plotted vs. position and time, calculated using the 1-D de-trapping model described in the text. (b) Trapped electron density plotted vs. time at the mid-point of the material. (c) Trapped electron density vs. time at the mid-point using different values for E_T and E_B, with all other values the same.

trapped electrons. Various values of the temperature T, the trap energy E_T, and the capture barrier energy E_B were tried; the results of a simulation with T = 300 K, E_T = 0.6 eV, and E_B = 0.4 eV are shown in Figs. 4a and 4b. At time t = 0 all traps are uniformly filled such that $n_T(0,x) = 8\times10^{14}$ cm^{-3}. As time evolves, near x = 0 (where the boundary condition is zero field) trapping dominates, whereas near x = L (where the boundary condition is zero potential, and the field is high) de-trapping dominates. This simple model demonstrates that a transition from trapping to de-trapping is physically plausible. The exact behavior observed in the model is sensitive to the barrier and trap energies, the temperature, the length of the material, the fraction of traps initially filled, and the boundary conditions (Fig. 4c).

Of course, the behavior observed experimentally will depend in detail on the geometry of the real device and the exact location of trapping, which is not captured in the simple 1-D model and requires the use of 2-D finite-element simulations. One possible scenario is that electrons are initially trapped in the AlGaN in the gate stack and/or in the region underneath the gate field plate. This will tend to raise the conduction band edge in this region, and will lead to strong band bending (and hence a large electric field) near the drain side edge of the gate and at the edge of the gate field plate. This high electric field, induced by the initial trapping, will in turn lead to a higher emission rate from the traps, as described by our model. TCAD simulations were performed in Silvaco's ATLAS software to examine the electric field profile in the devices. Fig. 5 shows the simulated magnitude of the electric field in the gate and gate field plate region of device type C with 2×10^{11} cm^{-2} electrons injected into the AlGaN layer under the gate at a bias condition of V_{GS} -7 V and V_{DS} = 50 V. The highest fields (red) occur in the AlGaN at the corners of the etched gate region, with the maximum at the drain side edge of the gate, consistent with the scenario described above. This field (of order 1 MV/cm) is of sufficient magnitude to induce de-trapping of electrons, as outlined in our model. Full time-dependent TCAD simulations utilizing the physics developed herein are in progress and will be presented in a future paper.

V. Summary

The electrical stability of AlGaN/GaN power switching HEMTs with three different gate stack structures was studied. All three device types had recessed gates for normally-off operation. Device type A had an AlGaN thickness of ~ 5 nm in the gate stack and an insulating Al_2O_3 layer on top of the AlGaN; device type B had only residual AlGaN and no insulating layer in the gate stack; and device type C had ~ 5 nm of AlGaN and no gate oxide. Device types A and C showed V_T shifts after blocking-state bias stress, while device type B did not show a V_T shift, suggesting that the V_T shift is related to electron trapping and de-trapping in the AlGaN. All three device types showed changes in reverse bias leakage current, possibly due to changes in a potential barrier in the gate stack. For device types A and C, the shifts in V_T were correlated with the changes in leakage current. Time-dependent measurements indicate that an initial period of electron trapping is followed by a longer period of electron de-trapping. We have explained this using a model in which the initial trapping period increases the local electric field, which in turn leads to an enhanced emission rate from traps due to field-induced barrier lowering and phonon-assisted tunneling. The exact behavior is highly dependent upon the energies and locations of traps in the device, the detailed geometry of the device, and the electric field profile. Further simulation studies utilizing the model developed herein will shed more light on the complex interplay between defect physics and device design underlying AlGaN/GaN power HEMT reliability.

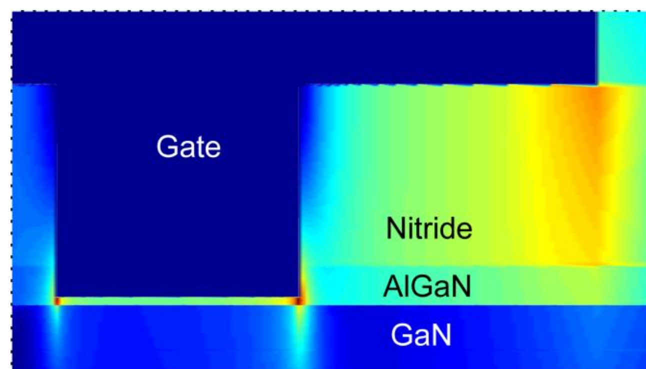

Fig. 5. TCAD-calculated electric field profile in the gate and gate field plate region of device type C with V_{GS} = -7 V and V_{DS} = 50 V. Source is to the left, drain is to the right.

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