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A New Wafer-Level Packaging Technology for MEMS with Hermetic Micro-Environment

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Device Fabrication: Franklin Austin, James Kalivoda, Tyler Jordan,

Thinning & Packaging: Denise Webb, Benjamin Thurston, Kenneth McGuire and Katherine Myers.

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Outline

- **Introduction**
  - ✓ Needs for Improved Cost/Performance in MEMS Packaging
  - ✓ Past work on Improved MEMS packaging
  - ✓ Our Approach
- **Wafer-Level processes**
- **Results**
- **Cost**
- **Conclusions**
- **Recommendations for Future Work**

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MEMS Packaging Requirements

- **MEMS require a clean empty volume around it to function reliably with high performance.**
  - ✓ Hermetic lid enclosure with micro-environment of either vacuum or dry gas (Nitrogen) is needed in many MEMS devices.

- **MEMS have to be low-cost for wide applications.**
  - ✓ Lower cost can be achieved by wafer-level packaging with high yields.

- **Packaged MEMS have to be in miniaturized volume to have performance advantage over incumbent technologies.**
  - ✓ Chip-scale-package

Objective of the Study

Develop a Wafer-level Chip-scale MEMS Packaging Technology that

1. **provides hermetic micro-environment**
2. **can be fabricated with simpler processes and with Low Cost**
3. **is miniaturized and can be integrated easily**

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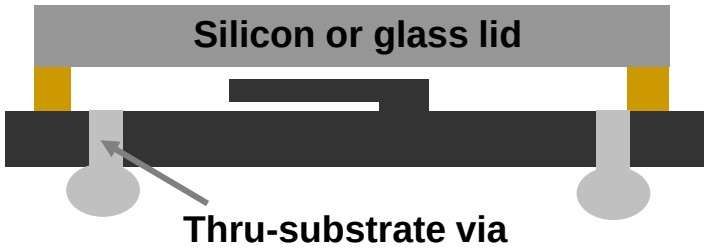
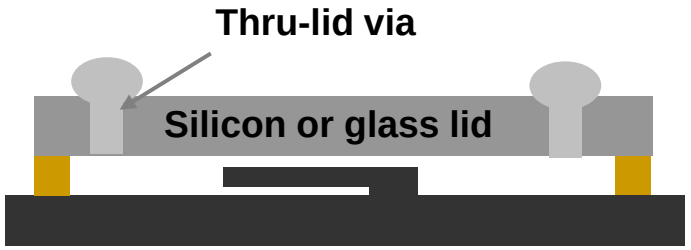
Past Investigators' Approaches



Thru-Silicon Substrate vias



Thru-Lid vias

(Lid can be either Silicon or Glass)

Hermetic Membrane Lid

(Involves fabricating membrane in a silicon Fab by removing sacrificial layer and then hermetically sealing the membrane)

All these are more costly processes that require special fabrication facility.

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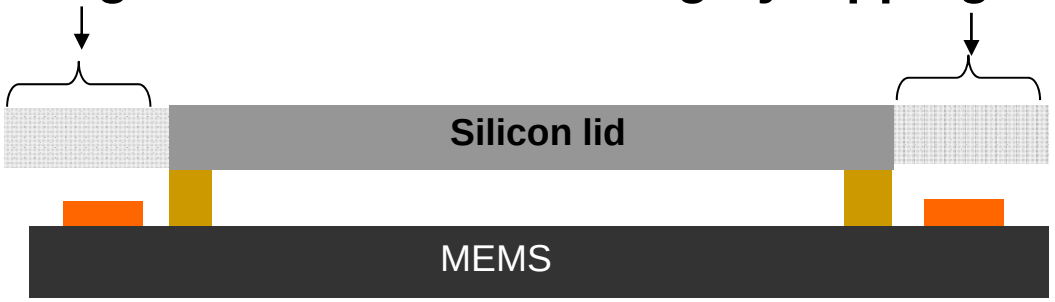
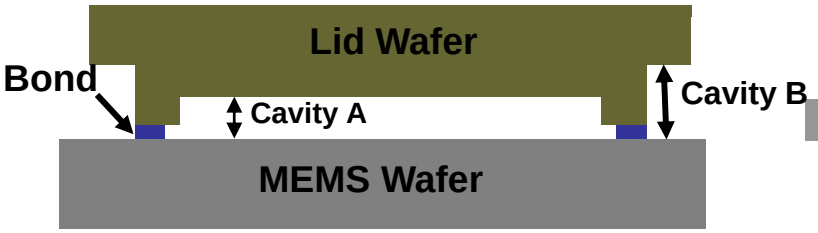
Our Packaging Approach

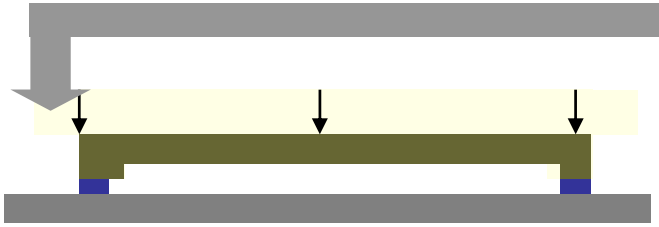
Removing the lid wafer overhang by lapping/etching





A. Starting MEMS-Lid Assembly
Cavity A - 20 μm, Cavity B – 120 μm

B. Thin MEMS to < 100 microns



C. Thin Lid to < 100 microns

D. Thinned MEMS- Lid Assembly
< 200 microns

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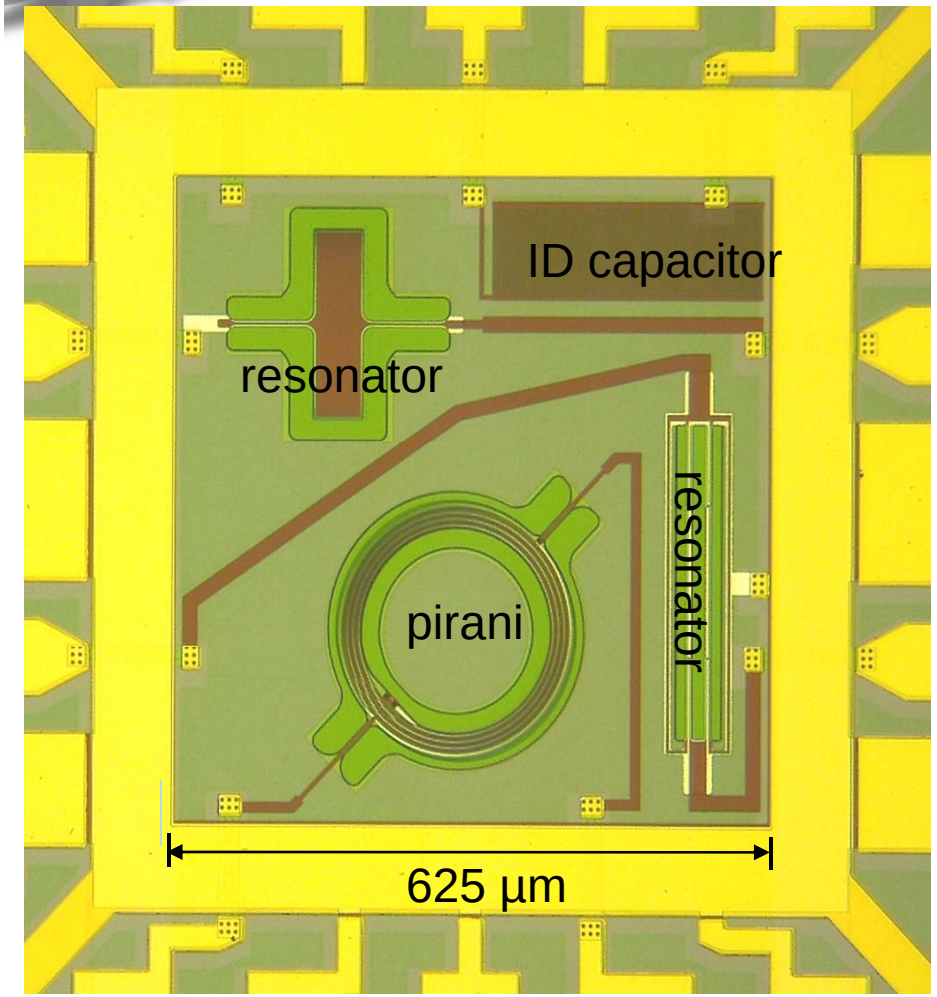
Test vehicle MEMS Structure



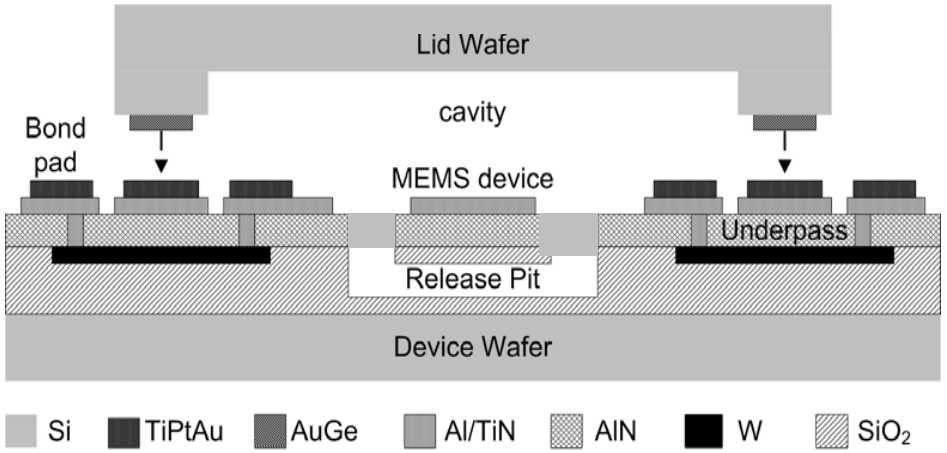
Features:

1. AlN-based microresonator.

2. Pirani Gauges located on the MEMS to monitor the pressure inside hermetic lid.

3. Seal ring on MEMS and on the lid for hermetic seal attachment.

4. The connection to the I/O pad is through an underpass isolated by AlN insulating layer



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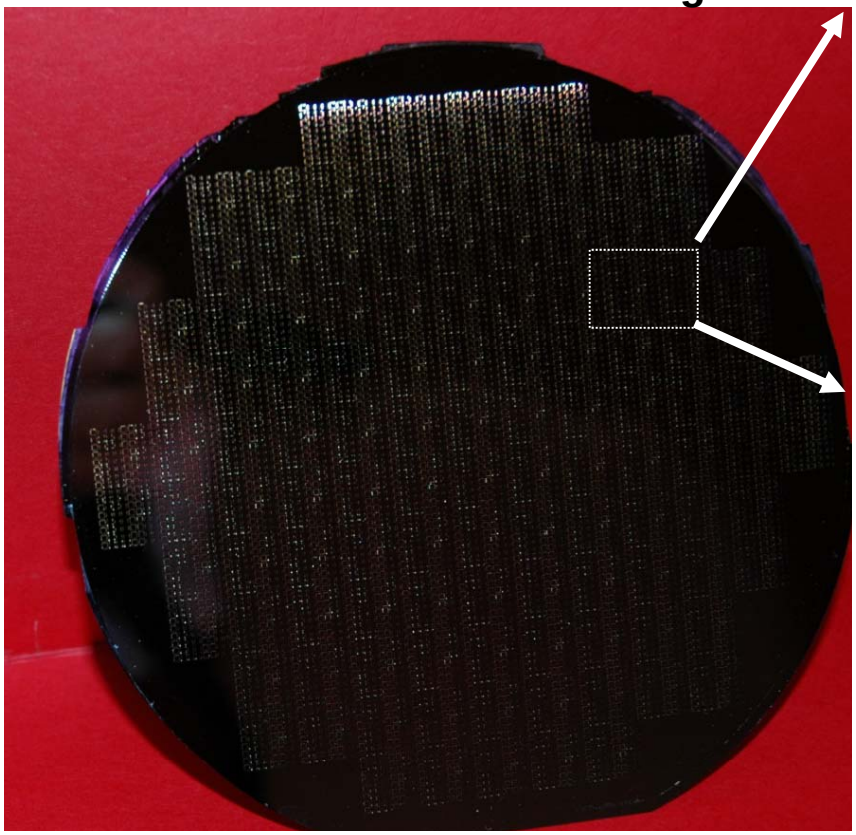
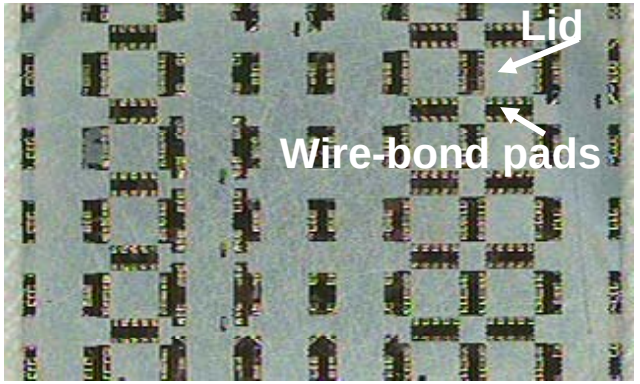
Wafer-Level Packages

Full Wafer after Processing



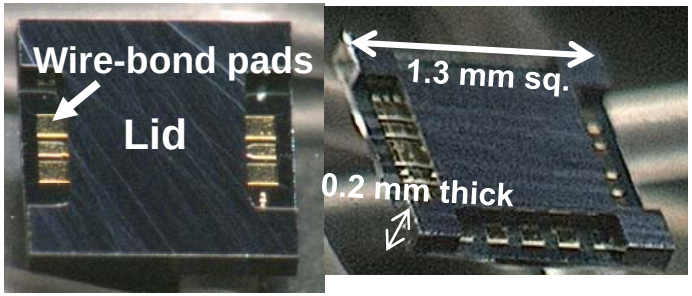
(a)

Magnified View



(b)

Singulated Devices



(c)

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Packaging Process Flow

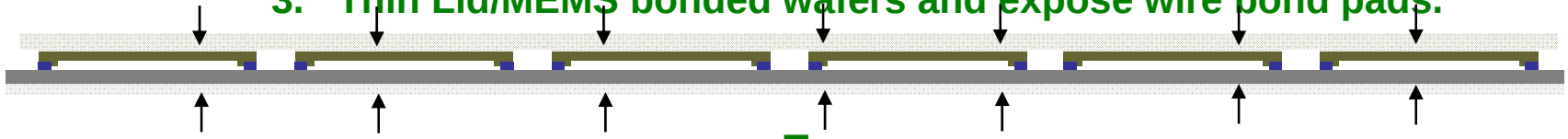
1. Prepare Lid and MEMS wafer

A. Lid wafer –Metallize seal ring and bosch-etch cavities

B. MEMS wafer – Metalize seal-ring

2. Bond Lid/MEMS wafers

3. Thin Lid/MEMS bonded wafers and expose wire bond pads.



4. Dice and Singulate the MEMS devices

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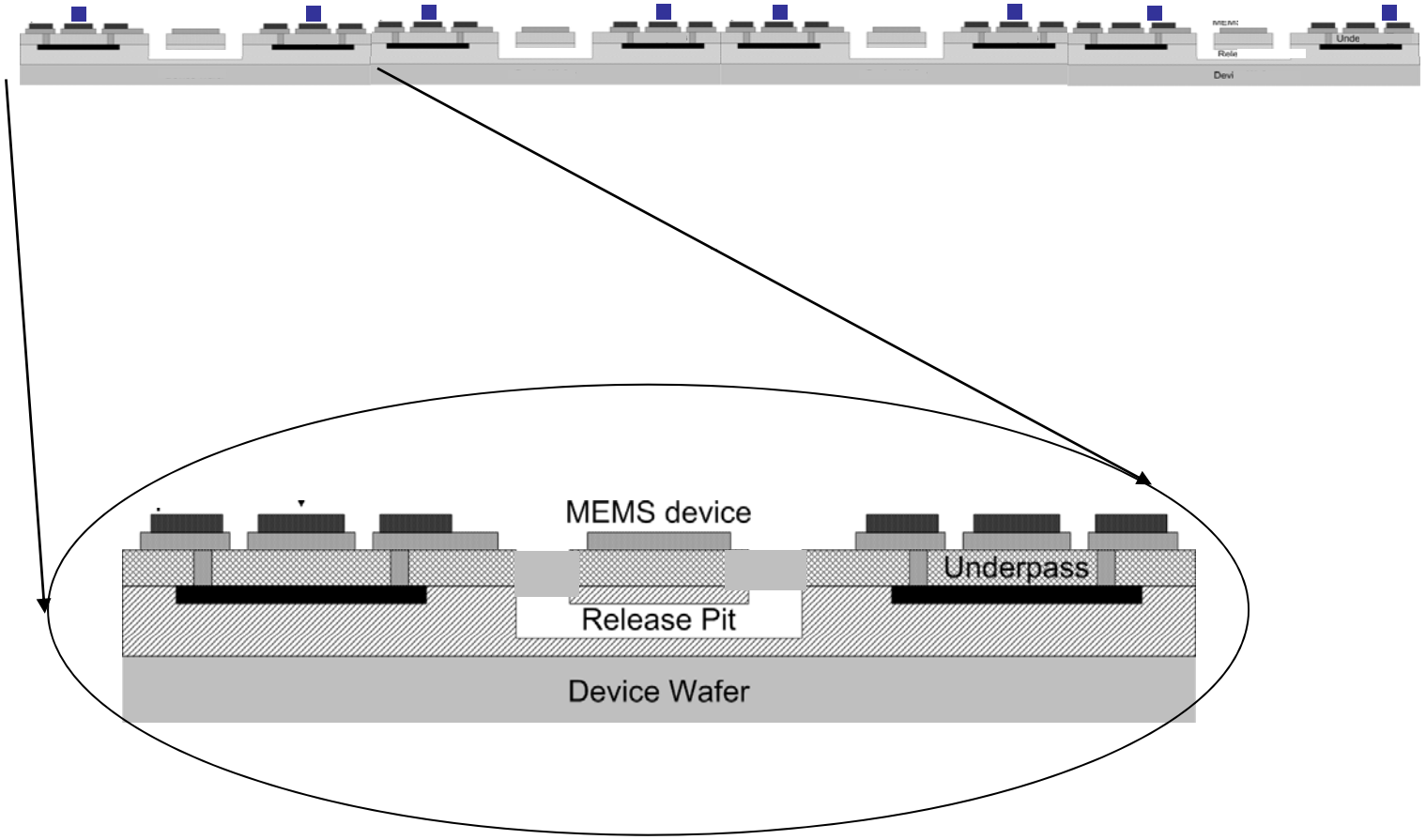
MEMS Wafer Preparation

Metallization - Ti/Pt/Au



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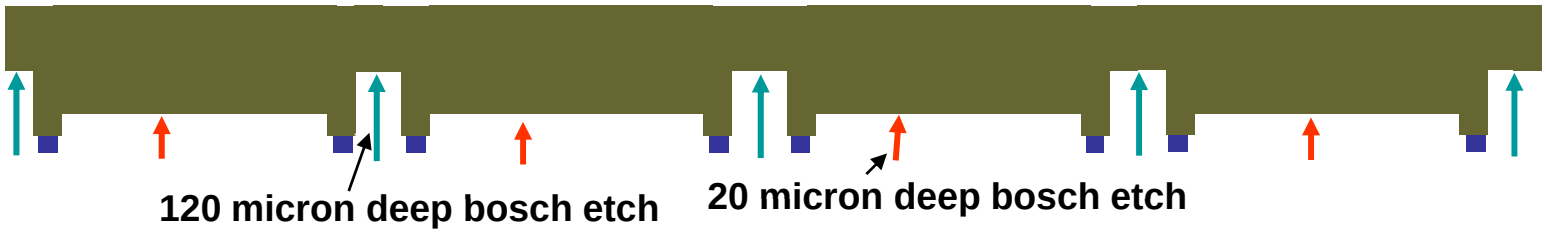
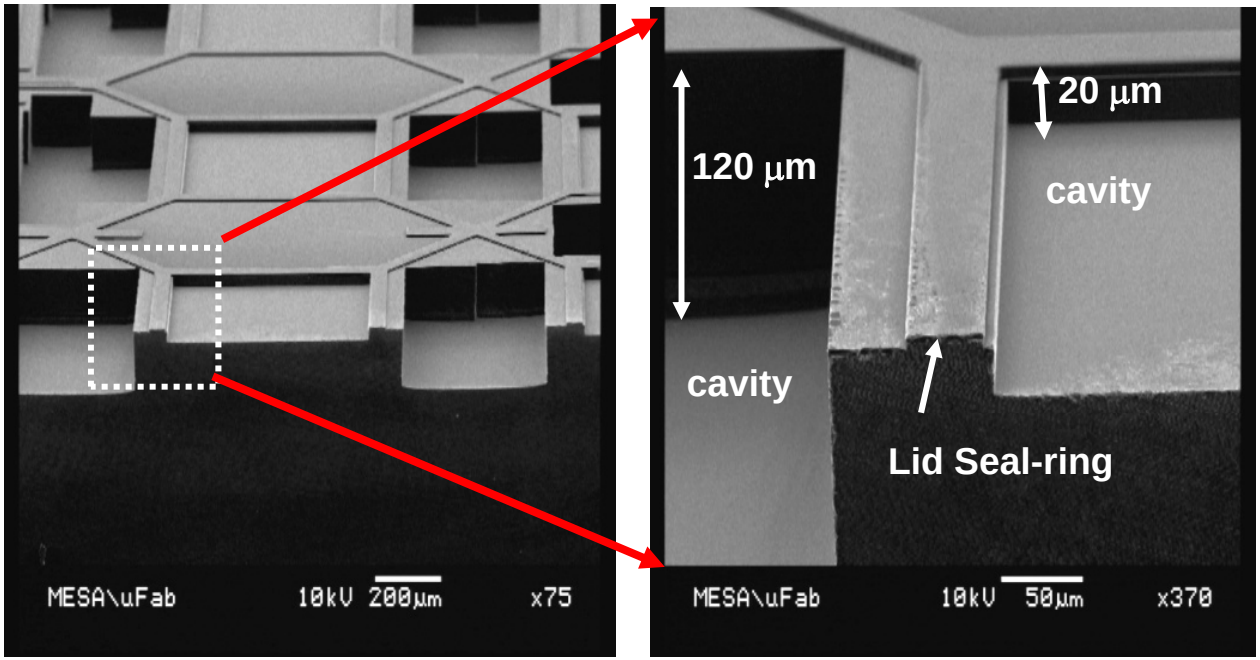
Lid Wafer Preparation





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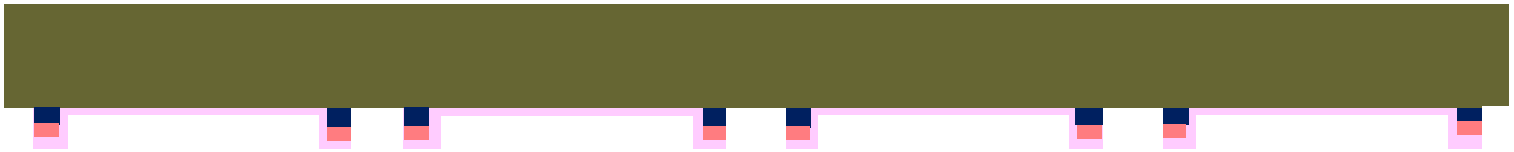
Process Flow for Etching Lid Cavities

Metallization - Ti/Pt/Au/Ge/Au

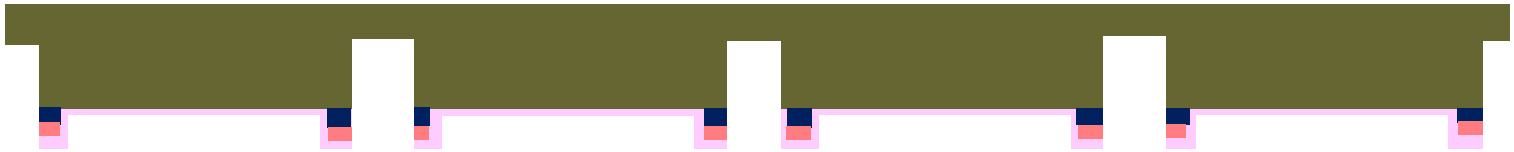
Step 1: Metallize Seal-Ring on Lid wafer



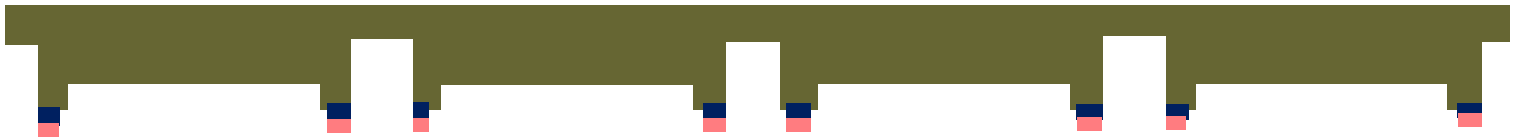
Hard Mask (Cured Photoresist)

Soft Mask (Uncured Photoresist)

Step 2: Deposit & Pattern two masks



Step 3: DRI Etch Deep Cavity (100 Micron deep cavity)



Step 4: DRI Etch Shallow Cavity (20 Micron deep cavity)

Step 5: Strip Mask

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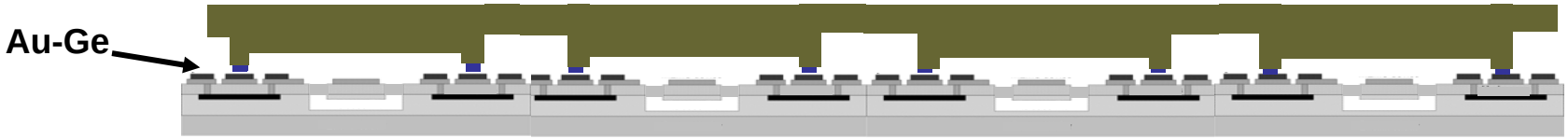
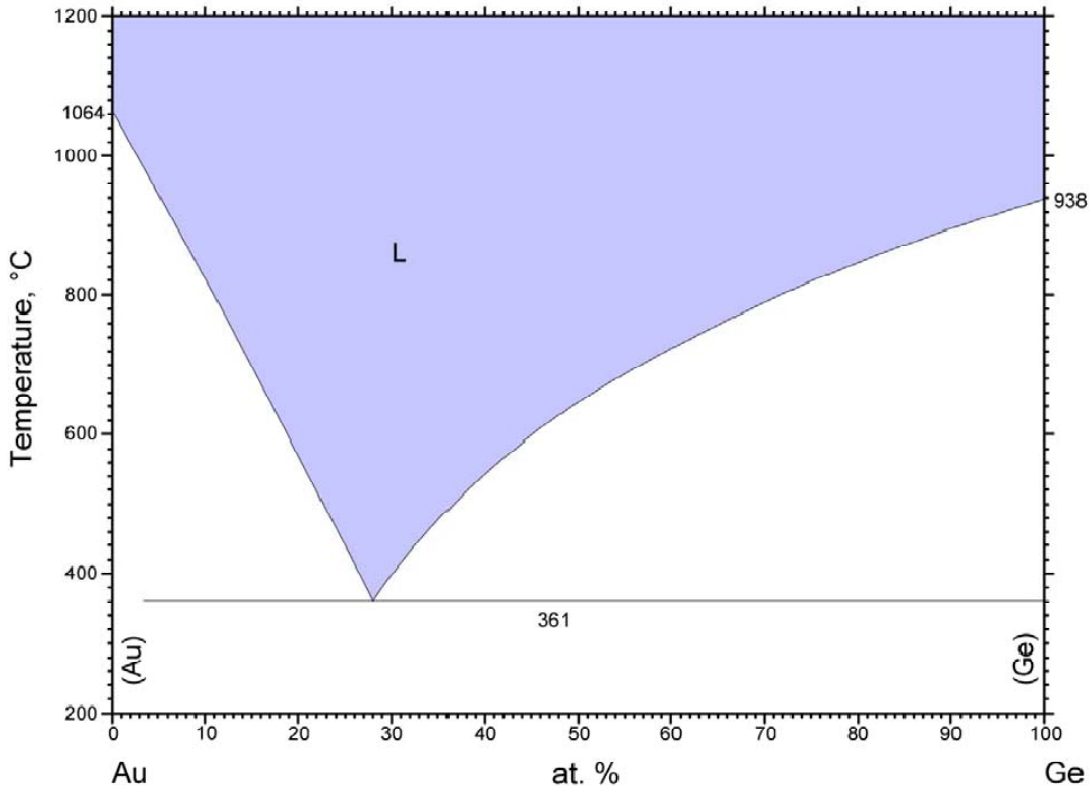
Wafer Alignment and Bonding



Au-Ge Eutectic Bonding

Au-Ge Phase Diagram (1991 Okamoto H.)



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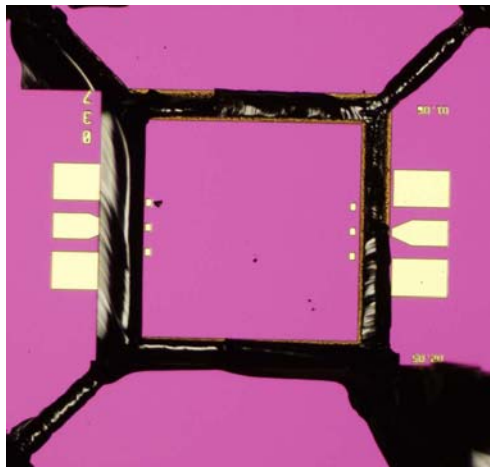
Wafer Alignment and Bonding

- We have used Au-Ge eutectic bonding
  - ✓The other alternative eutectic bonding metals are Au-Si and Au-Sn
- Bonding was done at > 363^{o}C for 5 minutes in Vacuum or nitrogen environment

Inspection of lid wafer seal-ring after Shear test.



Silicon around seal-ring broke indicating a strong bond

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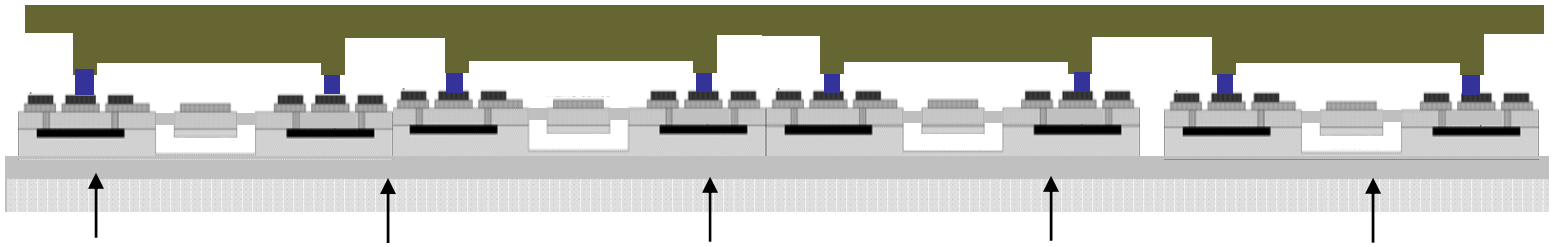
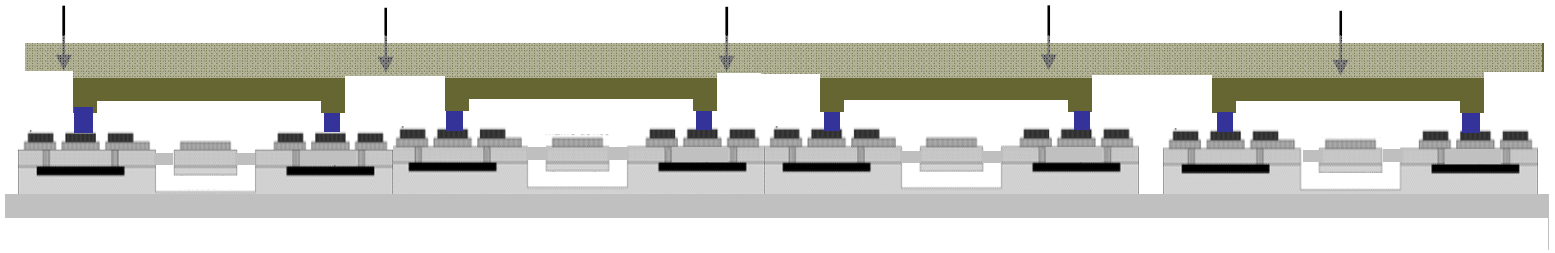
Thinning

Thinning was done in two steps:

Step 1: MEMS wafer-side was thinned to 100 microns



Step 2: Lid-side was thinned to 100 microns. This eliminated the overhang and exposed the I/O pads .



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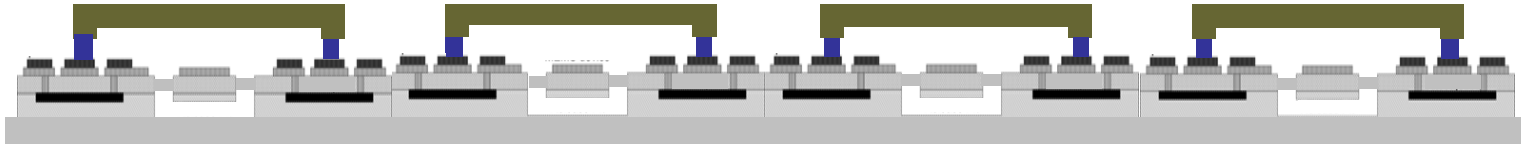
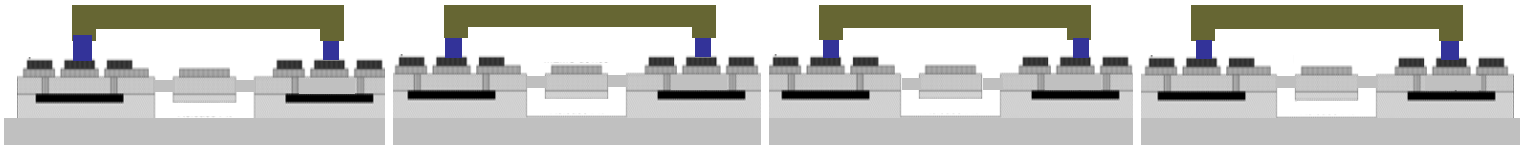
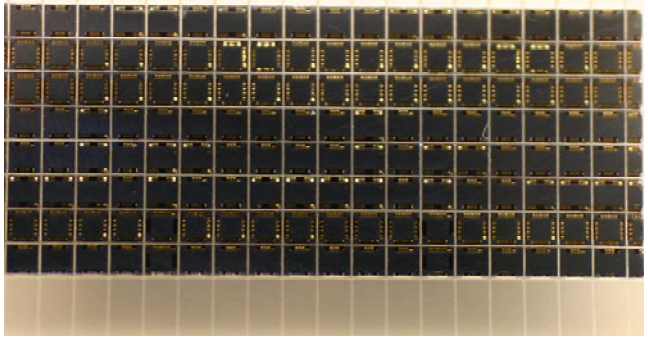
After Thinning



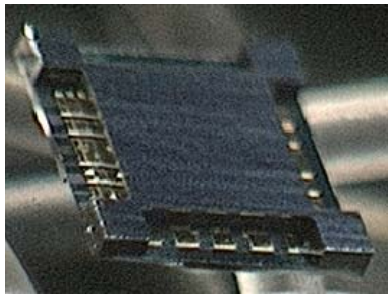
After Dicing

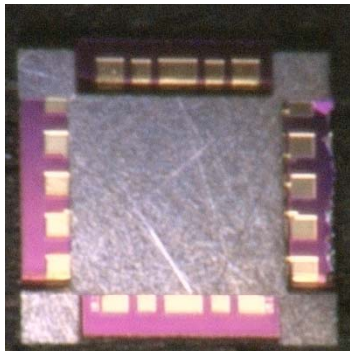


Diced Devices on a Tape



Singulated device





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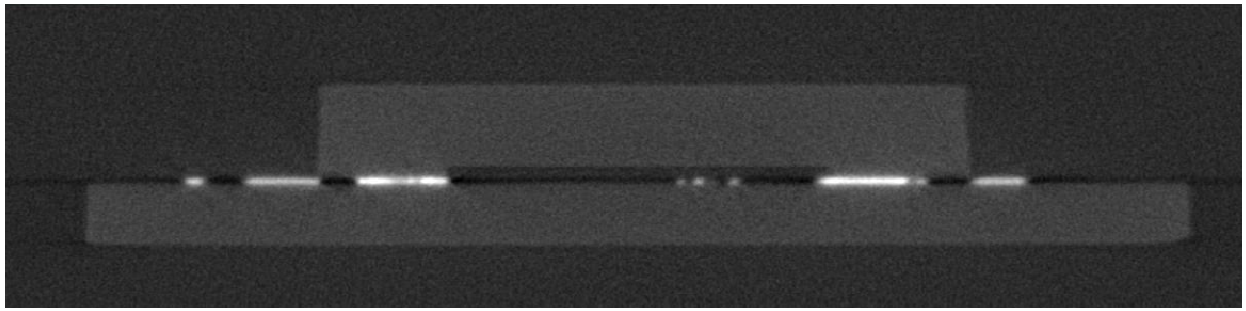
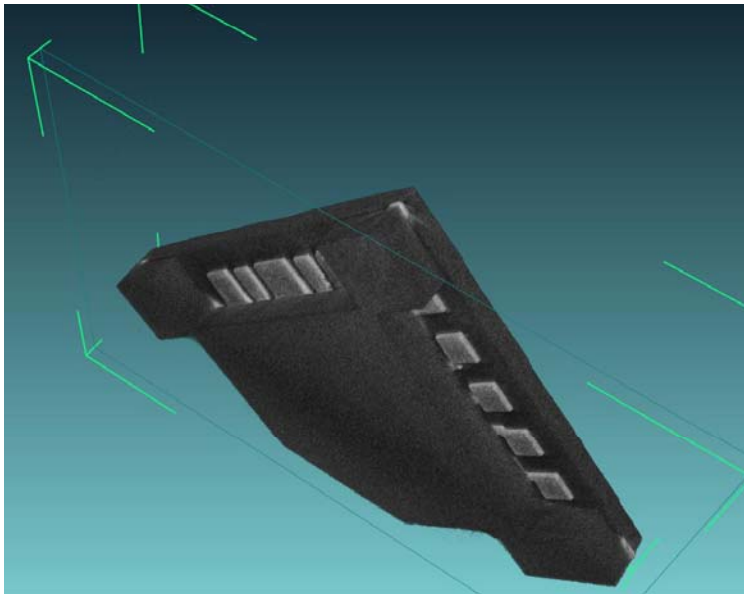
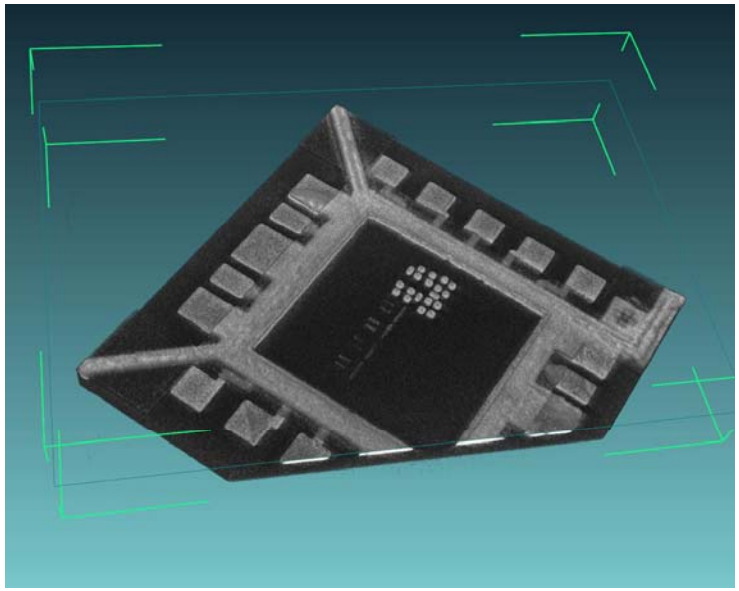
X-Ray Images

2D- XRay Image of the Cross-Section



3D- XRay Images





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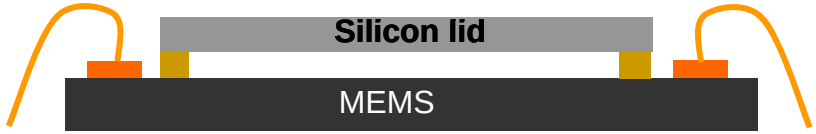
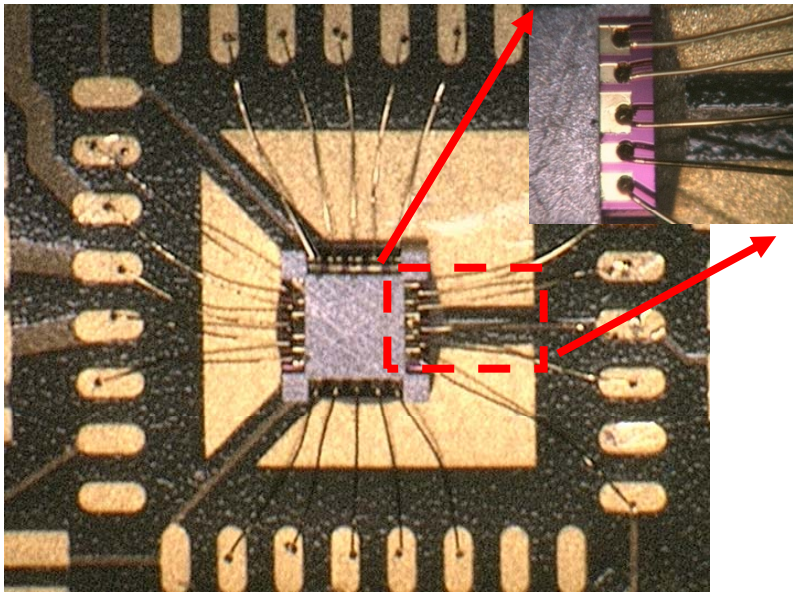
Next-level Integration

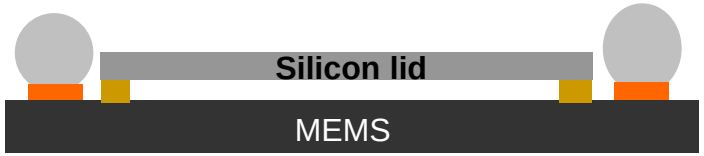
Wire-bonded version

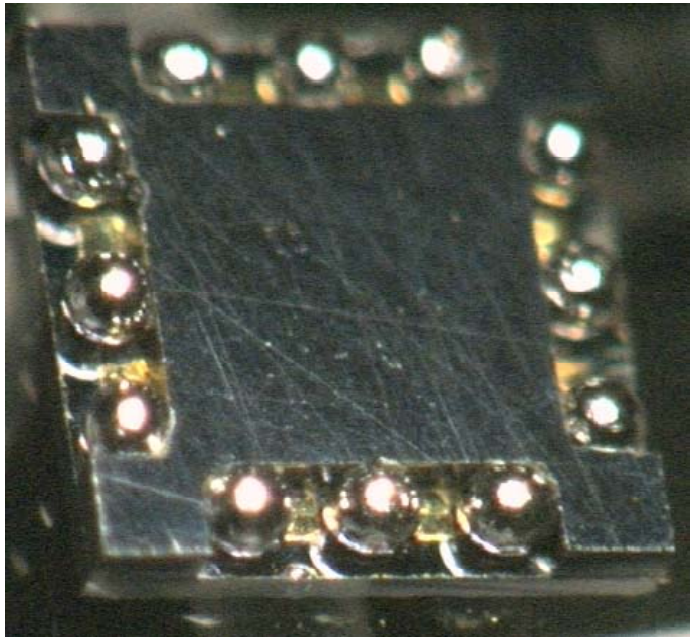


Wire-bond version



Surface- mount version





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Hermeticity Test Results

- **Due to a very small open space volume inside the hermetic lid, standard Fine and Gross Leak tests do not work for checking the hermeticity.**
- **Pirani gauges and resonators featured on MEMS can monitor in-situ pressure, which will confirm the hermeticity inside the lid.**
- **Our hermetic packages showed the pressure of 1 to 10 Torr range as also previously reported for devices without getters.**
- **We got yield of >50%.**
- **Most of the yield limiting failure modes were attributed to photolithography-related defects and inadequate cleaning.**

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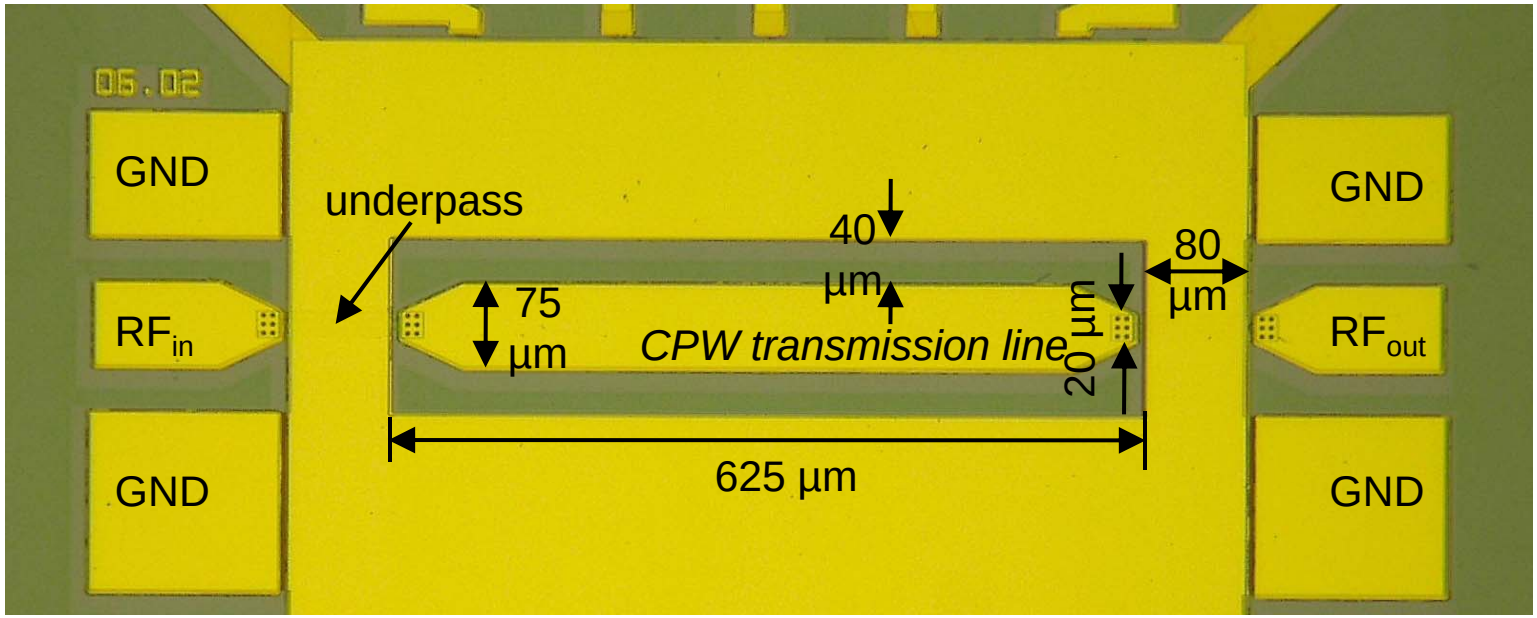
Electrical Test Results

➢ **The RF performance of the package was tested by measuring a 0.6 mm-long coplanar waveguide transmission line (width = 75 mm, gap = 40 mm) that traversed the width of the package and was connected to test pads by two 20 μm-wide, 0.6 μm-thick traces passing underneath the 80 μm thick sealring insulated by aluminum nitride insulator.**



- **This coplanar waveguide test structure with two underpasses was measured from 1-20 GHz**
- **Layer thicknesses:**
  - **W underpass: 0.6 μm, Ti/Pt/Au: 0.6 μm, AlN: 0.75 μm**

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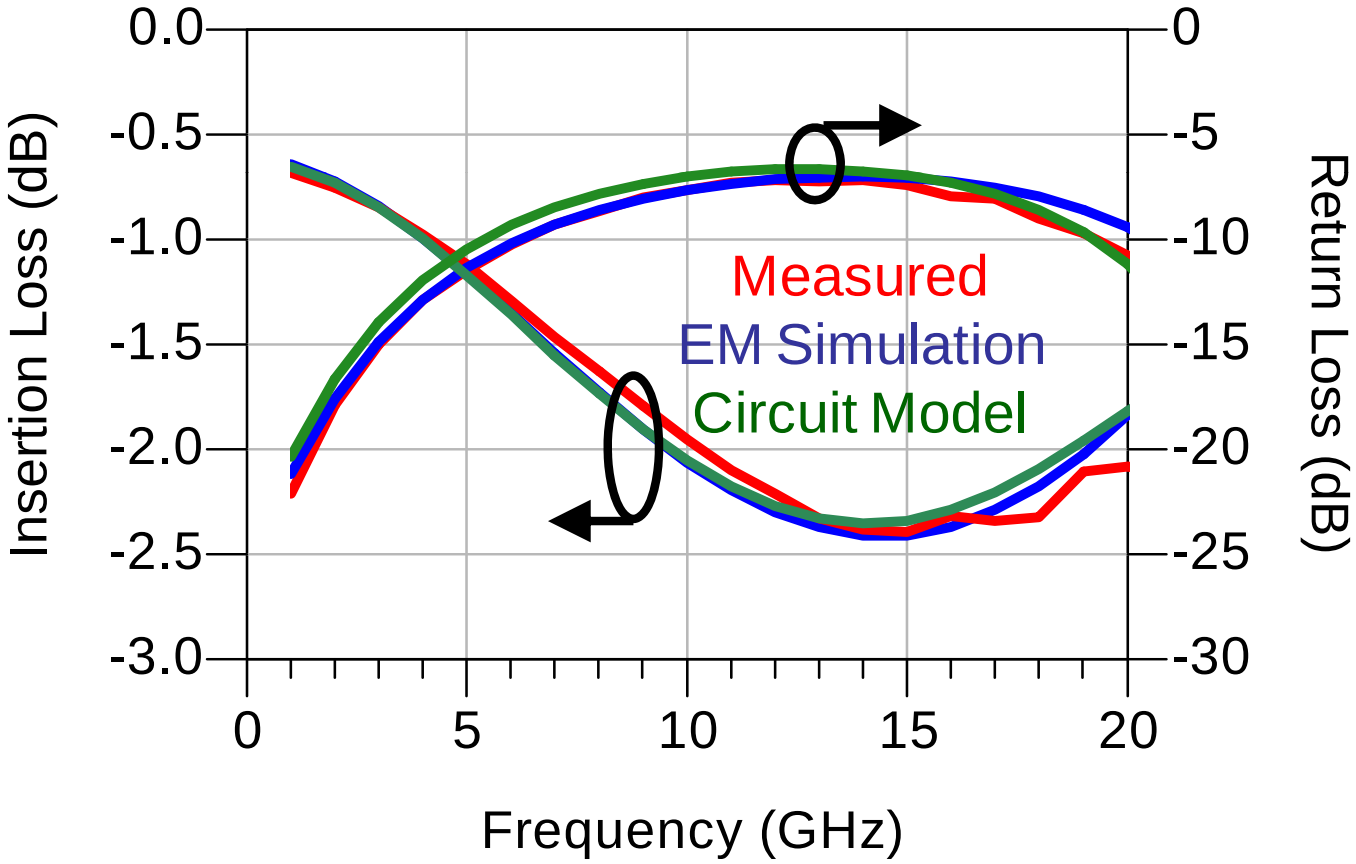
Electrical Test Results (cont…)

- **The measured and simulated performance is compared to an equivalent circuit model of the underpass.**



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Cost

We have developed processes that will be inherently low cost

- **Wafer-level Processes**
- **All process Steps are matured processes and can be outsourced**

Preliminary Cost Analysis has indicated that for

Assumption of

- **a high Yielding Process**
- **Mass-produced**

Wafer-Level Packaging Cost will be $0.10 to $0.90 per device

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Conclusions

- **We have developed a Wafer-Level Chip-Scale Packaging (WLCSP) technology. The unique feature of this technology is that it requires low-cost wafer-Level processes.**

- **We have demonstrated this technology by packaging AlN Microresonators in chip-scale packages with hermetic micro-environment.**

- **In these devices we get RF feed-throughs with <0.3B dB insertion loss at frequencies up to 2GHz. Pirani gauges have confirmed the hermetic yield of >50%.**

- **Our preliminary cost analysis has indicated the cost of CSWLP to be $0.10 to $0.90 per device.**

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Recommendation for Further Work

- **Improve the process yields and the hermetic yields by better control of the processes and more-effective cleaning steps.**

- **Develop mass-producible processes with internal capability and/or collaborating with external vendors.**

- **Refine the cost analysis of mass–produced devices.**

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