SAND2012-9009C

Development of an Ultra Scalable, Low Power, Rad-Hard Nonvolatile Memory for Space Applications

AIAA Albuquerque Chapter Meeting

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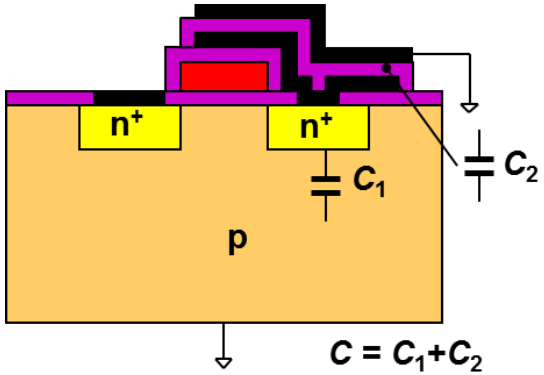
Outline

- The Status Quo: DRAM, SRAM and Flash
- The Future of Memory
- Memristor Development & CMOS Integration
- Rad-Hard Memory Development
- Novel Applications

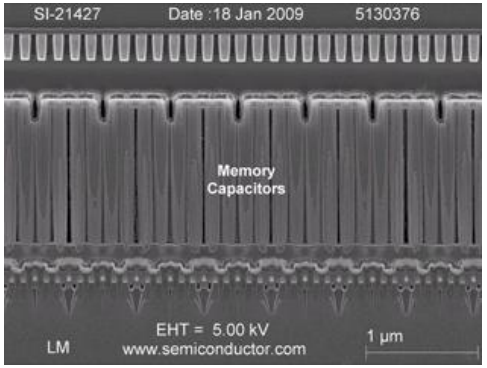
Dynamic Random Access Memory

- Most common memory
- Low cost
- ~30 nm cells in production as of 2012
- Volatile and changes memory state if not refreshed periodically
- DRAM Challenges:
  - DRAMs struggling to maintain reasonable equivalent oxide thickness
  - Dielectric for cells 30nm to 20 nm still TBD
  - Is scaling possible below 20 nm?
  - DDR2 interface is a power hog

Stacked DRAM Cell



Micron Stacked DRAM

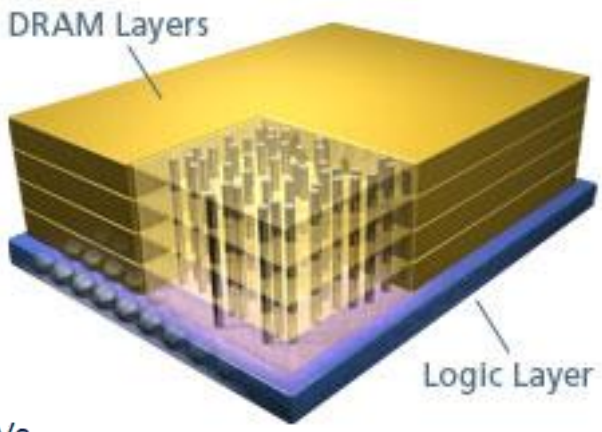


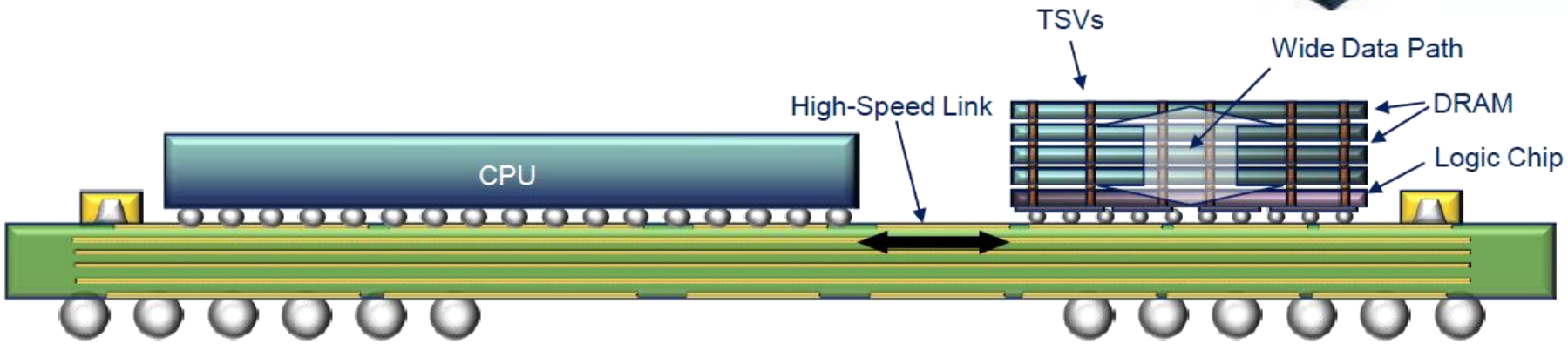
Courtesy Dieter Schroder, ASU

3D DRAM

- **Micron/Intel Hybrid Memory Cube**
- **DRAM die stacked on logic**
- **Connected via through-silicon-via**
- **Major energy savings**

Micron, Hotchips 2011

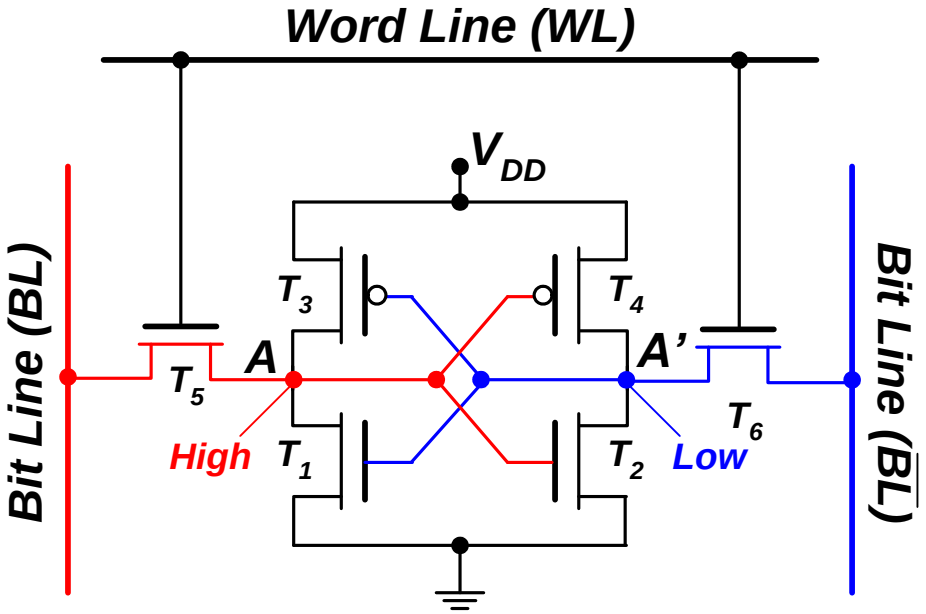




Technology	VDD	IDD	BW GB/s	Power (W)	mW/GB/s	pj/bit	real pJ/bit
SDRAM PC133 1GB Module	3.3	1.50	1.06	4.96	4664.97	583.12	762
DDR-333 1GB Module	2.5	2.19	2.66	5.48	2057.06	257.13	245
DDRII-667 2GB Module	1.8	2.88	5.34	5.18	971.51	121.44	139
DDR3-1333 2GB Module	1.5	3.68	10.66	5.52	517.63	64.70	52
DDR4-2667 4GB Module	1.2	5.50	21.34	6.60	309.34	38.67	39
HMC, 4 DRAM w/ Logic	1.2	9.23	128.00	11.08	86.53	10.82	13.7

Static Random Access Memory

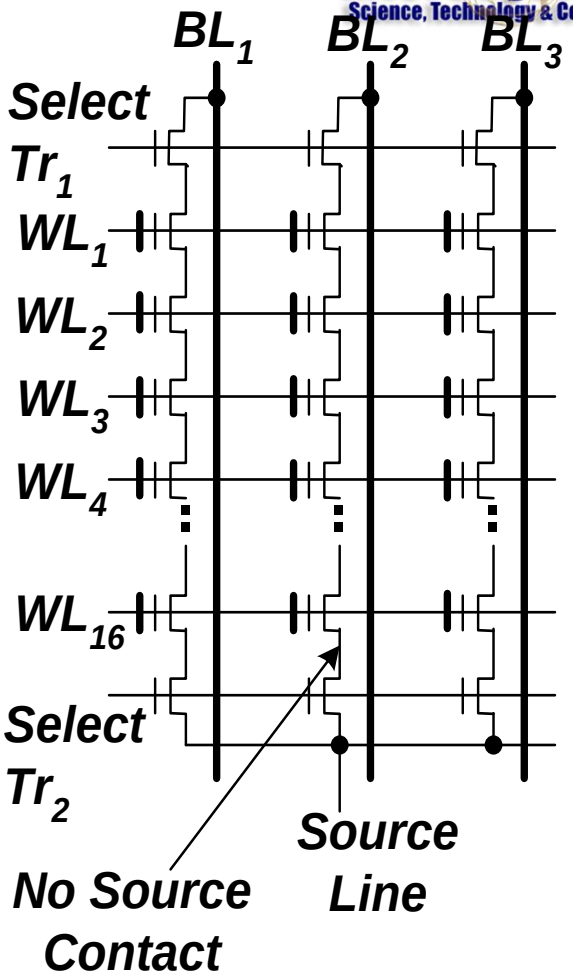
- Faster than DRAM (<1ns read/write)
- Larger cell size – requires ≥ 4 transistors
- Lower density than DRAM; lower power dissipation
- Set memory: WL high, BL and A high, BL and A' low
- WL low, cell isolated and will retain its memory as long as power is supplied without refresh

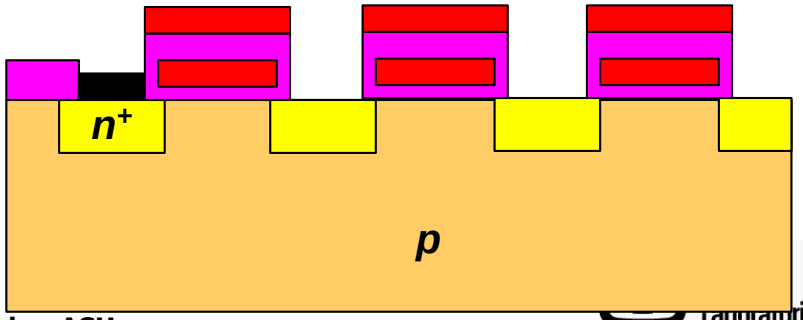


Courtesy Dieter Schroder, ASU

NAND Flash Memories

- Serial access; slower than NOR
- High density: F≈20 nm in 2012
- Low bit cost
- Write/Erase: Fowler-Nordheim
- Erased as blocks
- Small cell size (5-6 F^2), since no source contact required
- Memory cards (USB sticks, iPad)
- Challenges:
  - Non-scalable tunneling dielectric need > 6 nm for retention
  - Floating gate interference: capacitance coupling between floating gates
  - Reduced coupling ratio with scaling

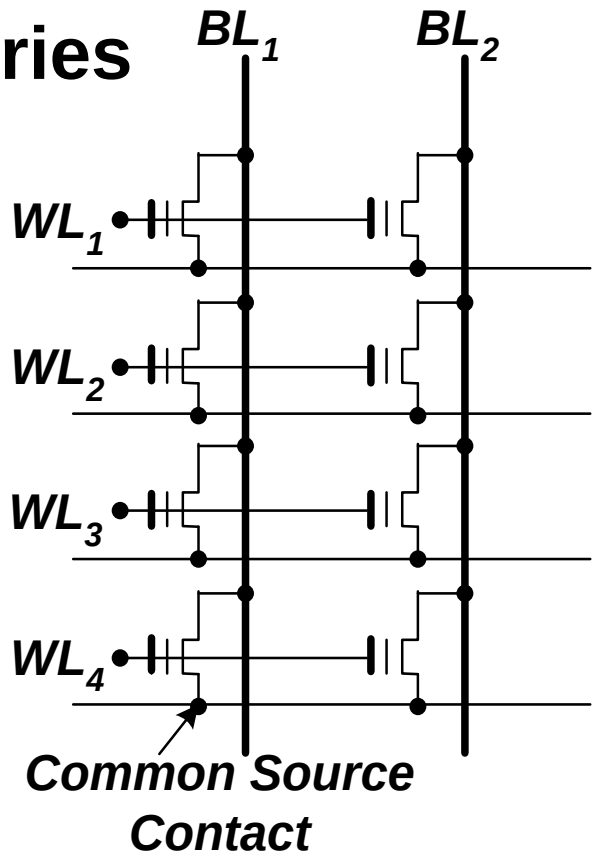


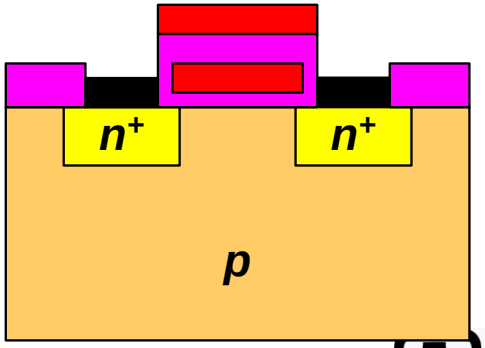


Courtesy Dieter Schroder, ASU

NOR Flash Memories

- Fast random access, similar to RAM
- Lower voltage (7-10V)
- Write: Hot electron injection, high V_D
- Erase: Fowler-Nordheim
- Erased as blocks
- Area: 9-11F^2 (need source contact)
- Embedded code (cellular phones, etc.)
- Challenges:
  - More severe drain disturbance with continuous scaling
  - Severely limited scaling below 32nm





Courtesy Dieter Schroder, ASU

Outline

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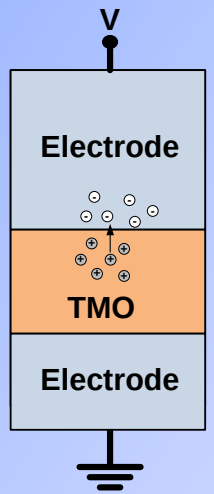
Emerging Memory Technologies

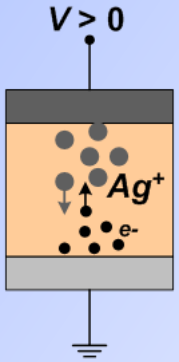
ReRAM

VCM



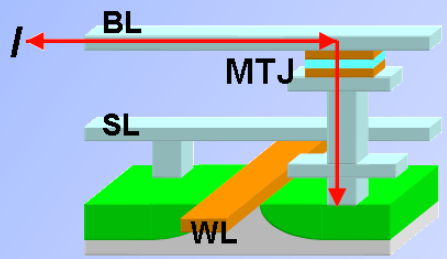
Anion

ECM



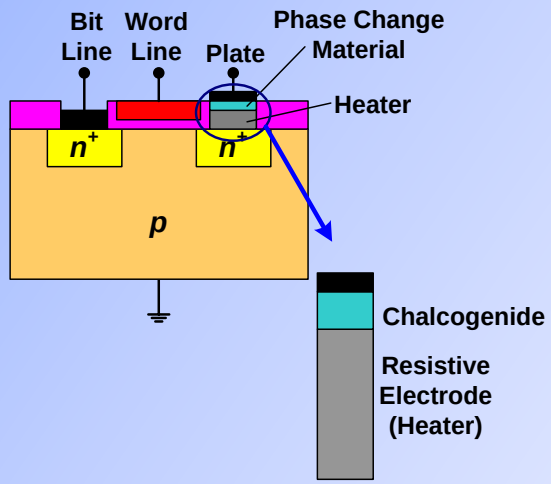
Cation

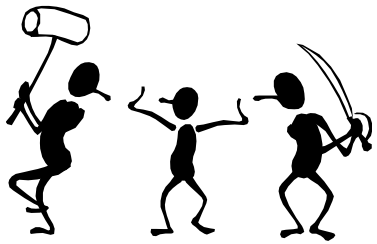
STT-MRAM



ITRS ERD 2010 Memory Rept.

Phase Change

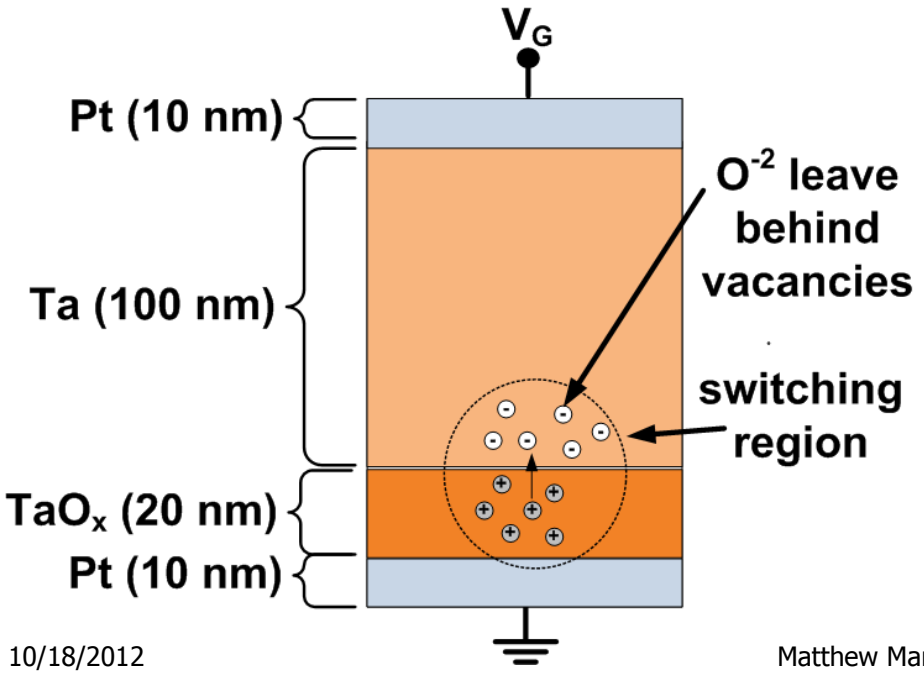


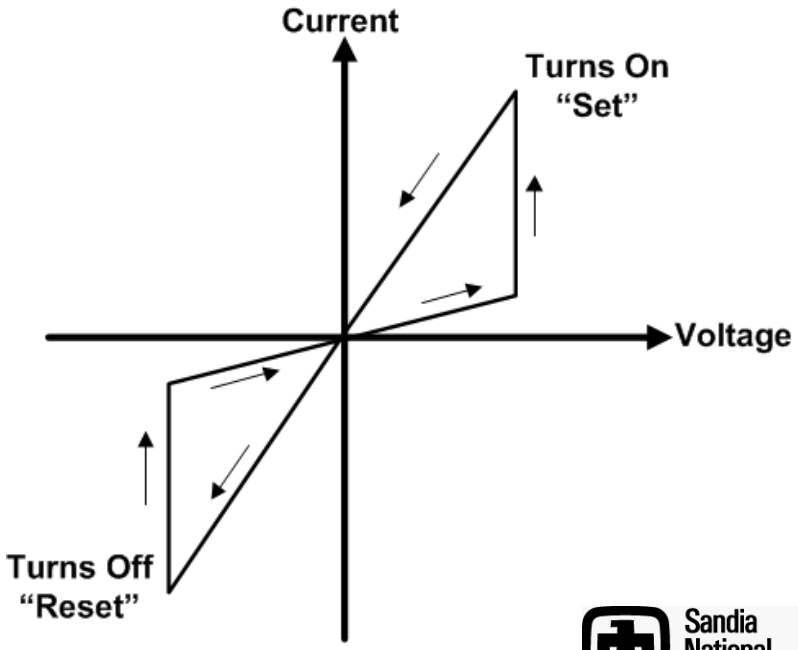


ECM, PCM courtesy Dieter Schroder

Valence Change Memories

- Type of resistive, or redox memory (a.k.a. memristor)
- Research led by HP Labs, Jülich/Aachen, Samsung/SAIT
- Sandia has recently established a major research program in this technology
- Resistance Change Effect (polarities depend on device):
  - Positive voltage/electric field: on, "set" – O^{-2} anions leave oxide
  - Negative voltage/electric field: off, "reset" – anions return





Side Note: What is a Memristor?

- Theoretical concept created by Leon Chua in 1971
- 4th passive element "necessary for the sake of completeness"
- Relatively obscure theory until 2008
- ReRAM is a memristor!

$$v = \mathcal{R}(w,i)\,i$$

$$\frac{dw}{dt} = f(w,i)$$

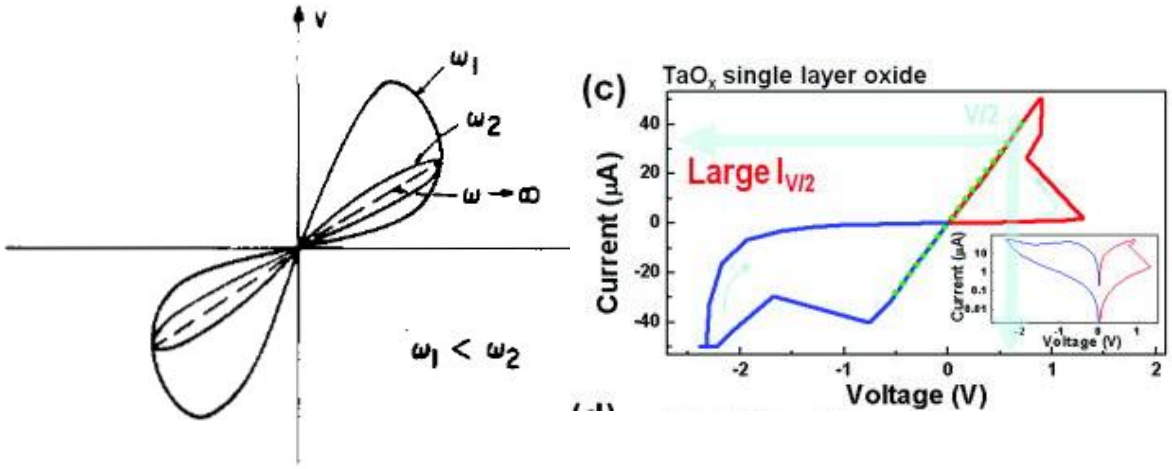
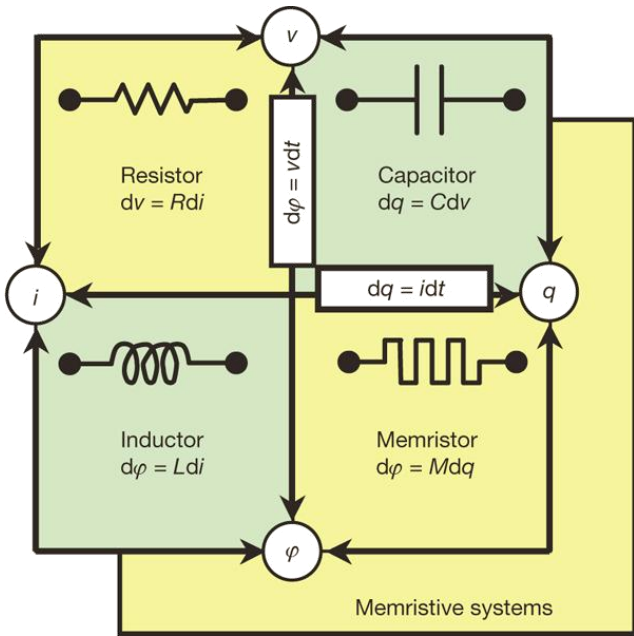


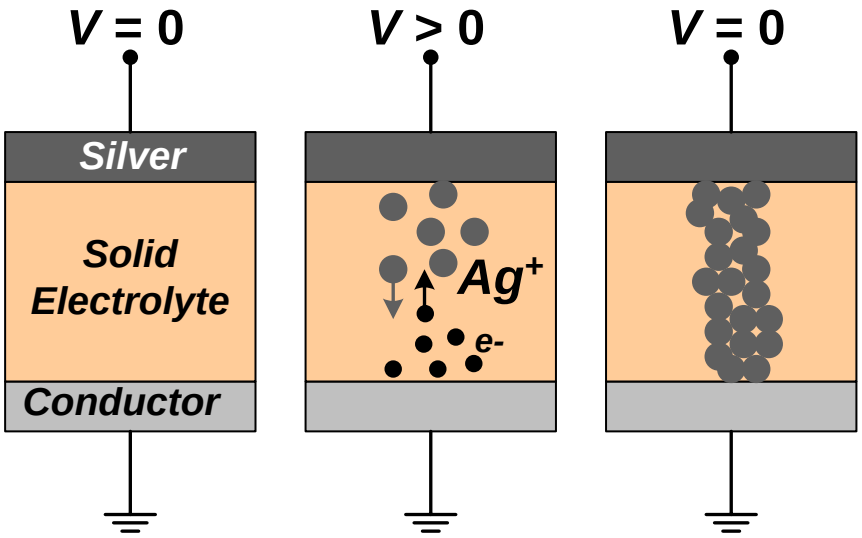
Fig. 6. Frequency response of Lissajous figures.



Chua and Kang, IEEE Trans Circuit Theory, 1976

CBRAM – Electrochemical

- Pioneered by Michael Kozicki (ASU/Axon/Adesto)
- Ions move under the influence of an electric field leading to *electrochemical reactions*
- Electrochemistry takes place at a few 100 mV
- The electro deposition process stops when a conducting link is formed
- Metallic link reduces the resistance of the structure by many orders of magnitude
- *On* resistance is determined by the programming current and is programmable



Courtesy D.K. Schroder (ASU)

http://www.axontc.com

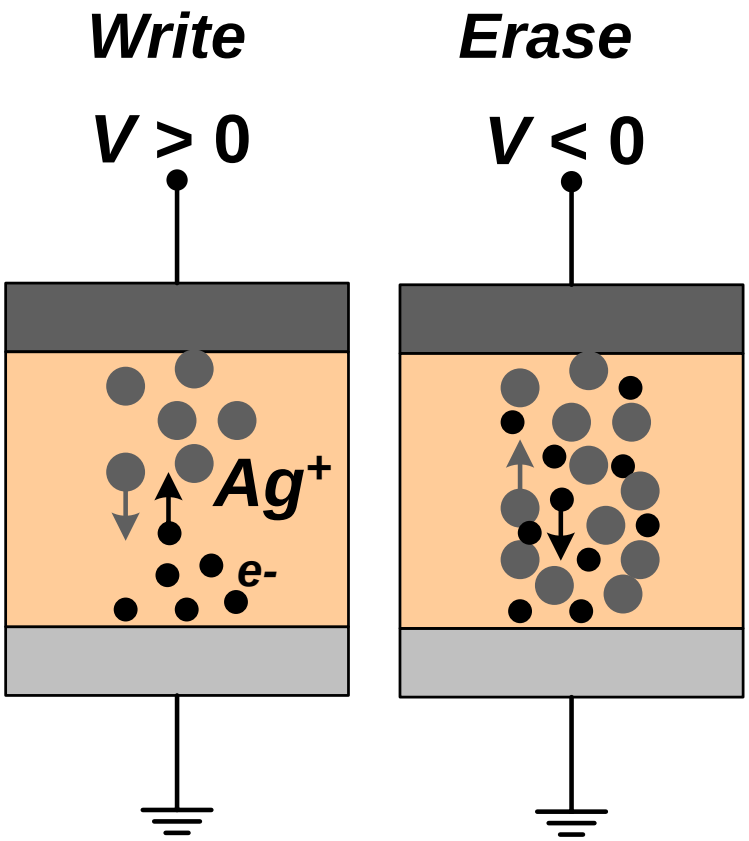
Programmable Metallization Cell

Write

- Low voltage injects silver ions into the electrolyte
- Ions are reduced by the electron current to form stable silver atoms
- Information is stored by the presence of excess silver
- Multiple levels possible

Erase

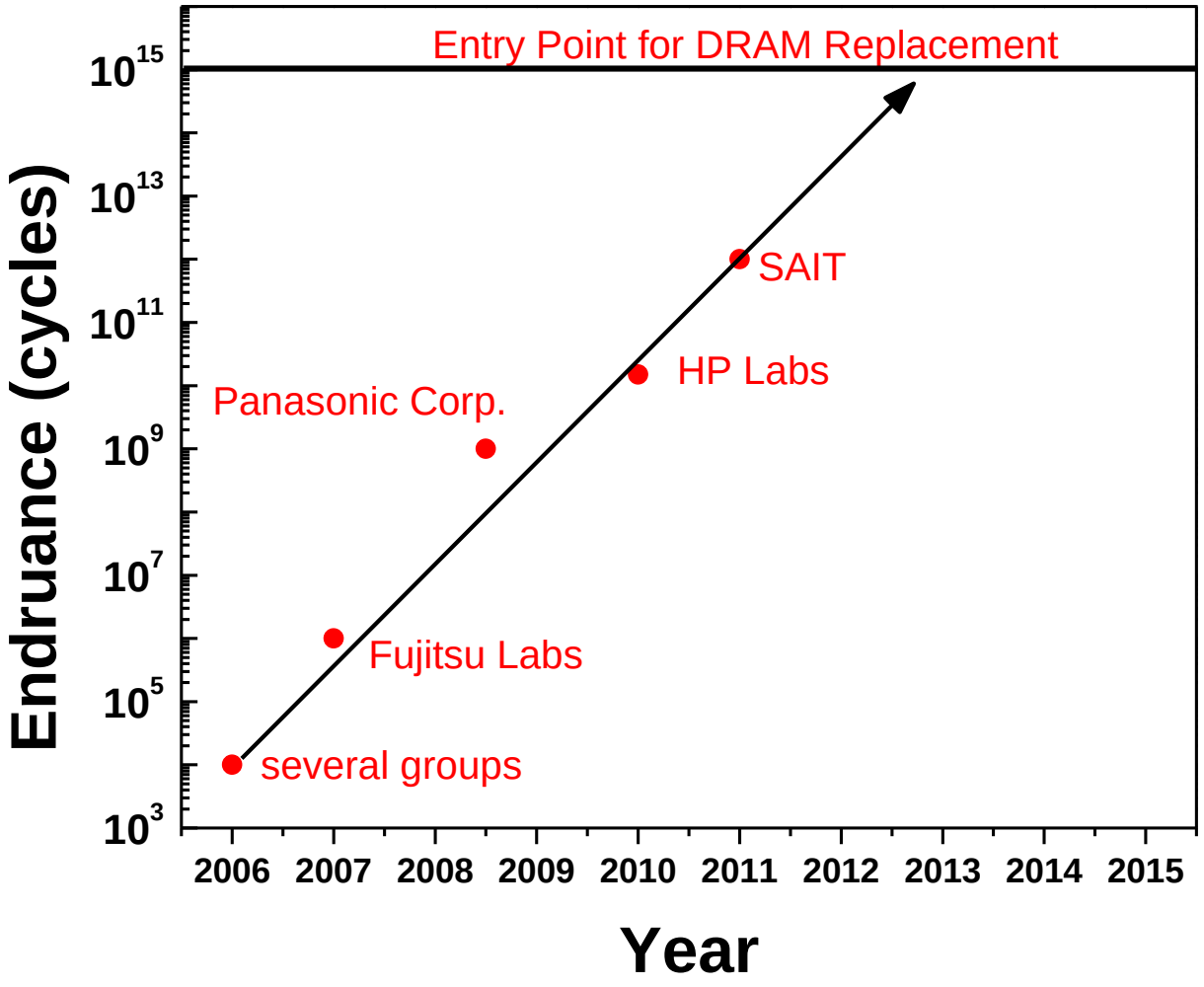
- A very small reverse voltage (a few hundred mV) removes excess silver from the electrolyte
- Device is easily erased
- Excess silver is replaced on the silver electrode in an easily reversible reaction



Courtesy D.K. Schroder (ASU)

ReRAM Endurance Improvements

Will this trend continue?

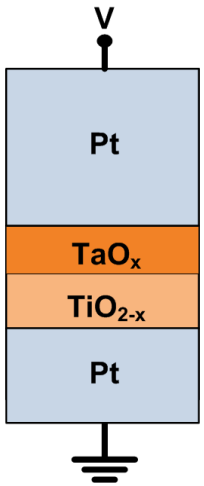


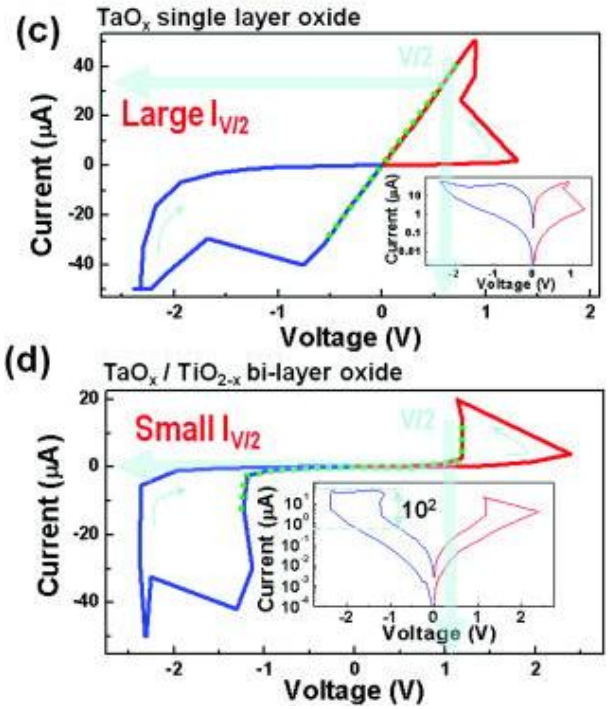
Courtesy J. Joshua Yang (HP Labs)

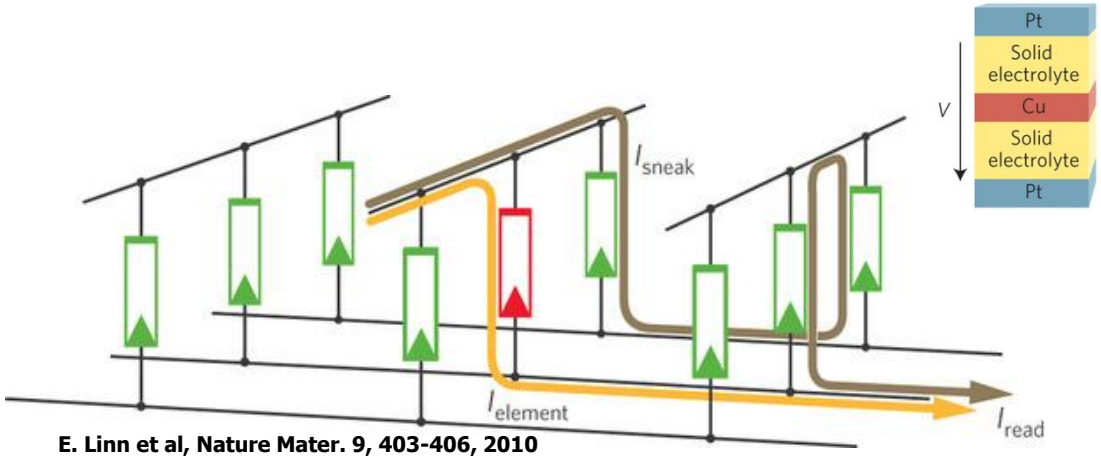
Select Device

- Major open issue with ReRAM
- I-V linearity governs array size
- Limits the array size
- DO NOT want a MOSFET
  - Kills scaling!
- Solutions:
  - Bilayer Nonlinearity
  - Complementary Resistive Switch

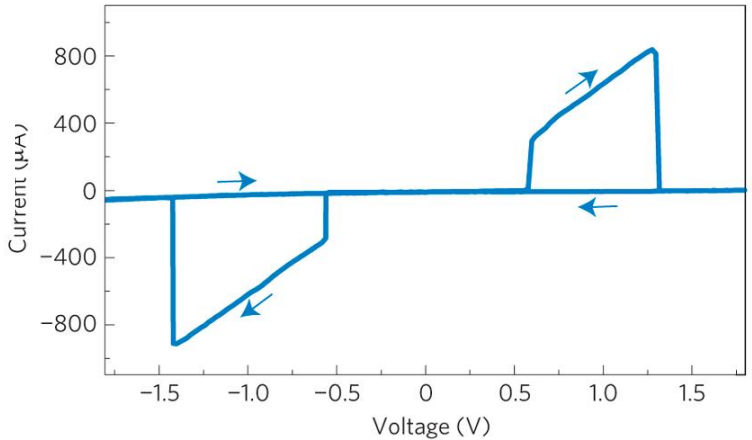
J. Yang et al, APL 100, 113501, 2012.





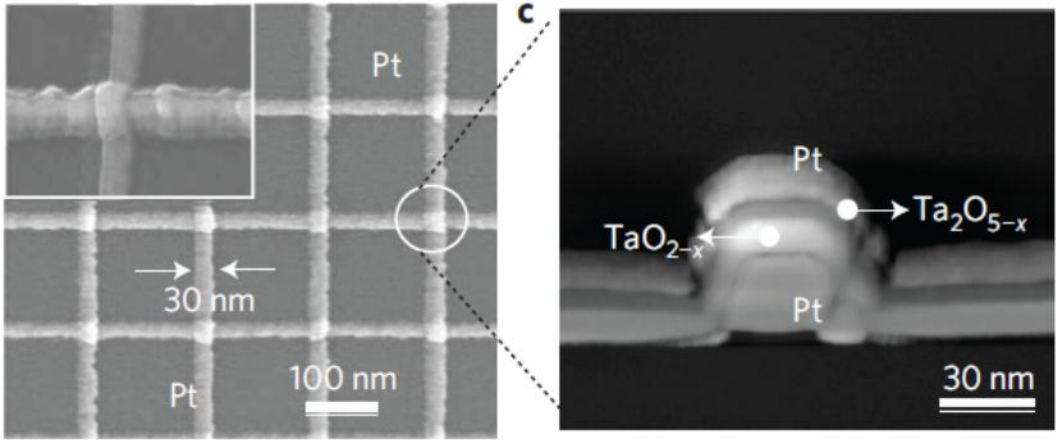


E. Linn et al, Nature Mater. 9, 403-406, 2010

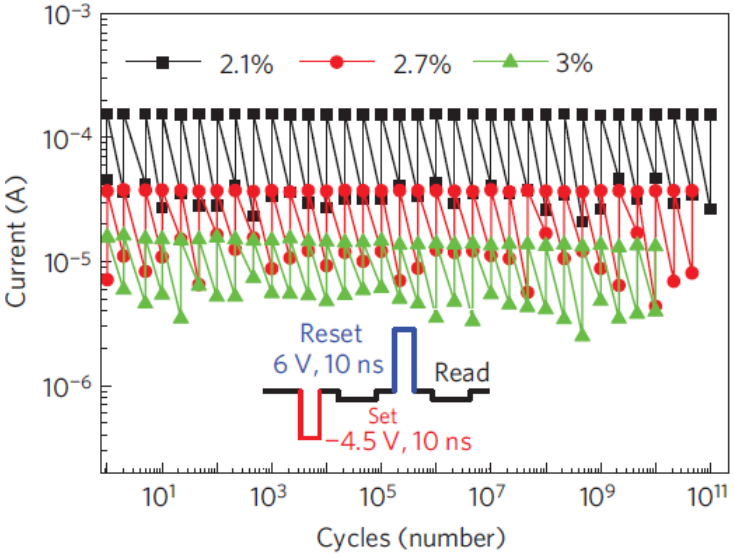


Current State of the Art

- **Records as of February 2012**
  - **Endurance 10^{12} (Samsung, TaO_x, shown below)**
  - **Scalability 10x10 nm^2 ($1F^2$), (IMEC HfO_x, right)**
  - **Switching time < 500 ps (HP Labs, TaO_x)**
  - **Retention >> 10 y (estimate by HP Labs),**
  - **Switching energy < 0.1 pJ/bit (HP Labs, TaO_x)**
- **State of the art is rapidly advancing**

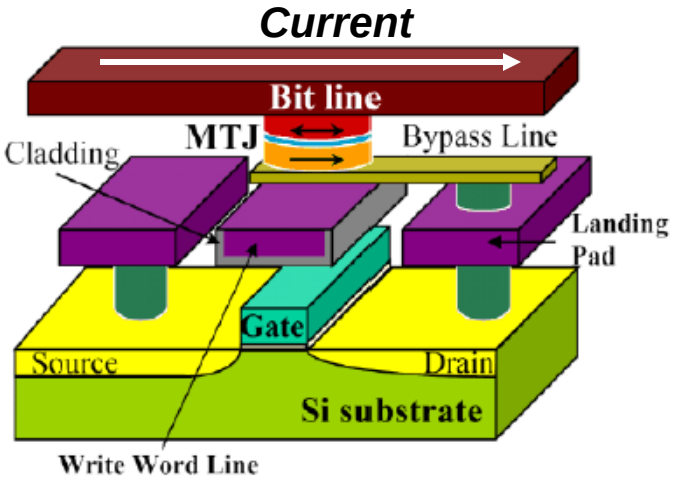


M.-J. Lee, *et al.*, *Nat Mater,* vol. 10, pp. 625-630, 2011.

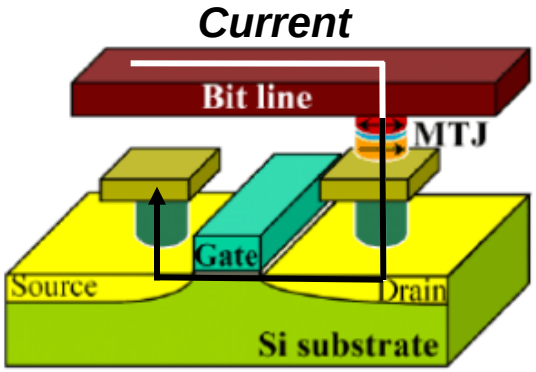


Spin Torque Transfer MRAM

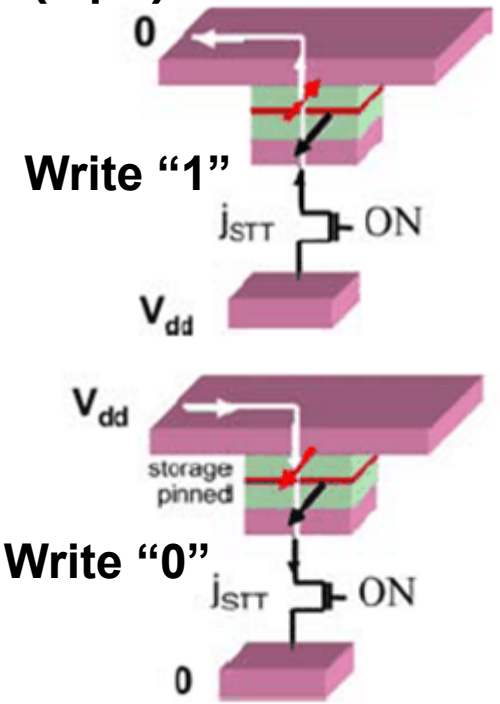
- Spin transfer: electron current through 2 ferromagnetic layers separated by thin nonmagnetic spacer ; magnetization manipulation instead of long-range Oersted field generated by remote current
- Current →spin polarized by transmission through first ferromagnetic layer (pinned reference layer); maintains this polarization as it passes through spacer and enters/interacts with second ferromagnetic layer (free layer)
- Field switched MRAM: complex cell architecture, high write current (~ mA)
- STT: current through MTJ, much lower switching current (~ μA)



Field Switched MRAM



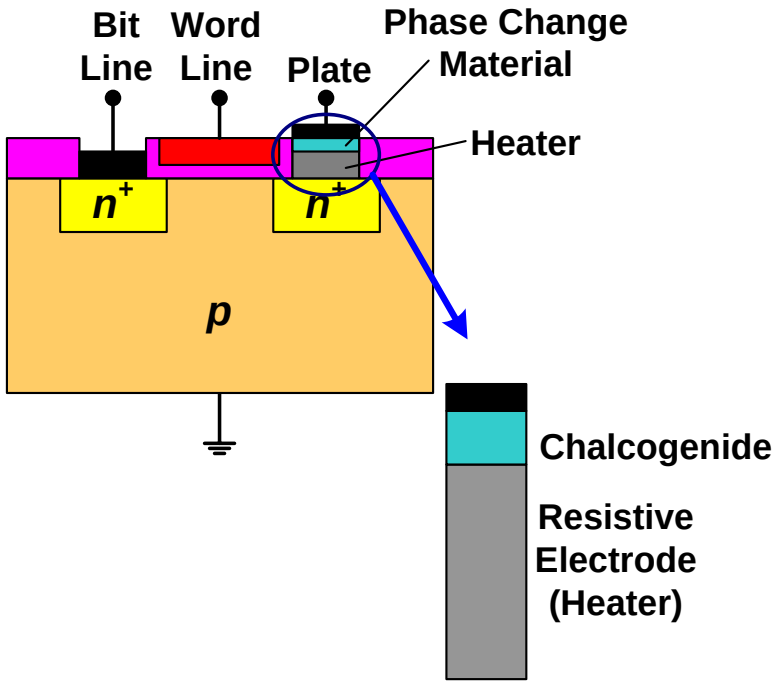
SST MRAM



Courtesy Dieter Schroder, ASU

Phase Change RAM

- Chalcogenide alloy ($Ge_2Sb_2Te_5$ (GST)) is heated and cooled
- Heated *above* melting point ⇒ amorphous
  - Rewritable CD, DVD
    - Laser ⇒ *low* reflectance
  - Memory
    - Current ⇒ *high* resistance
- Heated *below* melting point ⇒ crystalline
  - CD, DVD
    - Laser ⇒ *high* reflectance
  - Memory
    - Current ⇒ *low* resistance

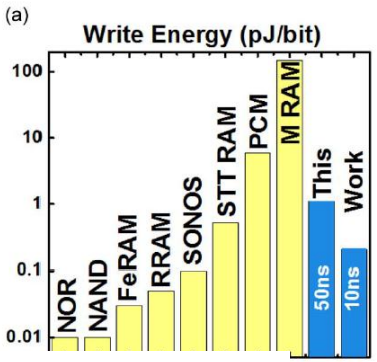


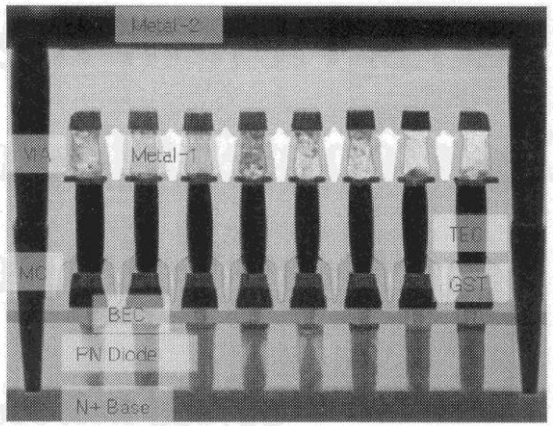
- Reset pulse
  - T = 650°C > T_m = 620°C melts and transforms the GST into high resistance amorphous state
- Set pulse
  - T = 550°C < T_m, crystallizes the material

Courtesy Dieter Schroder, ASU

Phase Change RAM

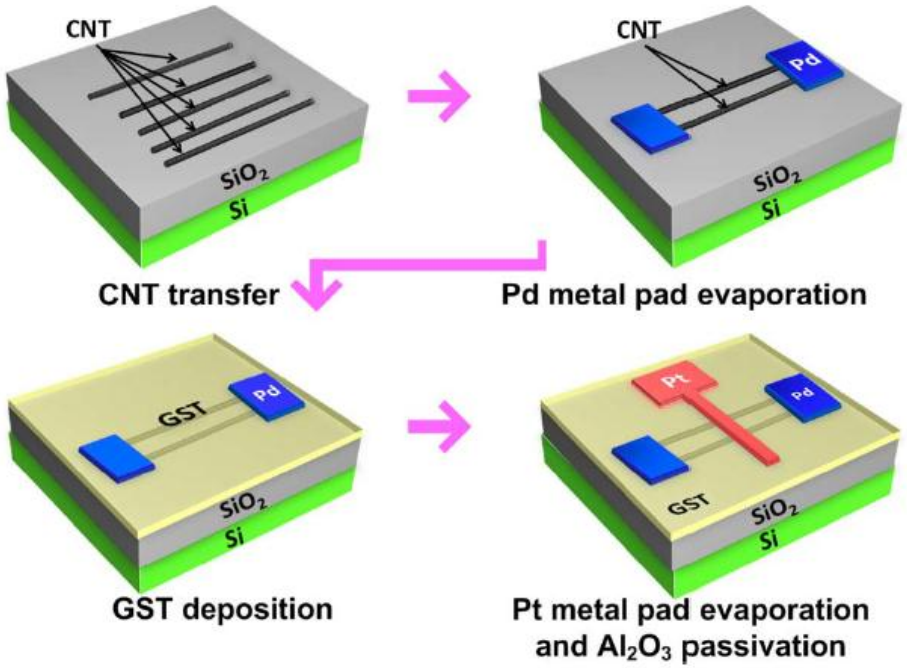
- **Problem**
  - **High reset current (~ 500 μA)**
- **Solution**
  - **Small contact area**
  - **Heat confinement**

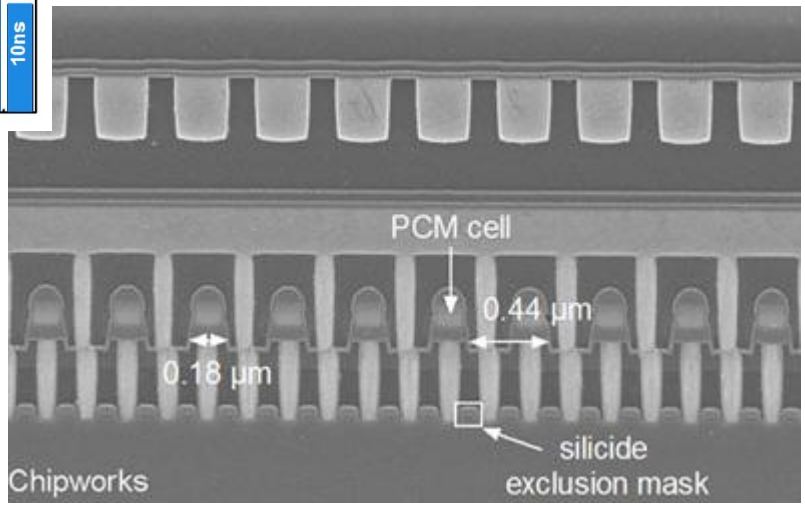




Samsung 512 Mb Array

Liang, TED 59, 1155-1162, April 2012





Numonyx PCM cell consists of a layer of $Ge_2Sb_2Te_5$, embedded in a dielectric structure and in contact with two electrodes

Images courtesy Dieter Schroder, ASU

Sandia National Laboratories

Emerging Nonvolatile Memories

The infamous comparison chart

Biggest challenge for ReRAM: Catch-up

	DRAM	Flash (NOR-NAND)	ReRAM/Memoristor	STT-MRAM	PC-RAM
2012 Maturity	Production (30 nm)	Production (18 nm)	Development	Production (65 nm)	Production (45 nm)
Min device size (nm)	20	18	<10	16	<10
Density (F^2)	6	4	4	8-20	$4F^2$
Read Time (ns)	< 10	10^5	2	10	20
Write Time (ns)	< 10	10^6	2	13	50
Write Energy (pJ/bit)	0.005	100	<1	4	6
Endurance (W/E Cycles)	$>10^{16}$	10^4	10^{12}	10^{12}	$>10^9$
Retention	64 ms	> 10 y	> 10 y	weeks	> 10 y
BE Layers	FE	FE	4	10-12	4
Process complexity	High/FE	High/FE	Low/BE	High/BE	Low/BE

Biggest challenge for STT-MRAM: Retention/Scaling/Temperature

Biggest challenge for PCM: High erase current

A More Subjective Survey

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
Parameter	**FeRAM**	**STT-MRAM**	**PCRAM**	**Emerging ferroelectric memory**	**Nanomechanical memory**	**Redox memory**	**Mott Memory**	**Macromolecular memory**	**Molecular Memory**
Scalability									
MLC									
3D integration									
Fabrication cost									
Endurance									

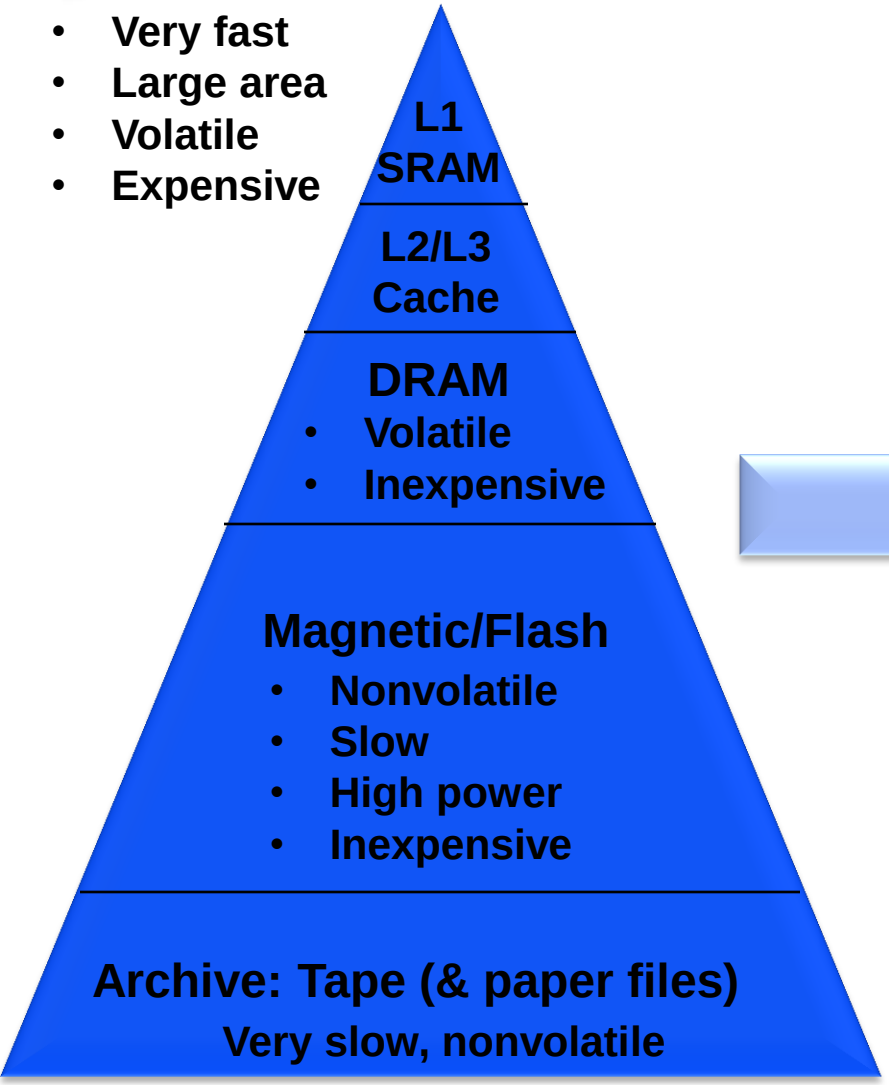
Scalability	F_{min} >45 nm
MLC	difficult
3D integration	difficult
Fabrication cost	high
Endurance	≤1E5 write cycles demonstrated

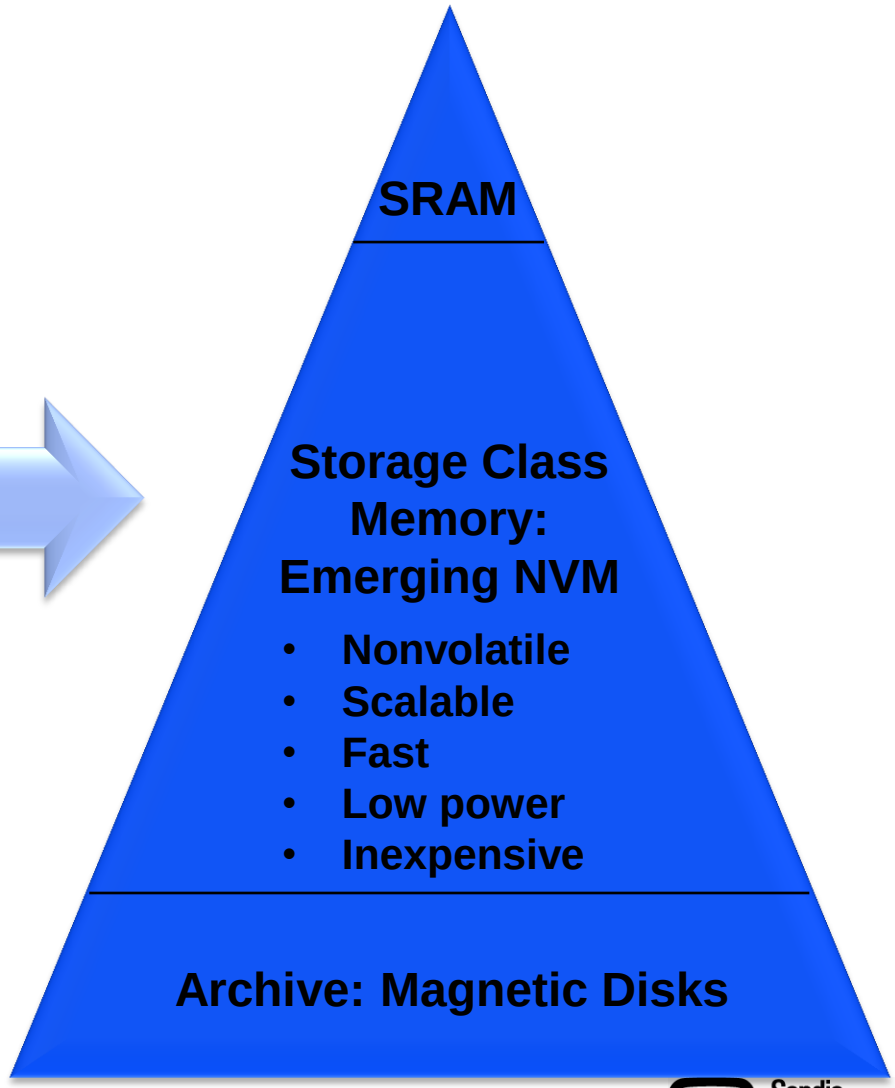
Scalability	F_{min}=10-45 nm
MLC	feasible
3D integration	feasible
Fabrication cost	medium
Endurance	≤1E10 write cycles demonstrated

Scalability	F_{min} <10 nm
MLC	solutions anticipated
3D integration	difficult
Fabrication cost	potentially low
Endurance	>1E10 write cycles demonstrated

Universal/Storage Class Memory: A Game Changer

- Very fast
- Large area
- Volatile
- Expensive



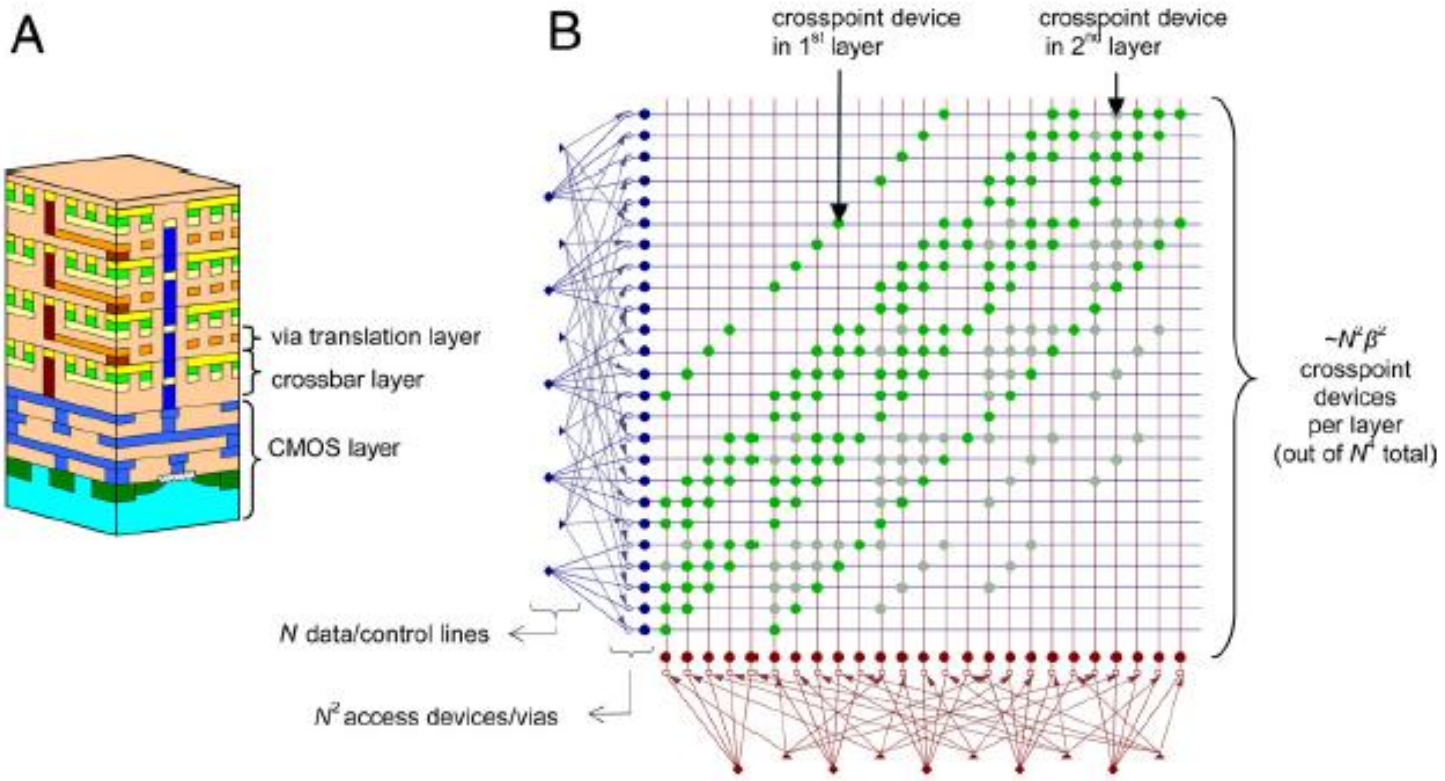


ITRS Requirements for SCM

Parameter	*Benchmark* [A]			*Target*	
	HDD [B]	NAND flash [C]	DRAM	Memory-type SCM	Storage-type SCM
Read/Write latency	3-5 ms	~100µs (block erase ~1 ms)	<100 ns	<100 ns	1-10µs
Endurance (cycles)	unlimited	10^4-10^5	unlimited	$>10^9$	$>10^6$
Retention	>10 years	~10 years	64 ms	>5 days	~10 years
ON power (W/GB)	~0.04	~0.01-0.04	0.4	<0.4	<0.04
Standby power	~20% ON power	<10% ON power	~25% ON power	<1% ON power	<1% ON power
Areal density	~ 10^{11} bit/cm^2	~ 10^{10} bit/cm^2	~ 10^9 bit/cm^2	$>10^{10}$ bit/cm^2	$>10^{10}$ bit/cm^2
Cost ($/GB)	0.1	2	10	<10	<3-4

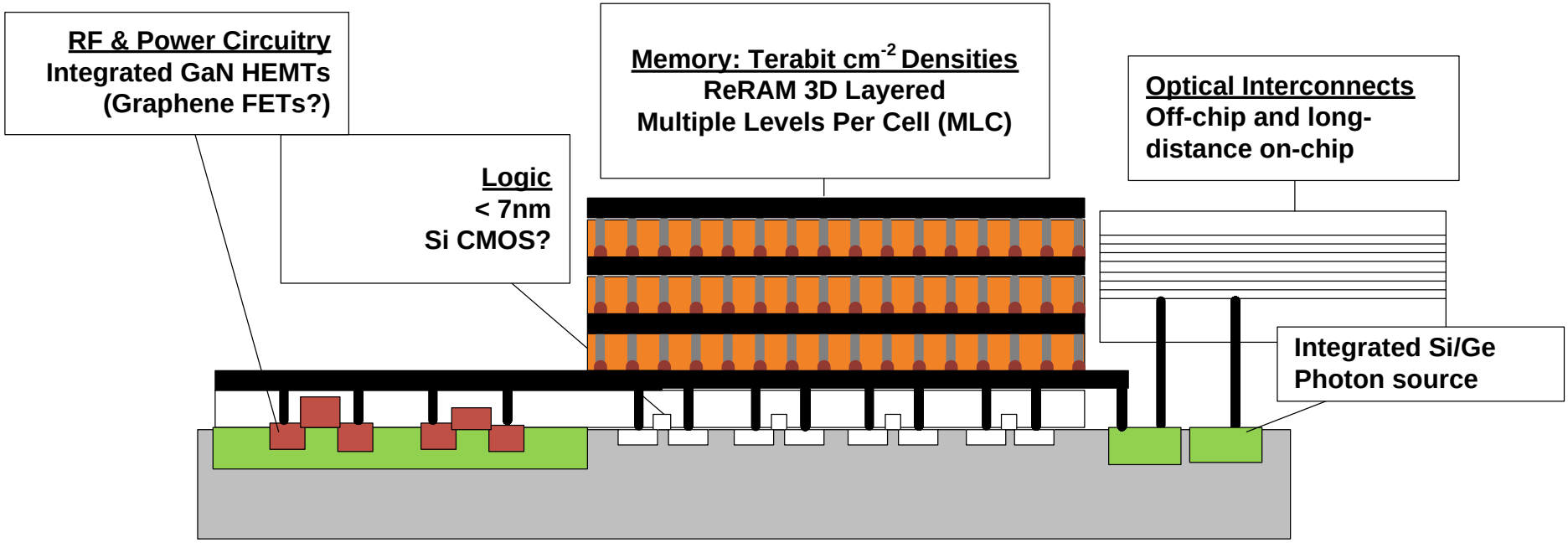
3D Stack Addressing

- **How do we control many layers with a CMOS base layer?**



Strukov et al, PNAS, 2009

What will Universal Memory Look Like?



Outline

- The Status Quo: DRAM, SRAM and Flash
- The Future of Memory
- Memristor Development & CMOS Integration
- Rad-Hard Memory Development
- Novel Applications

Sandia MESAFab

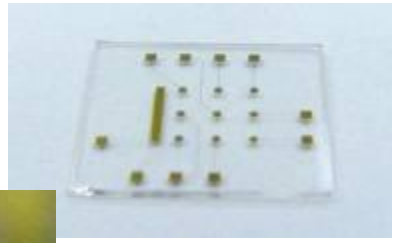
- **Microsystems and Engineering Sciences Applications**
  - **Largest single Federal investment in microtechnology**
  - **$462M capital line item; completed in 2008**
  - **391,000 square feet of fab, lab, and office space**
- **Useful to create any hardware imaginable**

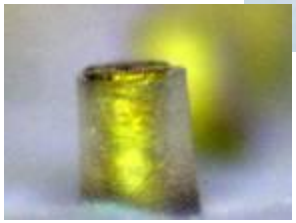
U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

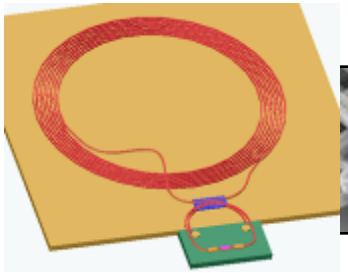
MESA Complex

Enabling Microfabrication Technologies

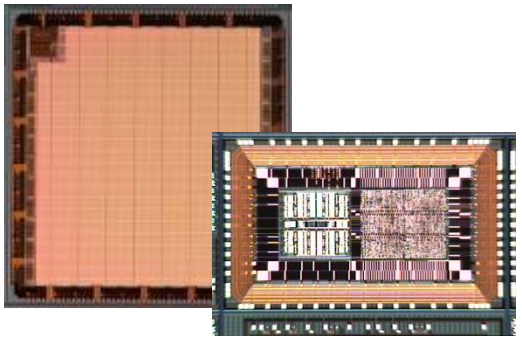




Flexible Fabrication

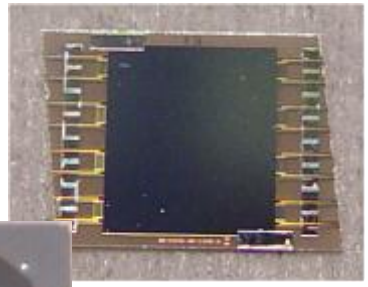


Photonics

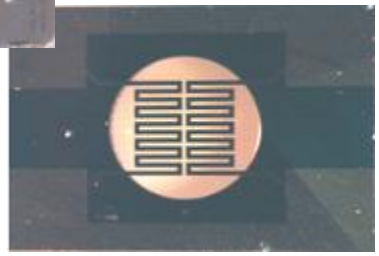


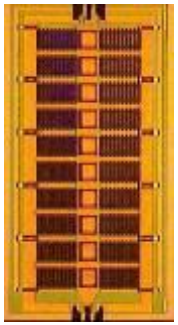
Si CMOS

Piezoelectrics



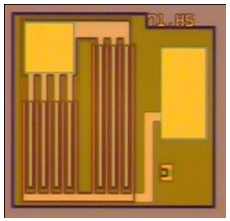
Si Bulk Micromachining





3.6mm

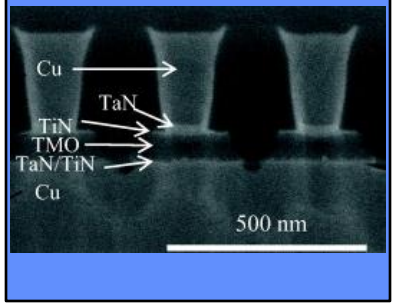
1.8mm



HBT Compound Semiconductors

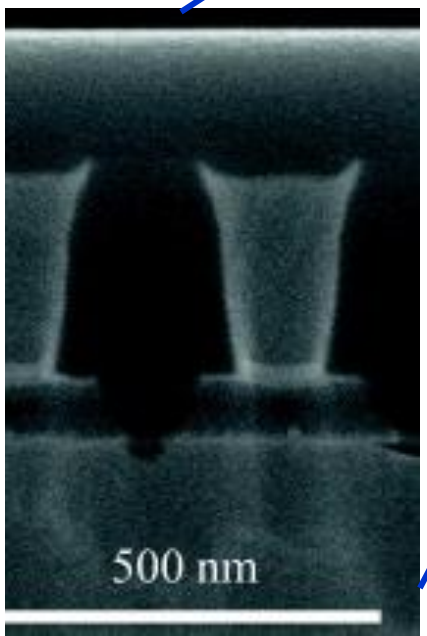
Advanced Packaging

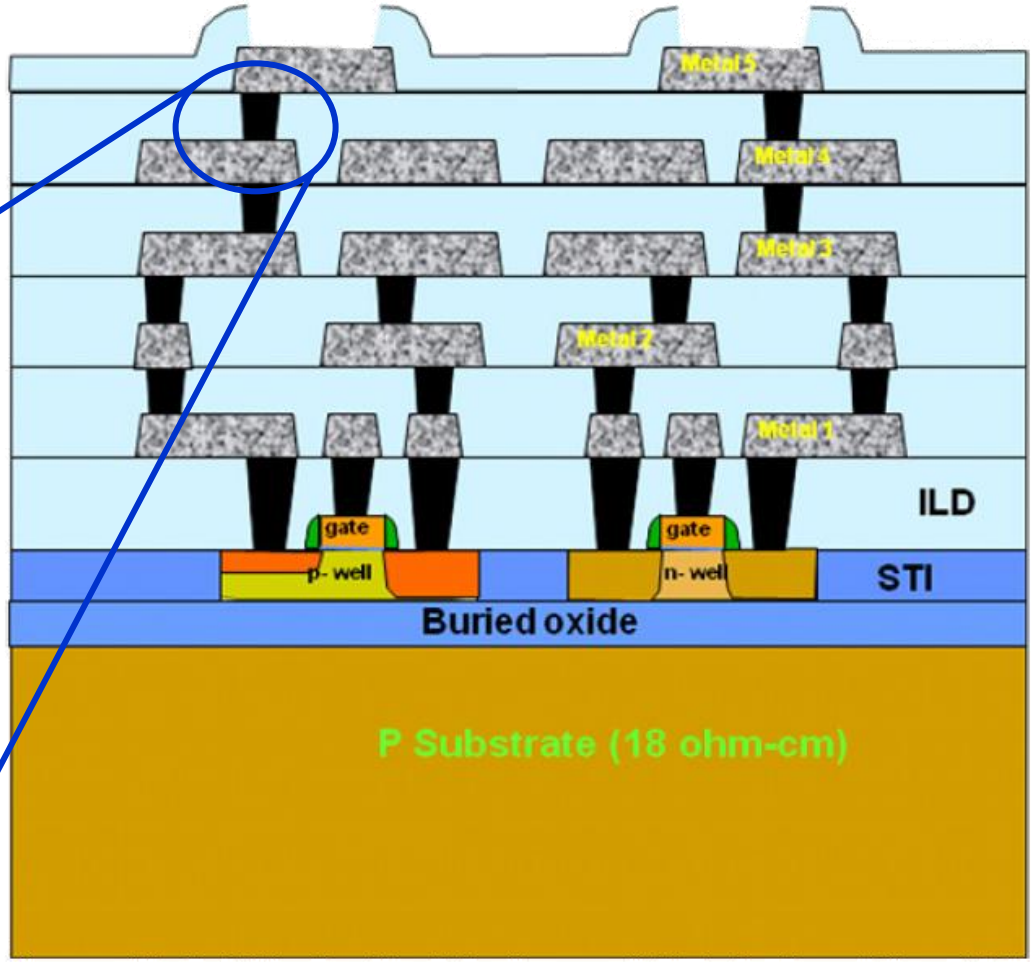
Memristors…



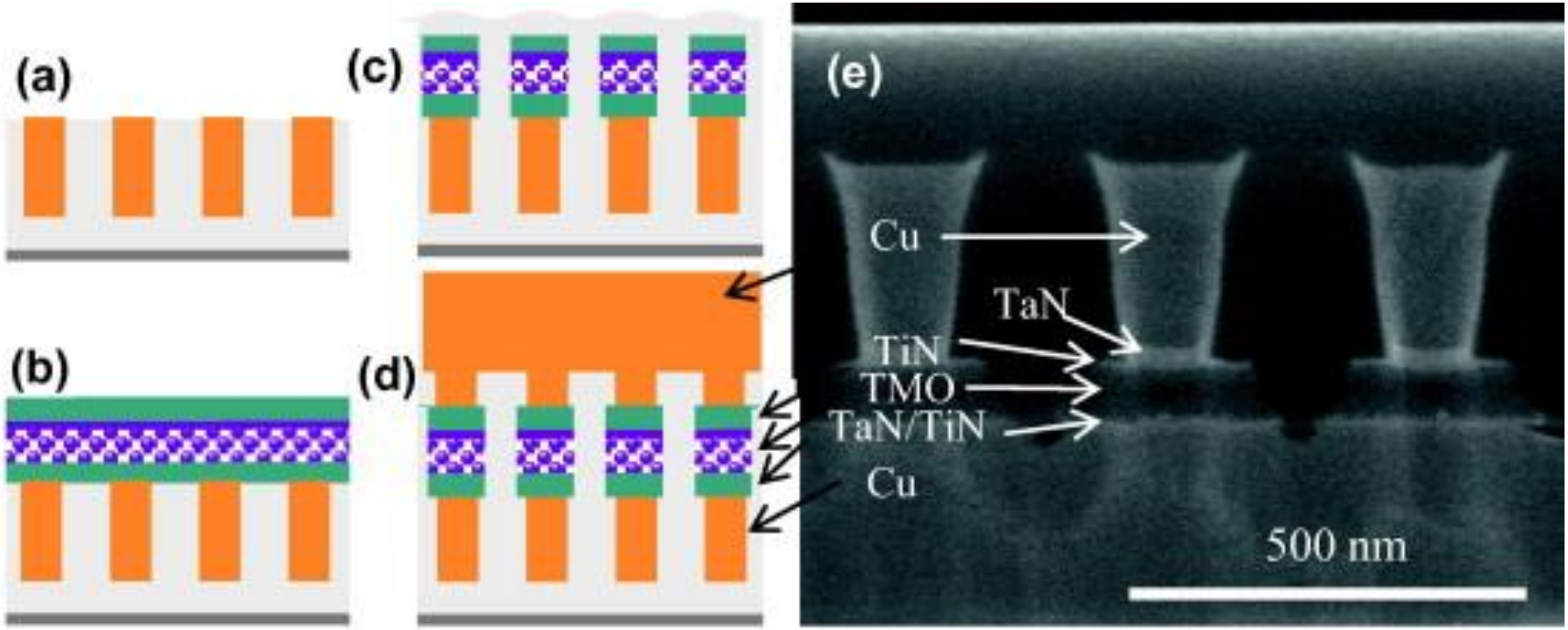
Memristors + CMOS

- **Sandia CMOS7 Process**
  - **3.3V, 350 nm, MOSFETs**
  - **Rad-hard**
- **Baseline for memristor integration**





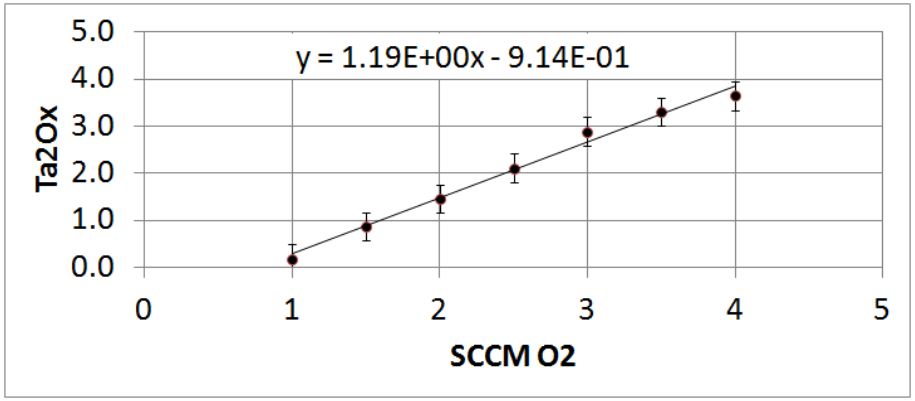
Memristor Fabrication Process

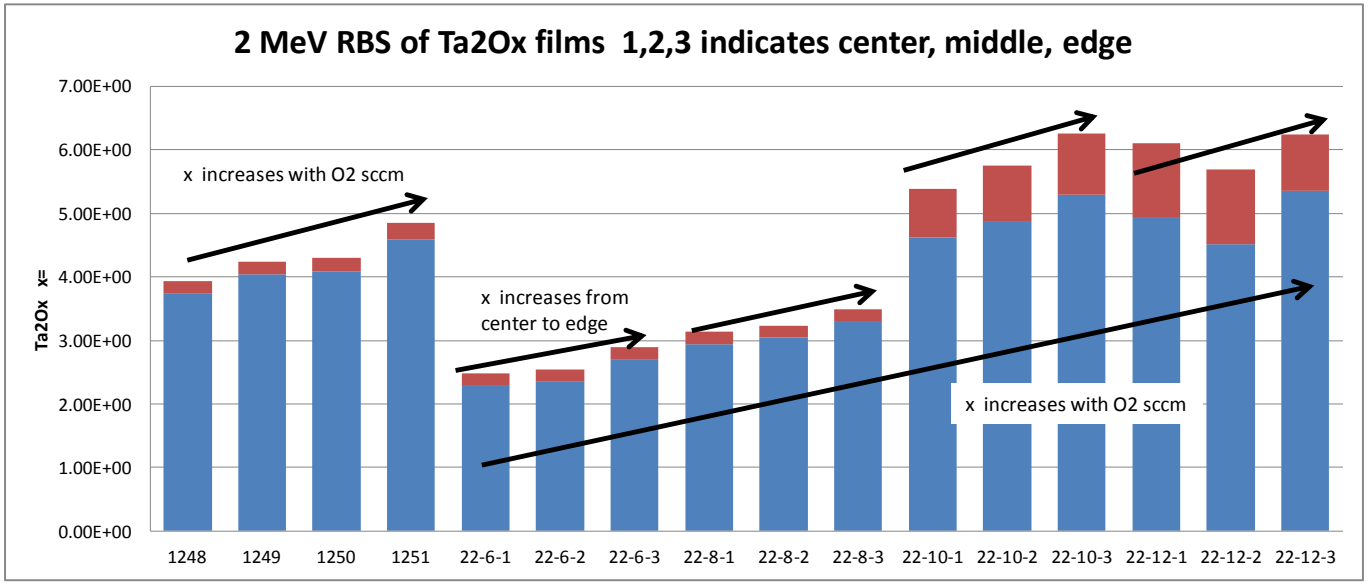


J. Nickel et al, Microelectron Eng, 2012

Film Development

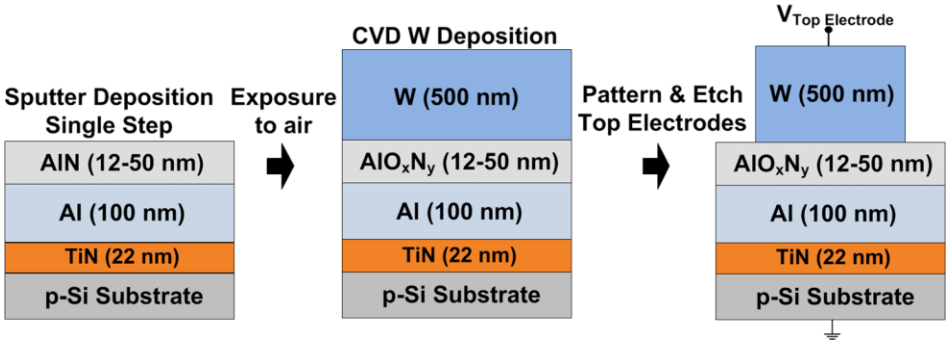
- **Creating exact stoichiometry is key**
- **Substoichiometric tantalum oxide: TaO_x**
  - **$x \approx 2$**

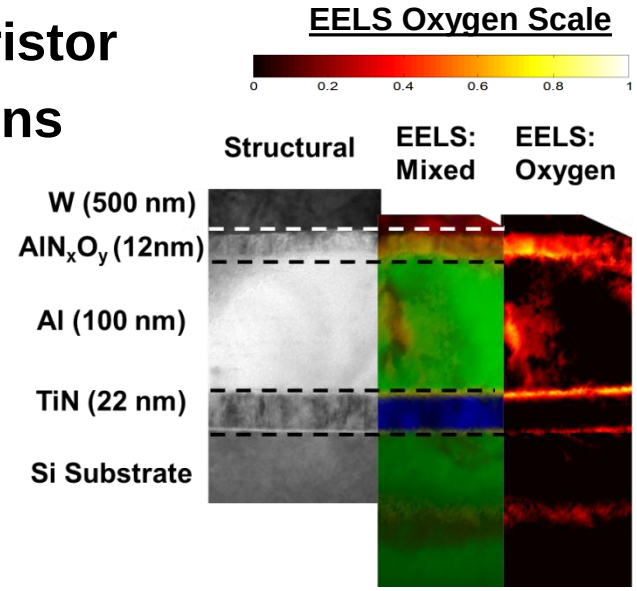


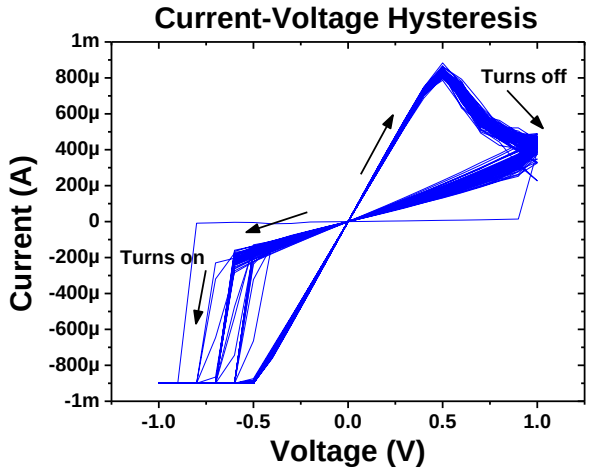


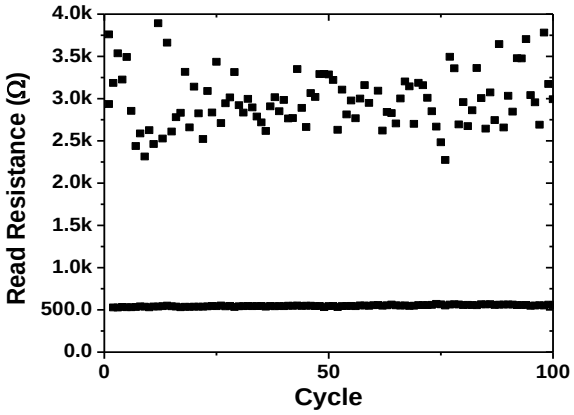
Novel Materials: AlO_xN_y

- We recently discovered the AlO_xN_y Memristor
- May be promising for rad-hard applications





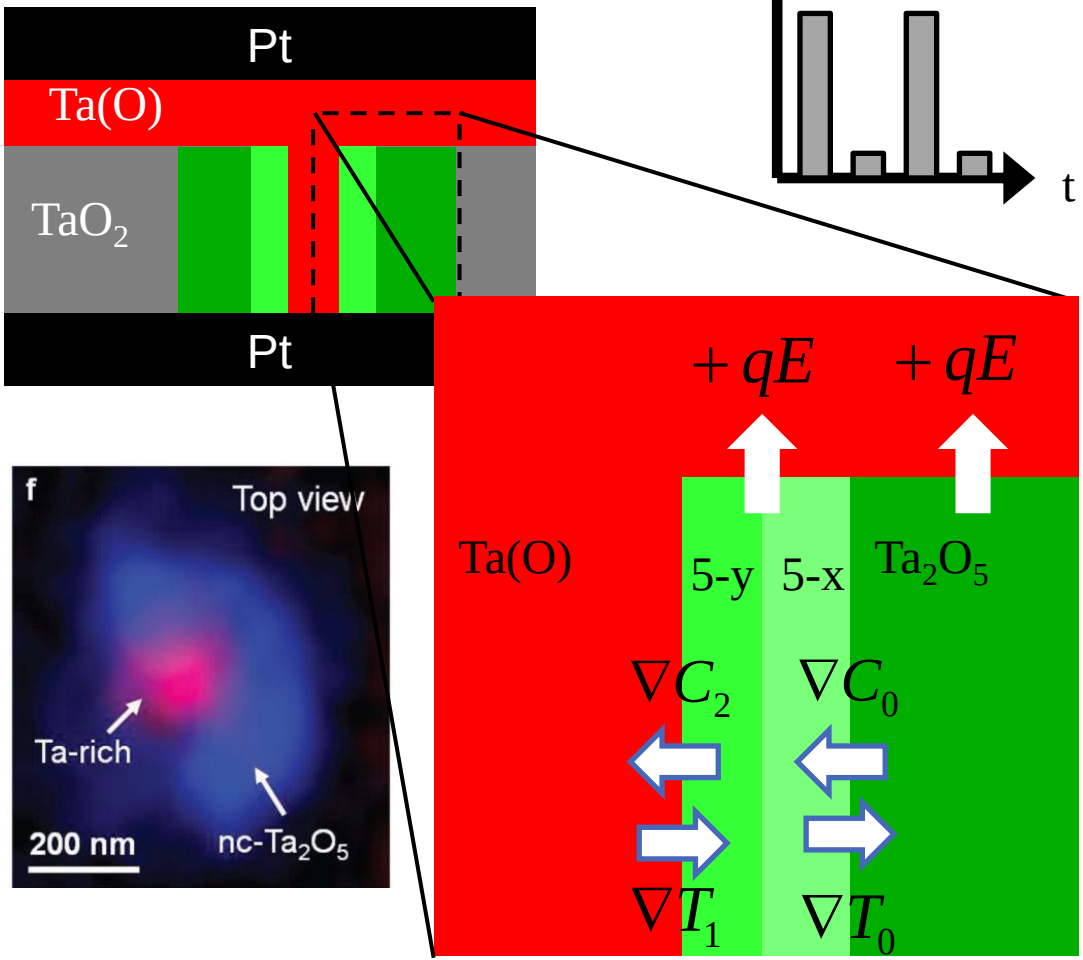




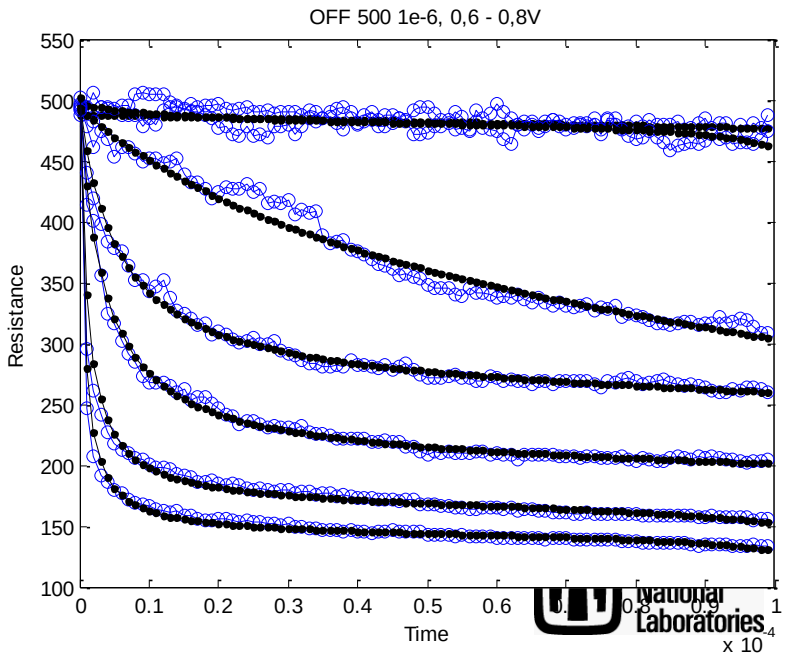
Mixed EELS Key
Red = W
Green = Al and Si
Blue = Ti-N
Yellow = Al-N-O

Electrical Modeling

$$\frac{\partial r}{\partial t} \propto a\nabla C - b\nabla T \pm c\,qE(r_{ON}^2 - r^2) \Rightarrow R(t) \propto \frac{1}{[x_1 + x_2 \tan(\frac{t + x_3}{x_2})]^2}$$



Pulsing provides fine tune control over resistance state

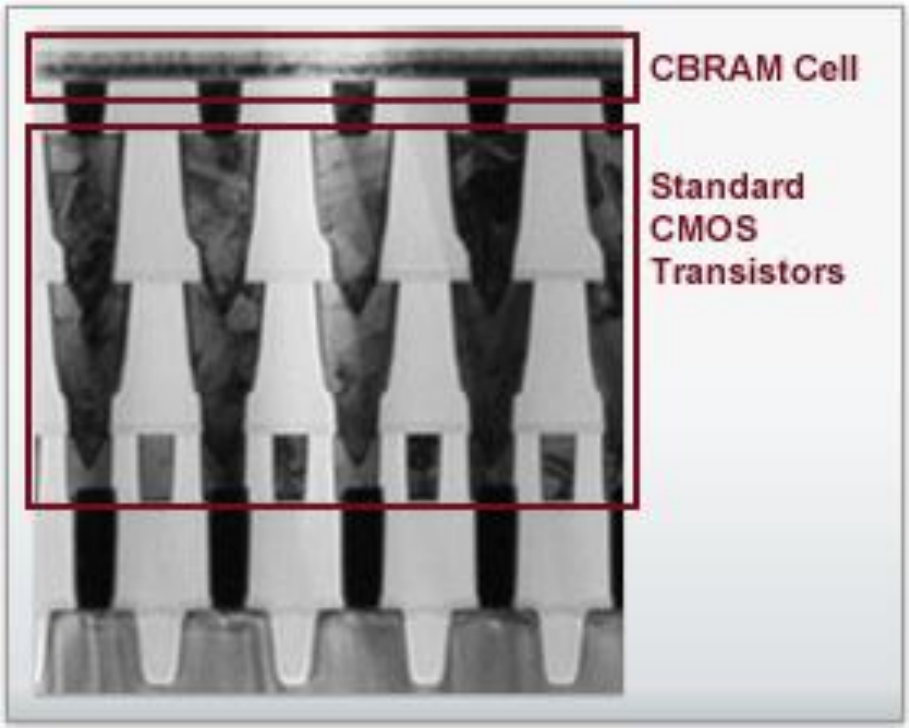


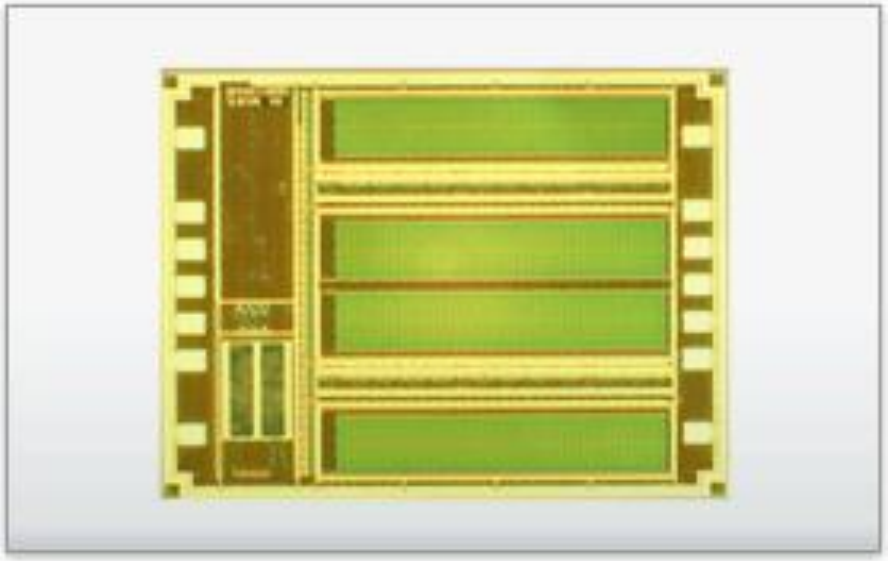
Adesto Commercial CBRAM Product

AXON Technologies Corporation

ASU Arizona State University

adesto™ TECHNOLOGIES





adesto.com

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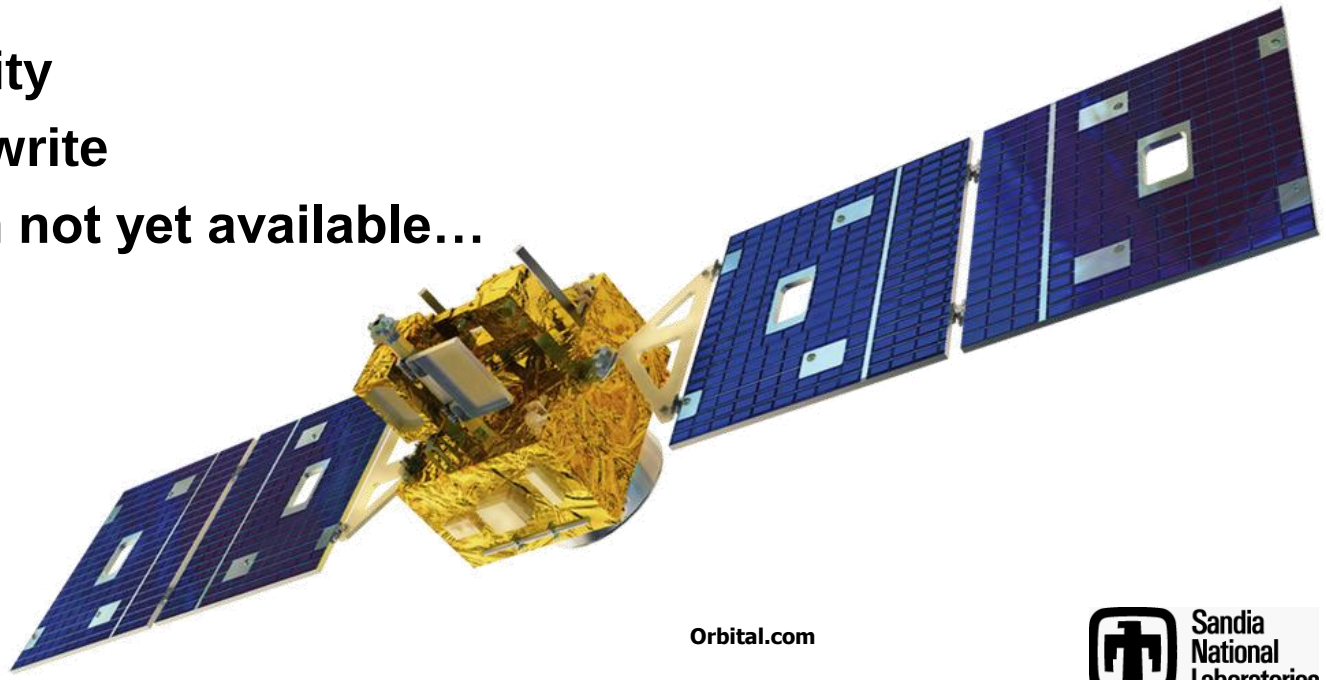
Space Computing

- Sensors can collect terabytes of data
- Stringent computer/memory requirements
  - Radiation-hard: Total dose, single event, etc.
  - High reliability (10-15 year missions)
  - Low energy
- Desired
  - High density
  - Fast read/write
- Ideal solution not yet available…

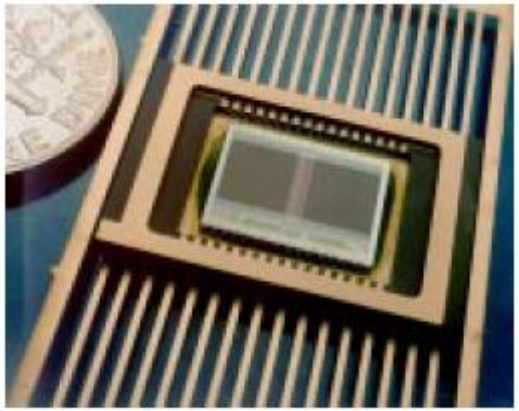


Orbital.com

Rad-Hard Nonvolatile Memory

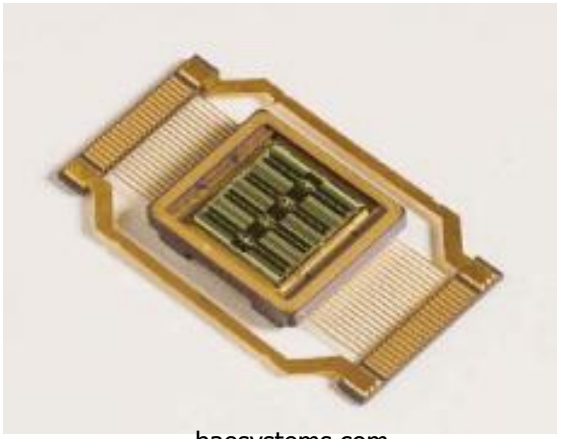
- Commercially available rad-hard nonvolatile memories
- NG EEPROM: 1Mbit, 100ms write, 10^4 cycles, 1.25µm RHCMOS
- BAE C-RAM: 4Mbit (planned 20 Mbit), 70ns write
- Honeywell MRAM: 16Mbit die, 140ns write, 10^{12} cycles
- *Rad-hard memory requires a rad-hard CMOS base process*

NG Rad-hard EEPROM



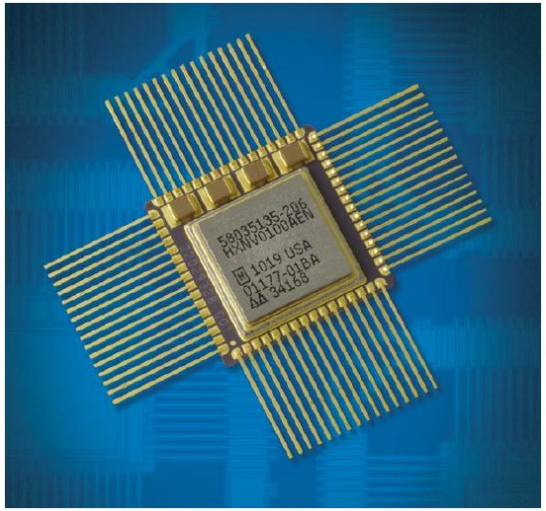
Rad Hard 256K EEPROM
northropgrumman.com

BAE C-RAM



baesystems.com

Honeywell M-RAM



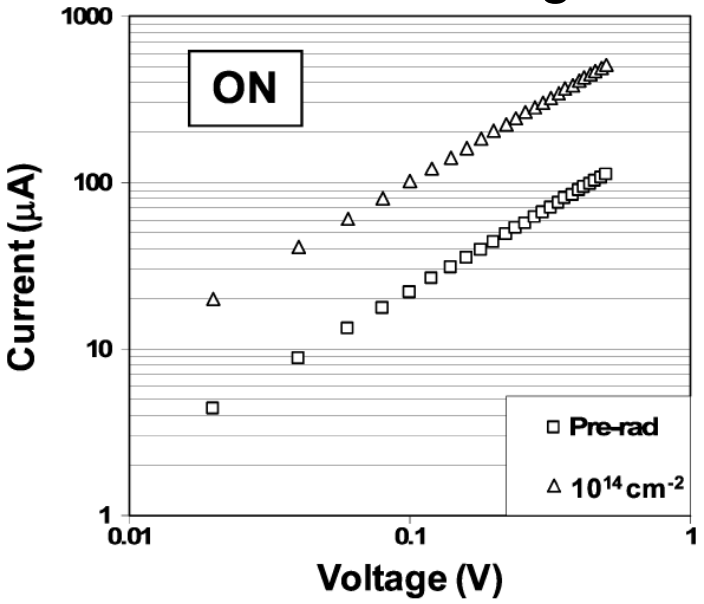
honeywell.com

Rad Hard Memory Requirements

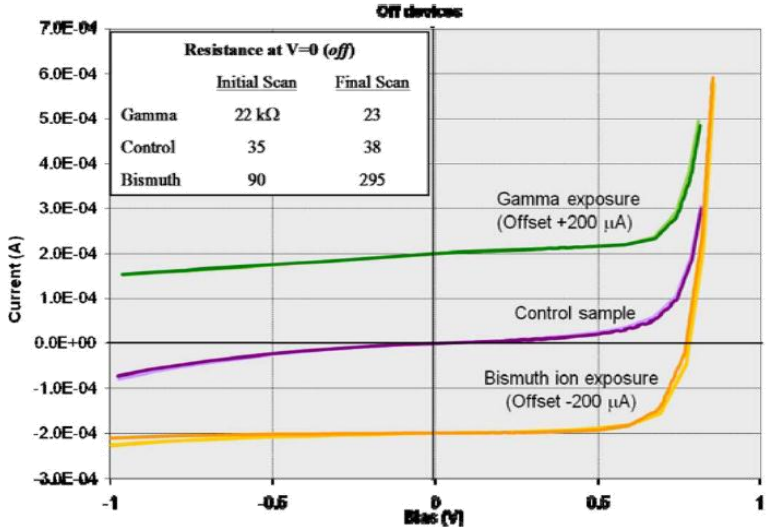
- Space and supercomputing stand to benefit from commercial progress in emerging NVMs:
  - Low power
  - Fast read/write
  - High endurance
  - High density
  - Long retention
  - Non-volatility
- Resiliency and fault-tolerance
- HPC and space benefit from radiation hard
  - SEU *is* a problem for supercomputers

Previous Rad-Effects Work

- TiO_2 memristors
  - Aerospace: no degradation under 45 Mrad(Si) γ-rays and 23 Mrad(Si) Bi ions
  - Arizona State University: Significant changes in R_{OFF} after fluence of 10^{14} cm^{-2} alpha particles
- HfO memristors
  - He et al: Little degradation after 5 Grad(Si) 1 MeV protons



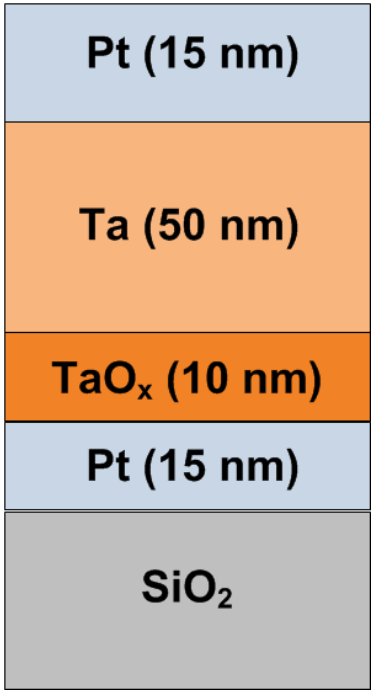
Barnaby *et al.*, *Trans Nuclear Sci,* vol. 58, pp. 2838-2844, 2011.

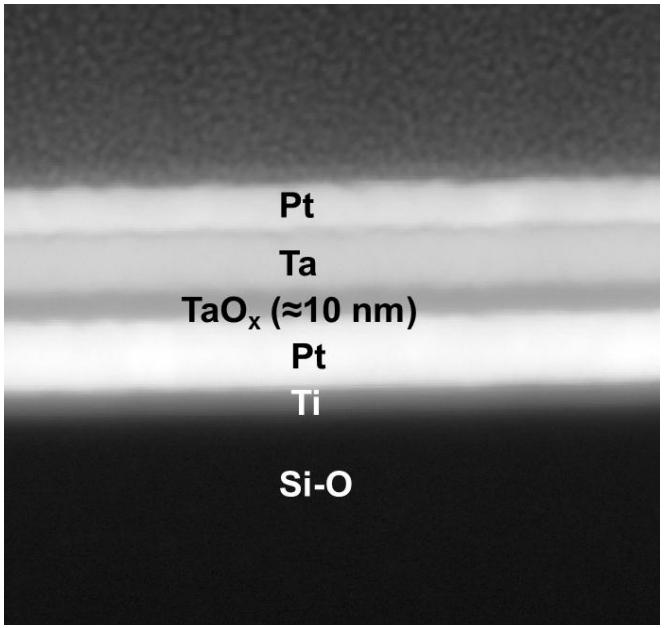


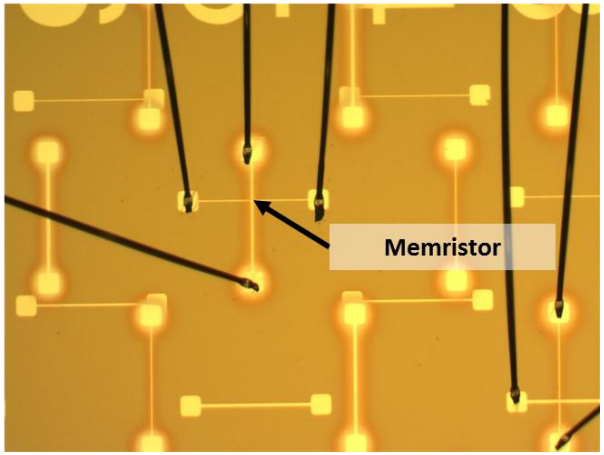
Tong *et al.*, *Trans Nuclear Sci,* vol. 57, pp. 1640-1643, 2010.

Recent Work at Sandia

- All samples use same stack:
  - Si/SiO_2(substrate)/Ti/TaO_x/Ta/Pt
- TaO_x (x<2.5) sputtered from substoichiometric target
- Random "dogbone" shadow mask

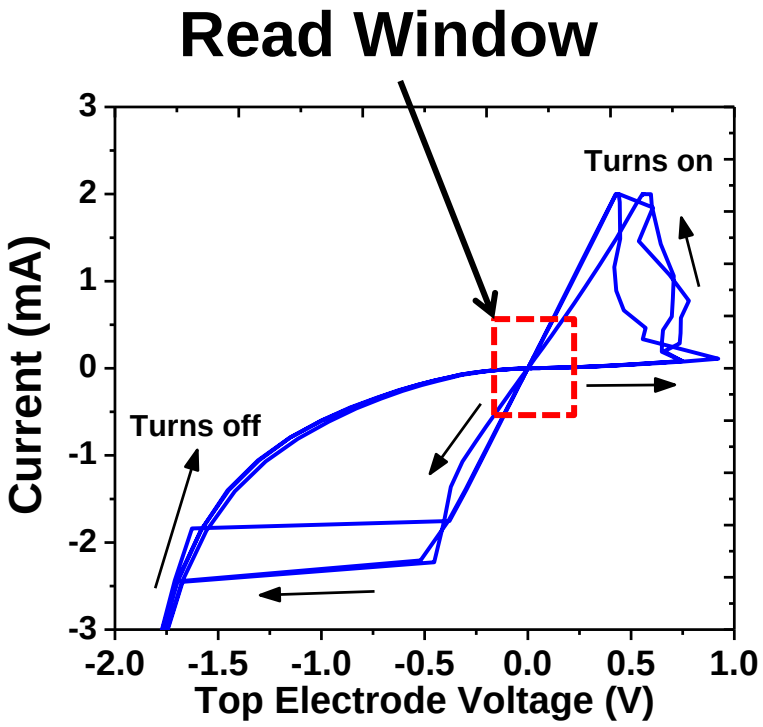


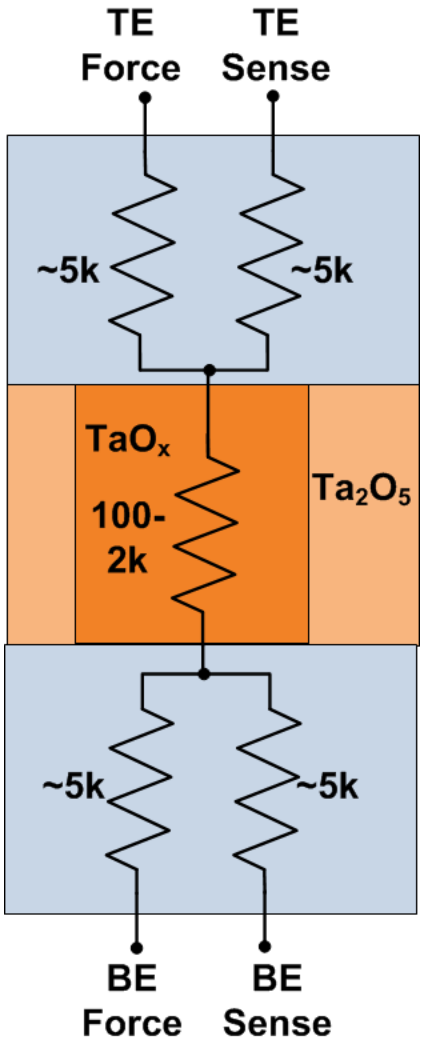




Electrical Characterization

- Devices initially cycled several times
- <u>Write Voltages:</u>
  - Set (on): 800 mV
  - Reset (off): -1.5 V
- <u>Typical Resistances:</u>
  - $R_{ON} \approx$ 30-150 Ω
  - $R_{OFF} \approx$ 300-5k Ω
- Grounded during irradiation
- Read after each shot
- Cycle after series of shots

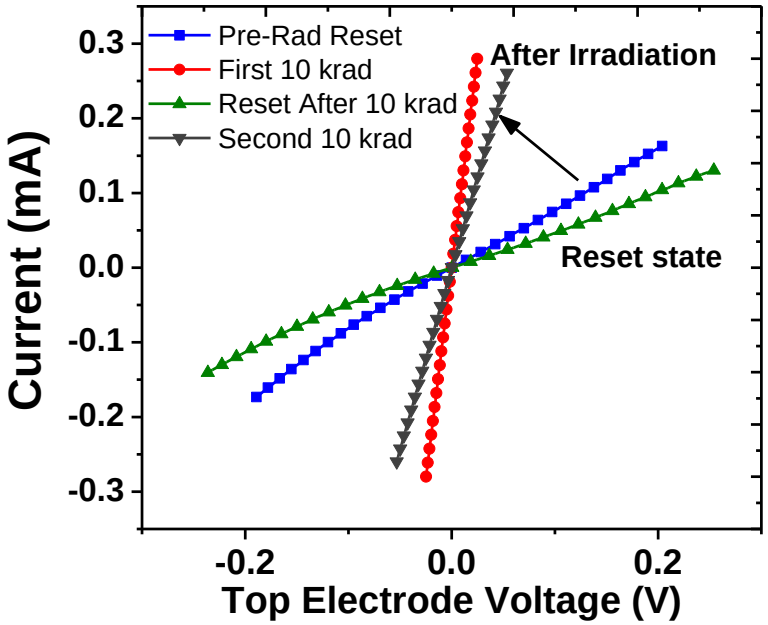




Initial Results: X-ray

- Aracor 4100 10 keV X-ray System
- All pins grounded during irradiation
- Sample removed and replaced to measure resistance change
- Ionization only
- R_{ON} lowered after less than 10 krad(Si)

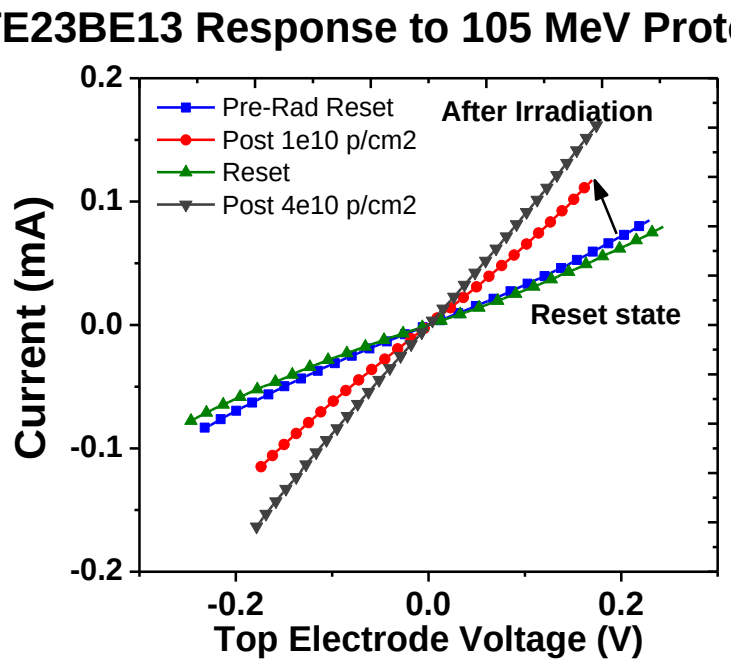
DUT 3 Response to X-ray Irradiation



Dose Rate (rads/s)	Pre-Rad	1667	Reset All	1667	Reset All	166.7	166.7	166.7	Reset All
Total Dose (krads)		10		20		21	22	23	
Incremental Dose (krads)		10		10		1	1	1	
DUT 1 R (ohms)	919 (reset)	74.3	628	223	713	832	871	11.5	*
DUT 2 R (ohms)	176 (set)	93.5	1940	129	1770	362	248	0.84	*
DUT 3 R (ohms)	1660 (reset)	88.5	1900	206	1500	1900	2070	40.3	485
DUT 5 R (ohms)	113 (set)	113	731	834	766	880	918	81.6	756
DUT 6 R (ohms)	1120 (reset)	26.9	439	80.4	354	56.4	56.7	16	*

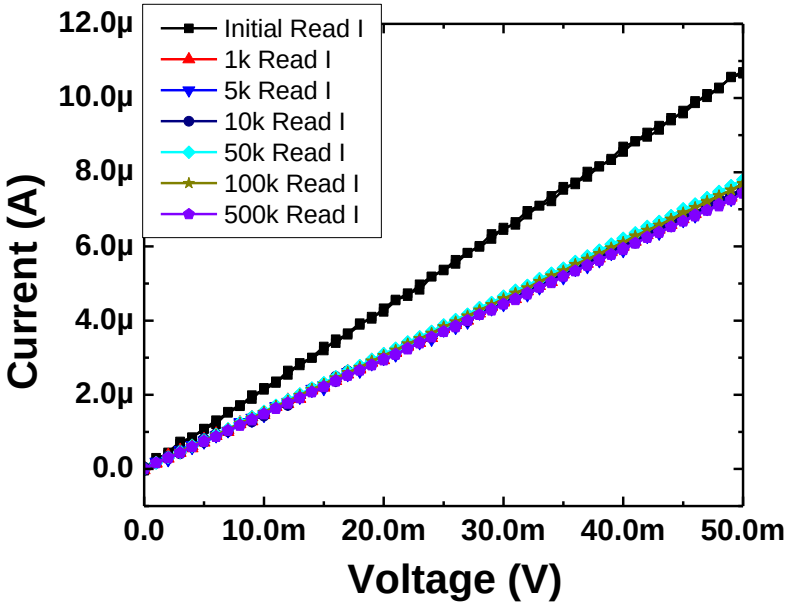
Initial Results: High Energy Protons

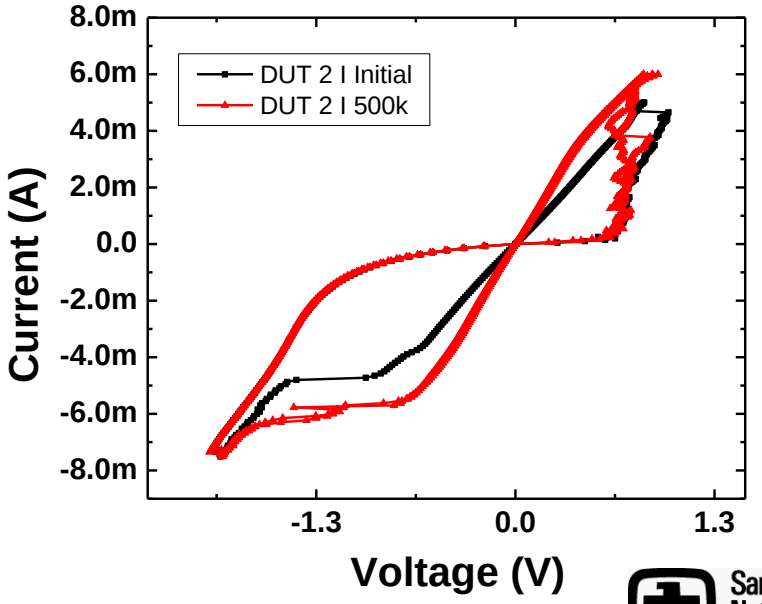
- 105 MeV and 480 MeV proton beam at TRIUMF Proton Irradiation Facility
- Tended to cause change from high to low resistance
- Results not consistent – possible single event effect



γ-rays

- Sandia Cobalt-60 Radiation Source, 53 rad/s
- In situ electrical testing, all pins grounded during irradiation
- R_{OFF} measured between shots, full curve after 500 krad(Si)
- No significant change in R_{OFF} due to irradiation
- Little changes in write characteristics

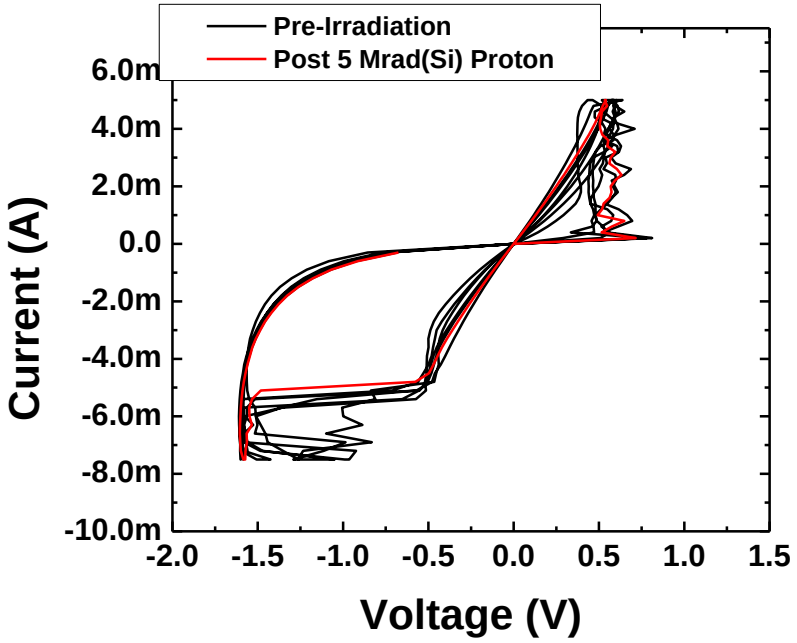




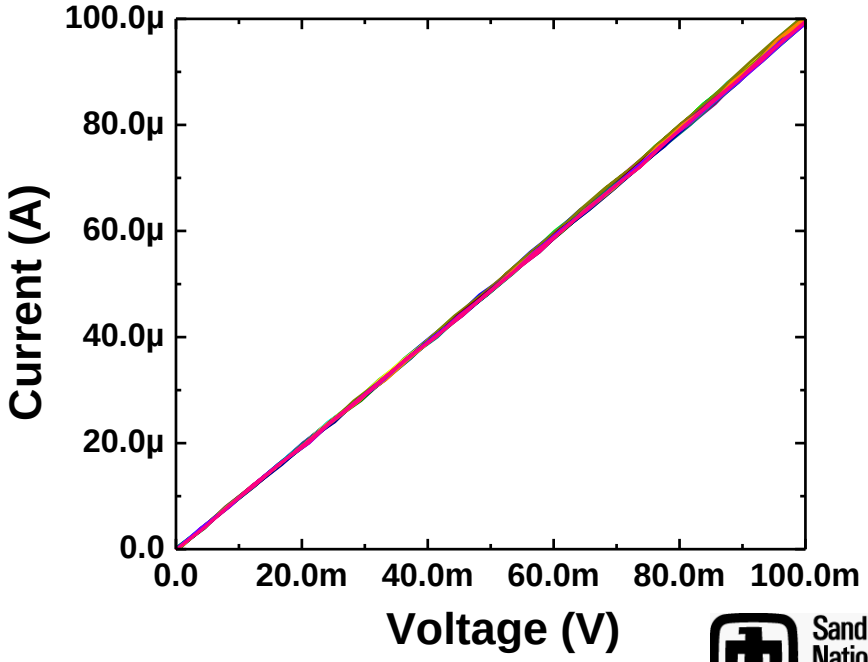
4.5 MeV Protons

- 4.5 MeV proton irradiation at Sandia's IBL
- In situ electrical testing in 10^{-5} torr vacuum
- 1 μm beam rastered across 25x25 μm area
- Little change up to 5 Mrad(Si)

Pre and Post Proton Irradiation I-V

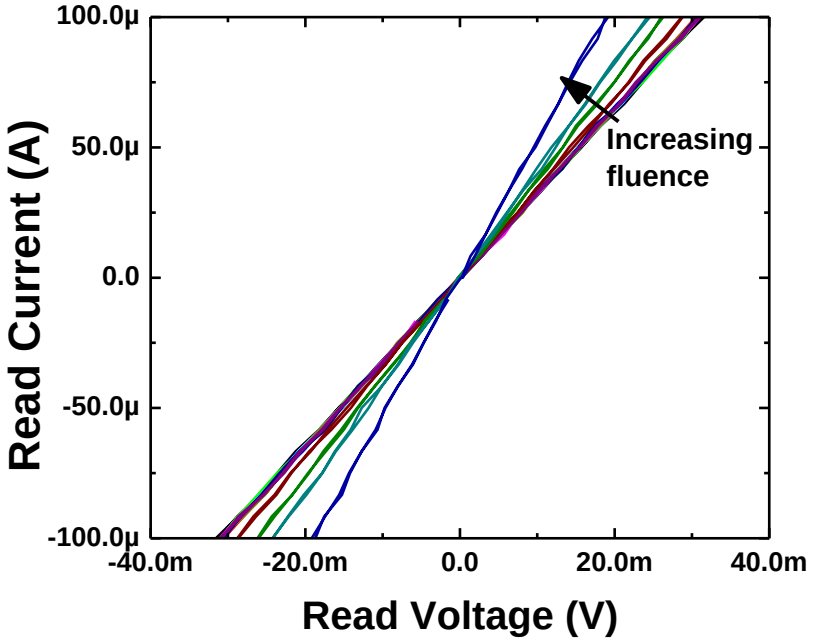


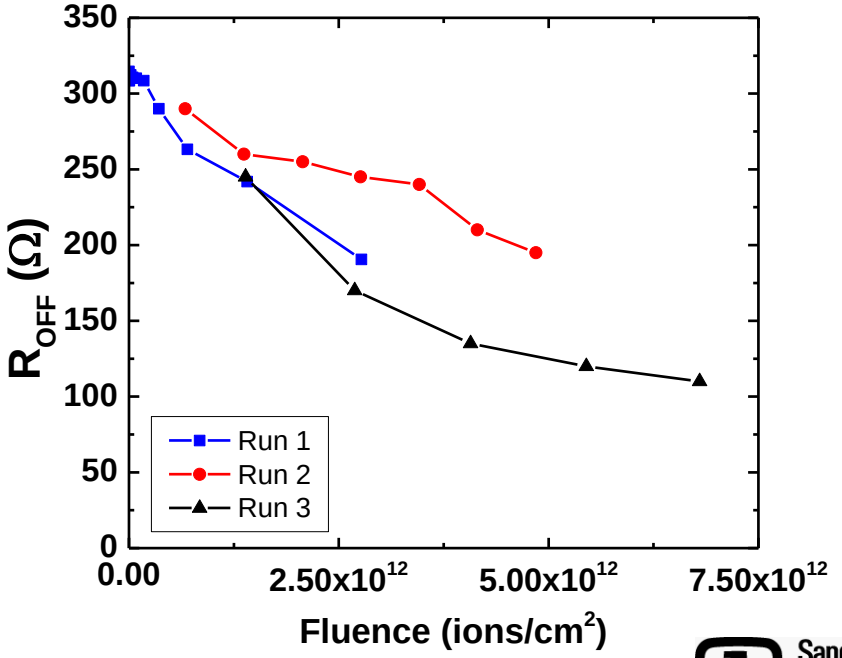
Read I-V Curves Between Proton Shots



800 keV Silicon

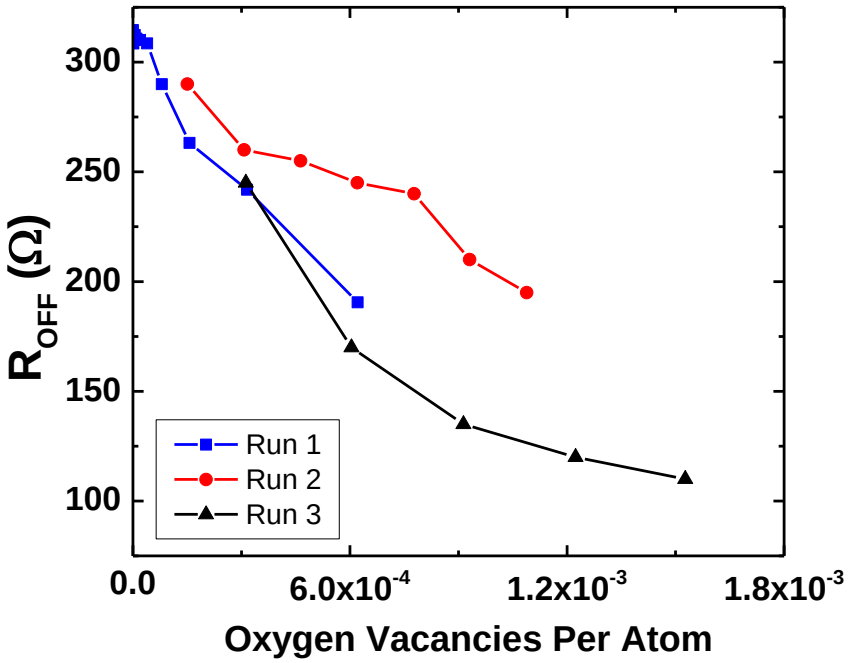
- 800 keV Si beam at Sandia's Ion Beam Laboratory
- All contacts grounded during irradiation
- Device with high R_{OFF}/R_{ON} was not affected by similar fluence

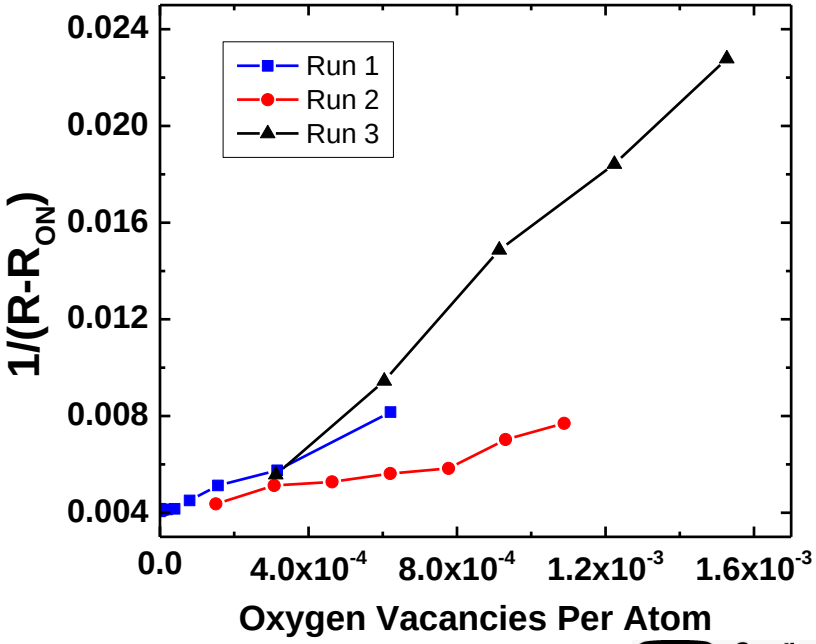




800 keV Silicon

- Drop in resistance expected from TaO_x switching theory
- Off-Resistance decrease exhibits a 1/R dependence
- May give insight as to vacancy concentrations needed for switching
- Effect varies greatly, even in one device





Proposed Mechanism

- **Si ions:**
  - Assume displacement damage dominated
  - Increase in oxygen vacancies expected to lower resistance
  - Fluence may vary with size of channel – indicated by device on/off resistance
- **Ionization damage:**
  - Mechanism less clear
  - Radiation induced photocurrent might create strong enough potential for shift
  - Could explain why higher dose rate X-ray alter devices, low dose rate sources do not

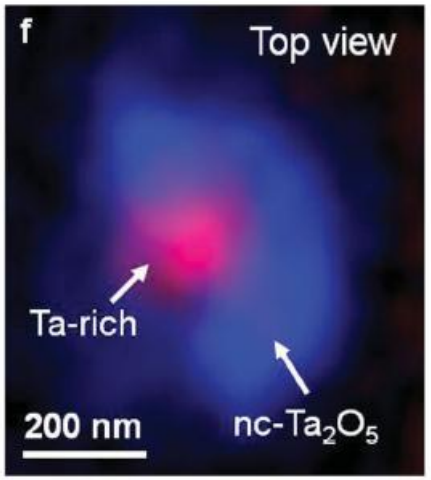


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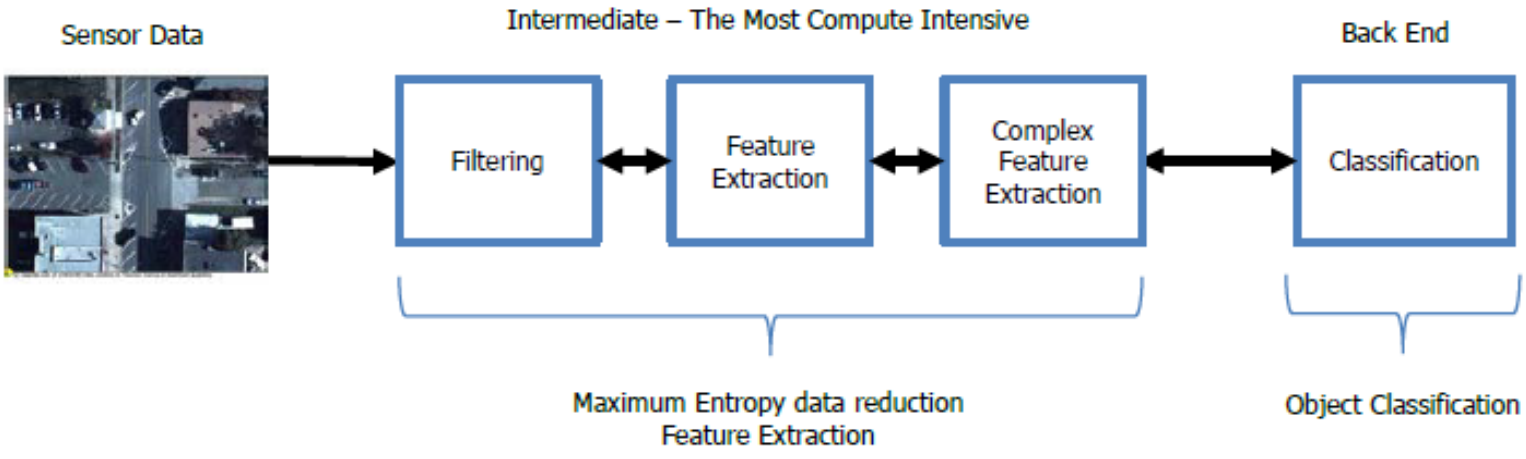
Image Recognition Problem

Major DoD Problem

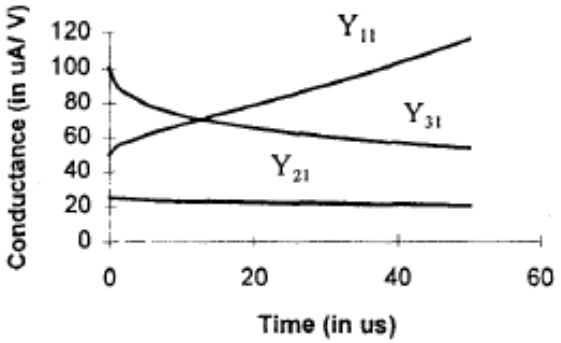
- ***"The DoD has become increasingly reliant on Intelligence, Surveillance and Reconnaissance (ISR) applications to accomplish their mission. Currently there is a pressing need to dramatically expand the DoD's capabilities into the real-time processing of wide-area, high resolution video imagery, with systems performing target recognition and tracking over large numbers of objects. Not only is the volume of sensor data increasing exponentially, there is also a dramatic increase in the complexity of analysis, reflected in the number of operations per pixel per second. These expanding processing requirements for ISR missions, as well as other DoD sensor applications, are quickly outpacing the capabilities of existing and projected computing platforms."***
  - **DARPA UPSIDE BAA, September 2012**

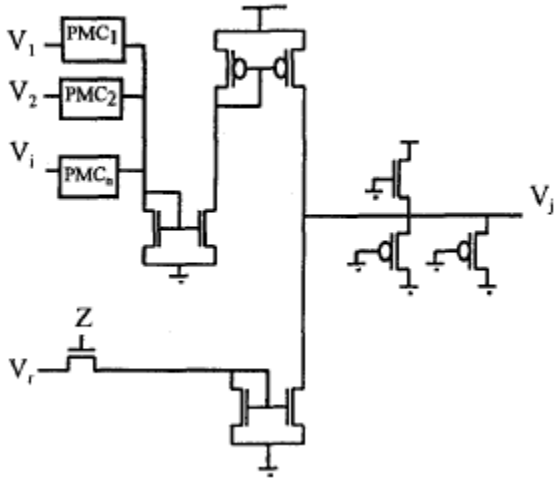


New Architectures

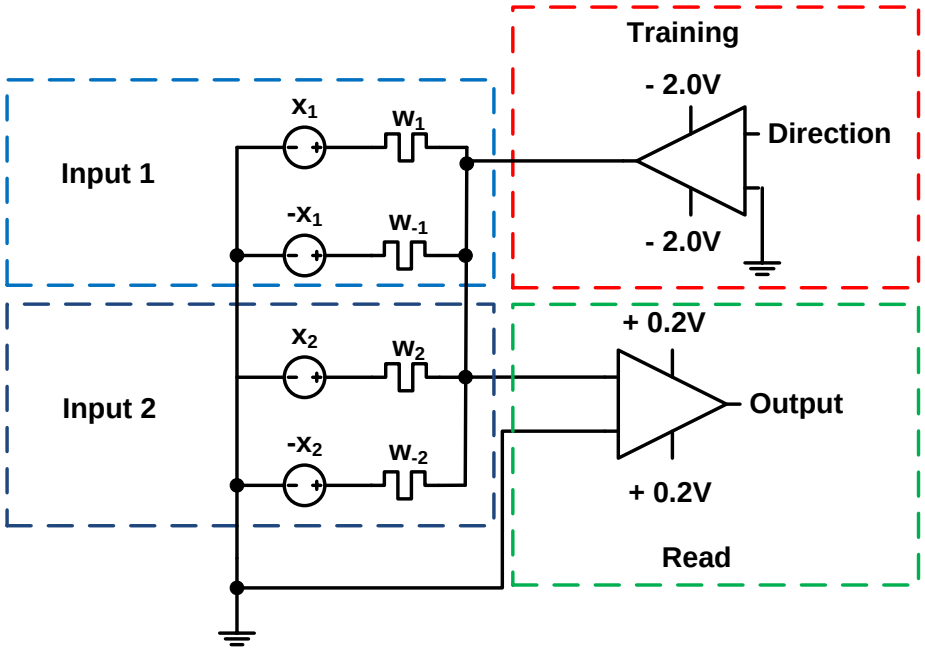
- **Neural networks implemented with memristors may enable pattern recognition at new performance levels**

Swaroop et al, ISCAS '98



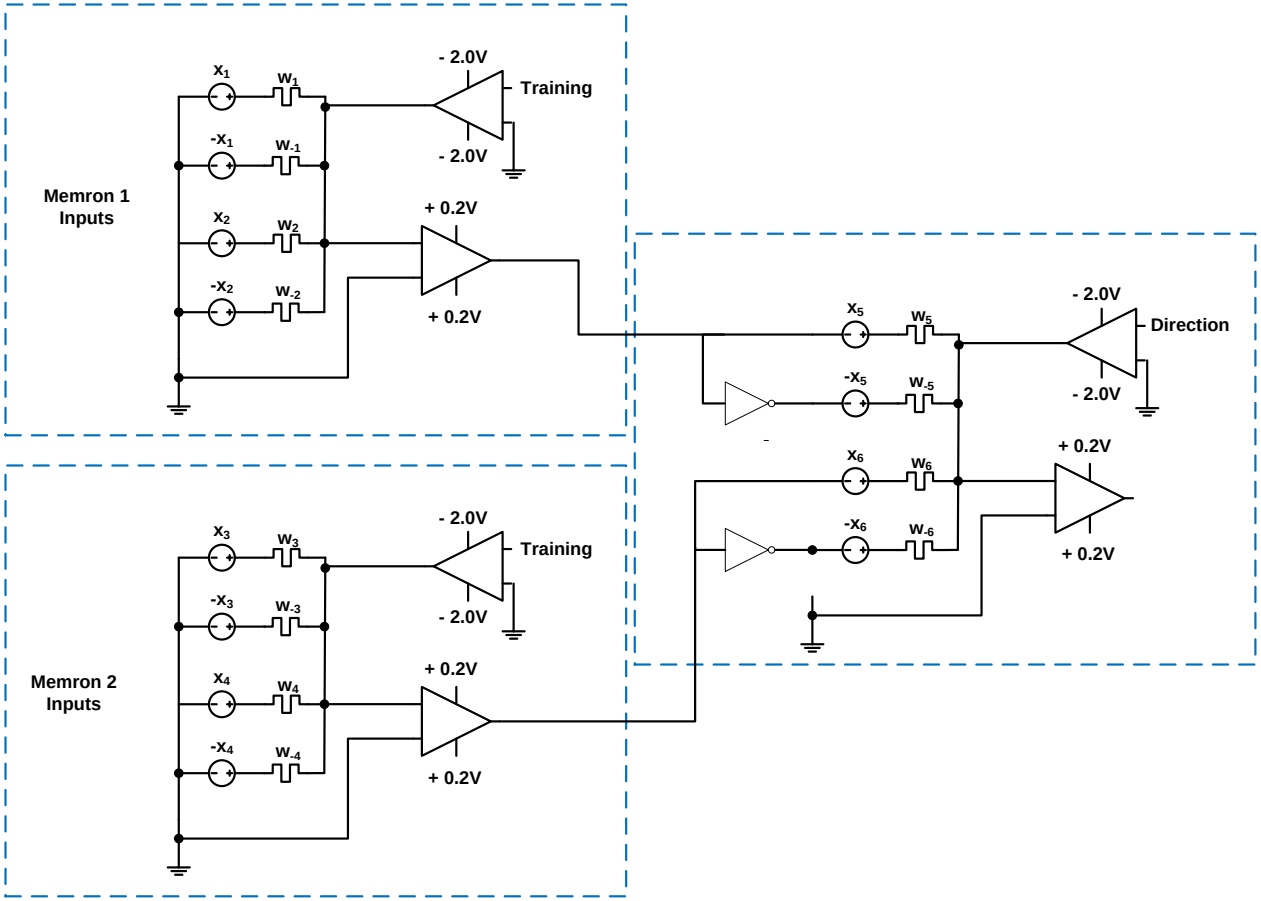


Memron – Memristor Neuron



Memron

- **Requires 3 Memrons can learn XOR**



Conclusions

- Novel memory technologies are emerging to replace traditional magnetic hard drives, flash, DRAM, and SRAM
- ReRAM or Memristor technology is especially promising
- Sandia is working to integrate state of the art TaO_x memristor technology with rad-hard CMOS7
- Many of these new technologies may be rad-hard
- Novel architectures based on these devices may solve tough DoD problems

Questions