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Performance and Reliability Characterization of 1200 V Silicon Carbide Power JFETs at High Temperatures

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Abstract

In this work, 1200 V Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) and Junction Field Effect Transistors (JFETs) have been characterized at high operational temperatures. For packaged JFETs obtained from a collaborating manufacturer, the threshold shift (ΔV_T) was measured under both static and dynamic voltage stress and in all cases was less than 2 mV, which is within the measurement margin of error. Temperatures up to 250°C and stress times as long as 200 hours were evaluated. As a comparison, commercially available SiC MOSFETS demonstrated shifts of up to 300 mV after 30 minutes of static gate stress at 175°C. In addition to packaged parts, results from unpackaged JFET die at temperatures up to 525°C show ΔV_T values of less than 10 mV for all stress conditions. Although V_T remained unchanged for the duration of the test for both static and dynamic stress conditions, under dynamic stress conditions the JFET packaged parts demonstrated a linear increase in sub-threshold leakage of around 15.6 nA per hour, compared to the MOSFET devices, which showed an exponential increase in sub-threshold leakage.

I. Introduction

THE low intrinsic carrier concentrations, high breakdown voltages, and high thermal conductivities of wide-bandgap semiconductor devices (E_G > 3 eV) make them attractive alternatives to traditional Si power electronics devices (E_G = 1.1 eV), especially for high-temperature power switching applications. Silicon Carbide (SiC) is an especially strong candidate to replace Si devices due to availability of SiC substrates, vertical device topologies, and the ability to thermally grow a Silicon Dioxide (SiO_2) layer on SiC to serve as a gate dielectric, similar to what is done for established Si technology.

An ideal solution for high-temperature power electronics applications would be a wide-bandgap substitute for traditional Si power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) that can utilize the specific advantages of wide-bandgap materials. One key metric for evaluating device reliability at high operating temperatures is the threshold voltage shift (ΔV_T). SiC devices show much higher instability in V_T due to the larger number of electrically active SiC bulk and SiC/SiO_2 interface states [1-3], as well as the small band offset between SiC and SiO_2 (Fig. 1a).

The application of a positive gate voltage results in electron injection from the inverted SiC channel into the oxide, populating traps at the SiO_2/SiC interface and/or within the SiO_2 bulk (Fig. 1b). These populated traps alter the surface potential and increase the V_T necessary to switch the device.

Our data have indicated that injection of electrons into the oxide layer, causing a positive V_T shift, is less severe than the negative V_T shift due to hole injection from the accumulated p-type SiC into the oxide, Fig. 1c) [4]. Holes are well-known to cause significant reliability degradation in SiO_2 on Si, e.g. by changing the charge state of the oxygen vacancy (E' defect) [5], and a similar model has been proposed for SiO_2 on SiC [6].

Previous investigations into SiC MOSFET V_T stability as a function of elevated operational temperatures and gate bias stresses (both static and dynamic) have shown monotonic changes in ΔV_T due to both of these variables, independent of

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packaging type [7]. At elevated temperature, the surface potential under strong inversion is reduced along with the concentration of interface traps that must be charged or discharged to achieve that potential [8]. This leads to potentially unreliable device operation at high temperature [9]. ΔV_T was also found to be a function of the magnitude and duty cycle of repeated switching events [4]. This is especially concerning for devices that will see a variation in parameters like duty cycle and operational temperature over the course of their lifetime.

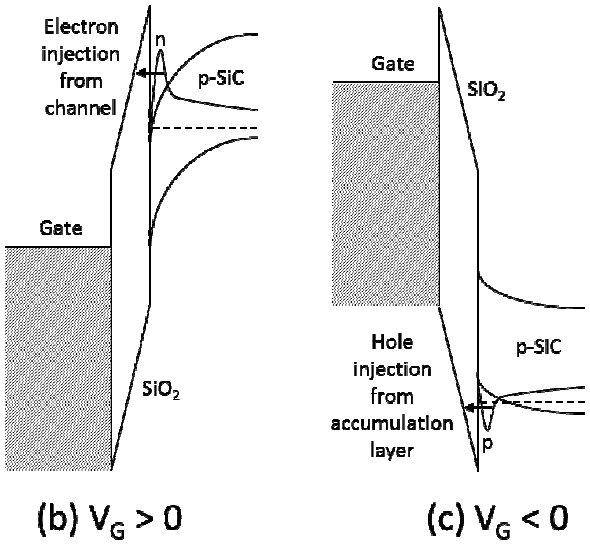

Fig. 1 (a) ΔV_T for first-generation plastic- and metal-packaged parts stressed at ±20 V as a function of temperature. Schematic band diagrams illustrating (b) electron injection for $V_G > 0$ and (c) hole injection for $V_G < 0$.

Junction FETs (JFETs) are conceptually simple transistor devices constructed without a gate oxide layer. However, JFETs are inherently normally-on devices with $V_T < 0$, which has impacted their utilization in circuits designed for traditional normally-off Si power devices. Indeed, Si JFET devices have become virtually obsolete, since circuit designers have turned to alternative FET devices such as MOSFETs. However, the lack of an oxide layer can be an advantage in high-temperature applications suitable for SiC, since the absence of a gate oxide and the associated carrier trapping phenomenon make it likely that SiC JFETs will demonstrate greater V_T stability than similarly-rated SiC MOSFETs.

In this work, we have characterized 1200 V SiC MOSFETs and 1200 V SiC JFETs at high temperatures under both static and dynamic gate bias stress conditions. It was found that SiC JFET devices are much more stable than SiC MOSFET devices with respect to ΔV_T for both types of gate bias stresses. For static gate bias stresses, packaged JFET devices ($\Delta V_T < 2$ mV) exhibited no shift in V_T for temperatures up to 250°C. At higher temperatures, bare JFET die demonstrated less than 10 mV VT shifts for temperatures up to 525°C. In contrast to SiC MOSFETS, V_T of the SiC JFET devices were unaffected by dynamic gate bias stresses over the 200 hour test period, although sub-threshold leakage at V_g = -30 V increased linearly with test time.

II. Experimental Details

Packaged power JFETs from a cooperating manufacturer as well as commercially available second-generation power MOSFETs were evaluated in our experiments. The power JFETs were encased in metal packages with a rated temperature of 175°C, while the MOSFETs were encased in plastic packages rated to 150°C.

Current-voltage measurements on packaged parts were performed by connecting the device to source-measure units using a Loranger high-power TO-247-3 test socket. Power was provided using a Keithley 2651A high-current source.

The devices were heated using a VWR aluminum hot plate. The temperature on the hot plate was verified using an Anritherm HL600 temperature probe. When heating a device, the part was allowed to stabilize at a given temperature for thirty to forty minutes, or until the gate sweep curve stopped

shifting. ΔV_T values were calculated relative to the initial V_T at the stress temperature, not the shift in room temperature V_T.

Fixed bias gate stress was applied to the device under test for 30 minutes at temperatures ranging from room temperature to 250°C (JFETs) or 175°C (MOSFETs). Stress voltages were chosen to be within the maximum and minimum manufacturer-recommended gate voltages for the devices. The JFETs were stressed with -30, 0, and +3 V, whereas the MOSFETs were stressed with -20, -5, and +5 V. After 30 minutes of stress, gate-sweep characterization curves were measured to ascertain changes in the devices' V_T. Following this, in order to recover the device to its original condition, a gate bias of opposite polarity to the stress gate bias was applied in small time increments until the characterization gate sweep curve matched the initial gate sweep curve at that temperature. V_T is taken to be the voltage resulting in I_d = 10 mA with the drain voltage set at 100 mV.

Bare JFET die were studied using a Signatone S-1160 probe station outfitted with a S-1060RH high temperature hot chuck system. In order to negate contact resistance, a four-point probe technique was used to obtain gate sweep curves. Contact to the die pads was carried out with Signatone S-926 probes outfitted with SE-TB probe tips.

In order to determine the V_T shift in a situation closer to real-world applications, dynamic bias gate stress was applied to the device under test. The MOSFET devices were tested using a switching gate bias of +20 V / -5 V at a frequency of 100 Hz and a 50% duty cycle (50% of time at +20 V, 50% of time at -5 V) at 150°C for 120 hours. The JFET devices were tested using a switching gate bias of -30 V / +3 V at a frequency of 100 Hz and a 50% duty cycle at 175°C for 200 hours. For each type of device, the switching stress was interrupted and V_T was sampled in half-hour increments.

III. Results and Discussion

A. Threshold Voltage Shift – Fixed Bias

When stressed under a under fixed gate bias, the V_T shift of the SiC JFET and second-generation MOSFET devices show very different trends (Fig. 2). Due to the lack of a gate oxide, the SiC JFET devices (black traces) show remarkable V_T stability at temperatures up to 250°C (75 °C above the rated operating temperature) regardless of the gate bias condition. The inset shows a close-up of the JFET ΔV_T data. The maximum measured ΔV_T value (1.9 mV) is below the resolution of the experimental setup and any measured shift in the device V_T is likely due to measurement error.

For the MOSFET devices, the ΔV_T behavior is a function of gate bias magnitude and sign as well as temperature. At a +20 V gate bias stress, the ΔV_T is positive with a maximum of 0.127 V at 175°C. This positive V_T shift (due to electron injection from the inverted SiC channel into the oxide) is less severe than the negative V_T shift (due to hole injection from the accumulated p-type SiC into the oxide) that occurs for negative gate bias conditions. At -5 V gate bias stress, the ΔV_T reaches a maximum value of -0.15 V at 175°C. At -20 V gate bias stress, the ΔV_T reaches a maximum value of -0.31 V at 175°C.

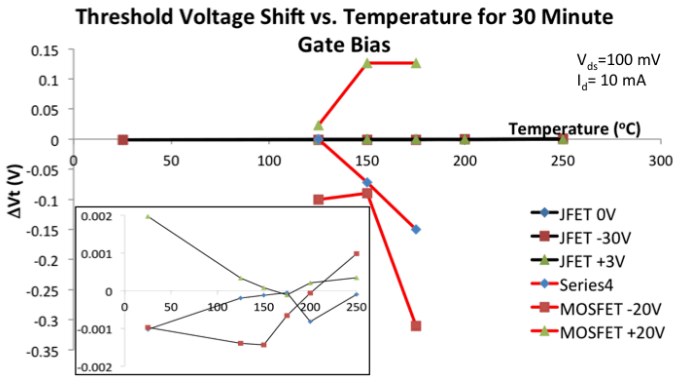

Fig. 2: ΔV_T for second-generation SiC MOSFETs plotted vs. stress temperature (red traces), for ±20 V and -5 V gate bias stress conditions as well as SiC JFETs (black traces) for -30, 0, and +3 V gate bias stress conditions. The inset shows a close-up of the JFET results gate bias stress results.

The 250°C maximum test temperature for the JFET devices is due to shortcomings in the device packaging, rather than the JFET device itself. In order to determine if any V_T shift occurred at temperatures above 250°C, bare JFET die were tested at temperatures up to 525°C using a Signatone probe station and hot chuck (Fig. 3).

The JFET die exhibited V_T shifts of less than 10 mV for temperatures up to 525°C. The largest shift (-6.7 mV) occurred at a zero gate bias condition at 400°C. At temperatures above 525°C, ΔV_T results

were highly variable, most likely due to degradation of the metal contacts.

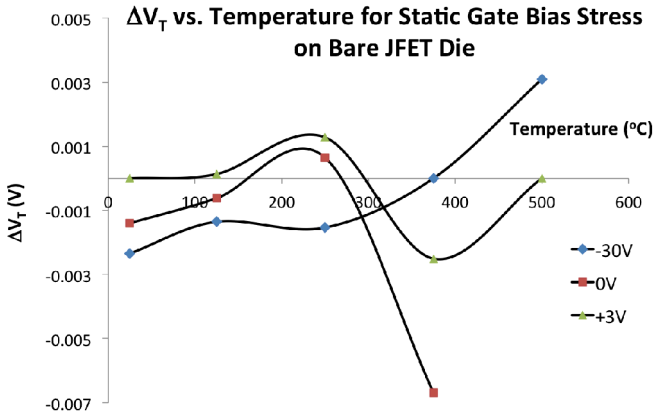

Fig. 3: ΔV_T SiC JFET die for -30, 0, and +3 V gate bias stress conditions.

B. *Threshold Voltage Shift – Switching Bias*

In real-world applications, a power semiconductor device will have a rapidly switching gate bias applied to it. Previous data has shown that V_T shifts can be smaller when using a switching bias on the gate, even when tested for months [10]. In addition to the static gate bias stresses discussed previously, we have applied more realistic long-term switching gate bias stresses to the JFET and MOSFET devices.

The results of these long-term switching bias tests are plotted in Fig. 4 for a 100 Hz switching speed at 50% duty cycle. The SiC JFET devices showed no appreciable shift in the value of the V_T over the entire test length of 200 hours. Maximum measured ΔV_T was sub-1 mV, which is below the resolution of the experimental test setup.

The SiC MOSFET device showed a very rapid initial drop in V_T (the first point recorded was after one-half hour of switching stress). Following this initial drop, V_T continues to shift in the negative direction, indicating that the device is more sensitive to hole injection under these switching stress conditions. The rapid initial drop in V_T after half an hour for is roughly 150 mV. The increased shift under switching stress may be due to self-heating resulting from switching loss, similar to what we have reported previously [11] (the temperatures reported here are hotplate temperatures, and thus self-heating is not taken into account). After an initial drop and slight recovery, the V_T shift gradually increases at a rate of -2.5 mV/hr. The final V_T shift after 120 hours is approximately -370 mV.

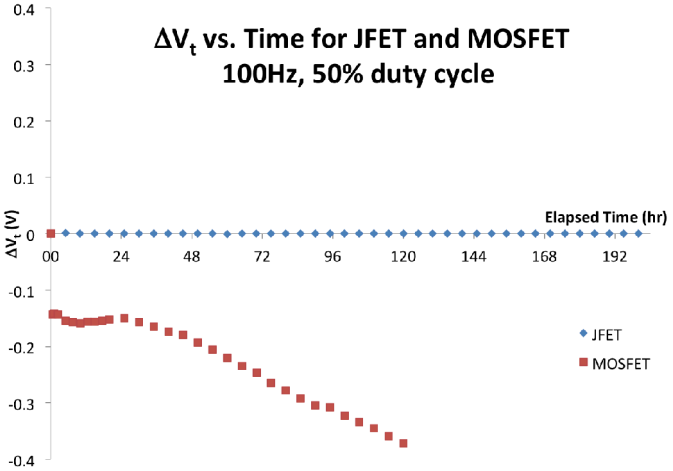

Fig. 4: ΔV_T for a SiC JFET (blue diamonds) and a second-generation SiC MOSFET (red squares) subjected to 50% duty cycle.

Sub-threshold leakage is an important parameter during device operation since it represents an off-state parasitic power consumption. The sub-threshold leakage can also be used to as a measure of defect density, since the interface trap density can introduce a parallel parasitic capacitance in parallel with the normal depletion region capacitance, C_{dm}. This parallel capacitance changes the value of the sub-threshold slope, increasing I_d for a given V_g [12-14].

The Sub-threshold leakage was monitored during each voltage sweep of the long-term switching bias tests. Fig. 5 shows the value of the drain current at the first point of the gate voltage sweep (-30 V for the JFET, 0 V for the MOSFET). The JFET device had an initial I_d = 78.1 nA which increased linearly during the 200 hour test at an average rate of 15.6 nA/hour. The total change in sub-threshold leakage throughout the test was 118.9 nA.

The SiC MOSFET device had an initial sub-threshold leakage (I_d = 0.4 nA), less than 1% of the JFET device. However, the sub-threshold leakage increases exponentially with time, so the final leakage value at 120 hours was measured to be 107.2 nA, 68% of the JFET device at that time.

The sub-threshold leakage of the MOSFET increases partly due to the shift in V_T. However, the large, discrete change in V_T at the beginning of the test is not mirrored in the sub-threshold leakage, indicating at least some change in sub-threshold

leakage due to device operation during the dynamic switching stress.

If the potential barrier at in the sub-threshold region may be considered triangular via the WKB approximation [15], an exponential increase in MOSFET I_d may be due to a lowering of the potential barrier height due to material inhomogeneity or charge pinning at the contact interface. It is also possible, if the leakage is a product of Fowler-Nordheim tunneling, that the creation of new bulk traps may effectively thin the triangular potential, allowing for an increase in tunneling.

Since the JFET device lacks a gate oxide, the linear increase of I_d during JFET operation cannot be due to changes in the metal/oxide interface. The linear increase in I_d could be due to a change in contact resistance at the ohmic metal-drain/source interfaces.

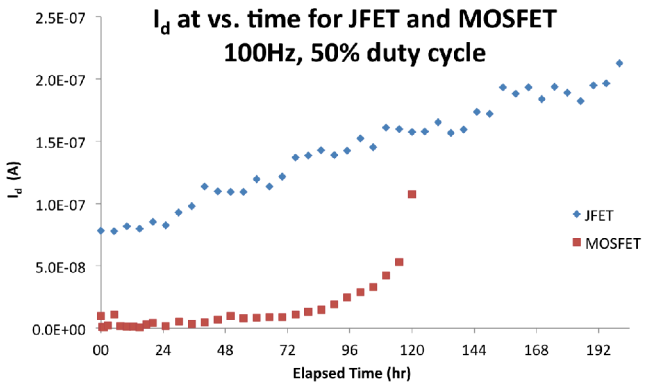

Fig. 5: Sub-threshold leakage vs. time of SiC JFET and MOSFET during long term switching bias test.

The ability to recover the MOSFET V_T to its unstressed state indicates that shifts in the V_T are due entirely to trapping/detrapping of pre-existing defects. However, the exponentially increasing sub-threshold leakage indicates that new defects are being created due to device stressing. This creation of defects would explain the large, discrete change in V_T in the first half hour of MOSFET operation, as seen in Fig. 4, as the V_T recovery may only be temporary.

Fig. 6 shows the results of a SiC MOSFET that has undergone four long-term dynamic gate stress tests at duty cycles ranging from 10 to 90%. Between each test, the part was recovered using the procedure described in Section II.

The measured I_d values at $V_g = 0$ V increase with time for duty cycles of 50% and 90%. The first point of the 90% duty cycle shows a decreased I_d value due to device recovery. However, after the initial measurement point, the value of I_d increases to match the I_d value at the end of the first 50% duty cycle test.

For a duty cycle of 10%, the value of I_d decreases with time, indicating some passivation of defects introduced during the 90% duty cycle test. However, when the duty cycle is increased to 50% again, the value of I_d rises very rapidly before slowing at a value of 1.07 μA. This indicates that the V_T recovery process does not totally recover the unstressed device state as I_d is not (or at most, temporarily) recovered in this process. This indicates that new defect states are created during device operation.

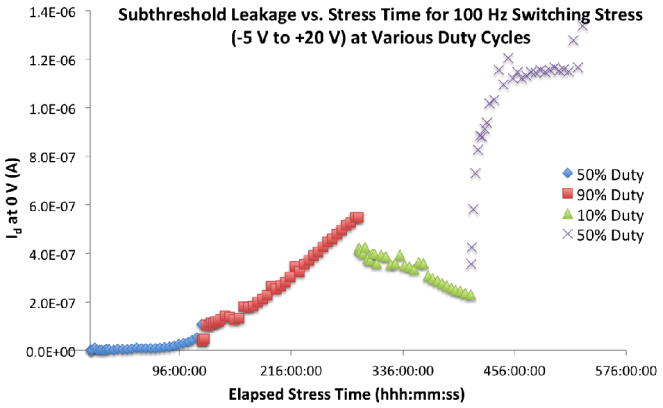

Fig. 6: Sub-threshold leakage vs. time of SiC JFET during long-term switching gate bias tests at different duty cycles. The device V_T was recovered after each test. However, the value of I_d was not permanently recovered from device distressing.

IV. Summary

This work has examined the change in V_T for SiC JFETs under both static and dynamic gate bias stress conditions at temperatures up to 250°C for packaged parts and 525°C for bare die. The JFET ΔV_T results were compared to similar tests run on commercially available second-generation SiC MOSFETs. For all temperature ranges and stress conditions considered, the JFET devices had remarkably stable V_T values with ΔV_T measured to be less than 10 mV, compared to the MOSFETs, which exhibited shifts in V_T upwards of -370 mV under gate switching conditions. Both the JFET and MOSFET devices exhibited increasing sub-threshold leakage during long-

term switching tests. However, while the leakage values of the JFET increased linearly with time, the MOSFET values increased exponentially. Although V_T could be recovered by applying a gate voltage of opposite polarity, the effect was only temporary and V_T and I_d degraded to stressed levels without 30 minutes.

The drift in device parameters under realistic temperature and gate stress is critical to system designers to ensure reliability system operation under a wide variety of usage conditions. In general, any drift or change in device parameters is undesirable and may significantly impact the system.

For example, PV inverters are beginning to incorporate SiC MOSFETs in the H-bridge power converter state in order to increase switching frequency (and therefore decreasing filtering requirements while increasing power quality) [16]. However, a shift in V_T would be highly undesirable in this application as even small changes (~100 mV) in V_T may inject a relatively large DC offset (~2 V) into the nominally AC output (Fig. 7).

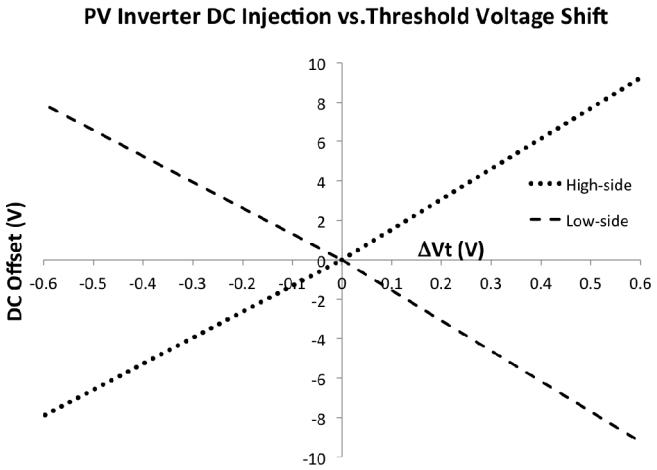

Fig. 7: For a PV inverter with an H-bridge power conditioning stage, a small change in VT can inject a large DC offset into the nominally AC signal. The sign of the offset depends on sign of ΔV_T and whether the device is on the high or low side.

Conventional Si JFET devices are virtually obsolete as circuit designers opt for MOSFET devices. However, in the SiC materials system, the relative simplicity and stability of JFETs compared to SiC MOSFETs may increase their utilization in the next generation of power handling circuits, especially for high temperature applications.

REFERENCES

[1] D. K. Schroder, "Progress in sic materials/devices and their competition," *International Journal of High Speed Electronics and Systems,* vol. 21 (01), p. 1250009, Apr 2012.

[2] T. Zheleva, A. Lelis, G. Duscher, F. Liu, I. Levin, and M. Das, "Transition layers at the sio2/sic interface," *Applied Physics Letters,* vol. 93 (2), p. 022108, 2008.

[3] X. Shen and S. T. Pantelides, "Identification of a major cause of endemically poor mobilities in sic/sio2 structures," *Applied Physics Letters,* vol. 98 (5), pp. 053507-053507, 2011.

[4] R. Kaplar, D. R. Hughart, S. Atcitty, J. D. Flicker, S. DasGupta, and M. Marinella, "Performance and reliability characterization of 1200 v silicon carbide power mosfets at high temperatures.," MAPS International Conference on High Temperature Electronics Network, 2013.

[5] P. M. Lenahan and P. V. Dressendorfer, "Hole traps and trivalent silicon centers in metal/oxide/silicon devices," *Journal of Applied Physics,* vol. 55 (10), pp. 3495-3499, 1984.

[6] C. J. Cochrane, P. M. Lenahan, and A. J. Lelis, "An electrically detected magnetic resonance study of performance limiting defects in sic metal oxide semiconductor field effect transistors," *Journal of Applied Physics,* vol. 109 (1), pp. 014506-014506, 2011.

[7] D. R. Hughart, J. D. Flicker, S. DasGupta, S. Atcitty, R. J. Kaplar, and M. J. Marinella, "Progress in sic mosfet reliability," *ECS Transactions,* vol. 58 (4), pp. 211-220, Oct 18 2013.

[8] R. Schorner, P. Friedrichs, and D. Peters, "Detailed investigation of n-channel enhancement 6h-sic mosfets," *Electron Devices, IEEE Transactions on,* vol. 46 (3), pp. 533-541, 1999.

[9] R. Singh, "Reliability and performance limitations in sic power devices," *Microelectron Reliability,* vol. 46 (5-6), pp. 713-730, Jun 01 2006.

[10] M. K. Das, S. K. Haney, J. Richmond, and A. Olmedo, "Sic mosfet reliability update," *Materials Science ...,* 2012.

[11] S. DasGupta, R. J. Kaplar, M. J. Marinella, M. A. Smith, and S. Atcitty, "Analysis and prediction of stability in commercial, 1200 v, 33a, 4h-sic mosfets," *Reliability Physics Symposium (IRPS), 2012 IEEE International,* p. 3, 2012.

[12] N. EH and G. A, "Si-sio2 interface - electrical properties as determined by metal-insulator-silicon conductance technique," *Bell System Technical Journal,* vol. 46 (6), pp. 1055-&, 1967.

[13] Y. Taur and T. H. Ning, *Fundamentals of modern vlsi devices*: Cambridge University Press, 2013.

[14] E. H. NICOLLIAN AND J. R. BREWS, *MOS (METAL OXIDE SEMICONDUCTOR) PHYSICS AND TECHNOLOGY*: WILEY-INTERSCIENCE, 2002.

[15] S. M. SZE AND K. K. NG, *PHYSICS OF SEMICONDUCTOR DEVICES*: JOHN WILEY & SONS, 2006.

[16] B. BURGER AND D. KRANZER, "EXTREME HIGH EFFICIENCY PV-POWER CONVERTERS," POWER ELECTRONICS AND APPLICATIONS, 2009. EPE &APOS;09. 13TH EUROPEAN CONFERENCE ON, 2009.