SAND2011-0255C

Monolithic Integration of Silicon Electronics and Photonics

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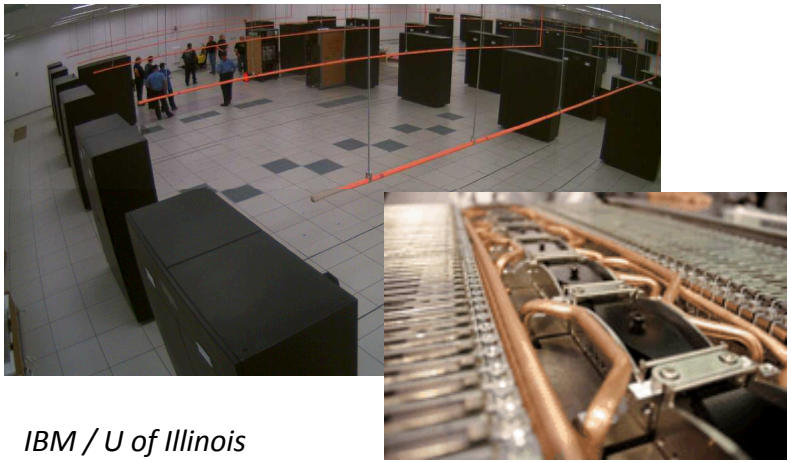
Sandia National Labs Albuquerque, NM
Applied Photonic Microsystems

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000

Applications for Integrated Photonics

Supercomputer inter-chip BW



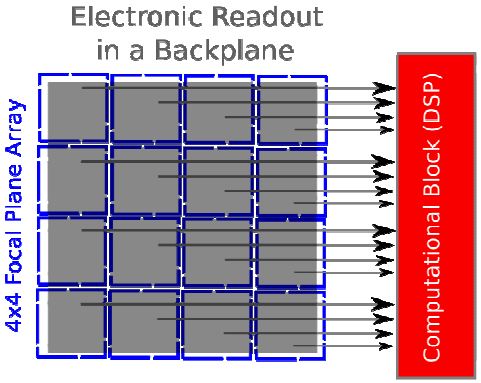
IBM / U of Illinois
Blue Waters, http://www.ncsa.illinois.edu/BlueWaters

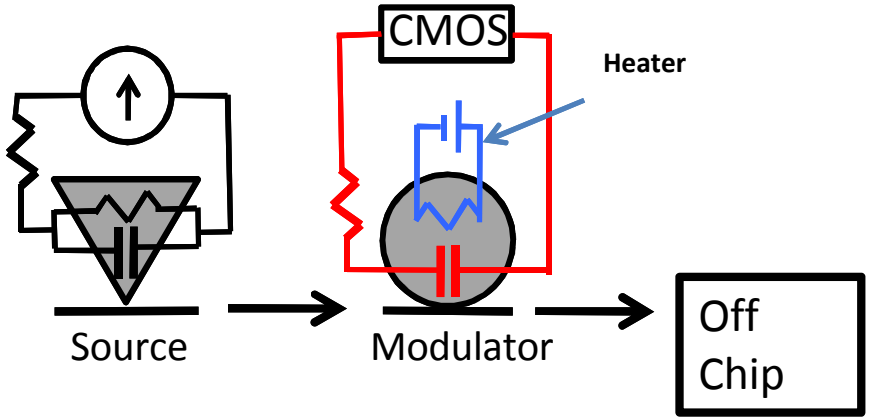
Data Center Energy Consumption

Google Dalles, Or
http://www.nytimes.com

http://scienceblogs.com

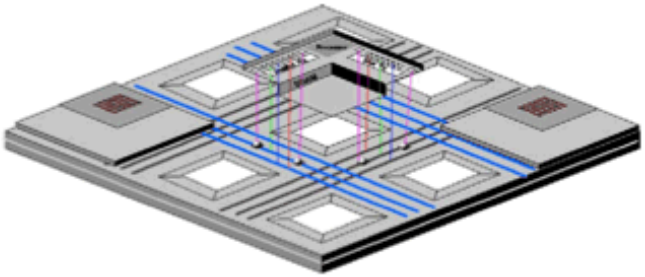
Satellite focal plane array readout





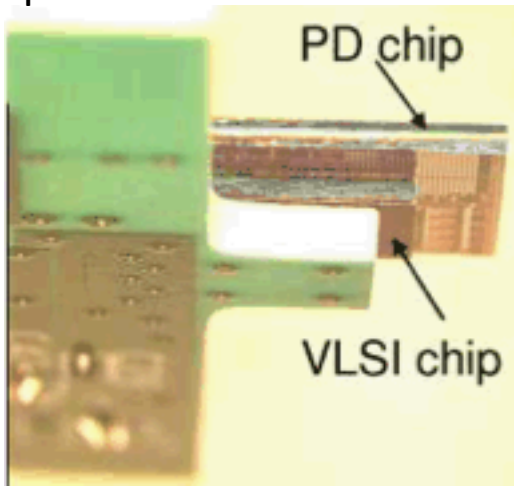
Photonic Integration – Very Active Area

Sun/Luxtera
Macrochip



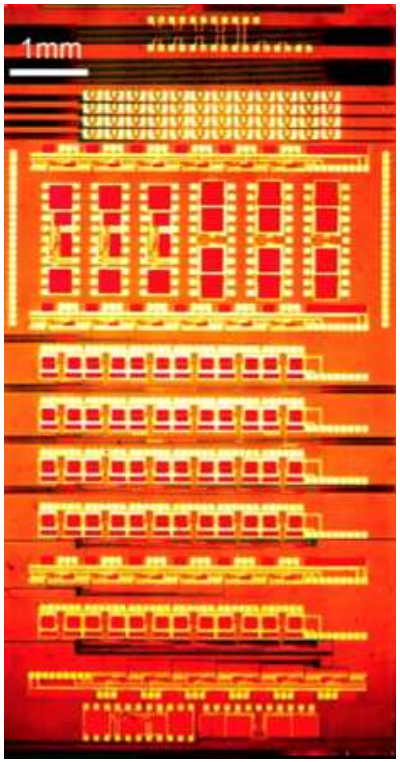
Krishnamoorthy et al Proc IEEE July 2009

CMOS integrated photodetector



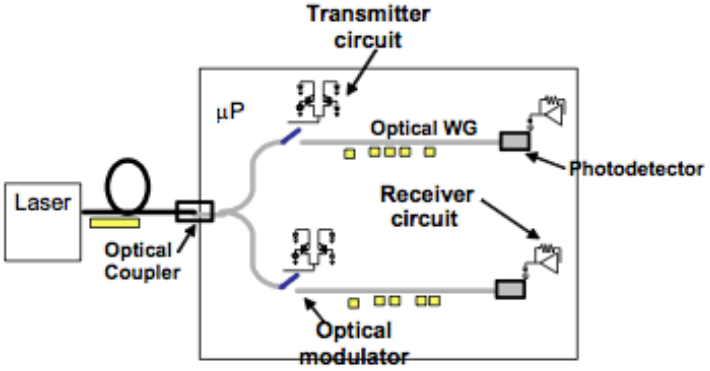
Zhen et al OPEX Dec 2009

IBM
Multichannel CMOS integrated modulators and detector



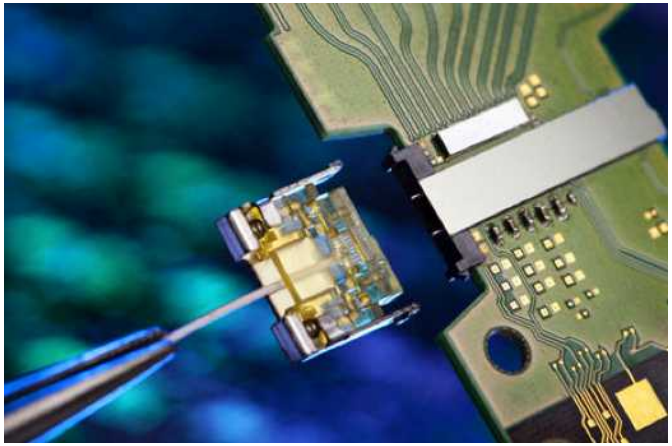
Green et al SEMICON 2010 Tokyo

Intel
On chip interconnect



Kobrinsky et al Intel Technology Journal 2004

Integrated transceivers



IPR Intel Press Release July 2010 Monterrey

What we did

.35um radhard

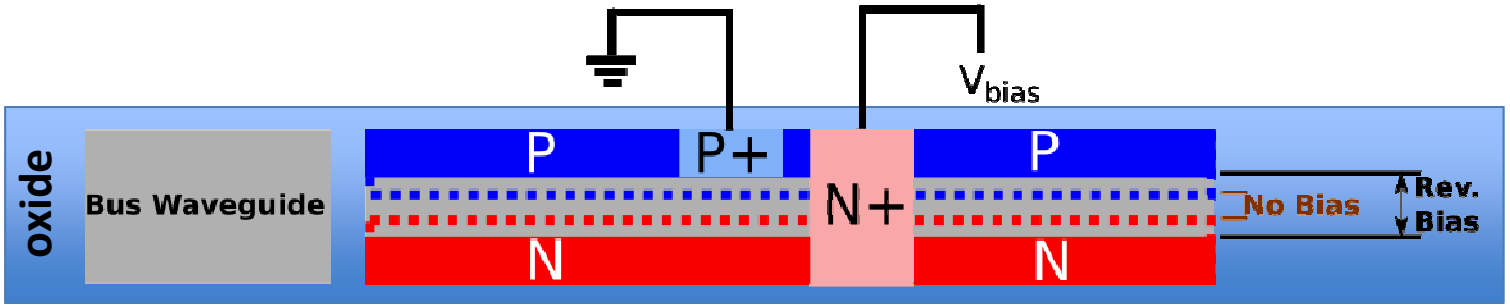
Disk

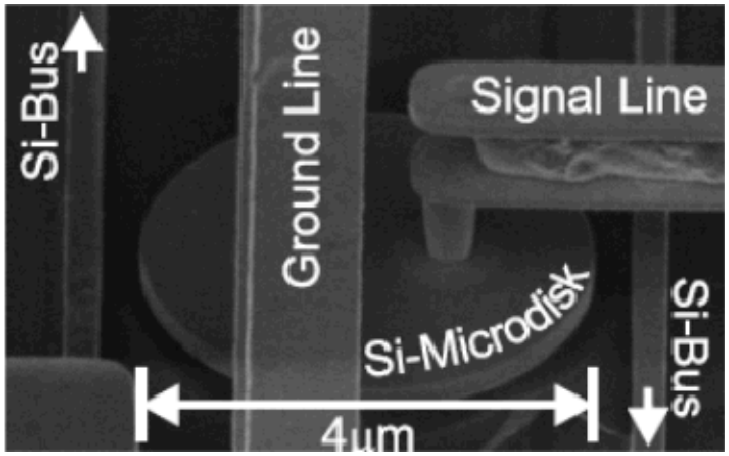
Efficient

50k – little effort

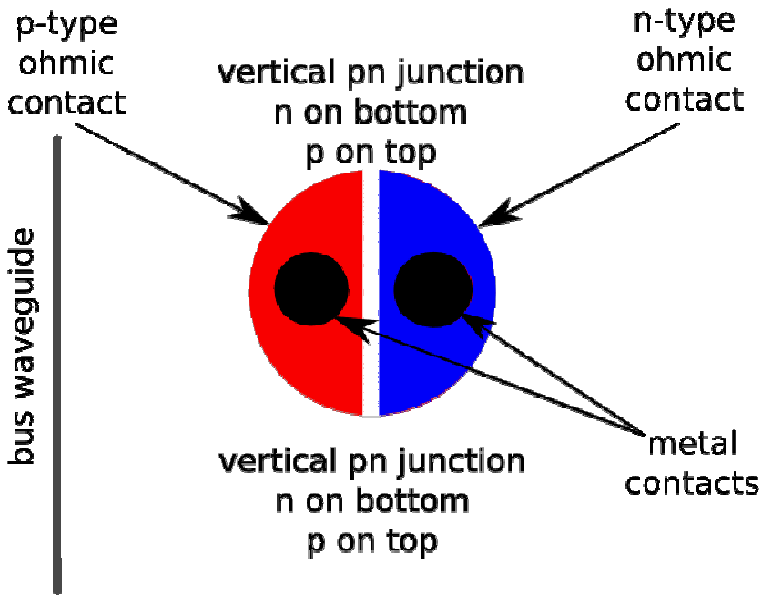
Disk Resonator Design

Depletion Mode Vertical PN Junction built on Silicon on Insulator



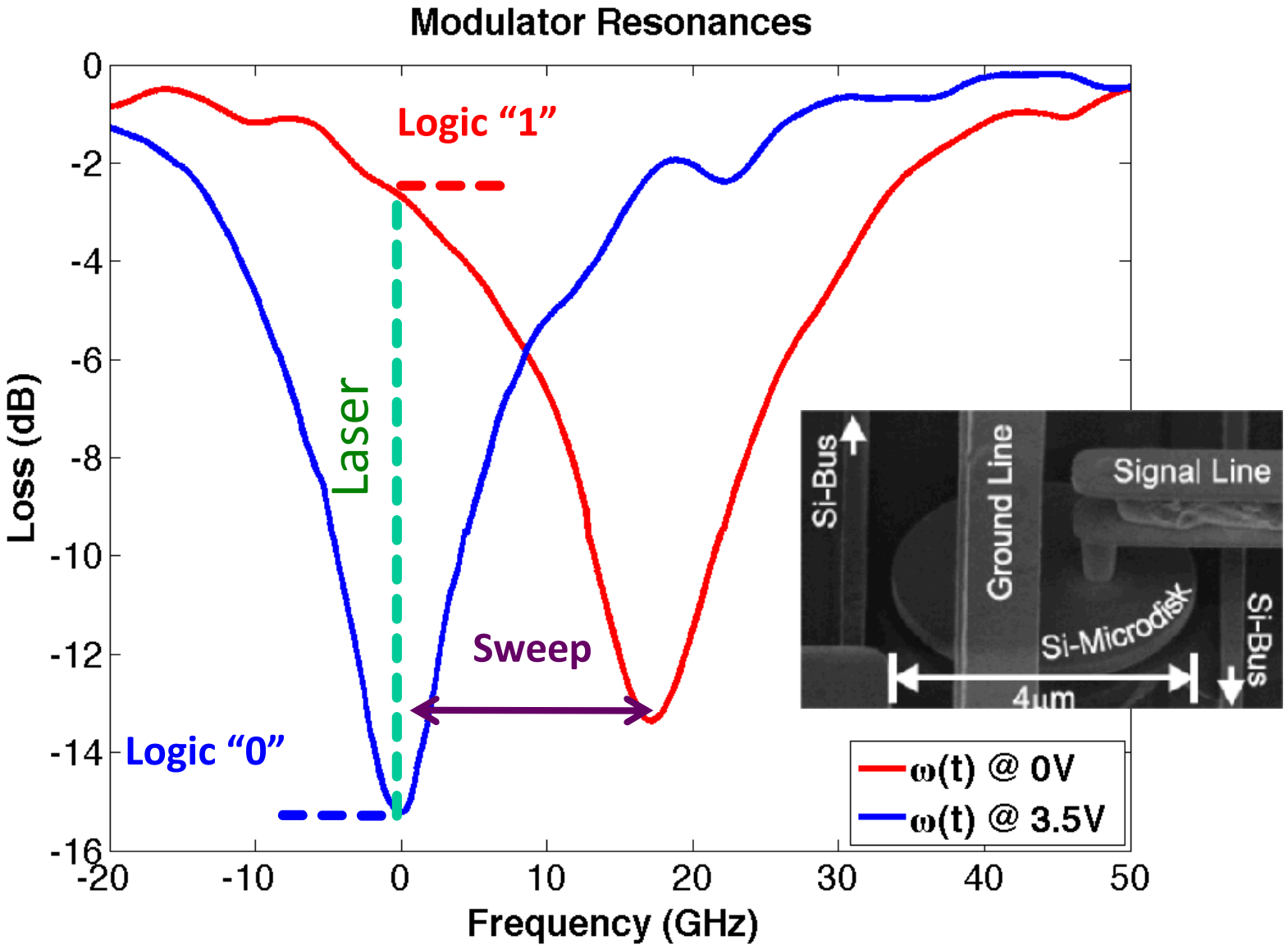


Top View of Fully Doped Modulator

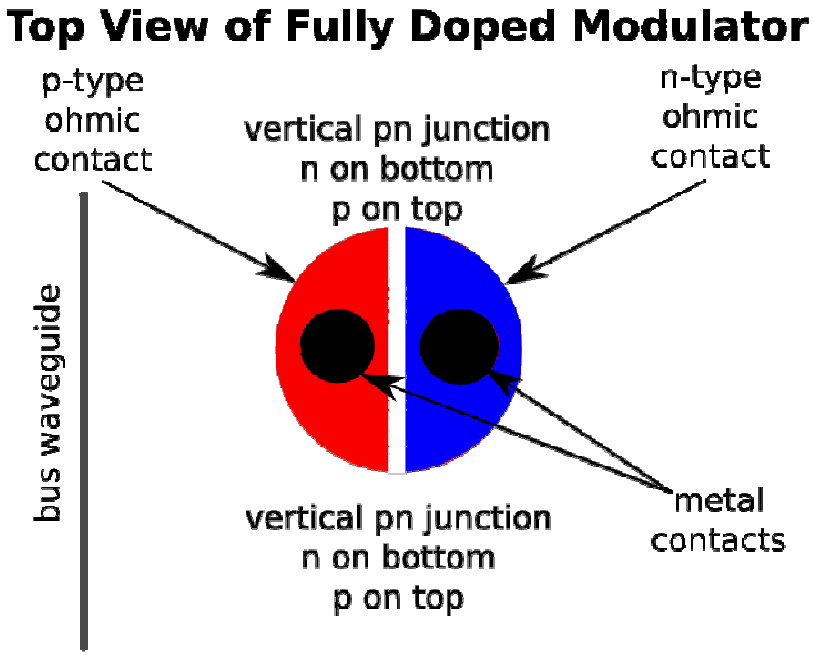


Reverse bias enabled expansion of the depletion region sweeps out carriers and changes the refractive index via the plasma carrier dispersion effect

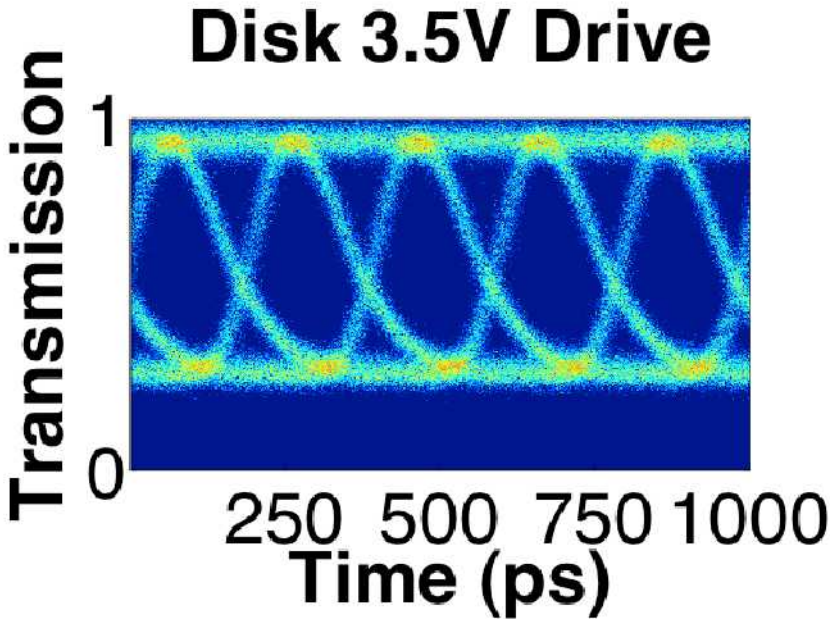
Reverse Bias Modulation Action

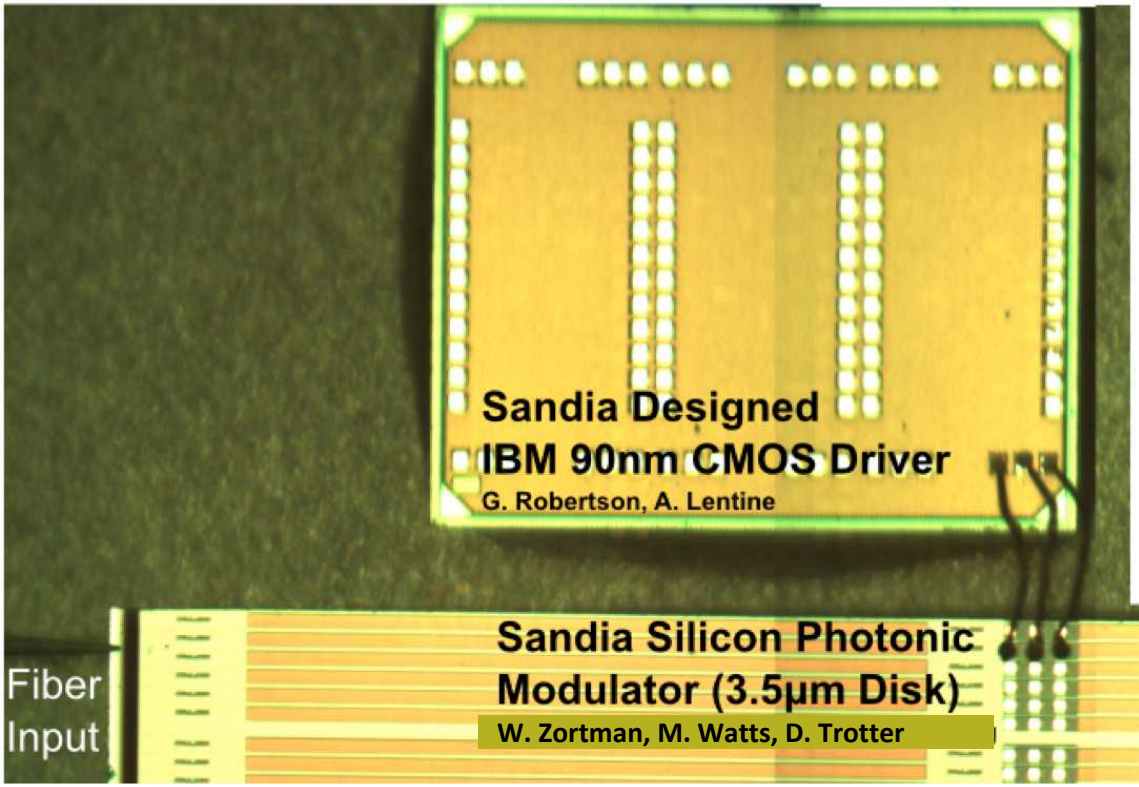


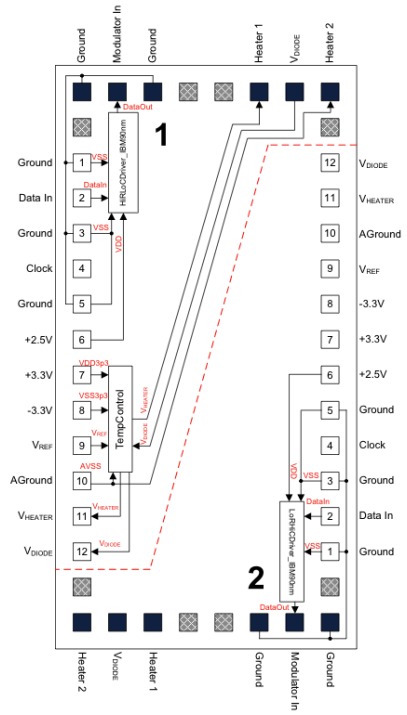
Resonator Integrated with CMOS



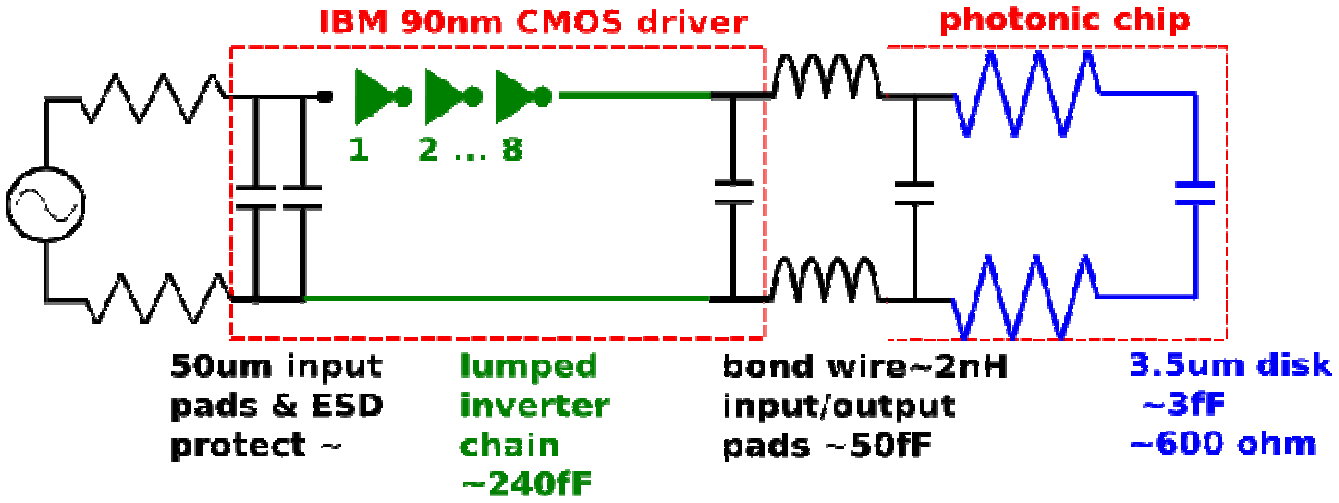
R=2X and C=2X




Sandia Designed
IBM 90nm CMOS Driver
G. Robertson, A. Lentine

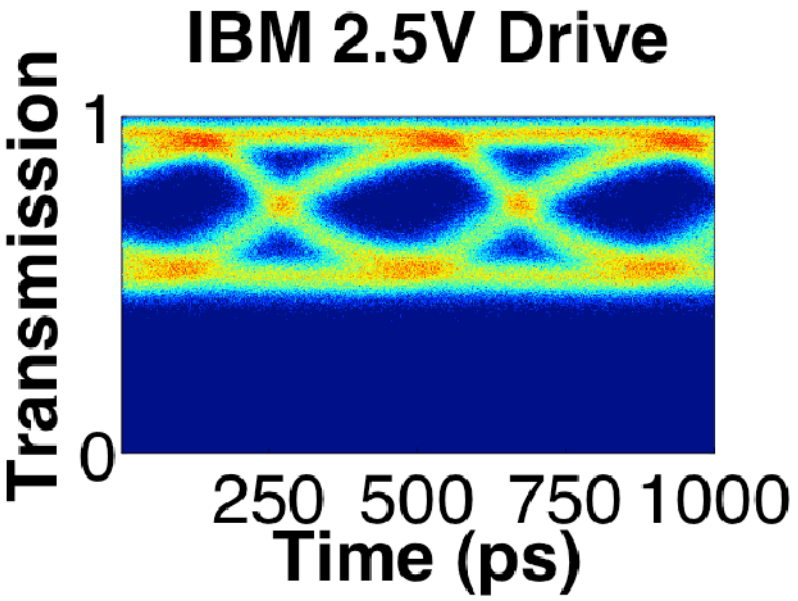

Ground
Modulator In
Ground
Heater 1
VDIODE
Heater 2
1
2
Ground
Data In
Ground
Clock
Ground
+2.5V
+3.3V
-3.3V
VREF
AGround
VHEATER
VDIODE
TempControl
LaRRKDriver_BM90nm
+2.5V
Ground
Clock
Ground
Data In
Ground
AGround
VHEATER
VREF
-3.3V
+3.3V
Heater 2
Heater 1
Ground
Modulator In
Ground

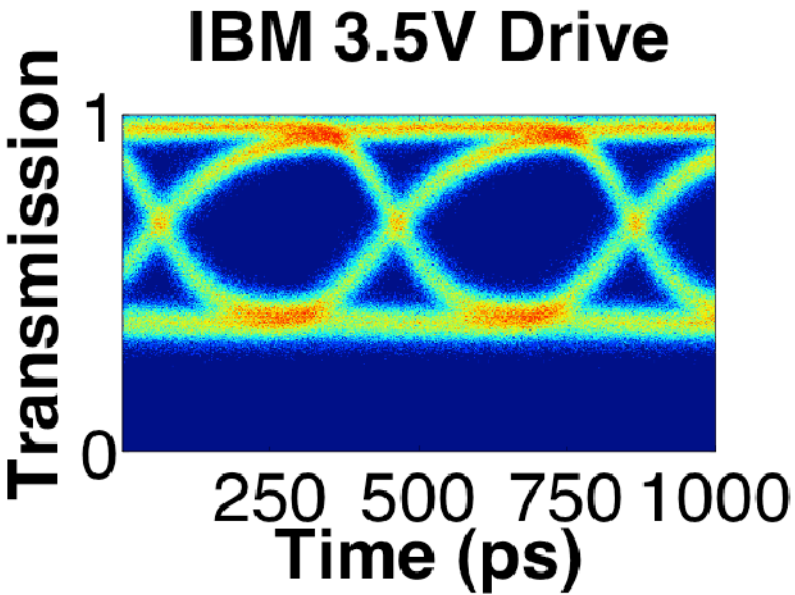

Sandia Silicon Photonic
Modulator (3.5µm Disk)
W. Zortman, M. Watts, D. Trotter
Fiber
Input
Fiber
Output


IBM 90nm CMOS driver
photonic chip
1 2 ... 8
50um input
pads & ESD
protect ~
lumped
inverter
chain
~240fF
bond wire~2nH
input/output
pads ~50fF
3.5um disk
~3fF
~600 ohm

Two Dimensional Integration

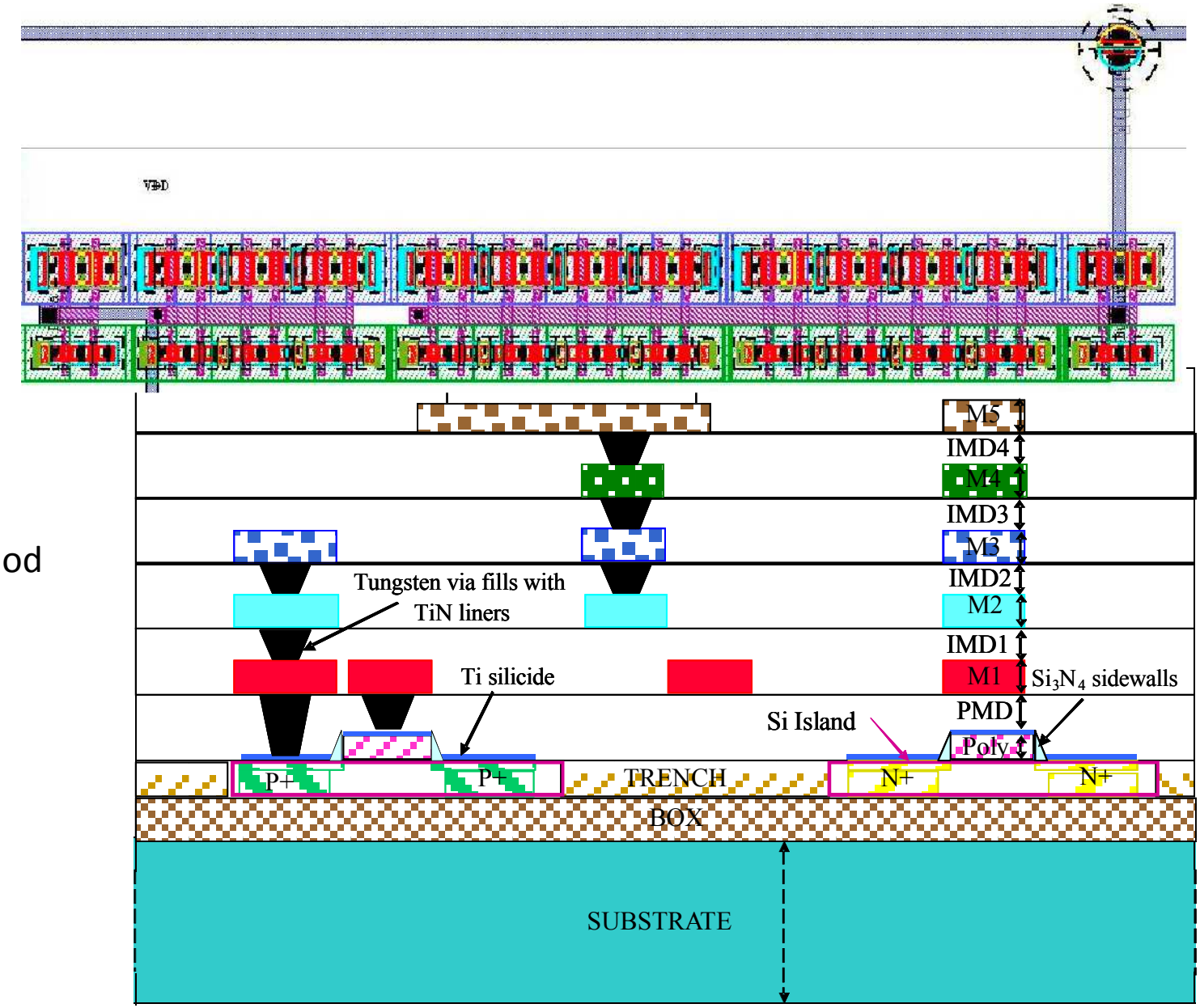
Energy buckets





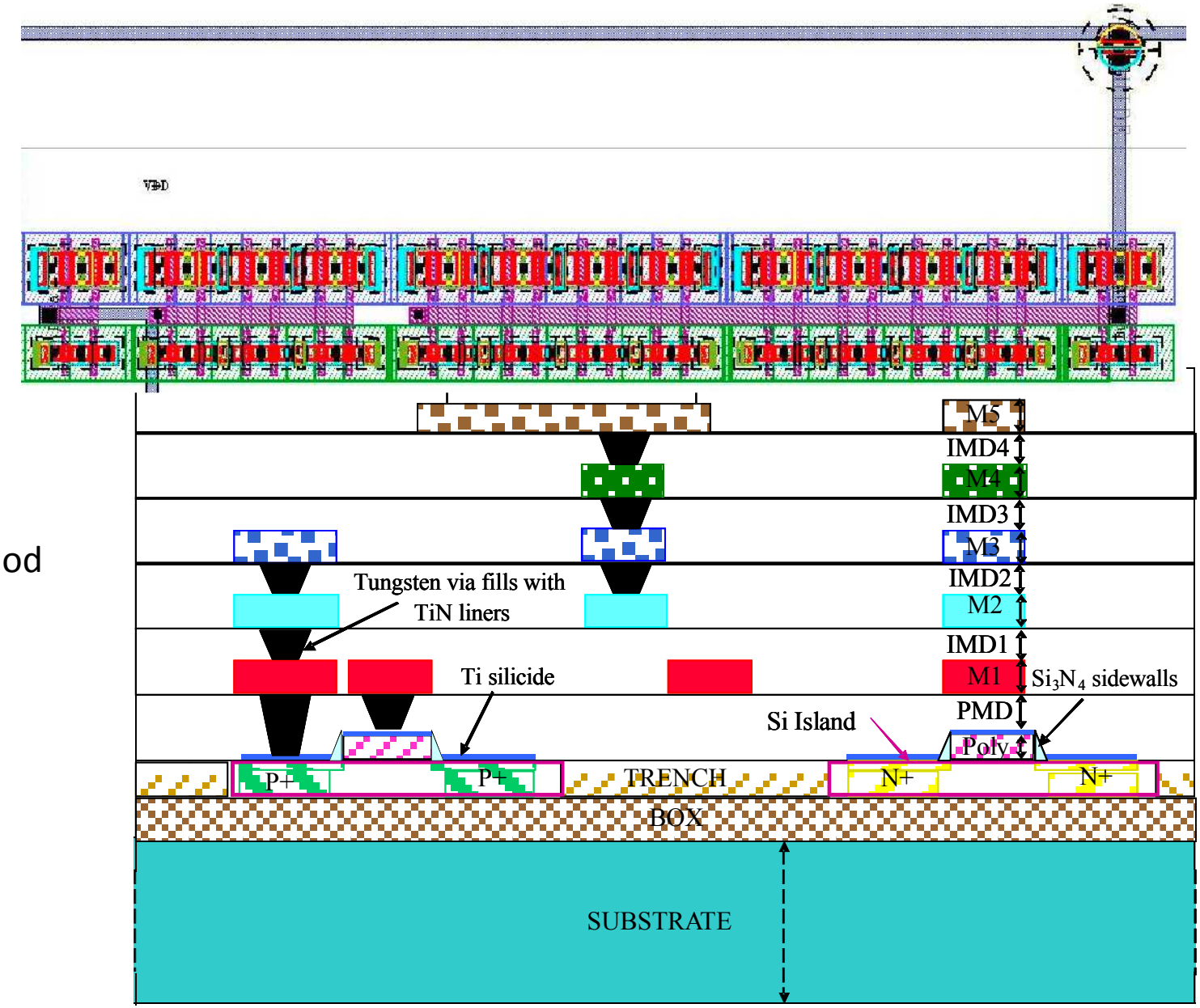
Layout of the Monolithic Chip

Add mod

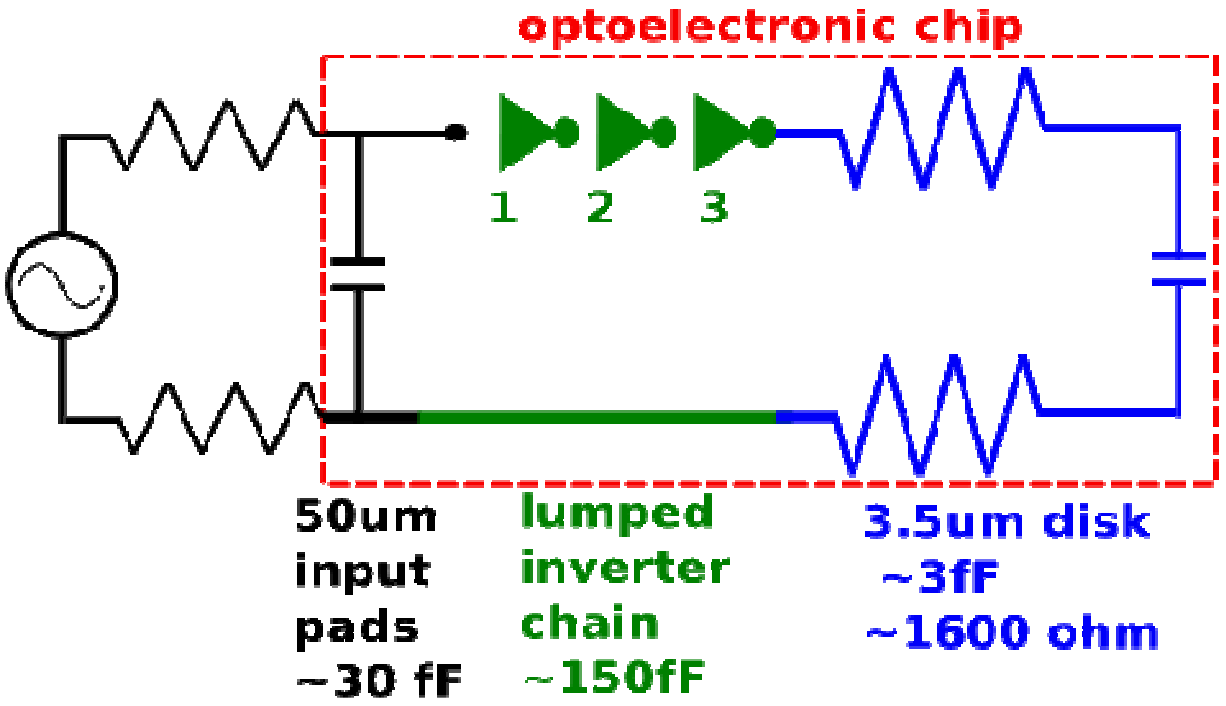


Layout of the Monolithic Chip

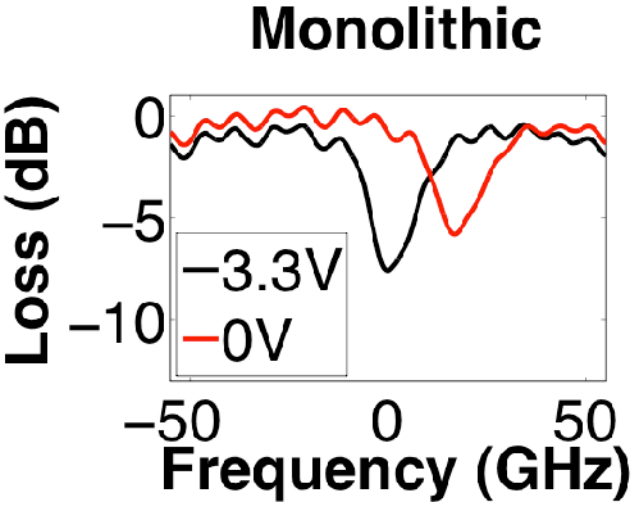
Add mod

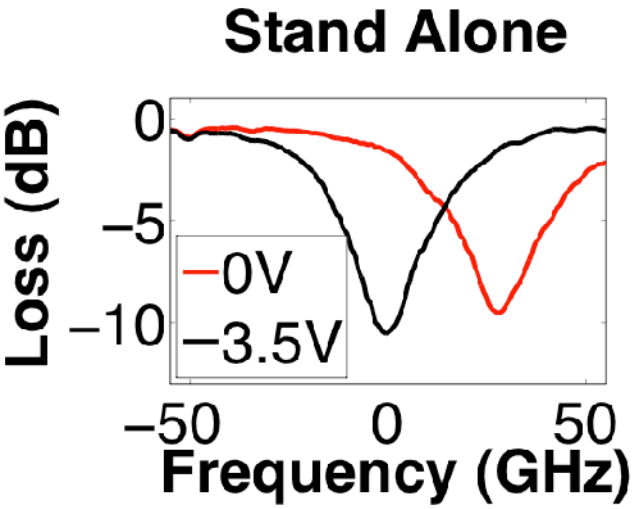


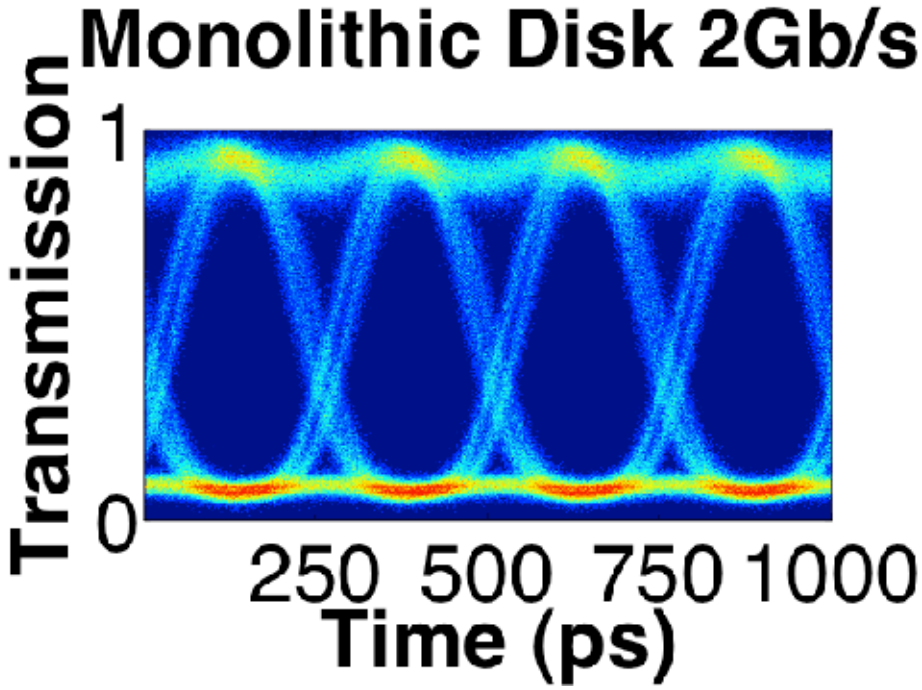
Equivalent Circuit



High Speed Modulation

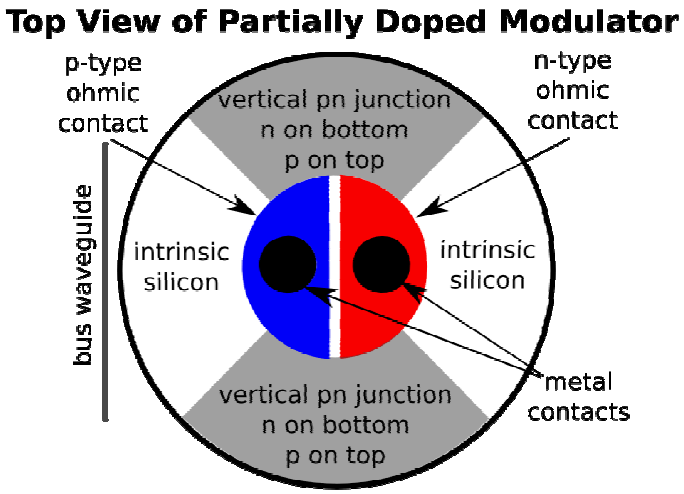


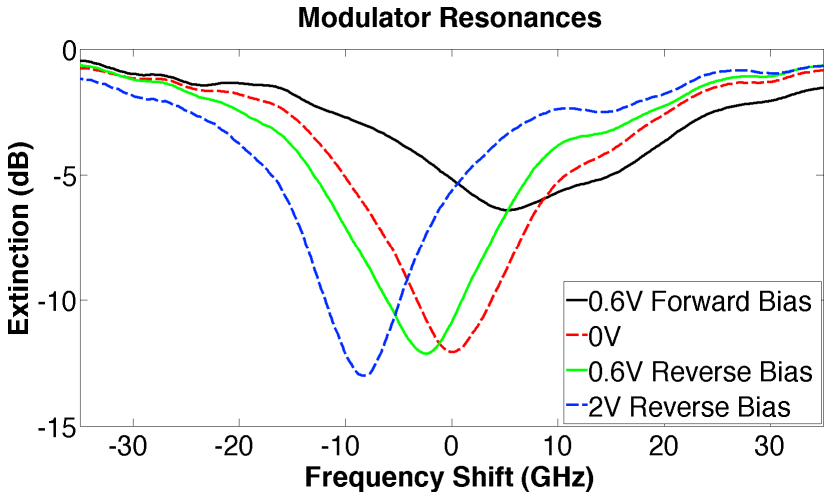


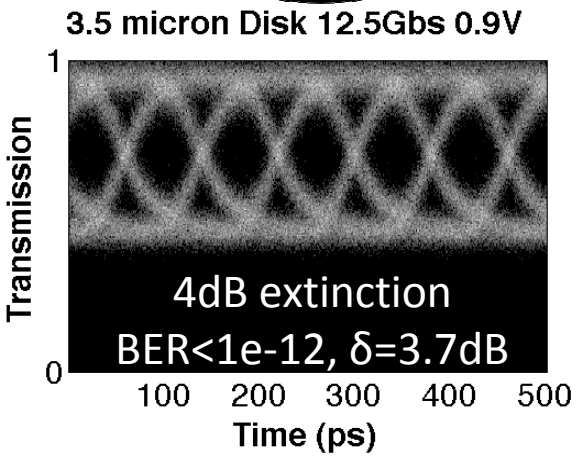


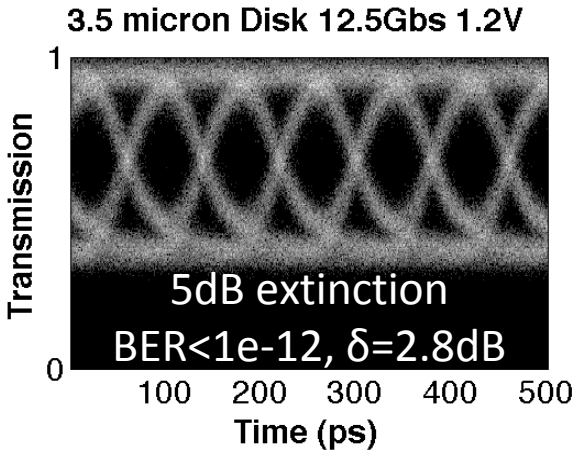
Device	Power	Energy	BW
Discrete Disk 3.5V	500uW	50fJ/bit	10Gbps
2D 2.5V	3.5mW	700fJ/bit	5Gbps
2D 3.5V	5.25mW	1pJ/bit	5Gbps
Monolithic 3.3V	1.68mW	840fJ/bit	2Gbps

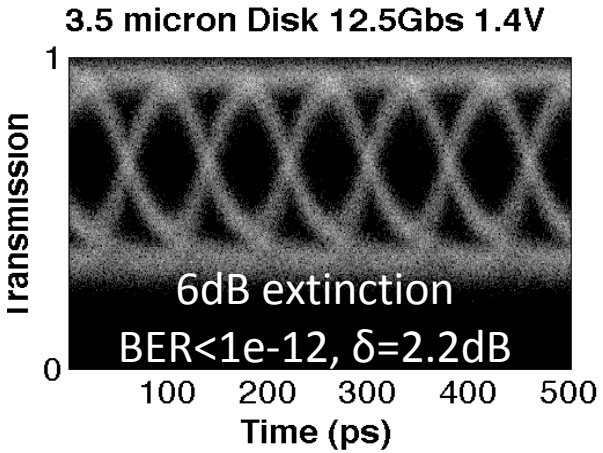
Disk Resonator











Energy/bit:	**0.9V**	**1.2V**	**1.4V**
Analysis:	**3.8fJ/bit**	**6.8fJ/bit**	**10.6fJ/bit**
Measured:	**3.2fJ/bit@1V**		**10.1fJ/bit@1.5V**

E_{bit}=3.2fJ @ 12.5Gb/s & 3.7dB Power Penalty

Summary

Multiprocessor chip and large machine performance is increasing the need for high bandwidth off chip solutions

Integration of low power modulators in monolithic and 2D regimes has been demonstrated

The potential for using a 1V low current (3mW) driver exists in a monolithic integration.

THE UNIVERSITY of NEW MEXICO

CHTM

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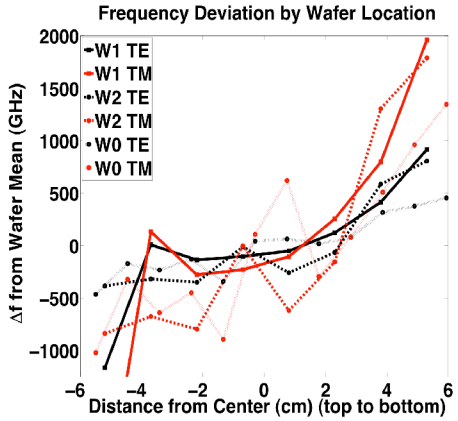
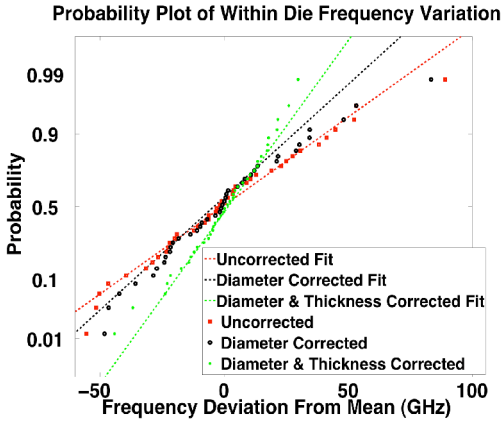
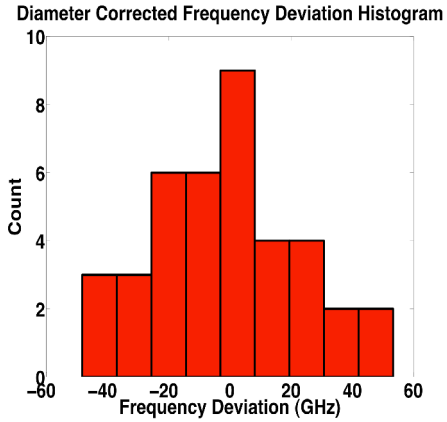
Sandia National Laboratories

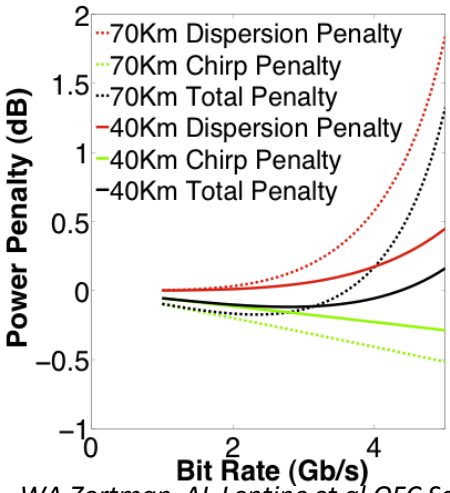
Manufacturability and Flexibility

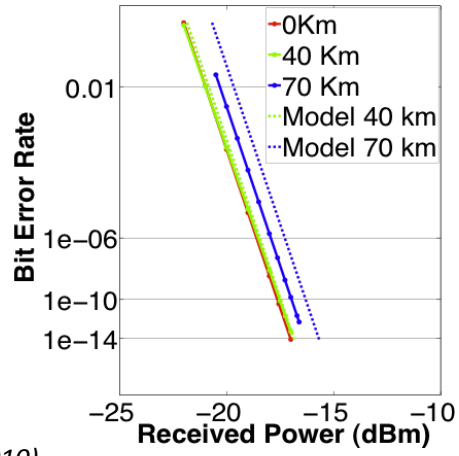






WA Zortman, DC Trotter et al OPEX (2010)
WA Zortman, MR Watts et al IPNRA Honolulu (2009)





WA Zortman, AL Lentine et al OFC San Diego (2010)

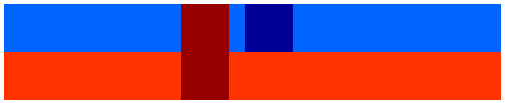
The process begins with 0.26 thickness silicon on insulator wafer of 0.5 microns of buried oxide.

The silicon is masked and etched into the waveguide and ring geometries.

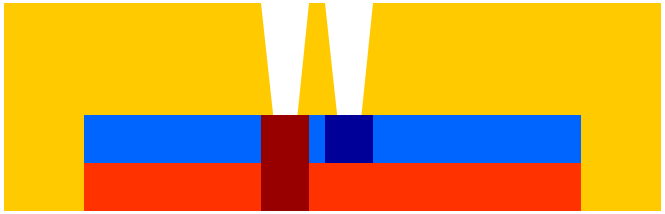
Following diagrams suppress the buried oxide and waveguides for clarity.

The wafer is masked to allow the P and N diode Dopants to be implanted at energies which allow depth separation.

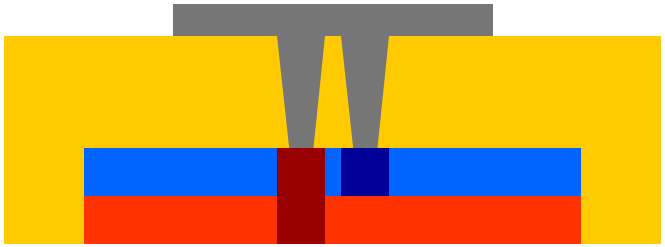
Ohmic contact masks and dopants are applied.



Oxide is deposited on the entire waver and then contact holes are masked and etched.

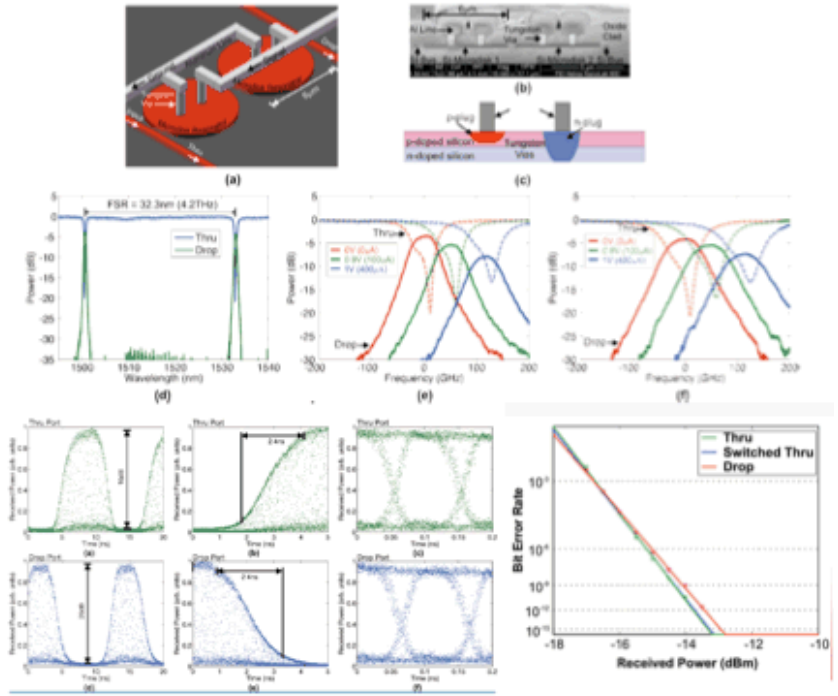


Finally the contact holes are metalized and interconnects are deposited and patterned onto the wafer.



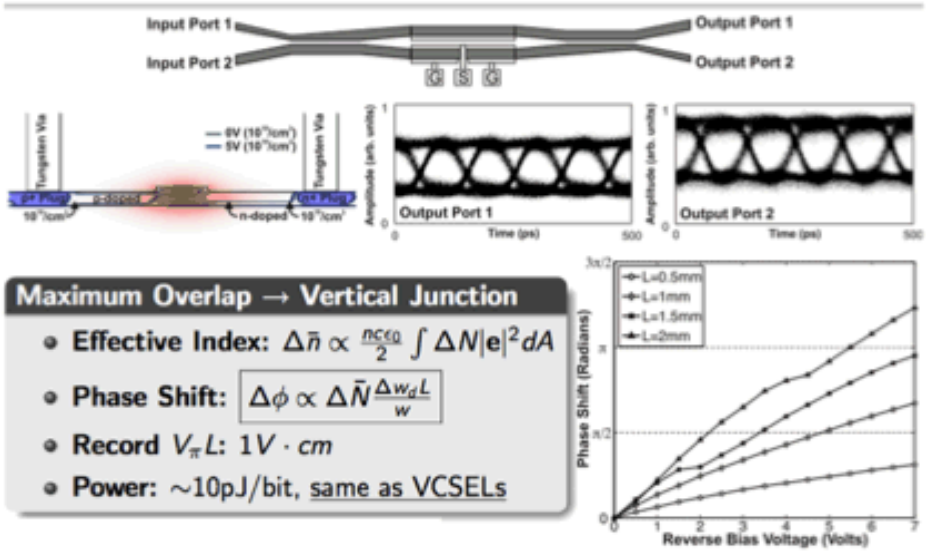
Sandia's Silicon Photonics Platform

Filter



MR Watts, AL Lentine, et al OFC (2008) (postdeadline)

Mach-Zehnder Modulator



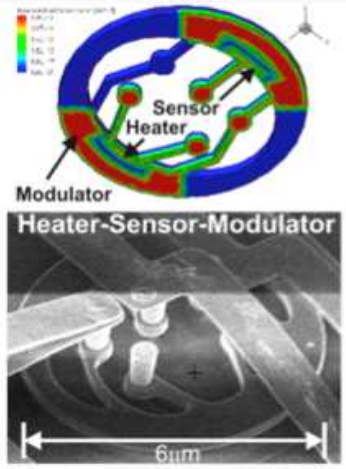
Maximum Overlap → Vertical Junction

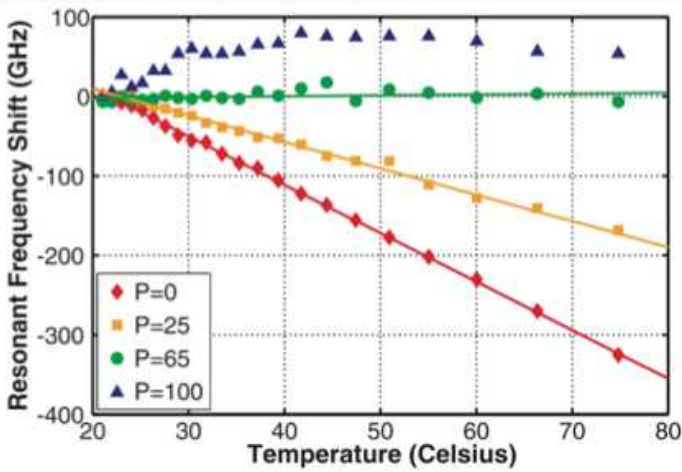
- **Effective Index:** $\Delta\bar{n} \propto \frac{n c \varepsilon_0}{2} \int \Delta N |\mathbf{e}|^2 dA$
- **Phase Shift:** $\Delta\phi \propto \Delta\bar{N} \frac{\Delta w_d L}{w}$
- **Record** $V_\pi L$: $1V \cdot cm$
- **Power:** ~10pJ/bit, same as VCSELs

MR Watts, WA Zortman, et al JSTQE Vol 16 2010
MR Watts, WA Zortman, et IPNRA Honolulu, Hi, 2009

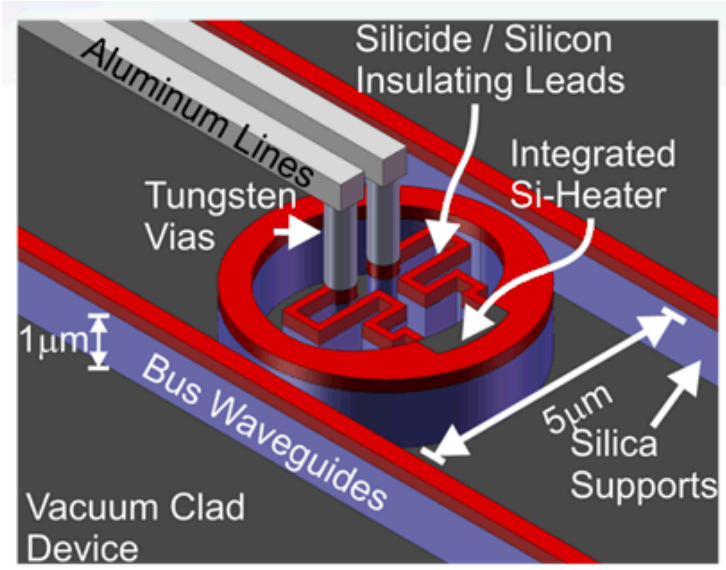
Sandia's Silicon Photonics Platform

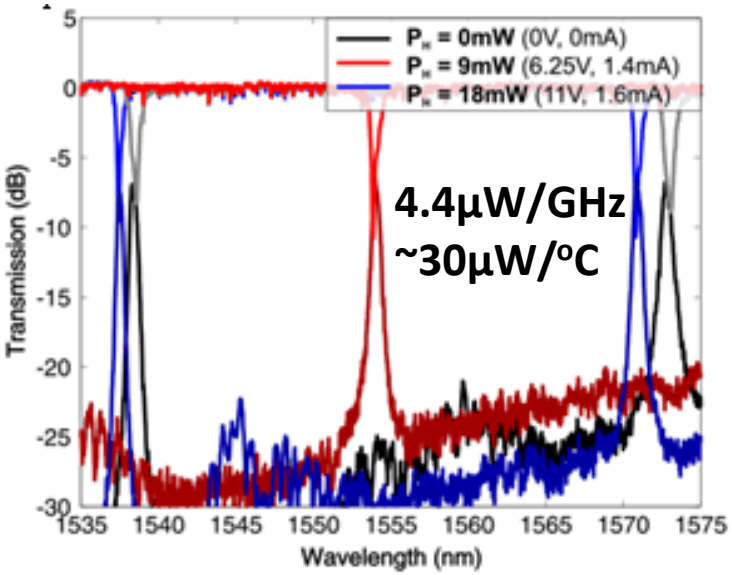
Single Mode Compact Tunable Resonators

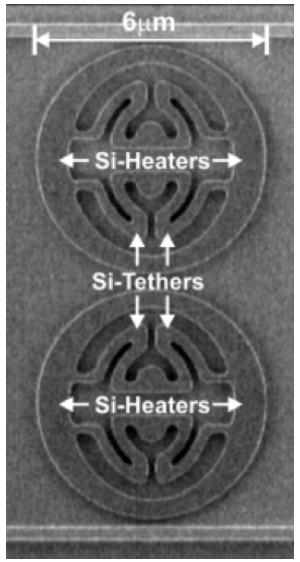




CT DeRose, MR Watts et al CLEO San Jose (2010) (post deadline)







MR Watts, WA Zortman et al CLEO San Jose (2009) (post deadline)