



# Low Voltage Differentially Signaled Silicon Resonant Modulators

SAND2011-7714C

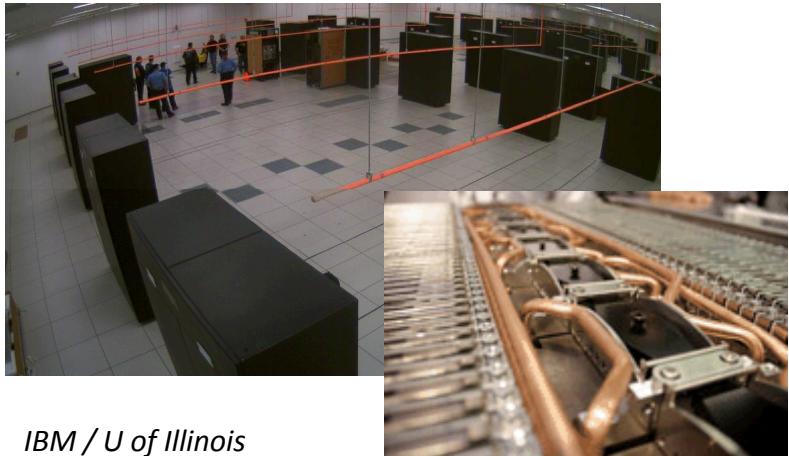
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Research Laboratory for Electronics

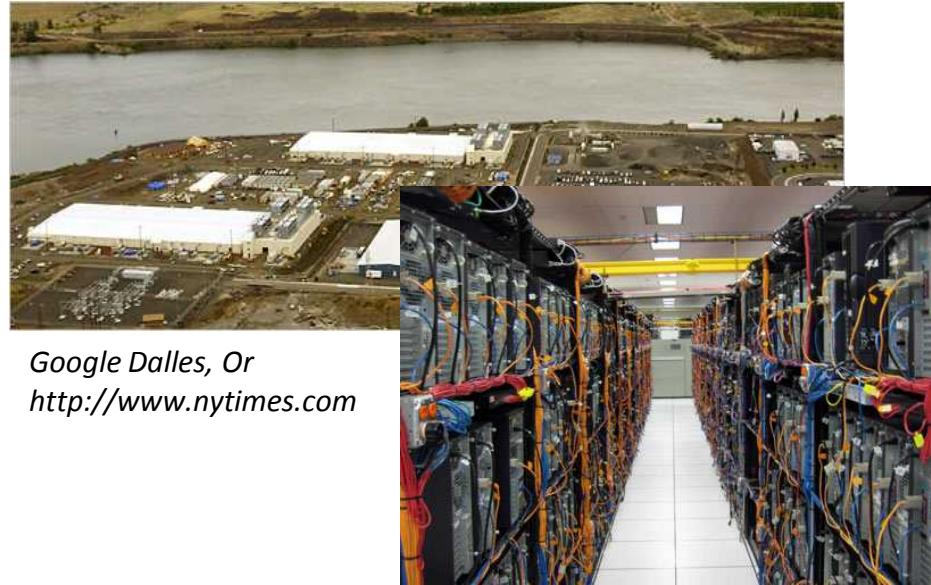
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# Supercomputer



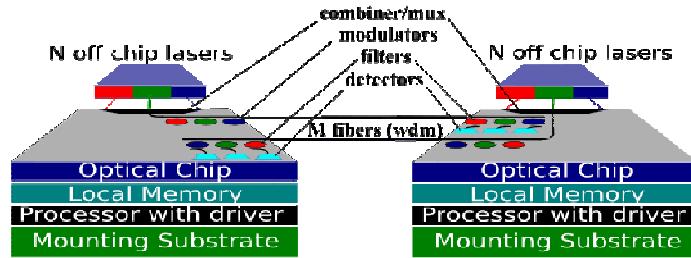
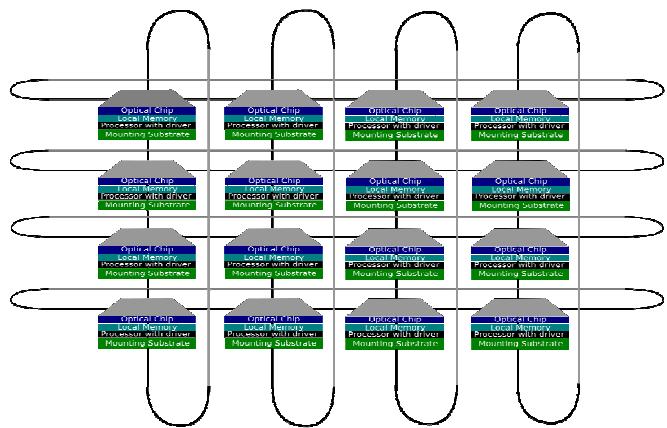
IBM / U of Illinois  
Blue Waters, <http://www.ncsa.illinois.edu/BlueWaters>

# Data Center



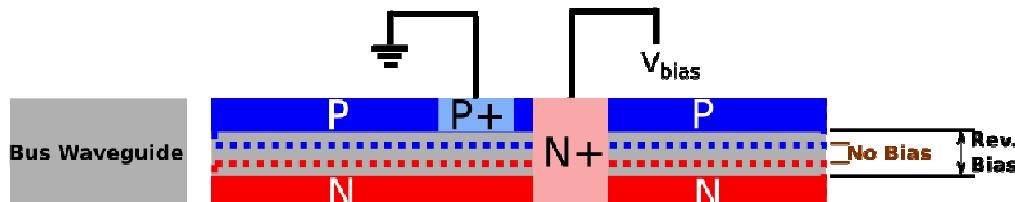
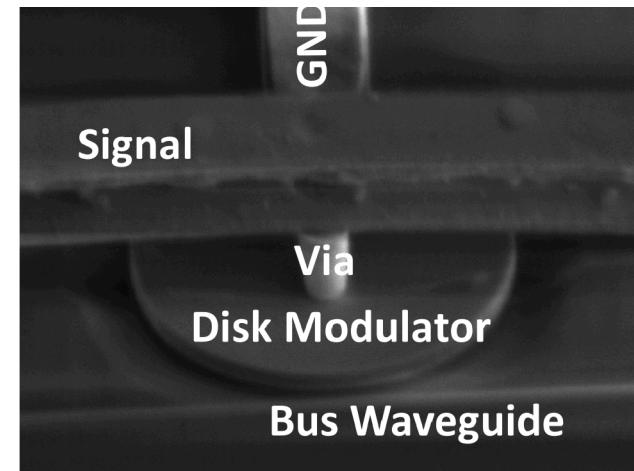
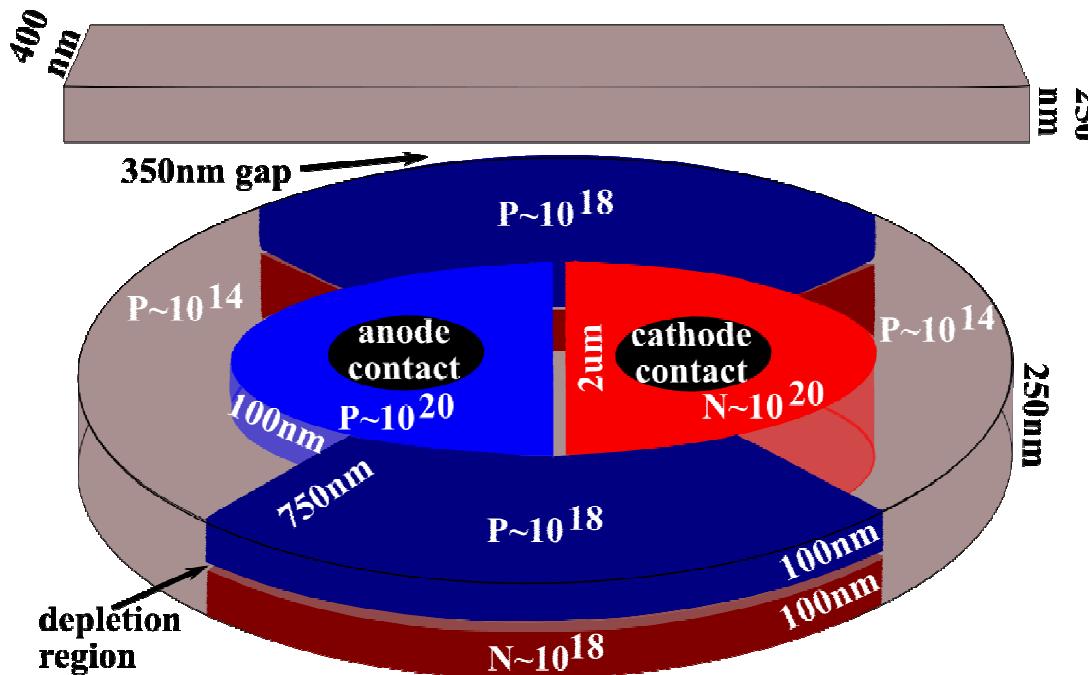
Google Dalles, Or  
<http://www.nytimes.com>

<http://scienceblogs.com>



These systems could likely run with electrical interconnect or continue with parallel multimode optics, however WDM waveguide integration offers BW and system simplicity advantages<sup>2</sup>

# Architecture of the modulator for today's talk



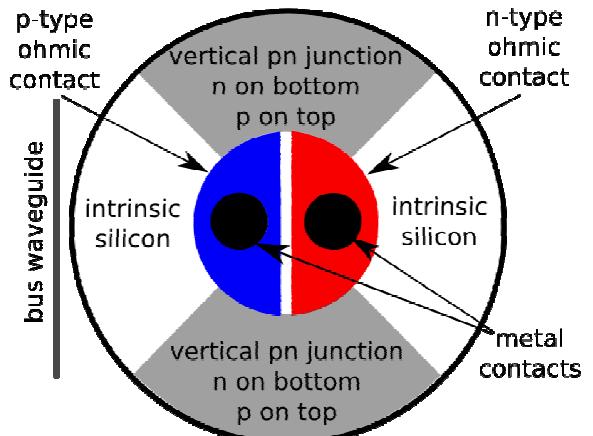
3.5 micron diameter

Silicon on Insulator 250nm thick silicon on 3 $\mu$ m buried oxide

5 $\mu$ m deposited oxide over the device and waveguide

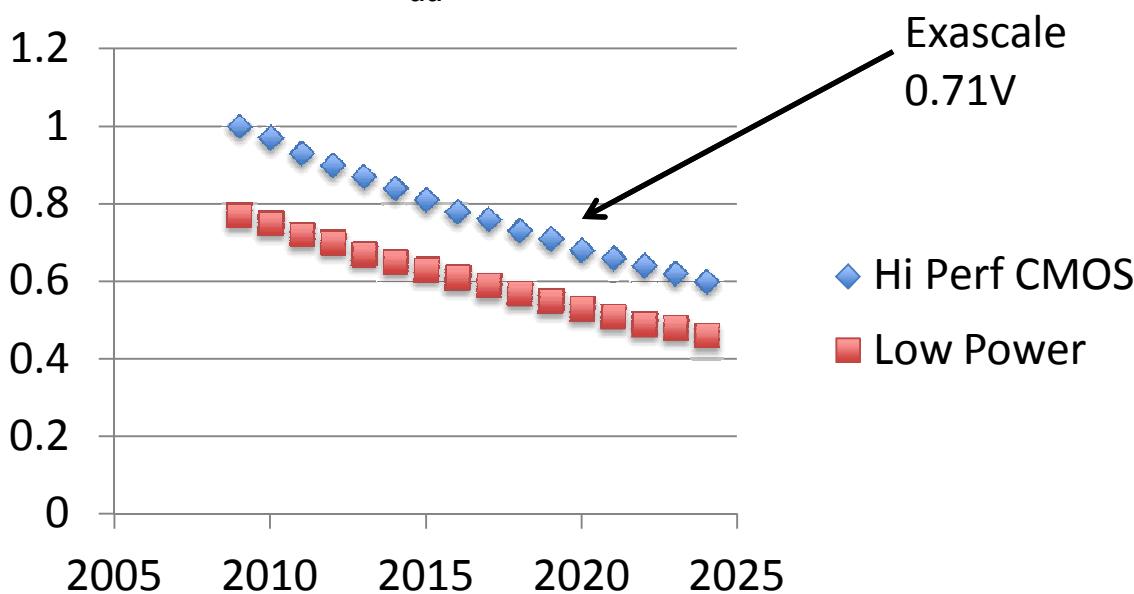
operates in reverse bias

## Top View of Partially Doped Modulator

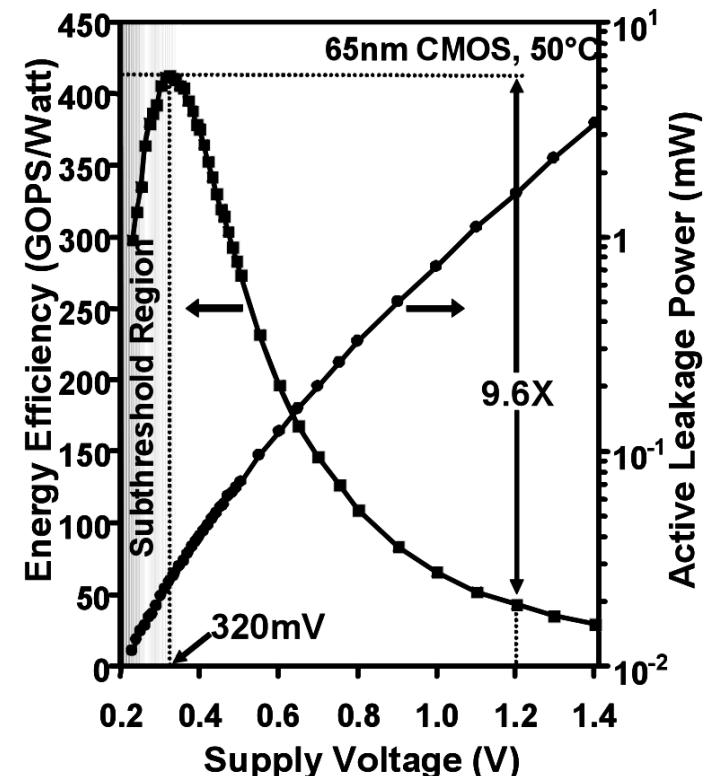
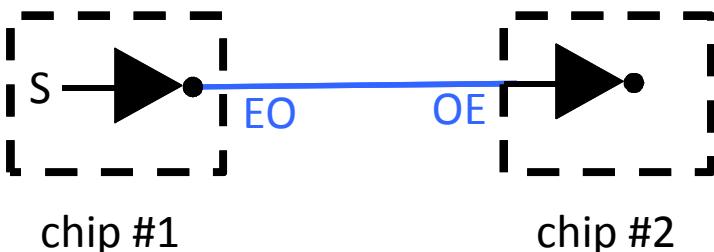


# Motivation for low voltage photonics

ITRS  $V_{dd}$  roadmap (2010)



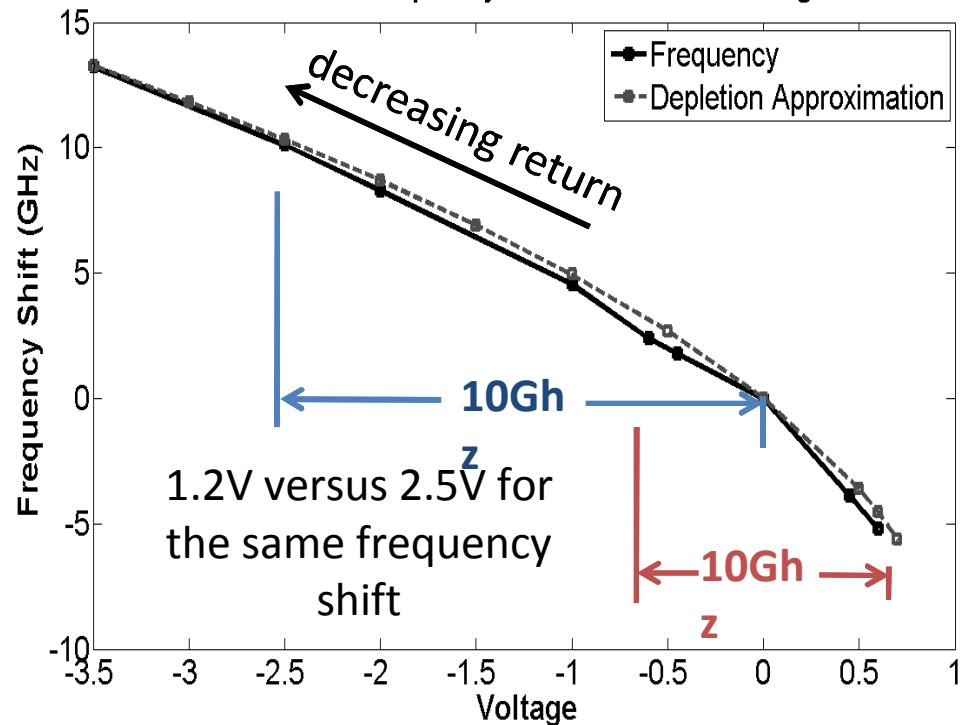
Ideally this situation is desired:



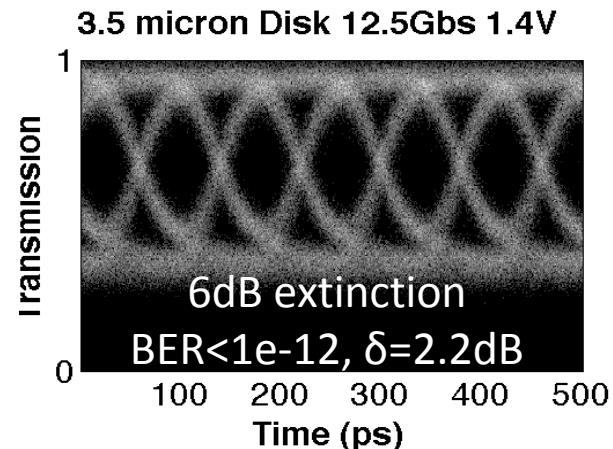
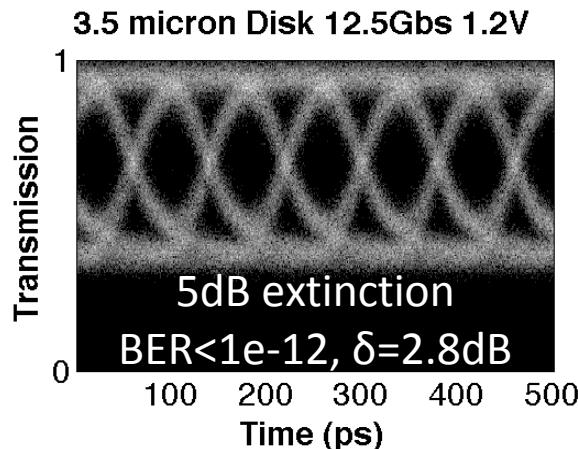
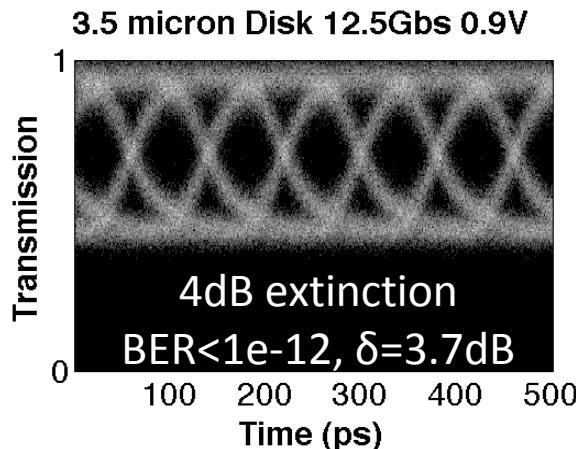
from Shekhar Borkhar,  
"The Exascale Challenge"

Differential signaling would ease integration with the potential for much lower  $V_{dd}$

### Resonant Frequency as a Function of Voltage



## AC coupling of drive signal



Energy/bit: **0.9V**

Analysis: **3.8fJ/bit**

Measured: **3.2fJ/bit@1V** Zortman, Watts, Trotter, Young, Lentine, CLEO, 2010

**1.2V**

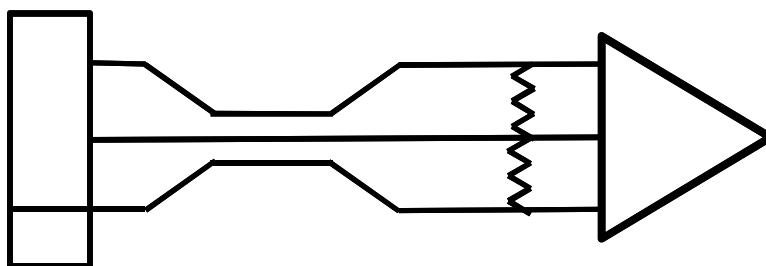
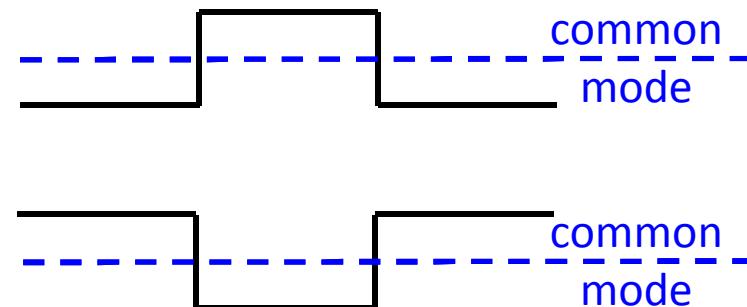
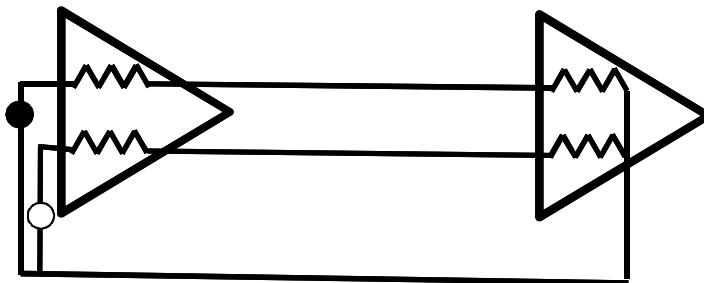
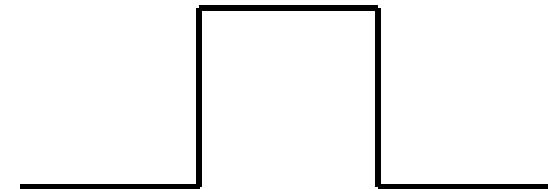
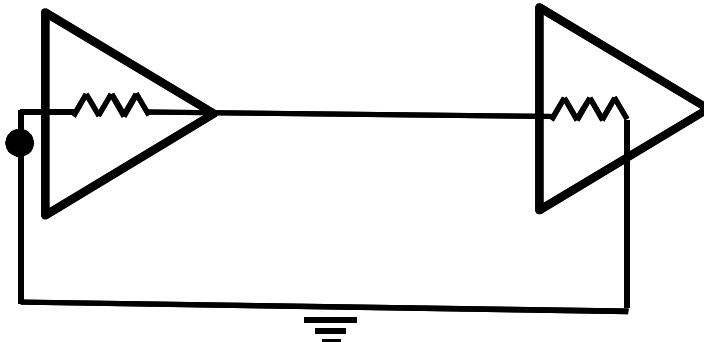
**6.8fJ/bit**

**1.4V**

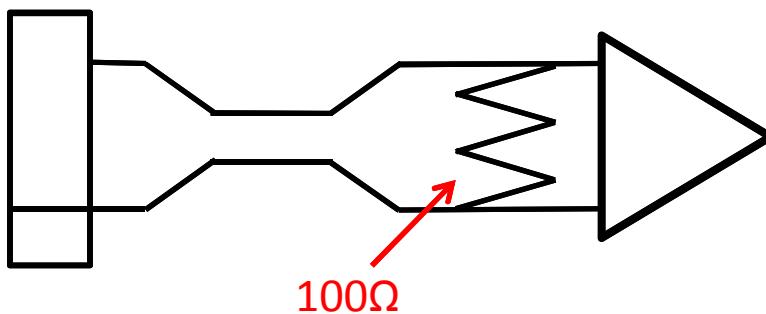
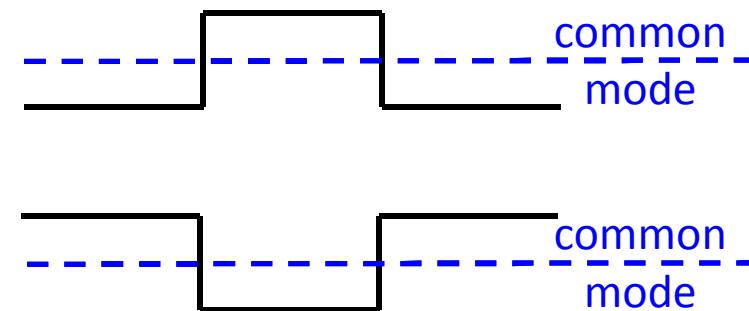
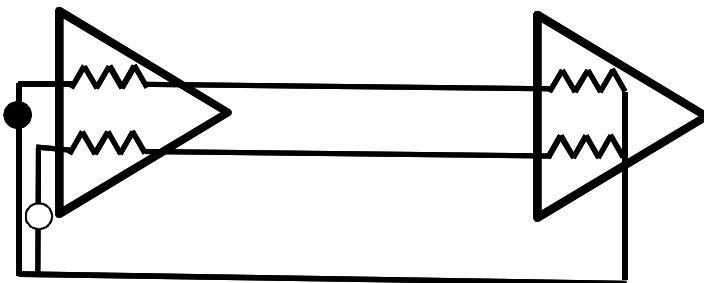
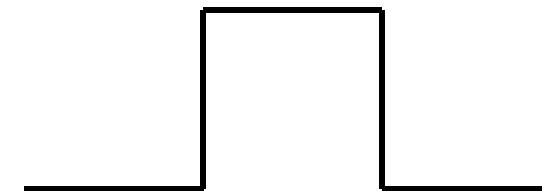
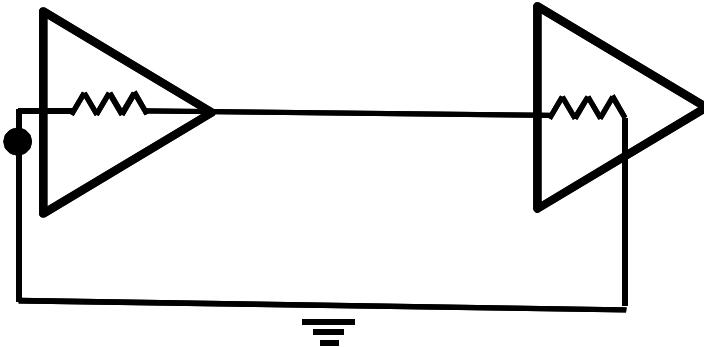
**10.6fJ/bit**

**10.1fJ/bit@1.5V**

For even lower voltage drivers: differential signaling is considered for driving the device

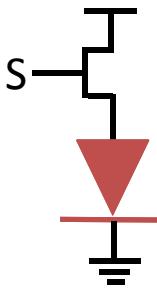


For even lower voltage drivers: differential signaling is considered for driving the device



## Forward Bias

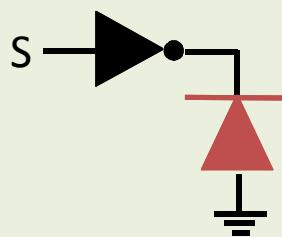
high current driver



CMOS

## Reverse Bias

high voltage driver



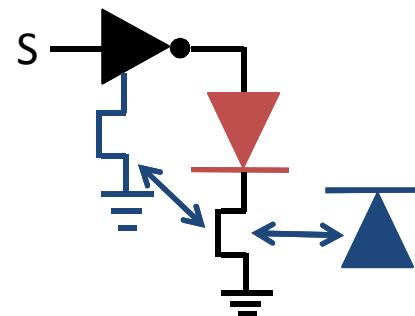
Xu et al, original  
Manipatruni et al CLEO

$\sim 1 \text{ PJ/bit}$   
 $V_{dd} = V$

Watts et al Gp 4 2008  
Dong et al OPEX 2009

$\sim 50 \text{ fJ/bit}$   
 $V_{dd} = 3.5 \text{ V}$

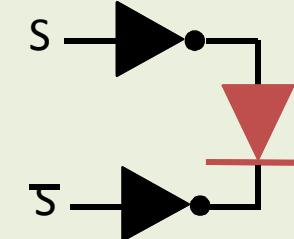
## AC Coupling



Zortman, Watts et al CLEO 2010  
Watts et al OPEX 2011  
Dong et al OL 2010  
Glenn et al OPEX 2011

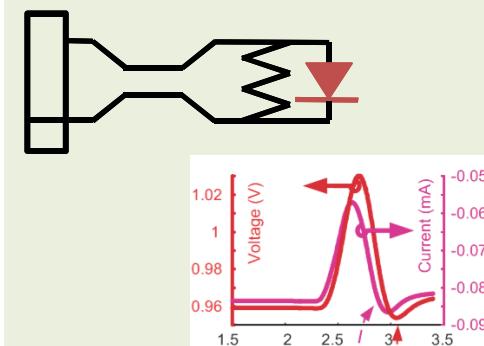
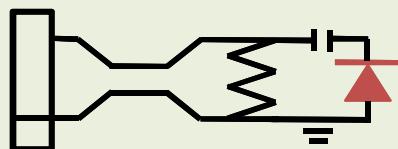
$3 \text{ fJ/bit}$   
 $V_{dd} = 1 \text{ V}$

## Differential Signaling



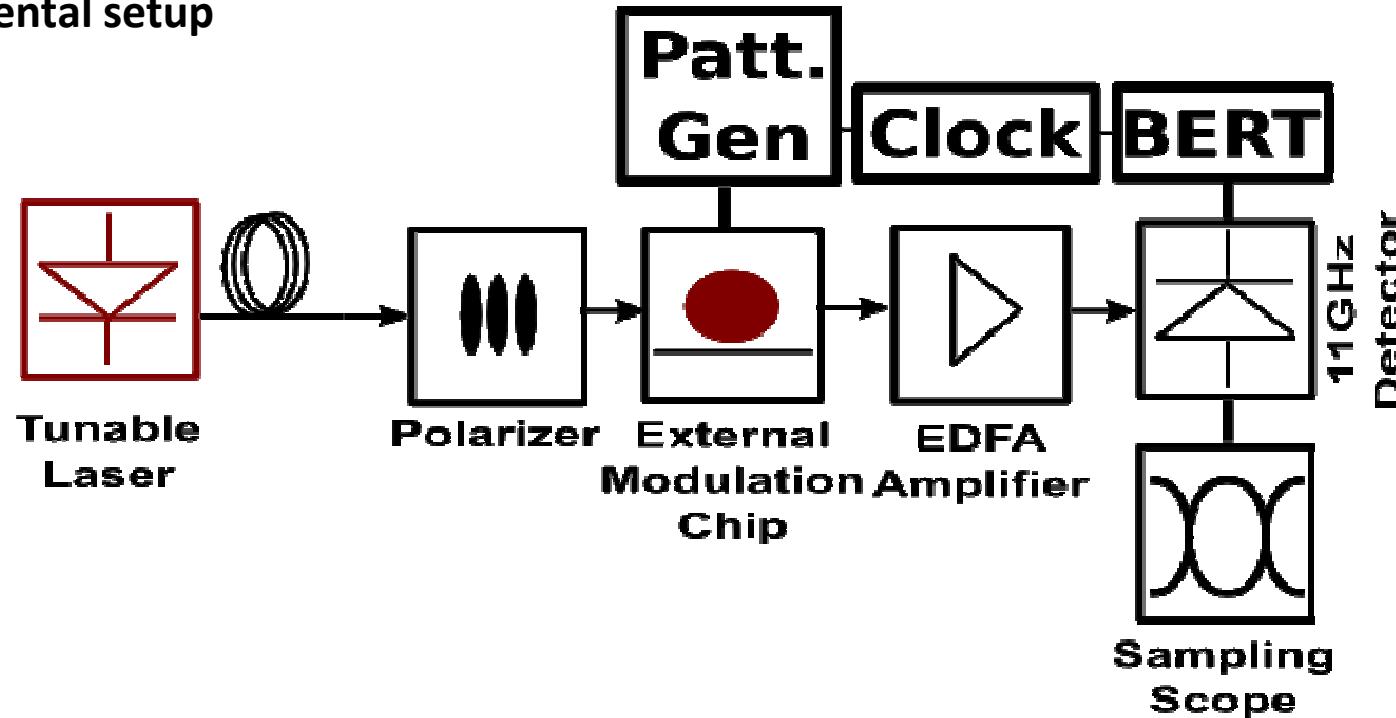
This Work

$3 \text{ fJ/bit}$   
 $V_{dd} = 500 \text{ mV}$

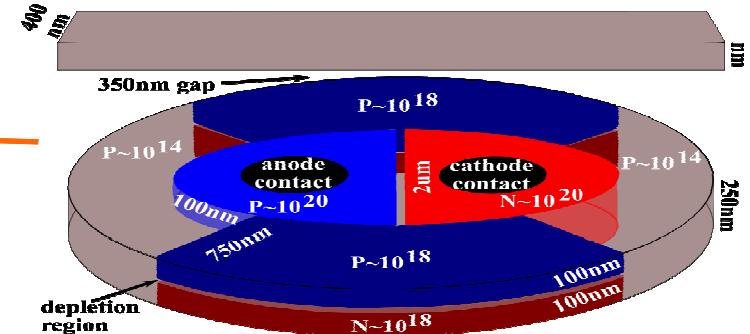
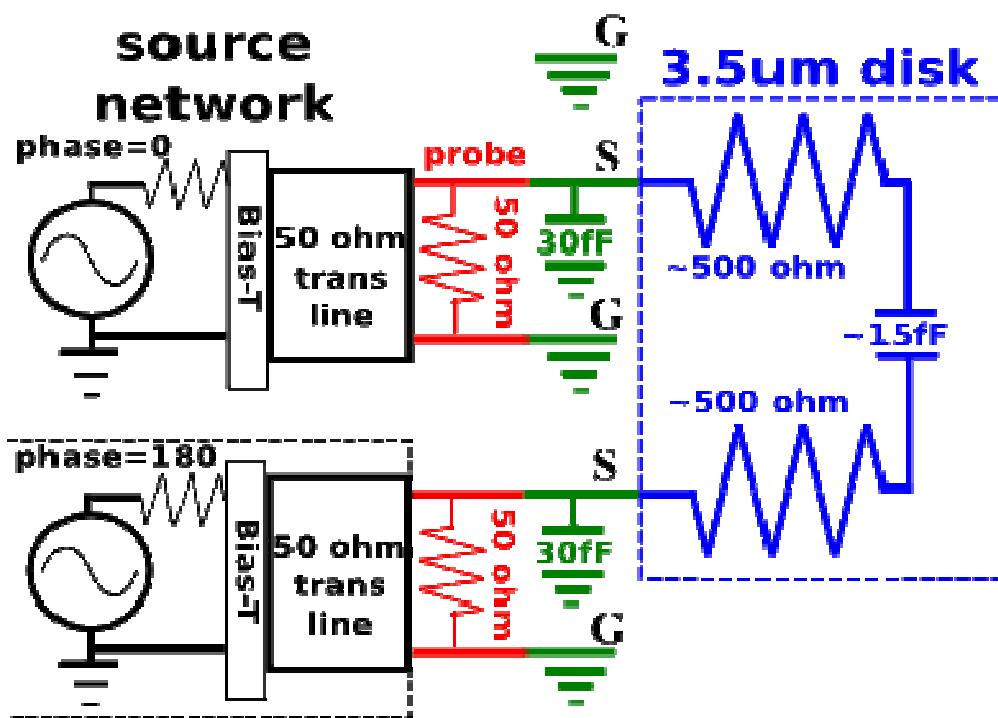
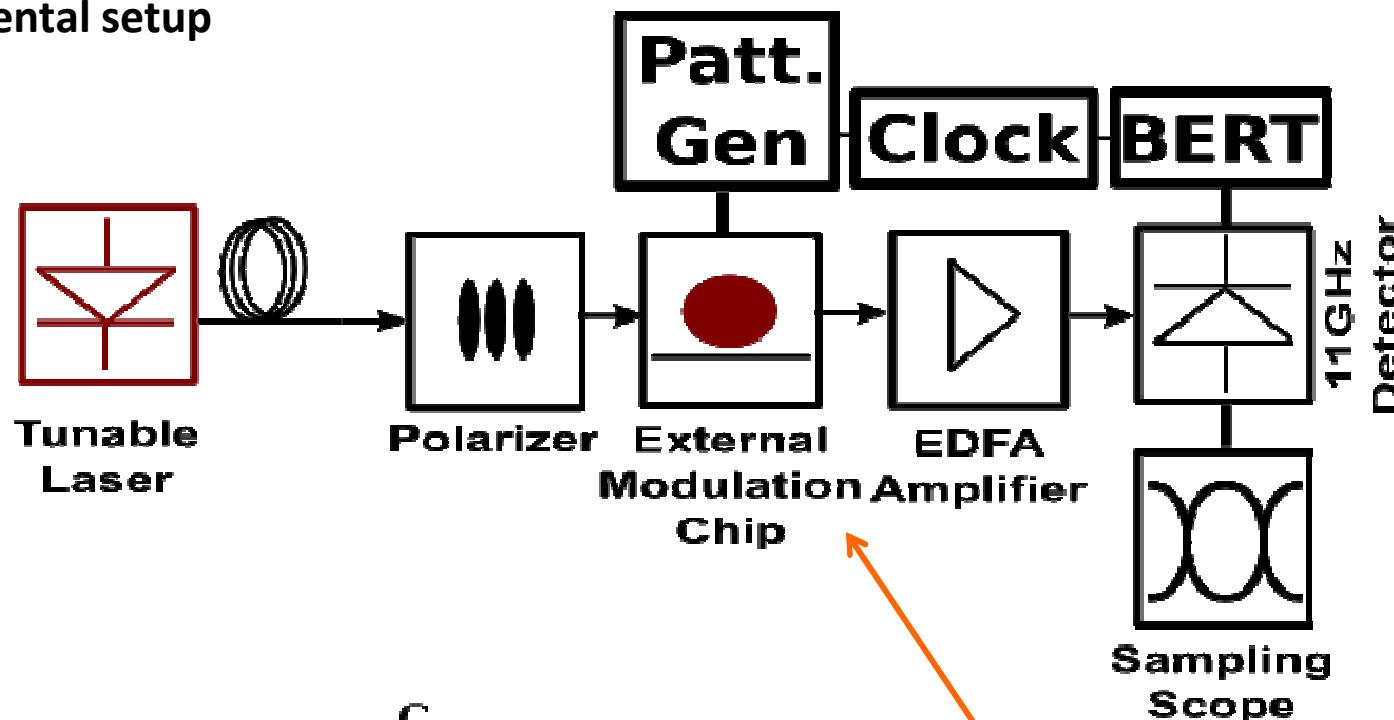


356fJ/bit 90nm 4Gbps CMOS LVDS  
Kim, Stojanovic ISSCC 2009

## Experimental setup

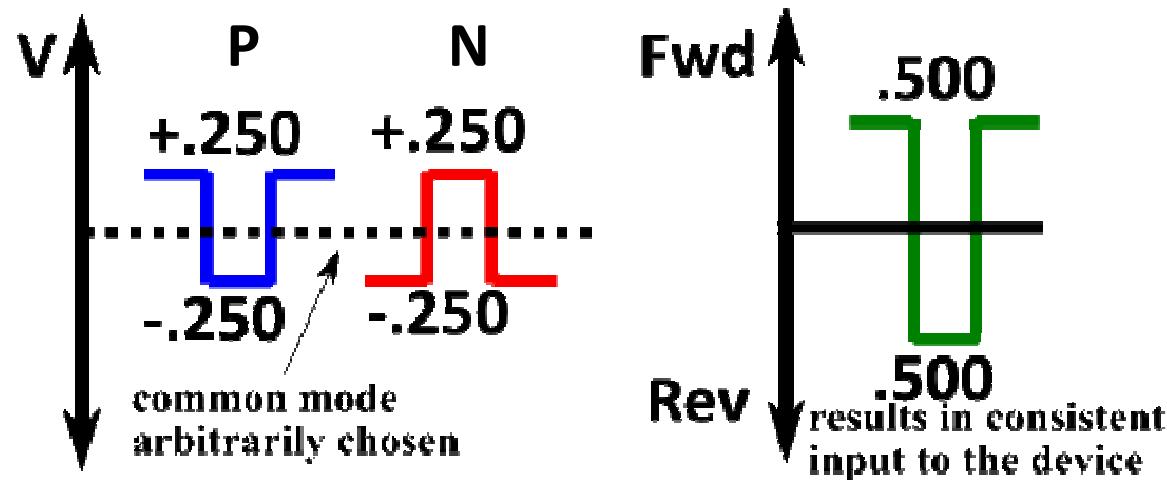


## Experimental setup



# The easiest to implement is symmetric differential signaling

... the common modes are the same and the BER <10<sup>-12</sup>



## common modes (AC or DC coupling)

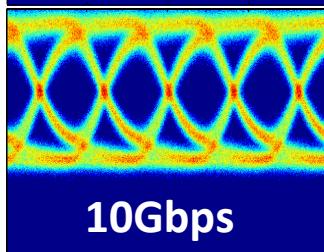
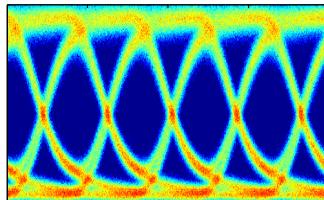
0V

1.25V

1.5V

drive amplitude

500mV



400mV

7dB

3.2

extinction

5dB

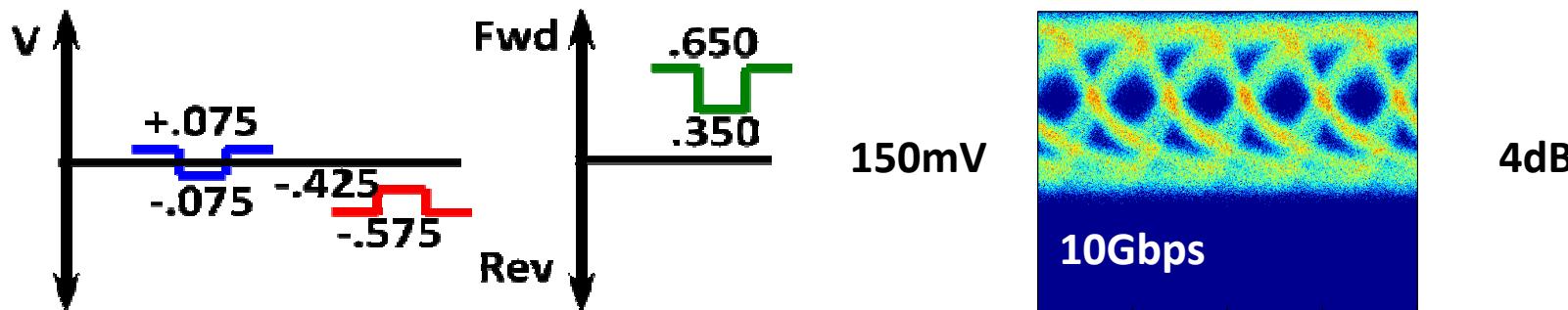
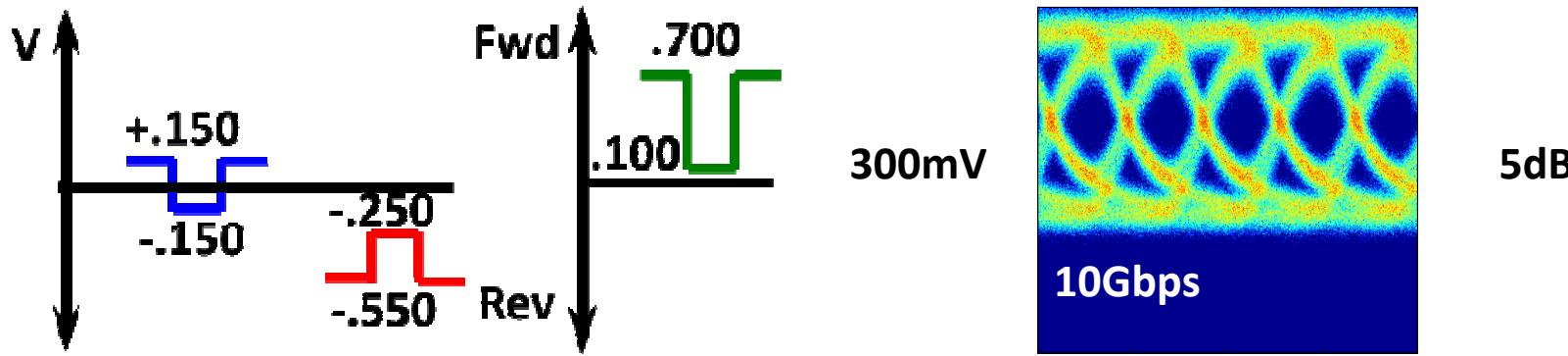
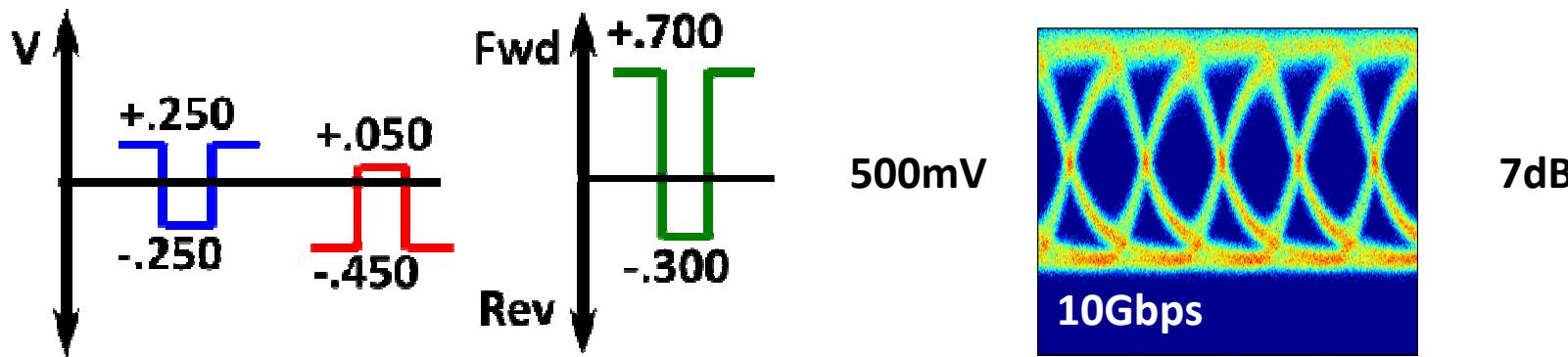
~2

energy/bit (fJ)

## Assymmetric signaling is a larger challenge

... the common modes are different and can require negative drive

however this allows drive into forward bias and a slight increase in extinction ratio for a given V

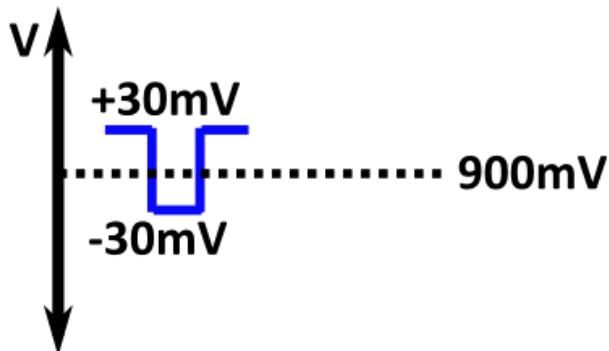
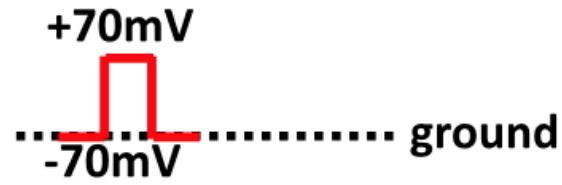
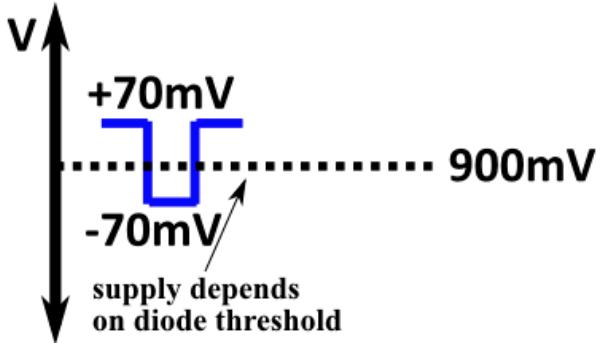


## Forward bias differential signaling

This requires a DC current, however the voltages to swing are very low

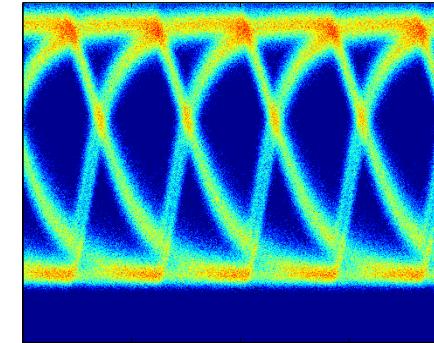
We find that going beyond 2<sup>7</sup>-1 PRBS with BER<10<sup>-12</sup> is not possible due to resistive heating

This would require fan-out to a larger driver because  $V_{I,\text{sat}}$  is forecast to be ~350mV



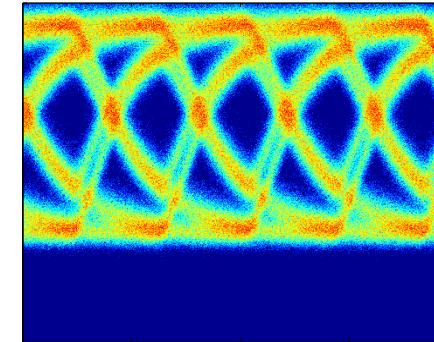
70mV

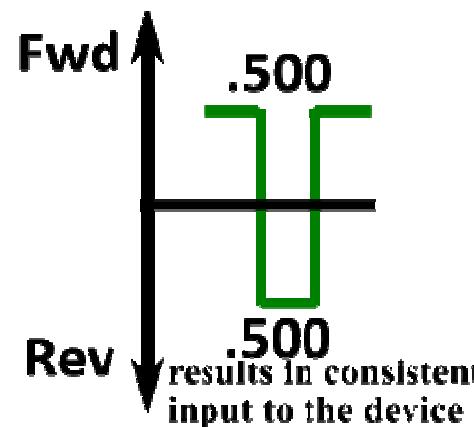
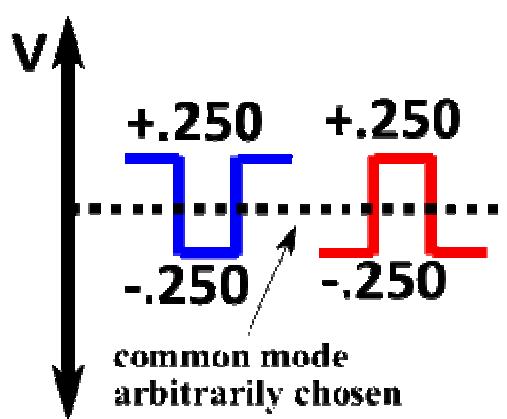
1Gbps



30mV

5dB





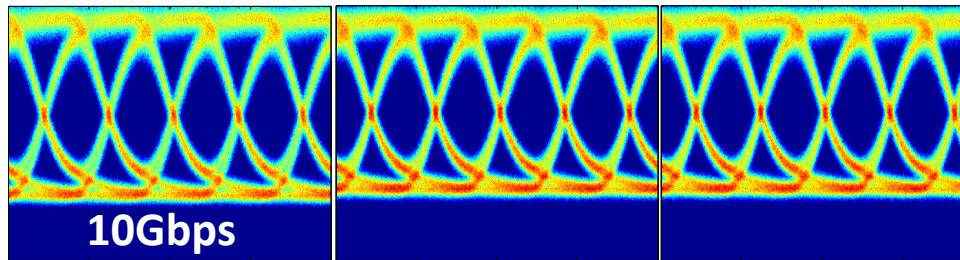
### common modes (AC or DC coupling)

0V

1.25V

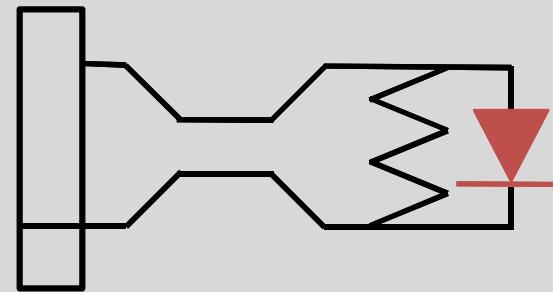
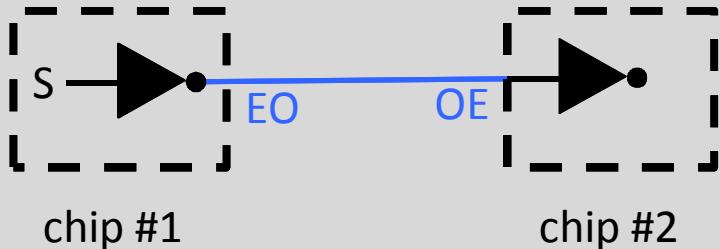
1.5V

500mV



7dB ext. 3.2fJ/bit

Compatible with LVCMOS, VCL, CML, LVDS and requires *no special drivers*





# Conclusion

## Advantages of Differential Signaling for Silicon Photonics

Broadens the design space

Direct interface to LVDS

Compatibility with future  $V_{dd}$  scaling

Works with  $V_{\text{applied}}/2$

## New Capabilities Demonstrated

BER < 1e-12 with 150mV supply and <1fJ/bit (asymmetric)  
with 400mV supply and ~2fJ/bit (symmetric)

## Questions

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