SAND2013-4924C

Comparative Analysis of Anti-Islanding Requirements and Test Procedures in the United States and Japan

Abraham Ellis[1], Yusuke Miyamoto[2], Sigifredo Gonzalez[1], Michael Ropp[3], Dustin Schutz[3], Takanori Sato[4]

[1]Sandia National Laboratories, [2]Kandenko Co., Ltd, [3]Northern Plains Power Technologies, [4]Japan Electrical Safety & Environment Technological Laboratories

***Abstract* — Existing standards require that DGs disconnect from the grid in a short period of time in order to coordinate with protection systems, avoid poor power quality that can cause damage to connected load, and for safety reasons. The goal is to prevent the unintentional formation of an electrical island. Based on industry experience, today's active anti-islanding algorithms are very effective. Consideration of scenarios with high penetration photovoltaic (PV) has renewed interest in anti-islanding performance in certain cases involving multiple inverters of different types, or inverters that incorporate voltage and frequency tolerance or control voltage. This paper describes the results of anti-islanding testing and analysis conducted by Sandia in collaboration with Kandenko Co. Ltd. (Kandenko) and Japan Electrical Safety & Environment Technological Laboratories (JET), to evaluate the performance of existing and new anti-islanding technologies in the multi-inverter case, and to compare anti-islanding requirements and test procedures applicable in the United States and Japan.**

***Index Terms* — PV inverter, anti-islanding, testing.**

I. Introduction

Medium voltage electric distribution feeders are typically configured in a radial topology. When a protection device (circuit breaker, recloser, sectionalizer or fuse) or a switch opens, intentionally or unintentionally, a portion of the distribution system is isolated from the rest of the grid. In addition to connected load, the isolated portion could have distributed generators (DGs) such as PV systems. Existing standards require that DGs disconnect from the grid in a short period of time in order to coordinate with protection systems, avoid power quality that can cause damage to connected load during an islanding scenario, and for safety reasons. DGs are required to incorporate functionality to detect the formation of an island, and reliably disconnect from the grid within a short period of time. Islanding detection is also referred to as loss of mains (LOM) detection. If the load and generation in the isolated part of the system are not balanced, voltage and frequency quickly exceed normal ranges, allowing DGs to easily and quickly detect the islanding condition. However, if the load and the generation in the island are closely matched, it is possible that a condition will occur such that voltage and frequency remain within normal operating range for a long period of time. In these cases, it may be difficult for DGs to reliably detect islands based solely on passive monitoring of line voltage and frequency. To ensure effective islanding detection, various anti-islanding control methods can be used. The basic principles of anti-islanding and their expected performance have been documented extensively [1], [2].

Based on industry experience, today's active anti-islanding algorithms are very effective. Consideration of scenarios with high penetration PV has renewed interest in anti-islanding performance with respect to the number of inverters in the island [3-4], different types of anti-islanding controls [5-6], presence of other types of DGs or rotating machines [7-8], emerging voltage control requirements as well as voltage and frequency ride-through requirements [9], and possible impact of active anti-islanding on system stability [10-11]. There is high interest in determining whether testing procedures for anti-islanding should be modified in the future, in light of these factors.

This paper describes the results of anti-islanding tests conducted in the US and Japan, with the purpose of comparing anti-islanding requirements, test procedures applicable in the United States and Japan, and how the test results are analyzed. Section II compares requirements and test procedures applicable in the US and Japan. Section III shows the result of laboratory tests conducted at Sandia and Japan, using the same type of PV inverter. Section IV offers general conclusions.

II. Comparison of Anti-Islanding Requirments and Test Pocedures in the US and Japan

In the United States, as well as in Japan and other countries, generators designed for interconnection to the distribution system, including PV inverters for residential and commercial applications, are typically certified by an independent laboratory to be non-islanding. Currently, the anti-islanding requirement and test procedure applicable in the United States is contained in the IEEE Standard 1547 [12] and IEEE Standard 1547.1 [13], respectively. The corresponding IEC standard is IEC Standard 62116 [14]. In the US, PV inverters are usually certified for anti-islanding according to Underwriters Laboratory (UL) Standard 1741 [15], an adaptation of the IEEE Standard 1547.1. In Japan, the anti-islanding requirement and corresponding test procedure are specified in JET Standard JETGR0003-4-1.0 [16]. Both standards permit external means to detect an islanding condition and disconnect. In both jurisdictions, certification is required as a condition for interconnection of DG in distribution systems. The key differences in the anti-islanding requirements are as follows:

- The IEEE/UL standard specifies a maximum disconnect time of 2.0 seconds, whereas the JET standard specifies a maximum disconnect time of 0.2 seconds. It should be noted that IEEE Standard 1547 also specifies that DGs are required to disconnect "prior to reclosing", which presumably would take place in a time frame shorter than 2 seconds; however, this requirement is not typically enforced.
- The IEEE Standard 1547 does not specify the type of anti-islanding algorithm (any type of algorithm that passes the test is allowed). Since 2011, PV inverters designed for deployment in Japan are required to implement the Japanese Standard Islanding Detection (JSID) algorithm [17]. Section III has a description of this algorithm.

The US and Japan requirements and test procedures are similar, but differ in key areas (Table 1). The UL 1741 certification test applies to a single inverter connected to an RLC (resistive-inductive-capacitive) circuit where real power demand matches the inverter output, and the capacitive and reactive elements with a quality factor of 1.0. The quality factor, Q, defines the relative size of the reactor and capacitor with respect to the size of the inverter, according to the relationship $Q=R\sqrt{(C/L)}$, where R is selected to match the inverter output. Tests are performed with the inverter operating at 100%, 66% and 33% of rated capacity, with active power load matched to the inverter output. For each output scenario, tests are conducted with matched reactive power, and with +/-1%, +/-2%, +/-3%, +/-4%, +/-5% reactive imbalance. The Japanese standard also addresses testing for a single inverter as well as multiple inverters (up to 10) with the same anti-islanding algorithm. The test circuit includes an induction motor with a specified minimum inertia.

During the test, the motor is unloaded, and draws approximately 150W. Resistive and capacitive loads are added to achieve the prescribed set of test conditions consisting of combinations of active and reactive power imbalance of 0 (matched), +/-5% and +/-10%. A specific quality factor is not required; however, because capacitance is added only to compensate for the reactive consumption of the induction motor under steady state conditions (pre-islanding), the equivalent quality factor is significantly lower than 1.0. After the island is formed, the quality effective factor varies widely due to the non-linear response of the motor load under varying voltage and frequency. Unlike the UL test, the JET test procedure does not require testing at partial output.

II. DESCRIPTION OF THE JSID ALGORITHM

Interconnection requirements in Japan specify the type of anti-islanding algorithm that distribution-connected PV inverters are required to have. The JSID algorithm consists of two parts: a frequency feedback function (Figure 1a), and a reactive power step injection function triggered by an increase in voltage harmonics distortion (Figure 1b). The frequency feedback function results in an injection of reactive power when there is a frequency change. Since all inverters are required to use the same feedback function and frequency is common within the potential island, this approach results in reactive power injection in the same direction when multiple PV inverters are connected in the circuit. The magnitude of the reactive injection is a function of the magnitude of the frequency change. The slopes of the first and second gains, as well as the threshold between the two and the maximum reactive power injection, need to balance the need to minimize non-detection zones and the need to avoid negative power quality impacts during normal conditions. For the inverters tested as part of this effort, the threshold frequency between first and second gain was set at +/- 0.01 Hz, and the maximum reactive power injection was set to +/-0.25 p.u. The step injection function serves as a complement to the frequency feedback function, and is intended to destabilize an island in the event that frequency does not change sufficiently for the frequency feedback function to detect the island. When the inverter detects a change in voltage harmonics above a threshold for longer than 3 cycles and frequency is not changing, reactive power is injected for 2 cycles. The resulting frequency change activates the frequency feedback function.

Table 1 - Comparison of US and Japan anti-islanding testing procedures

	US (IEEE 1547.1 / UL-1741)	**Japan (JETGR0003-4-1.0)**
Test conditions	• ΔP: 0 • ΔQ: 0, +/-1%, +/-2%, +/-3%, +/-4%, and +/-5%	• ΔP: 0, +/-5%,+/-10% • ΔQ: 0, +/-5%,+/-10%
Type of load	• RLC with quality factor (Q) = 1.0 • Q = R × Sqrt (C/L)	• Induction motor • RLC circuit to adjust net P,Q load • No Q specified (typically, Q<<1.0)
Number of tests for <u>single</u> inverter	• 2 tests at ΔQ=0 • 1 test at other ΔQ mismatch levels[1] • Repeat at 100%, 66%, and 33% • Total tests: **36**	• 2 tests for each (ΔP, ΔQ) combination • DG at 100% output • Total tests: **50**
Multiple inverter test	• No requirement for multiple inverter testing	• Multiple inverters with the same AI functionality (up to 10 maximum): test only at worst run-on-time condition (15 times)
Equipment Required	• Grid connection • PV simulator • Adjustable RLC load	• Grid connection • PV simulator • Adjustable RLC load and induction motor

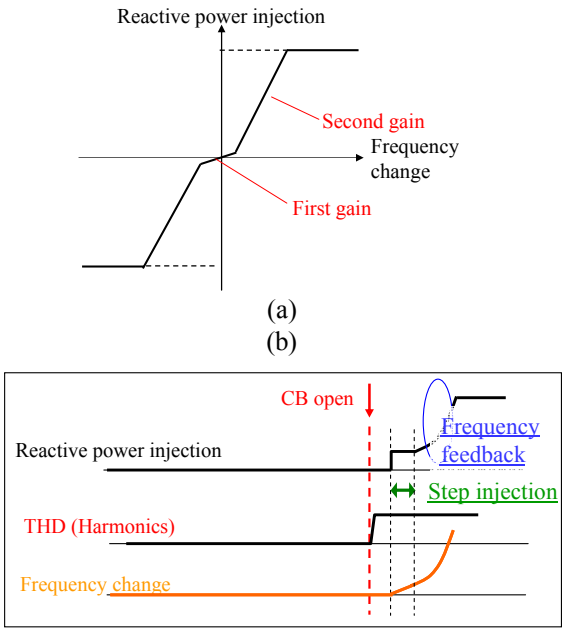


Fig. 1 – JSID anti-islanding algorithm consisting of frequency feedback function (a) and step injection function (b).

Based on limited testing conducted at Sandia, the JSID method is very effective at detecting the island condition well within 150ms without significant degradation in cases involving multiple inverters. Other attributes of the scheme, such as impacts on power quality and propensity to nuisance tripping, are also relevant to anti-islanding performance; however, these aspects have not been evaluated at Sandia.

Development of the JSID algorithm was driven in large measure by the relatively short disconnect time requirement in Japan (0.2 seconds). It is difficult to meet this requirement using other established anti-islanding methods, particularly in the case of multiple inverters. Figure 2 shows an example of increasing run-on-times observed with an inverter that does not have the JSID algorithm implemented based on tests conducted at Kandenko. Because the JSID algorithm results in synchronization of reactive power injection among multiple inverters, this type of trend is not expected.

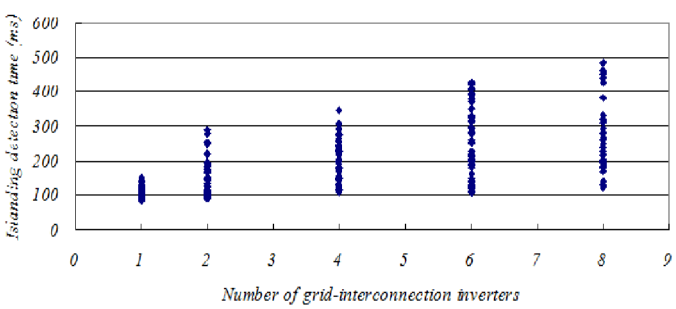


Fig. 2 - Increase in run-on-times with the number of inverters, based on tests conducted by Kandenko [17]

Generally speaking, the significance of this increase in run-on-time is considered less significant for the United States, where the maximum required disconnect time is 2 seconds.

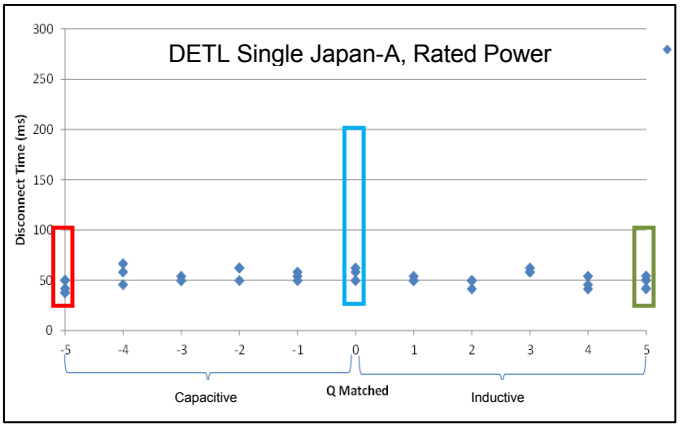
III. TEST RESULTS

The Sandia-Kandenko/JET collaboration involved testing of several types of inverters. A specific type of PV inverter, herein referred to as "Japan-A" inverter, was tested at Sandia's Distributed Energy Technologies Laboratory (DETL), as well as test in Japan conducted by Kandenko and Japan Electrical Safety & Environment Technological Laboratories (JET). The Japan-A inverter is a 4 kW 101/202V 50/60 Hz unit with the JSID anti-islanding algorithm implemented, as required in Japan. Tests conducted at Sandia generally following the UL Standard 1741 test procedure. Tests conducted in Japan generally followed the JETGR003-4-1.0 test procedure.

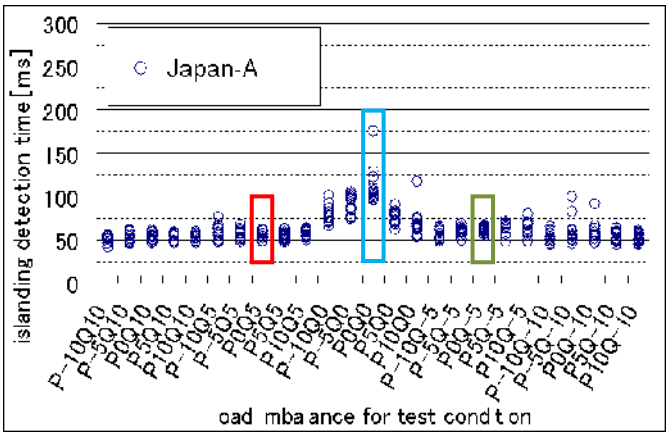
Section III.A discusses the results of testing of a single PV inverter. Section III.B discusses the test results for two inverters, and III.C has a detailed discussion of anti-islanding performance based on the tests conducted. The purpose is to compare the results of the tests conducted under different conditions, and to describe analysis methods.

A. Single Inverter case

Figure 3 shows the disconnect time for a single Japan-A inverter. The test results shown are at rated power output to allow for a more meaningful comparison. The red, blue and green rectangles indicate the test conditions that are approximately comparable in terms of active and reactive load balance. The vertical scale represented by the rectangles is the same for all tests. According to the test conducted at Sandia (Figure 3a), the disconnect time is 55ms on average, ranging between 40ms and 60ms, regardless of the reactive power imbalance up to +/-5%. In other words, for this inverter, the disconnect time obtained with the UL method is not sensitive to reactive power imbalance within the test range. The results obtained with the JET procedure (Figure 3b) show that, with a +/-5% reactive power imbalance, the disconnect time is 60ms on average, ranging between 50ms and 65ms. This compares very well to the results using the UL test procedure with +/-5% reactive imbalance, as indicated by the data in the red and green rectangles. However, for balanced reactive power conditions (blue rectangle), the average disconnect time is about twice as long (110ms) as the disconnect time obtained in the UL test. One of the tests shows a run-on time of 175ms. In addition, a pattern of longer disconnect times can be observed around balanced reactive power conditions in the JET test, but not in the UL test.



(a)



(b)

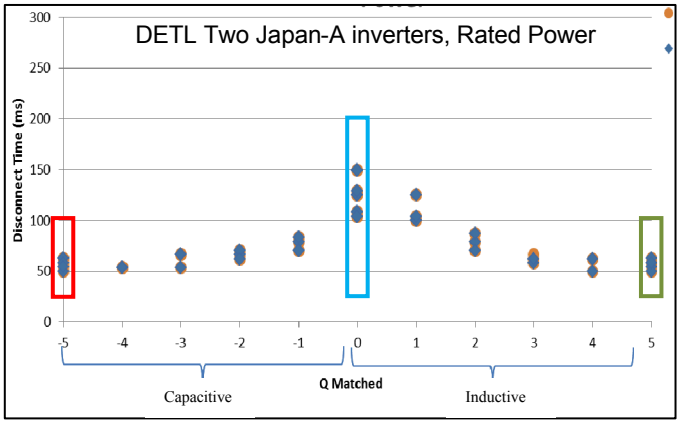
Fig. 3 – Disconnect times for one Japan-A inverter using the UL procedure (a) and the JET procedure (b).

The differences in run-on times in the balance reactive power conditions are due to the different test conditions. While the inverter tested at Sandia and JET is the same, the load composition in the island is very different. The JET test involves an induction motor, while the UL test only has passive RLC elements. Also, the UL test has a much higher quality factor (larger capacitance and reactance). Overall, the presence of the induction motor appears to make islanding detection more challenging, even though the quality factor of the circuit is lower. This observation applies only to this particular inverter and anti-islanding algorithm, and only to the single inverter case.

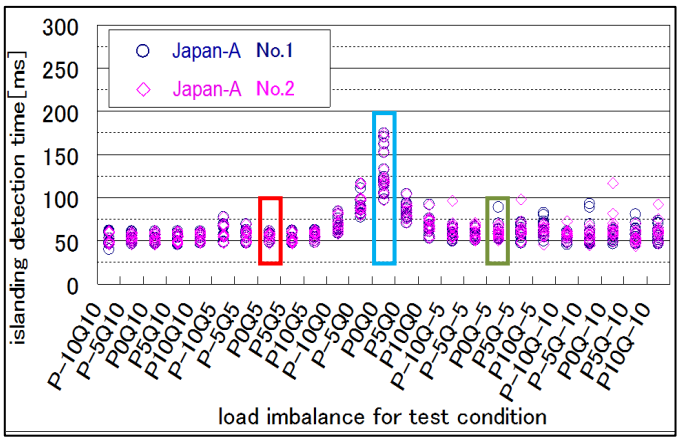
B. Multiple Inverter Case

Figure 4 shows the results of the anti-islanding tests with two Japan-A inverters. As in the single inverter case, test conditions are comparable in terms of load reactive power balance at the locations indicated by the rectangles. Both tests were conducted at balanced active power, and with the inverter at full load. Average disconnect times are very similar in both balanced and unbalanced reactive power conditions. On average, disconnect times are about 55ms for the unbalanced cases, and 125ms for the balanced case. The spread is about the same. In both tests, a pattern of longer disconnect times can be seen near balanced conditions. This pattern was not discernible in the single inverter case tested according to the UL test procedure.

It should be kept in mind that the UL test procedure does not cover multiple inverters, but the JET test does. To conduct the test at Sandia, a matched load with quality factor of 1.0 was connected to each inverter. This is a modified UL procedure that is consistent with the approach specified in the JET procedure.



(a)



(b)

Fig. 4 – Disconnect times for two Japan-A inverters using a modified UL test procedure (a) and the JET procedure (b).

C. Analysis of Anti-Islanding Performance

Figures 5 and 6 show, for the tests conducted at Sandia an in Japan, respectively, the instantaneous current and voltage waveforms (top), estimated voltage frequency (middle), and RMS active and reactive power (bottom) for the case of two

Japan-A inverters. Each of these tests corresponds to one data point in Figure 4 above. In all the plots, island was formed at t=0 seconds. The disconnect time corresponds to the instant in which the current goes to zero. Frequency and power traces are estimated from measured voltage and current waveforms. Sampling was 60k samples per second for both tests.

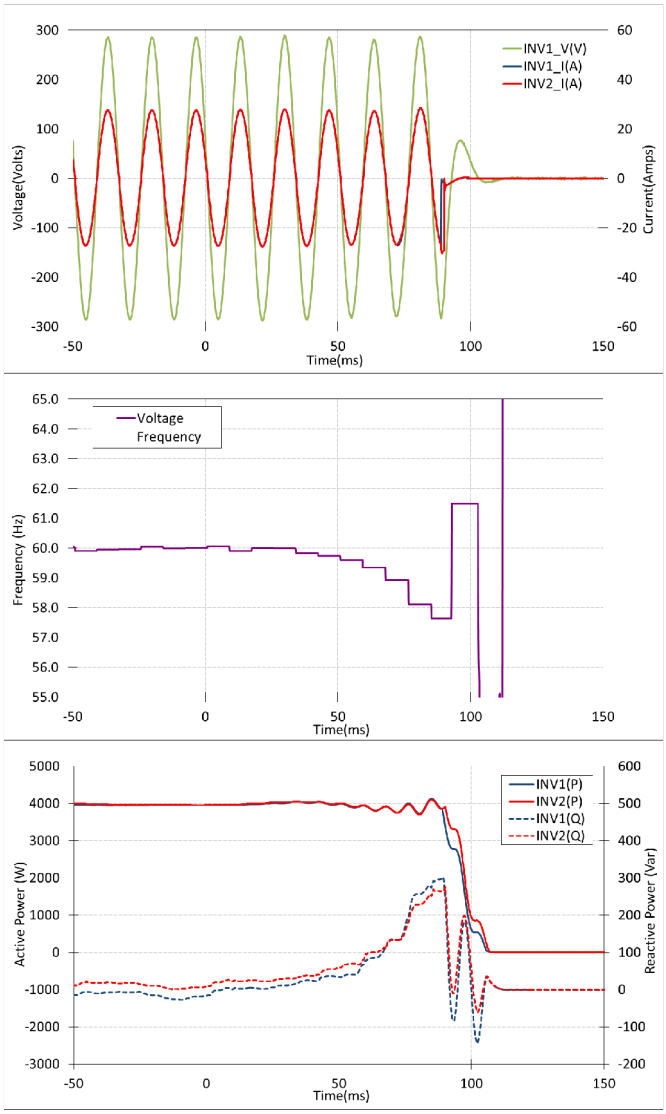


Fig. 5 – Analysis of anti-islanding performance for two Japan-A inverters, using a modified UL procedure.

Estimates of frequency and phase angle were obtained using a zero-crossing method, which can introduce a time delay in the frequency and phase estimation. Active and reactive power estimates are based on cycle-by-cycle RMS calculations on filtered voltage and current waveforms. In this case, voltage and frequency were pre-processed through a fast Fourier transform filter to extract the magnitude and phase. The cycle-by-cycle RMS computation involves integration over a cycle, which has the effect of averaging the power estimates. This effect is clearly seen in Figures 5 and 6. Active and reactive power go to zero approximately one cycle (16.6ms) after current goes to zero. Since phase estimation after current goes to zero is not reliable, estimated reactive power after tripping is not reliable.

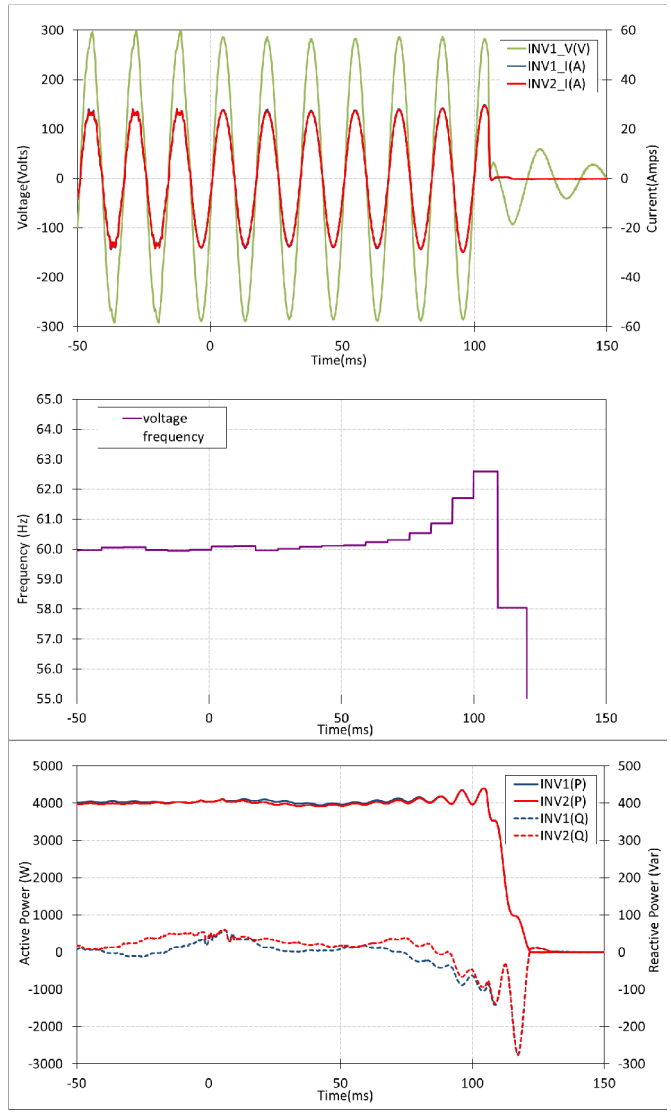


Fig. 6 - Results of anti-islanding testing of two Japan-A inverters at JET

For the test conducted at Sandia, the disconnect time is approximately 90ms. Following the formation of the island at t=0, it can be seen that reactive power output for each of the inverters changed from zero to 300 VArs, approximately. This resulted in a decrease in frequency from 60 Hz to a low of 58.5 Hz, at which point the inverter tripped. The rate of change if reactive power and frequency increases, and this behavior is consistent with the JSID algorithm described in

Section III. Both inverters tripped at the same time. The test conducted in Japan has similar results. The disconnect time was slightly longer (approximately 120ms). Inverter tripping occurred when frequency reached approximately 62.5 Hz. Reactive power injection from the inverters changed from zero to about 100 VArs. Frequency and reactive power changed in the opposite direction compared to the test conducted at Sandia. The direction of frequency change is a function of the condition at the moment the island is formed. The key result is that both inverters injected reactive power in the same direction, causing a monotonic change in frequency. The observed performance is consistent with the description of the anti-islanding algorithm implemented in the inverter.

IV. Conclusions

This paper compared anti-islanding requirements and test procedures in Japan and the United States. Testing was conducted on the same type of PV inverters at Sandia and in Japan, using procedures that are. The inverter tested implements the JSID algorithm, which features the ability to synchronize reactive power injection. This algorithm is required in to be implemented in PV installed in Japan. Results of single and two inverter tests were compared, and were found to be substantially equivalent, even though the test conditions are different. The test results clearly demonstrate the expected performance of the anti-islanding algorithm.

Two fundamental observations van be made about these test results. First, because the anti-islanding algorithm is the same in both inverters, the frequency feedback function causes reactive power to change in the same direction. For this reason, frequency changes monotonically until it reaches a trip threshold. Second, the anti-islanding test results were confirmed to be substantially consistent, even though the test conditions and test procedures are not the same. These observations apply only to the type of inverter tested.

V. Acnowledgement

This test research was conducted as part of a broader collaboration between Sandia and Japan's New Energy and Industrial Technology Development Organization (NEDO). Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

VI. References

[1] W. Bower and M. Ropp, Evaluation of Islanding Detection Methods for Utility-Interactive Inverters in Photovoltaic Systems, SAND2002-3591. Sandia National Laboratories, Albuquerque, NM, November 2002.

[2] M.E. Ropp, M. Begovic, A. Rohatgi, G. A. Kern, R. Bonn, S. Gonzalez, "Determining the Relative Effectiveness of Islanding Prevention Techniques Using Phase Criteria and Nondetection Zones", IEEE Transactions on Energy Conversion 15(3) September 2000, p. 290-296.

[3] R. Bhandari, M. Ropp, and S. Gonzalez, Investigation of two anti-islanding methods in the multi-inverter case, Proceedings of the IEEE Power Engineering Society 2008 Summer Meeting, July 2008, 6 pp.

[4] Y. Miyamoto, N. Fukuoka, H. Sugihara, T. Miyata, and S. Osaka, Development of Examination Method When Plural Islanding Detection Systems Are Interconnected, Proceedings of the 34th Photovoltaic Specialists Conference, 2009.

[5] E. Estébanez, V. Moreno, A. Pigazo, and M. Liserre, An Overview of Anti-Islanding Detection Algorithms in Photovoltaic Systems in Case of Multiple Current-Controlled Inverters, 35th Annual IEEE Industrial Electronics Conference, 2009, pp. 4555-4560.

[6] M. Xue, F. Liu, Y. Kang, and Y. Zhang, Investigation of Active Islanding Detection Methods in Multiple Grid-Connected Converters, 6th IEEE International Power Electronics and Motion Control Conference, 2009, pp. 2151-2154.

[7] M. Mills-Price, M. Ropp, D. Joshi, M. Scharf, S. Hummel, K. G. Ravikumar, and G. Zweigle, Solar Generation Control with Time-Synchronized Phasors, IEEE Western Protective Relaying Conference (IEEE WPRC), October 2010, 8 pp.

[8] M. Ropp, R. Bonn, S. Gonzalez, and C. Whitaker, "Sandia Smart Anti-Islanding Project Task II: Investigation of the Impact of Single-phase Induction Machines in Islanded Loads", Sandia National Laboratories rpt. SAND2002-1320, May 2002.

[9] Z. Ye, R. Walling, L. Garces, R. Zhou, L. Li, and T. Wang Study and Development of Anti-Islanding Control for Grid-Connected Inverters, NREL/SR-560-36243, May, 2004.

[10] X. Wang, J. Zheng, S. Zhu, W. Xu, Investigation of the impact of positive feedback anti-islanding controls on dynamics of motor load, Developments in Power System Protection, 2010.

[11] IEA International Energy Agency, Evaluation of Islanding Detection Methods for Photovoltaic Utility Interactive Power systems, in Task V Report IEA PVPS T509: 20022002.

[12] IEEE 1547 Std. 1547-2008, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, Institute of Electrical and Electronics Engineers, Inc., New York, NY.

[13] IEEE 1547 Std. 1547.1-2011, Conformance Test Procedures for Equipment Interconnecting DR with EPS, Institute of Electrical and Electronics Engineers, Inc., New York, NY.

[14] Testing Procedure of Islanding Prevention Measures for Utility Interactive Photovoltaic Inverters, IEC 62116, 2008.

[15] UL 1741, Std 1741, Static Inverter and Charge Controllers for Use in Photovoltaic Systems, Underwriters Laboratories Inc, North Brook, IL.

[16] Electrical Safety & Environment Technology Laboratories, Individual Test Method of Grid-connected Protective Equipment etc. for Multi-unit Grid-connected PV Power Generating Systems JET GR 0003-4-1.0 (2011)

[17] Y. Miyamoto, Technology for high penetration residential PV systems on a distribution line in Japan, Presentation at Workshop on PV Integration in Distribution Networks, Berlin, Germany, December 3, 2012.