SAND2011-4609C

ReSpace/MAPLD 2011 Paper Submission
Extended Abstract

Sandia Rad-Hard, Fast-Turn Structured ASIC – The ViArray

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A structured ASIC enables rapid turn-around times, lowers non-recurring engineering (NRE) costs, and reduces development risk by using pre-qualified base array platforms. Beginning in 2004, Sandia has developed the ViArray family of structured ASIC base arrays for its internal 350-nm radiation-hardened silicon-on-insulator (SOI) foundry. The ViArray employs a regular fabric-like circuit, similar to an FPGA (Field Programmable Gate Array), that uses a one-time metal-via mask to configure user functions into the base array. With the metal-via configuration approach, the ViArrays are competitive to custom ASICs in speed, power, and circuit density. The architecture is based on ViASIC® ViaMask™ technology. Figure 1 shows the basic architecture of the ViArray.

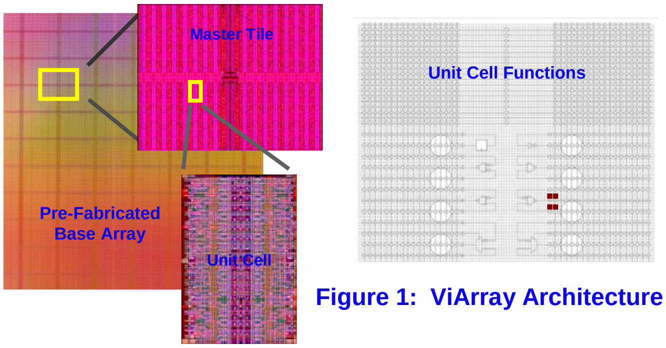
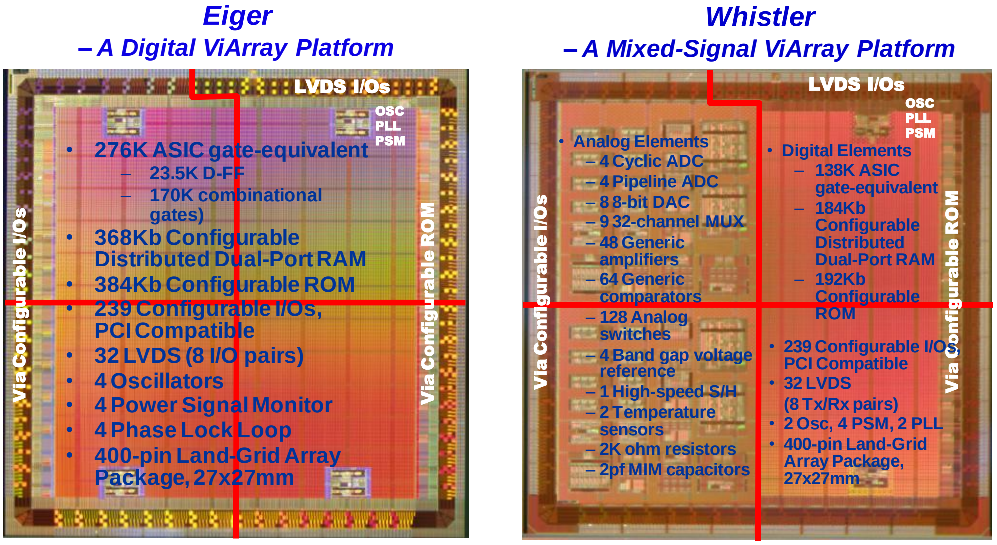


Figure 1: ViArray Architecture

Sandia's ViArray is developed specifically for high-reliability systems that operate in radiation environments. The ViArray family includes various base arrays. Figure 2 shows two examples of ViArray platforms.


Eiger
– A Digital ViArray Platform

Whistler
– A Mixed-Signal ViArray Platform

Figure 2

Eiger is optimized for embedded digital applications and Whistler is designed for mixed-signal instrumentation or monitor applications.

All base arrays have power handling features with fine-grain power gating to disconnect unused transistors and power supply partitioning to enable power sequencing and redundancy. The power handling features lower power consumption, improve reliability, and minimize photo current. The ViArray base arrays meet the same stringent power and radiation levels that are required for Sandia's standard cell ASICs. Figure 3 shows the granularity of ViArray's power partitioning.

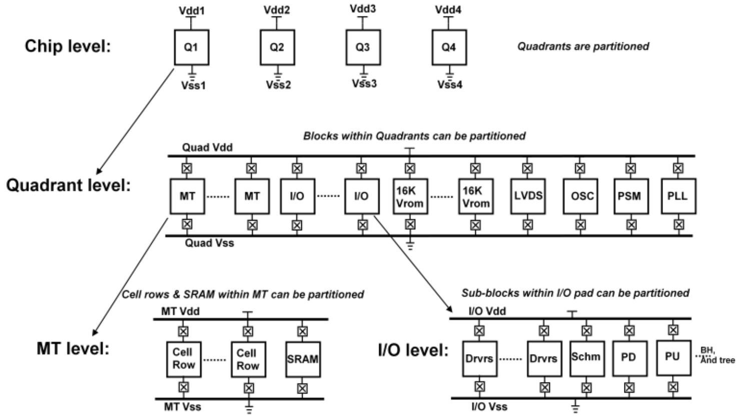


Figure 3: ViArray Power Partitioning Granularity

The ViArray family is a generic implementation platform. Sandia's foundry pre-fabricates the base arrays up to the metal-2 level and stockpiles them. It takes only 3 weeks from tape-out to completion of foundry fabrication for a custom design. This is 4-5x improvement compared to traditional custom ASIC fabrication flow. Likewise, ASIC development costs have decreased by 2-5x in switching from custom ASICs to ViArray structured ASICs. The combination of fast-turn design iteration and lower development cost enables ViArray users to inexpensively insert prototype ASICs into their systems much earlier than in the past, when they have historically waited until late in the system development cycle to produce a more costly standard-cell ASIC. Some ViArray users have eliminated using FPGAs during their early system development phase. Instead, they iterate their ASIC designs, which are form-fit-function equal to the final system, many times during development. This eliminates the performance, cost and schedule risks of final FPGA to ASIC conversion. Figure 4 depicts the front-end-of-line ViArray base array fabrication vs. back-end-of-line user design implementation.

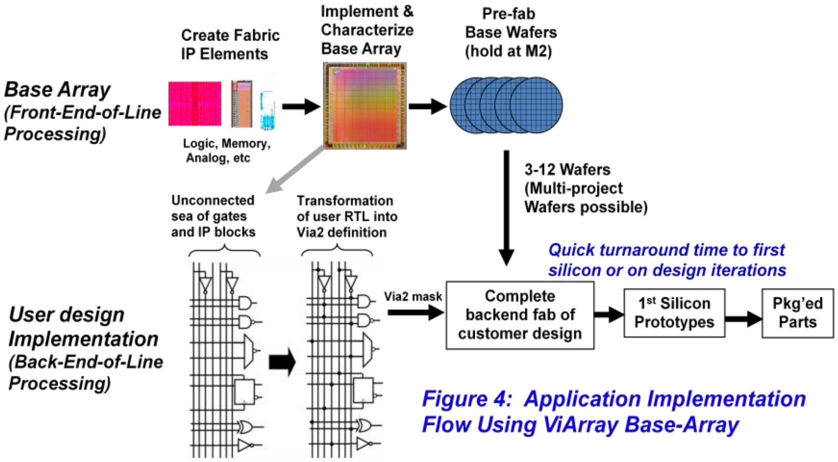
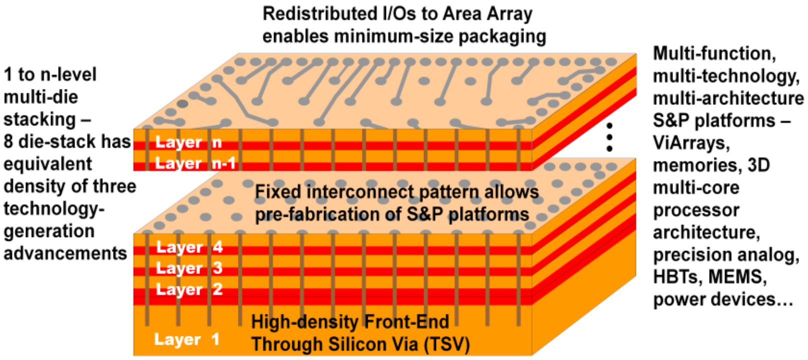


Figure 4: Application Implementation Flow Using ViArray Base-Array

A common validation vehicle (CVV) design is used to validate, characterize, and qualify the ViArray base array designs. The CVV is developed to represent a typical user circuit. It is scalable to fit different base array resources, and has dedicated functions to exercise all ViArray features in the base array. ViArray users may leverage the CVV test, characterization and qualification results to further reduce their ASIC development costs.

Currently, the Eiger digital ViArray and the Whistler mixed-signal ViArray platforms are the most mature of Sandia's ViArray products. Additional platforms are currently in development and test. While each base array is built from a common library of silicon blocks, they are customized in their logic resources, mixed-signal capability, I/O capacity, and packaging types for different classes of applications. In addition, Sandia has a plan to initiate a 3-D chip stacking and chip-scale packaging development in the near future. Figure 5 shows the concept of this effort, which is named the Stack & Pack program. The Stack & Pack will further enhance ViArray's performance, increase density, and minimize package size.


Redistributed I/Os to Area Array enables minimum-size packaging

1 to n-level multi-die stacking – 8 die-stack has equivalent density of three technology-generation advancements

Multi-function, multi-technology, multi-architecture S&P platforms – ViArrays, memories, 3D multi-core processor architecture, precision analog, HBTs, MEMS, power devices…

Fixed interconnect pattern allows pre-fabrication of S&P platforms

High-density Front-End Through Silicon Via (TSV)

Figure 5: Stack and Pack (S&P) for Sandia Silicon and Micro Fabs