Joint ICTP-IAEA workshop on Physics of Radiation Effects and its Simulation for non-Metallic Condensed Matter, August 13-24, 2012, Trieste, Italy

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Radiation Effects in Microelectronic Devices

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Overview

- Radiation environments
- Fundamental damage mechanism
- Total dose effects in MOS devices
- Displacement damage in detectors
- Single Event Effects and Failure Analysis Using a Nuclear Microprobe

Recommended reading list

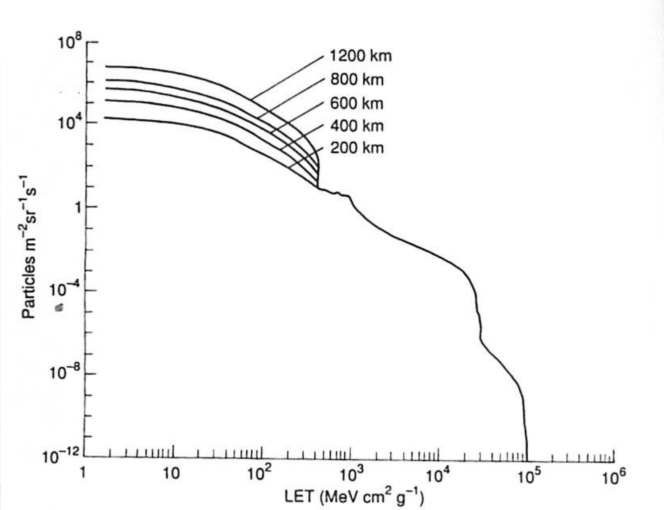
- Messenger, G.C. and M.S. Ash, *The Effects of Radiation on Electronic Systems*. 2nd edition, 1992, New York: Van Nostrand Reinhold.
- Holmes-Siedle, A. and L. Adams, *Handbook of Radiation Effects,* 2002, New York: Oxford University Press Inc.
- Simoen, E. and C. Claeys, *Radiation Effects in Advanced Semiconductor Materials and Devices*. Materials Science, ed. R. Hull, S.E. Osgood, and J. Parisi, 2002, Berlin Heidelberg: Springer-Verlag.
- Ma, T.P. and P.V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits,* 1989, New York: John Wiley & Sons, Inc.
- IEEE TNS December (NSREC) and August (RADECS) issues
- IEEE NSREC Short Course Notebooks
- S.M. Sze, K.K. Ng, *Physics of semiconductor devices, Wiley-Interscience,* Hoboken, NJ, 2007

Radiation environments

- Space
- High-energy physics experiments
- Nuclear reactors
- Natural environments
- Processing-induced radiation

Space (TID and SEE)

- Protons (several hundreds of MeV) and electrons (few MeV) trapped in the Van Allen belt
- Heavy ions trapped in the magnetosphere
- Galactic cosmic rays, protons and heavy ions, up 100s of GeV
- Proton and heavy ions from solar flares, > 100 MeV



Holmes-Siedle, A. and L. Adams, *Handbook of Radiation Effects,* 2002, New York: Oxford University Press Inc.

High-energy physics experiments

- Protons and electrons with 100s of GeV energy
- The primary hadron-hadron interactions produce high flux of charged particles, gamma rays, and neutrons
- Up to 1.6×10^{14} 1 MeV neutron/cm^2 equivalent integrated fluence
- Displacement damage, detector degradation

Fusion and fission reactors

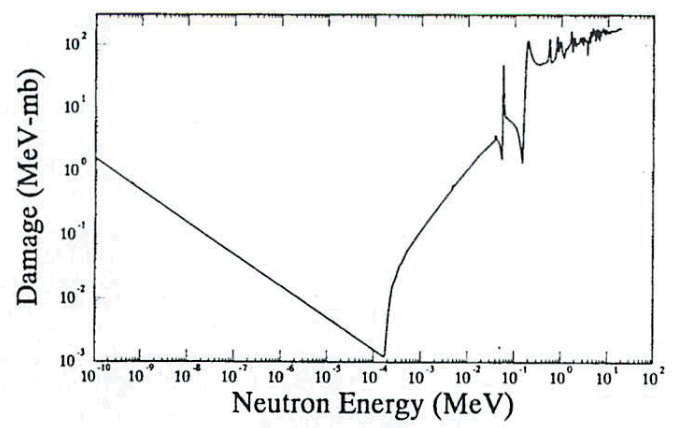
- Reactor core, environment of the reactor, accidents
- Neutrons, gamma rays, and hydrogen isotopes (fusion)
- Significantly higher fluences than in space environments
- Displacement damage and TID

Natural environment and processing

- Alpha radiation from radioactive impurities (U and Th)
- Alpha particles from $^{10}B(n,\alpha)^{7}Li$ reaction in BPSG
- Terrestrial neutrons
- Ion implantation, lithography, sputtering, ion milling, plasma etching, etc.

Definitions

- Ionization: 1 rad =100 erg/g (1 Gray=1 J/kg=100 rad)
- Displacement: dpa – displacement per atom
- LET – linear energy transfer (MeV/(mg/cm^2))
- NIEL – non-ionizing energy loss (MeV/(mg/cm^2))
- SRH – Shockley-Read-Hall recombination
- TID – Total ionizing dode
- 1 MeV neutron equivalent fluence – displacement damage caused by 1 MeV neutrons – both neutron and ion fluence can

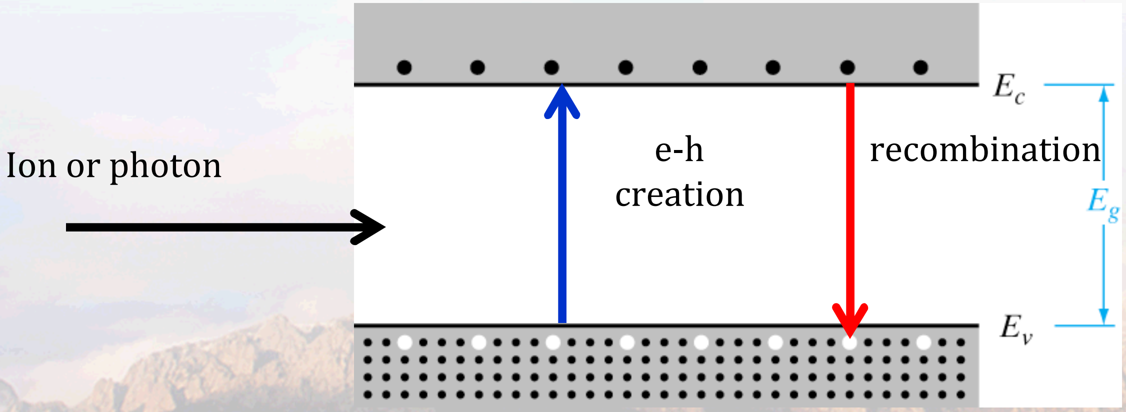


for Si = 95 MeV·mbarn

ASTM, *Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an Equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics.* ASTM Standards, 2004. **E722-04e2**: p. 1-17.

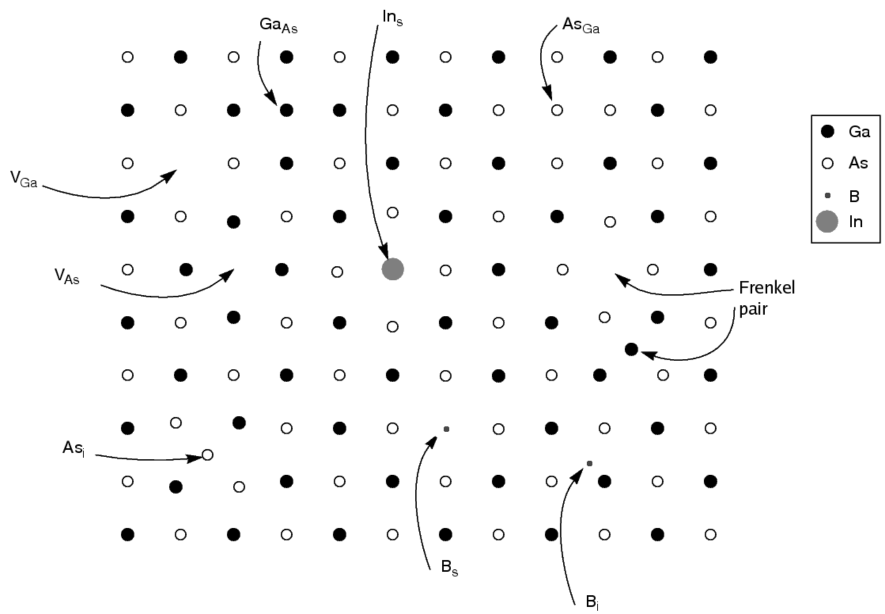
Fundamental damage mechanism

- Ionization (removing or exciting electrons of atoms, creating electron-hole pairs)
  - Energy necessary to create an e-h pair $f \cdot E_g$, 3.62 eV for Si, 17-18 eV for SiO_2
  - Photocurrent (SEE)
  - Trapped charge (bulk or interface) (TID)

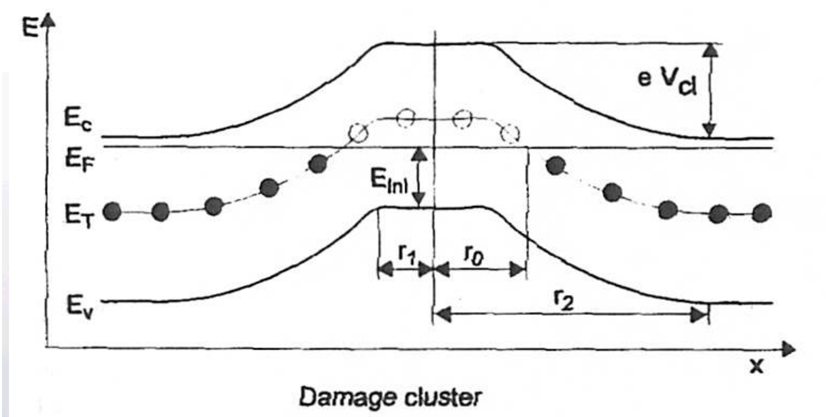


Displacement damage

- Recoils with energy larger than E_d leave the lattice site and can create permanent defects
- Vacancies, interstitials, anti-sites, clusters
- Carrier lifetime is decreased due to recombination in defects (SRH)
- Clusters distort the energy band locally

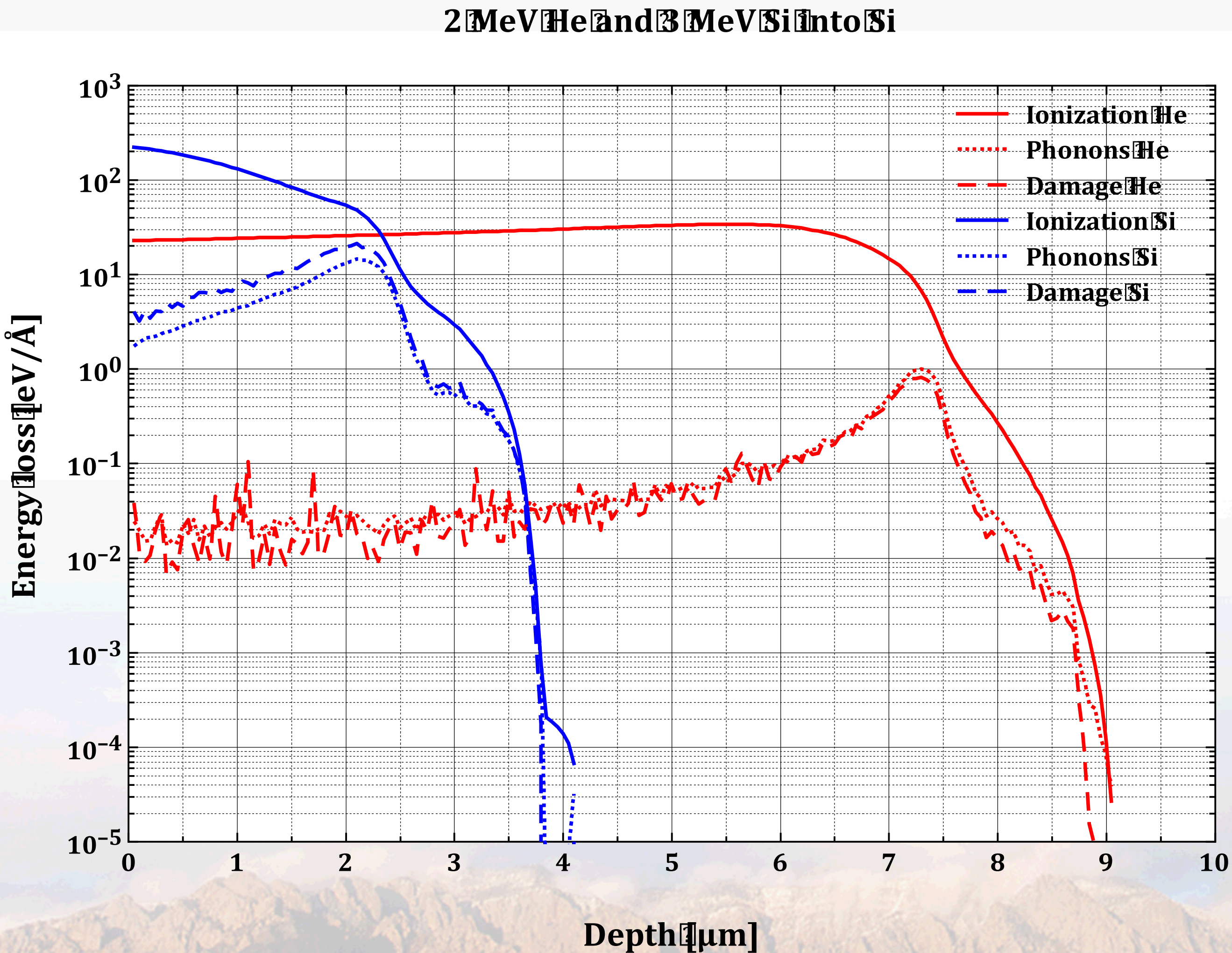


Wikipedia



Simoen, E. and C. Claeys, *Radiation Effects in Advanced Semiconductor Materials and Devices*. Materials 2002, Berlin Heidelberg: Springer-Verlag.

LET and NIEL



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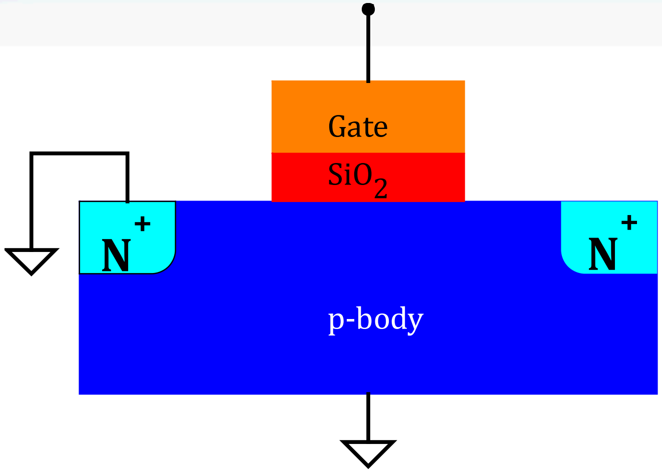
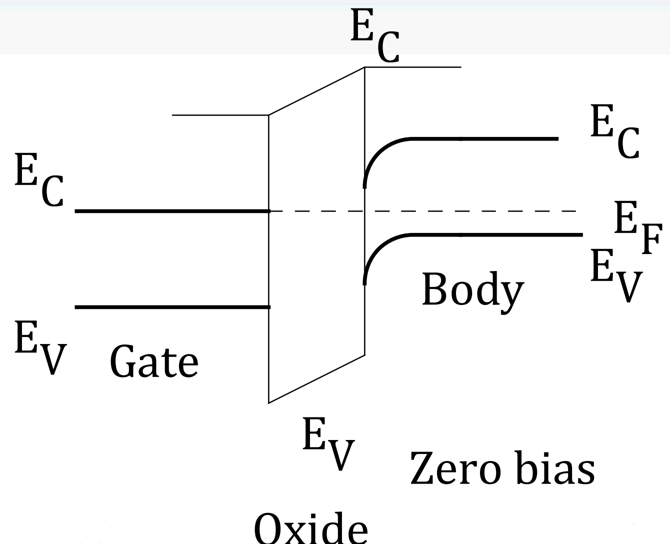
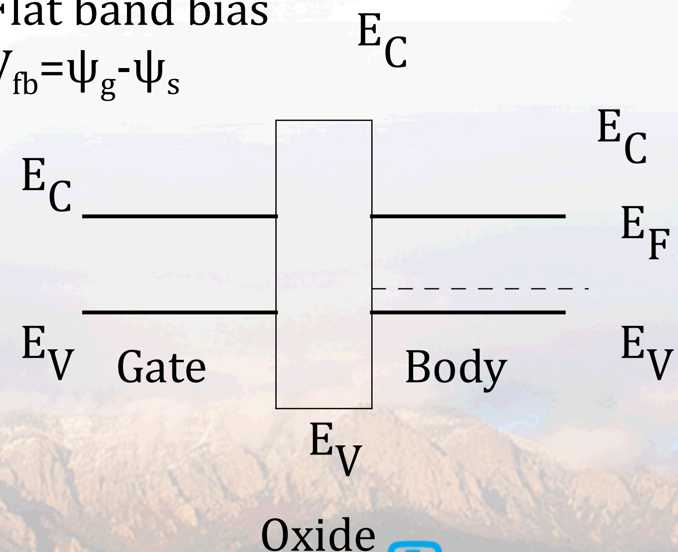
MOS basics



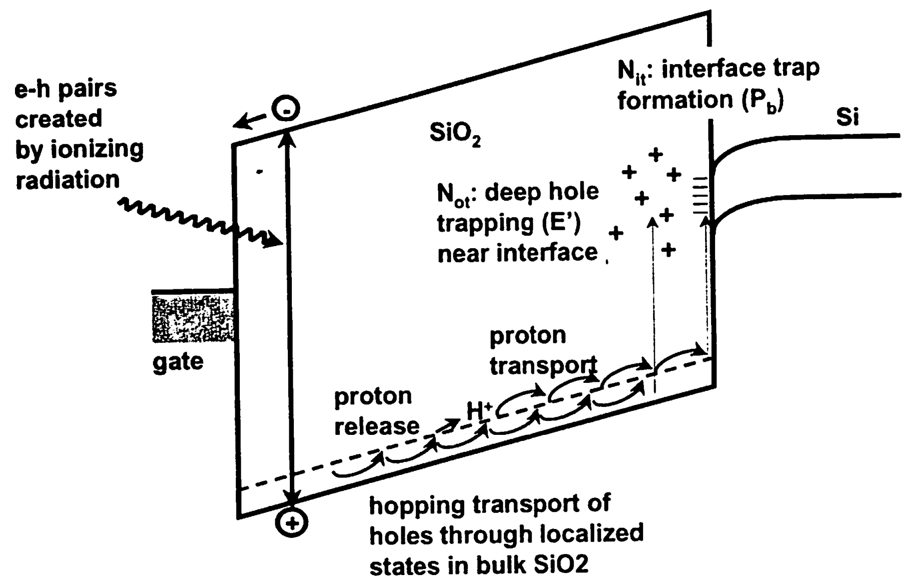


- Accumulation: Negative gate voltage, holes are attracted to the interface
- Depletion: Positive gate voltage, holes are repelled from the interface
- Inversion: More positive gate voltage, electrons are accumulated at the surface, p-type inverted to n-type
- Threshold: electron density is equal to the donor concentration

Flat band bias
$V_{fb}=\psi_g-\psi_s$



The basics of TID in MOS devices

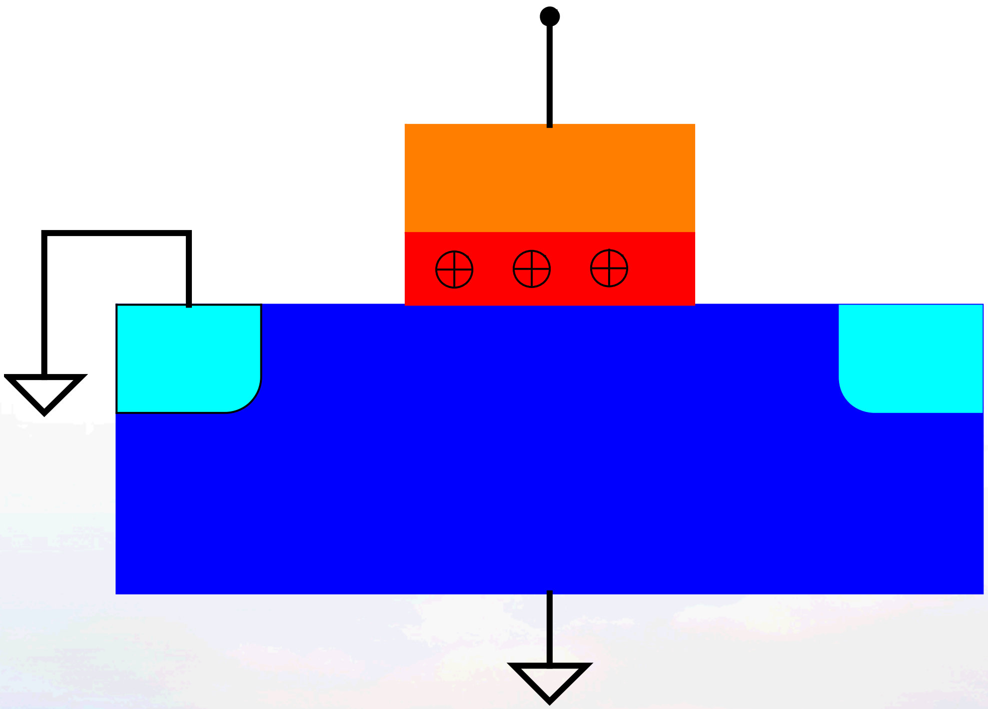


Schwank, J.R., *Total dose effects in MOS devices*, in 2002 IEEE NSREC Short course note book, 2002

- e-h pairs are created by the ionizing radiation
- Some of the e-h pairs immediately recombine
- Electrons are swept out toward the gate in ps
- Holes will move toward the Si/SiO_2 interface by hopping through localized states (polarons)
- Some holes are trapped and form positive oxide trapped charge
- Hydrogen released during "hopping" that can drift to the interface and form interface traps
- Interface traps are predominantly charged positive for p channel and negative for n channel transistors

Excellent recent review: Oldham, T.R. and F.B. McLean, *Total ionizing dose effects in MOS oxides and devices.* IEEE Transactions on Nuclear Science, 2003. **50**(3): p. 483-499.

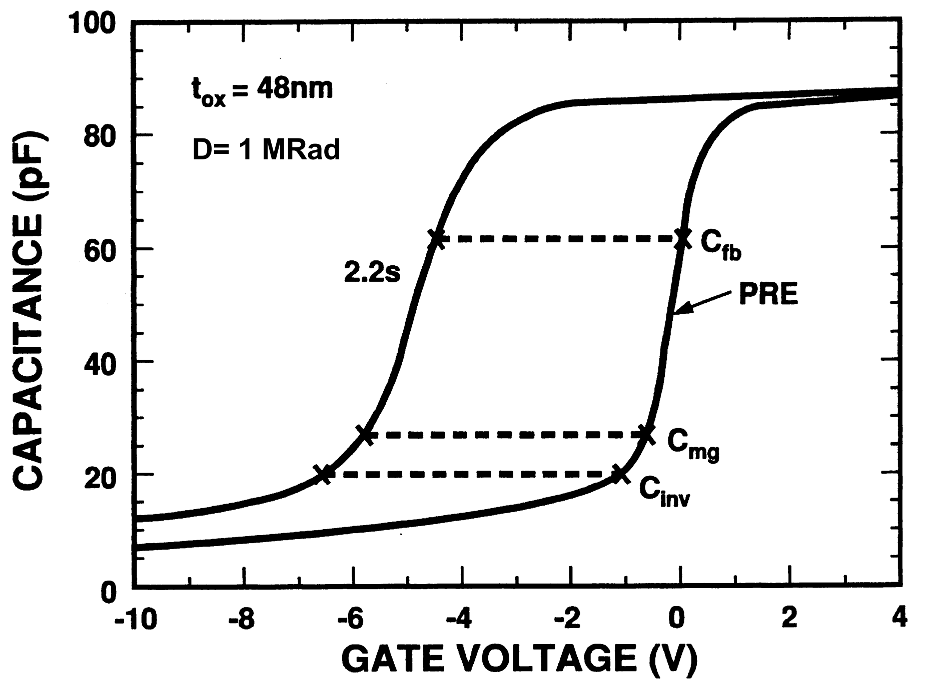
How can cause the trapped and interface charge problems?



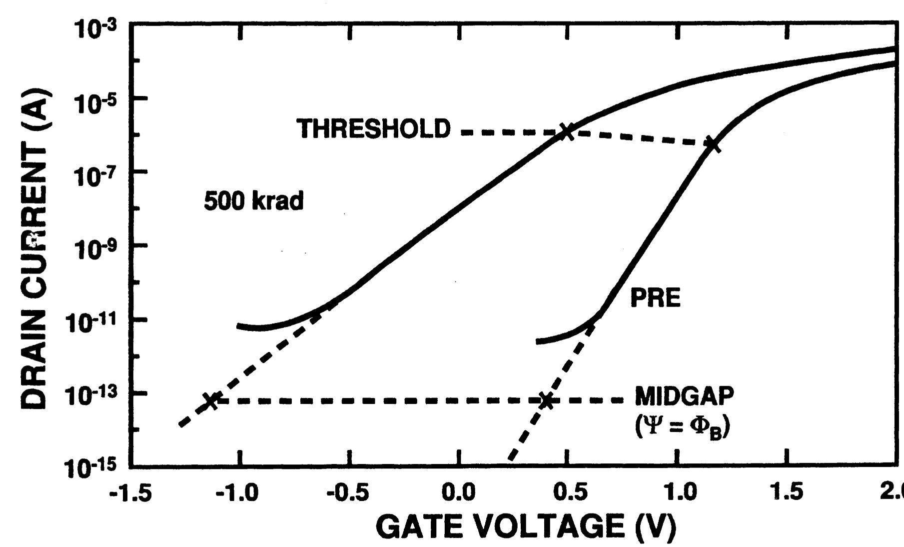
The extra charge in the oxide will add extra voltage to the gate voltage and the transistor will be switched on at lower voltage or even at zero gate bias. Also, it increases the leakage current form the PS.

Problems occurs not only in MOS devices but also with SOI and all other devices that have field oxide.

How to measure the oxide and interface trapped charge



Midgap I-V technique



C_{fb} at 0 V, C_{mg} at Φ_B, C_{inv} at $2\Phi_B$ $\quad \Phi_B = \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_{dopant}}{n_i}\right)$

$$N_{it} = \frac{C_{ox}}{q} \cdot \left(\Delta V_{th} - \Delta V_{ot}\right)$$

$$N_{ot} = \frac{\Delta V_{ot} \cdot C_{mg}}{q} \qquad \Delta N_{it} = \frac{C_{ox} \cdot \Delta V_{it}}{q}$$

Schwank, J.R., *Total dose effects in MOS devices*, in 2002 IEEE NSREC Short course note book, 2002

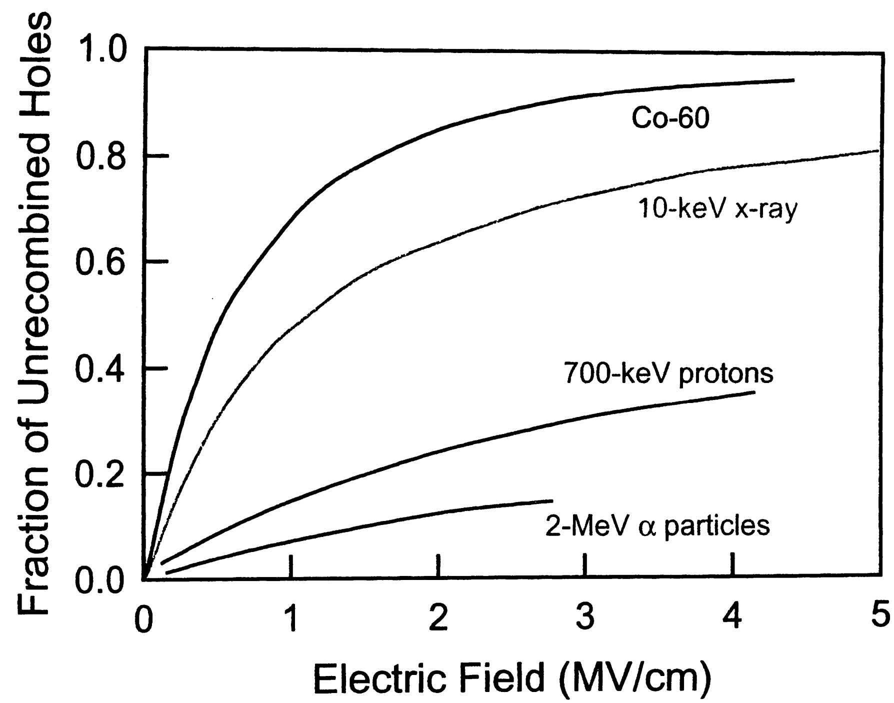
Charge yield

e-h pairs can recombine immediately and decrease the number of hole. This recombination depends on

- Electric field
- e-h plasma density (particle type)

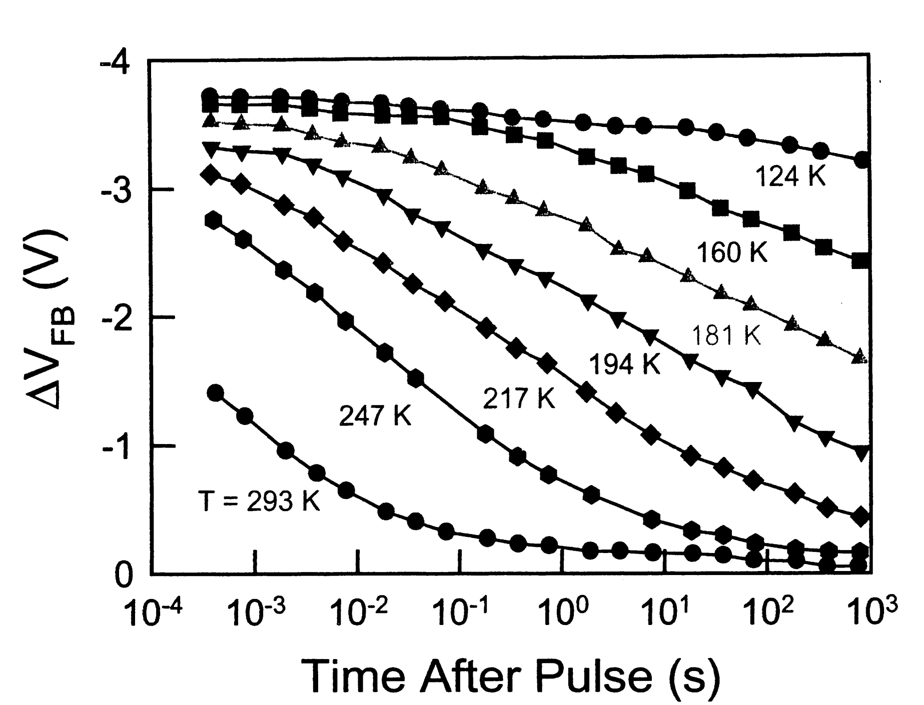
$$N_h = f\left(E_{ox}\right)\cdot g_0 \cdot D \cdot t_{ox}$$

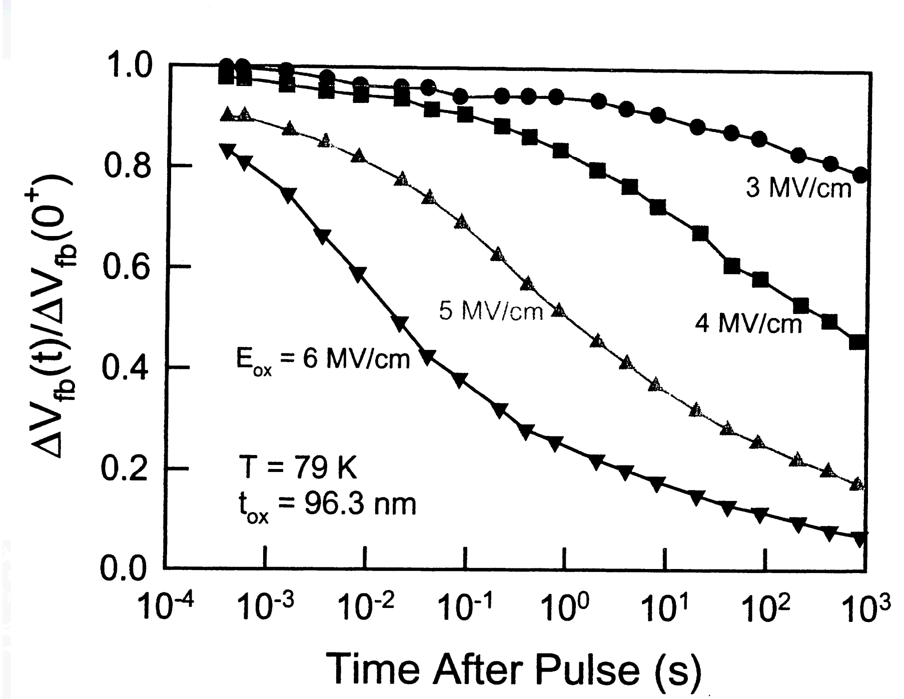
$$\Delta V_{ot} \sim f\left(E_{ox}\right)\cdot g_0 \cdot D \cdot t_{ox}^2$$



F.B. McLean, T.R. Oldham, Basic Mechanics of Radiation Effect in Electronic Materials and Devices, in, Harry Diamond Laboratories, 1987.
M.R. Shaneyfelt, D.M. Fleetwood, J.R. Schwank, K.L. Hughes, CHARGE YIELD FOR CO-60 AND 10-KEV X-RAY IRRADIATIONS OF MOS DEVICES, IEEE Transactions on Nuclear Science, 38 (1991) 1187-1194.

Hole transport





H.E. Boesch, J.M. McGarrity, F.B. McLean, TEMPERATURE-DEPENDENT AND FIELD-DEPENDENT CHARGE RELAXATION IN SIO2 GATE INSULATORS, IEEE Transactions on Nuclear Science, 25 (1978) 1012-1016.

H.E. Boesch, F.B. McLean, J.M. McGarrity, P.S. Winokur, ENHANCED FLATBAND VOLTAGE RECOVERY IN HARDENED THIN MOS CAPACITORS, IEEE Transactions on Nuclear Science, 25 (1978) 1239-1245

- Hole causes distortion of the local potential that increases trap depth
- Polaron – hole and its strain field, increased mass, decreased mobility
- Polaron hopping

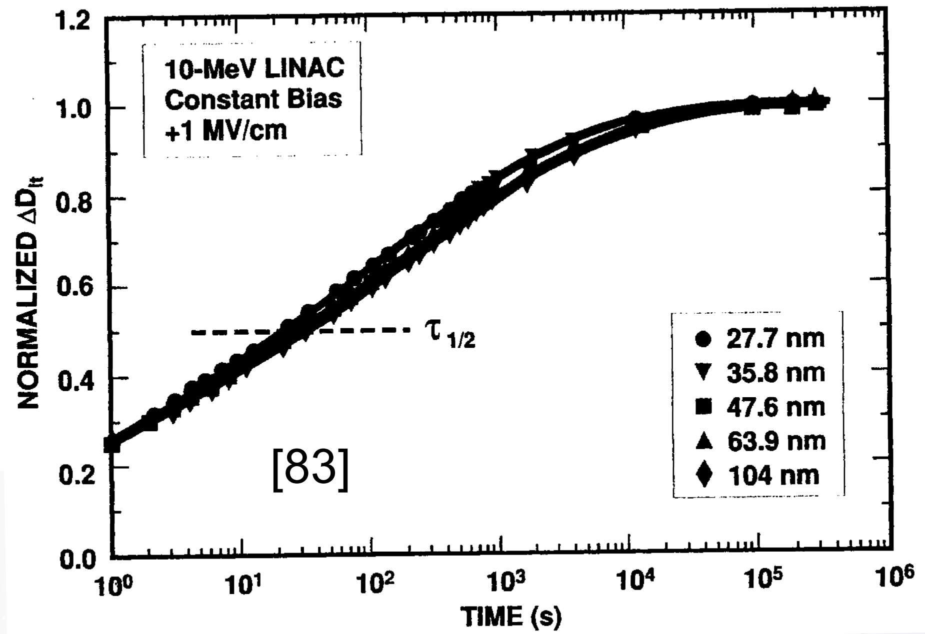
$$\tau \sim \tau(0)\cdot e^{-\frac{c\cdot E}{k\cdot T}}$$

Interface trap build-up

- During hopping the holes break H-Si bonds and H (Svensson) or H^+ (Winokur & McLean) is released
- Neutral H diffuses, H ion drifts toward the interface
- H breaks H-Si bond at the interface and creates dangling bond
- The bias dependence supports Winokur & McLean theory

$$H^+ + e \rightarrow H$$

$$H + H - Si \equiv Si \rightarrow H_2 + \bullet Si^- \equiv Si$$



M.R. Shaneyfelt, J.R. Schwank, D.M. Fleetwood, P.S. Winokur, K.L. Hughes, G.L. Hash, M.P. Connors, INTERFACE-TRAP BUILDUP RATES IN WET AND DRY OXIDES, IEEE Transactions on Nuclear Science, 39 (1992) 2244-2251.

$$H^+ + H - Si \equiv Si \rightarrow H_2 + \bullet Si^+ \equiv Si$$

The positively charged trap will turn rapidly into negatively charged by capturing electrons from the Si inversion layer

Oxide charge build up

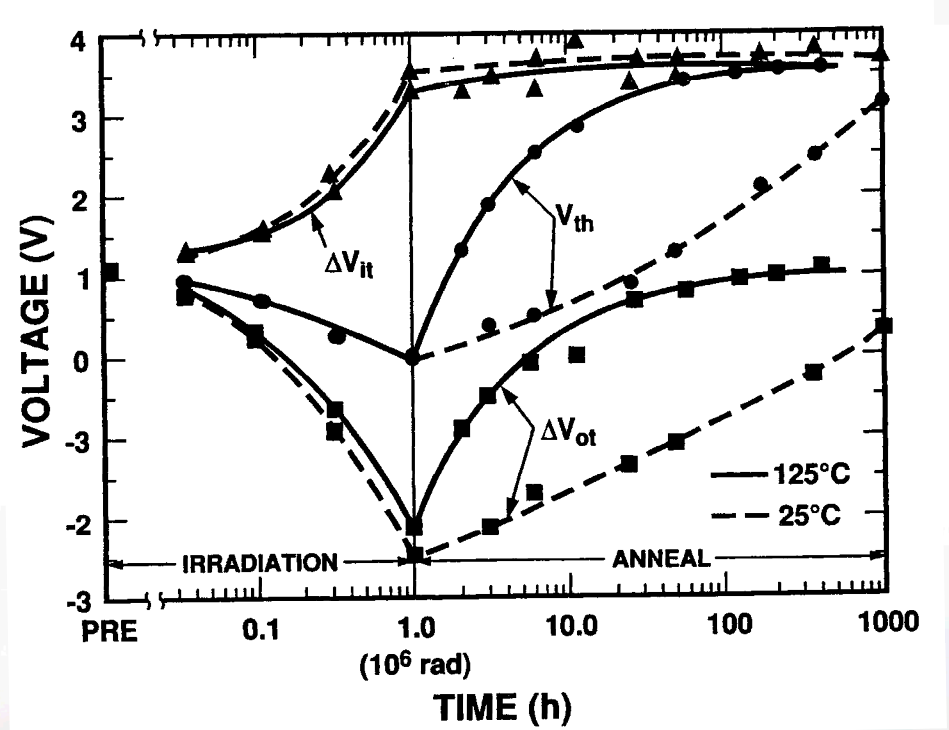
- Holes transport through the oxide by hopping towards the Si/SiO_2 interface
- Oxygen vacancies due to oxygen diffusing into Si
- Vacancies can trap holes, cross section is device independent, from few % for hardened oxide to 50-100% for soft oxides
- This positive trapped charge always causes negative threshold shift for both n and p channel devices.
- n-channel devices can be turned on easier, p-channel devices can be turned on harder

Device properties

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}$$

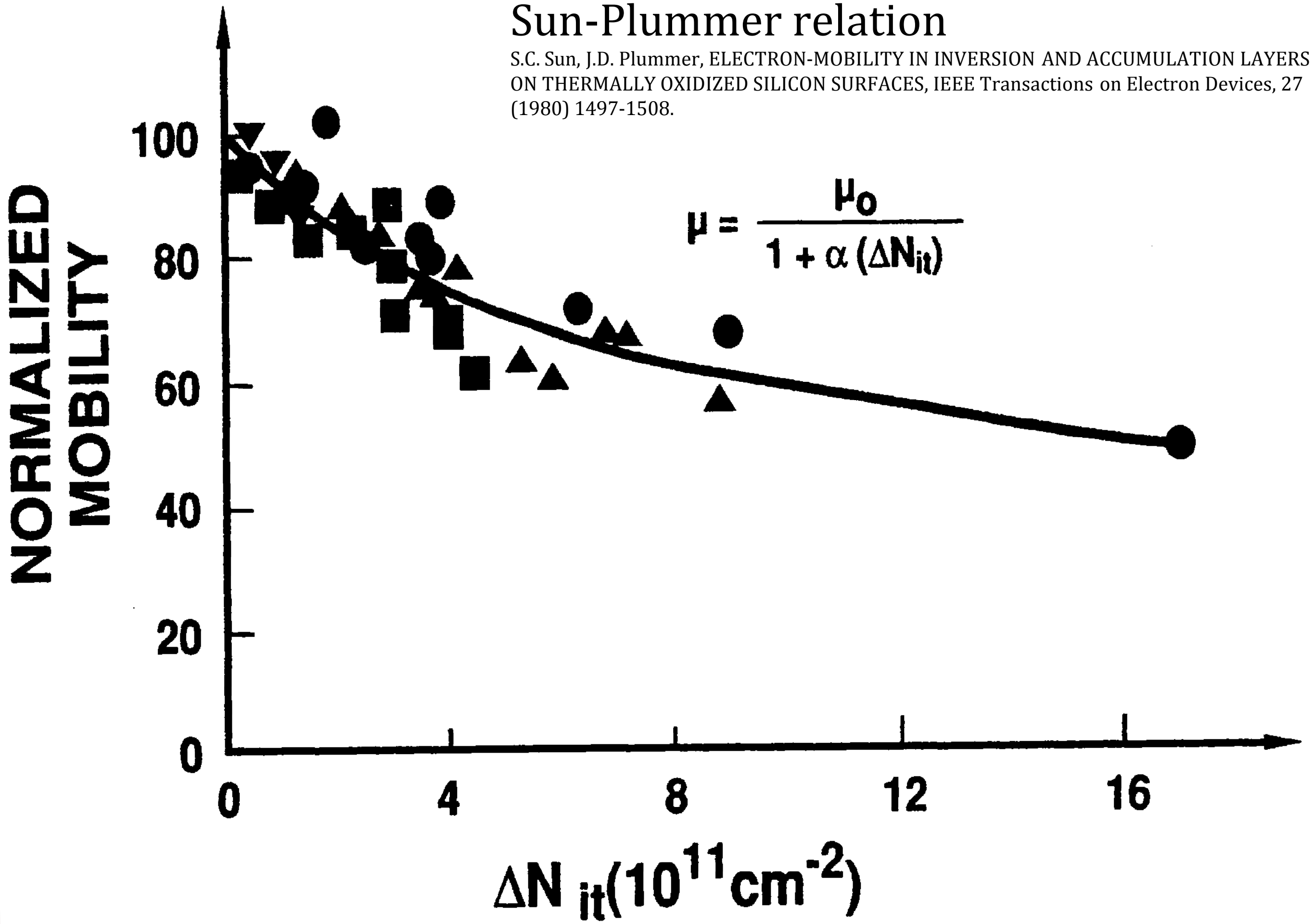
$$\Delta V_{ot,it} = -\frac{\int_0^{t_{ox}} x \cdot \rho(x) \cdot dx}{C_{ox} \cdot t_{ox}}$$

- High dose rate: large ΔV_{ot}, small ΔV_{it}
- n-channel: compensate
- p-channel: add up



J.R. Schwank, P.S. Winokur, P.J. McWhorter, F.W. Sexton, P.V. Dressendorfer, D.C. Turpin, PHYSICAL-MECHANISMS CONTRIBUTING TO DEVICE REBOUND, IEEE Transactions on Nuclear Science, 31 (1984) 1434-1438.

Interface trap effect on mobility



Sun-Plummer relation

S.C. Sun, J.D. Plummer, ELECTRON-MOBILITY IN INVERSION AND ACCUMULATION LAYERS ON THERMALLY OXIDIZED SILICON SURFACES, IEEE Transactions on Electron Devices, 27 (1980) 1497-1508.

F.W. Sexton, J.R. Schwank, CORRELATION OF RADIATION EFFECTS IN TRANSISTORS AND INTEGRATED-CIRCUITS, IEEE Transactions on Nuclear Science, 32 (1985) 3975-3981.

Planar detectors

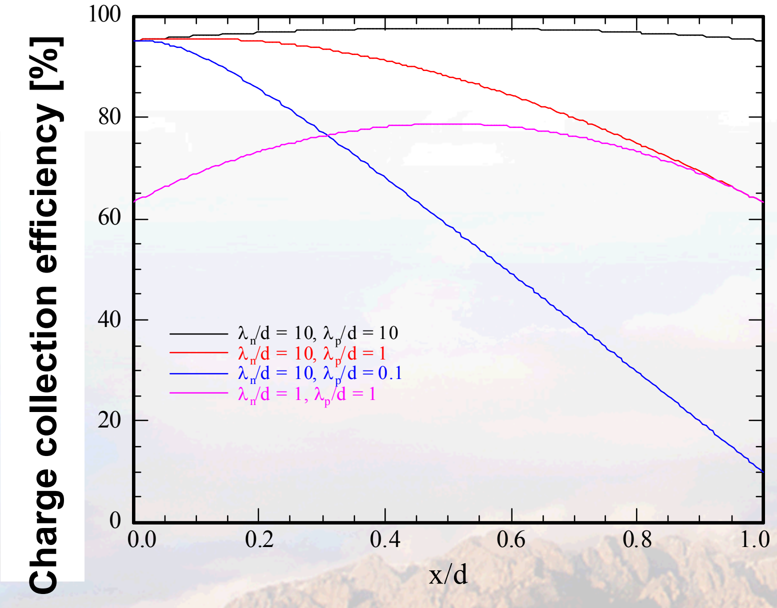
Hecht equation

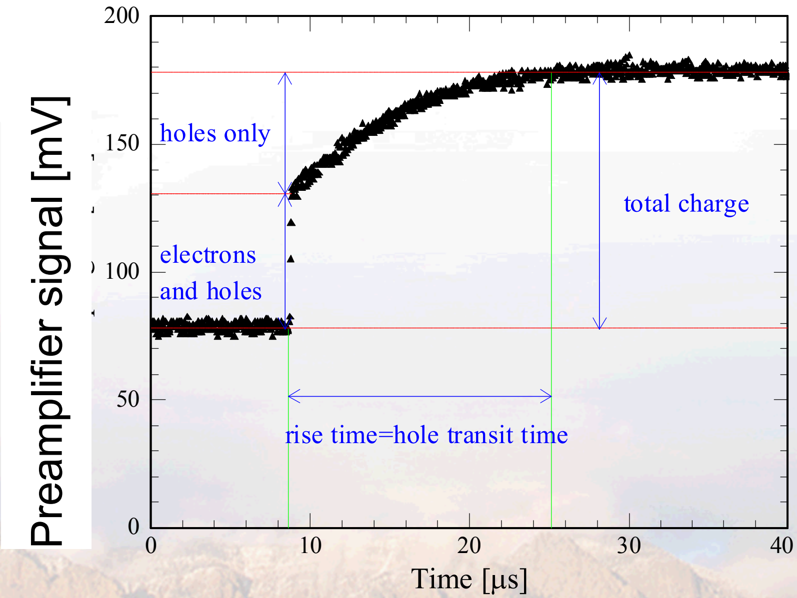
$$q(x) = N_0 e \left\{ \frac{\lambda_n}{d}\left[1 - e^{-\frac{x_n}{\lambda_n}}\right] + \frac{\lambda_p}{d}\left[1 - e^{-\frac{x_p}{\lambda_p}}\right] \right\}$$

$$\lambda = v_d \tau = \mu \tau E$$

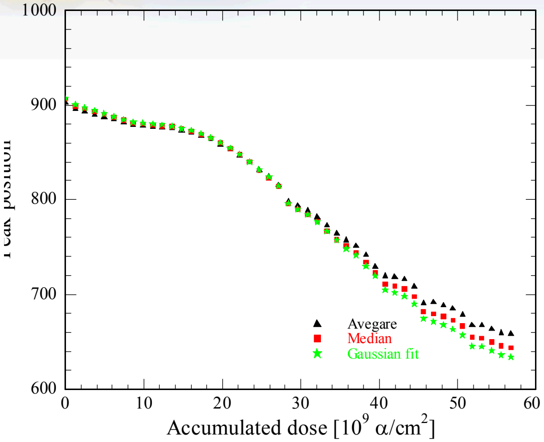
$$q(x,t) = \frac{Ne}{d}\left\{ \int_0^{\min(t,T_{r_n})} v_{d_n}(t') e^{-\frac{t'}{\tau_n(t')}} dt' + \int_0^{\min(t,T_{r_p})} v_{d_p}(t') e^{-\frac{t'}{\tau_p(t')}} dt' \right\}$$

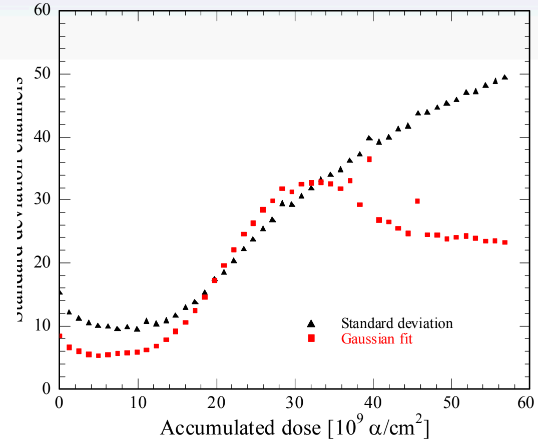
where x_n and x_p are the distances traveled by the electrons and holes.

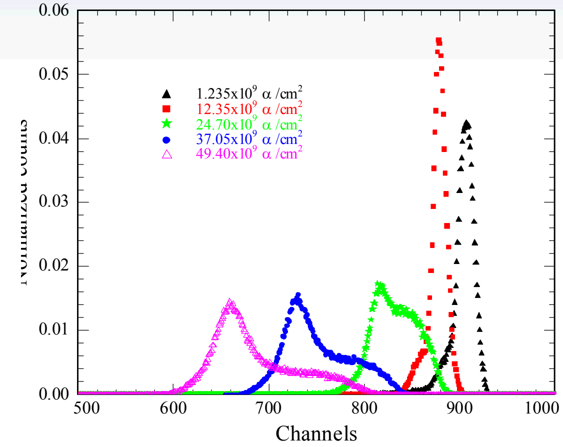


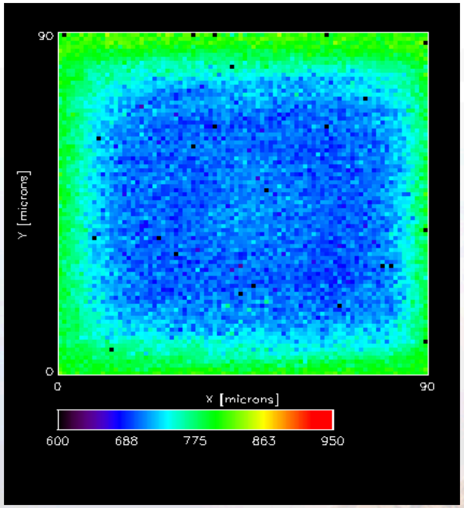


Performance degradation

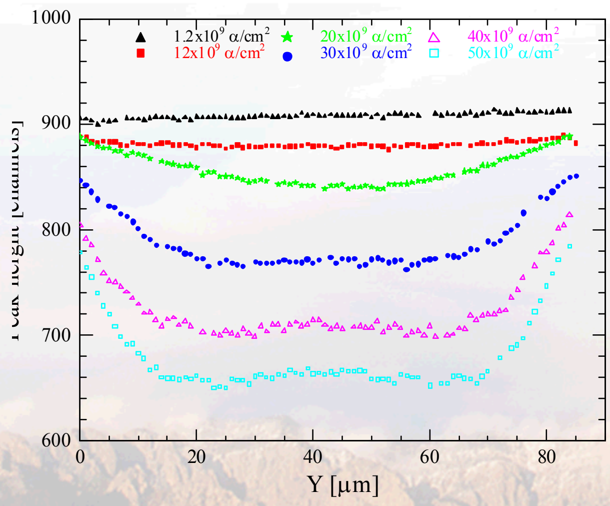








39.51x10^9 ⟨/cm^2



What can cause the wide (> 10 μm) border?

- Scan overlap (< beam spot size)
- Lateral damage spread overlap (~ 1 μm)
-
- **Lateral diffusion of electrons**

Damage model

Assumptions

- Only the electrons contribute to the signal.
- The electrons drift in the *z* direction and diffuse in the *x*-*y* plane.
- There is a damaged region at z_{max}=20 mm that where the electrons are trapped with *p*=a probability.
- Those electrons that are outside of the damage region when they reach $z=z_{max}$ are collected with *p*=1 probability.
- No additional trapping or detrapping.

The *f* electron distribution at (*x*,*y*,*z*) when the electron was created in (x_0,y_0,z_0) with $t=(z-z_0)/\mu E$ (m mobility, *E* electric field, *D* diff. coeff.)

$$f(x,y,z,x_0,y_0,z_0)=\frac{1}{4\pi Dt}e^{-\frac{(x-x_0)^2+(y-y_0)^2}{4Dt}}$$

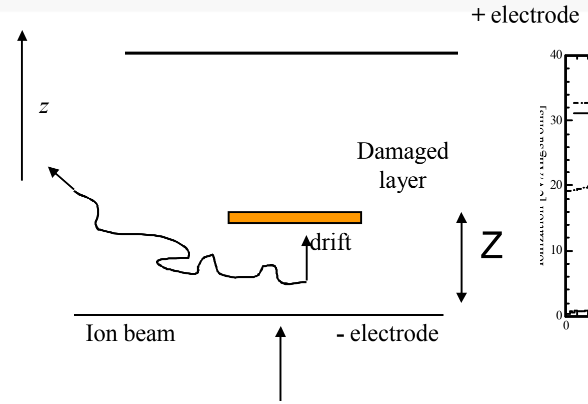
The charge collection efficiency for an electron created in (x_0,y_0,z_0)

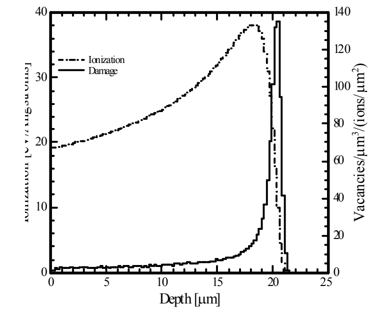
$$F(x_0,y_0,z_0)=1-\alpha\int_{inside} f(x,y,Z,x_0,y_0,z_0)dxdy$$

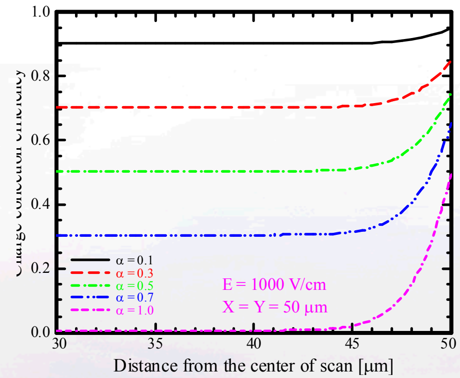
$$F(x_0,y_0,z_0)=1-\frac{\alpha}{4}\left[erf\left(\frac{X+x_0}{\sqrt{4Dt_Z}}\right)+erf\left(\frac{X-x_0}{\sqrt{4Dt_Z}}\right)\right]\left[erf\left(\frac{Y+y_0}{\sqrt{4Dt_Z}}\right)+erf\left(\frac{Y-y_0}{\sqrt{4Dt_Z}}\right)\right]$$

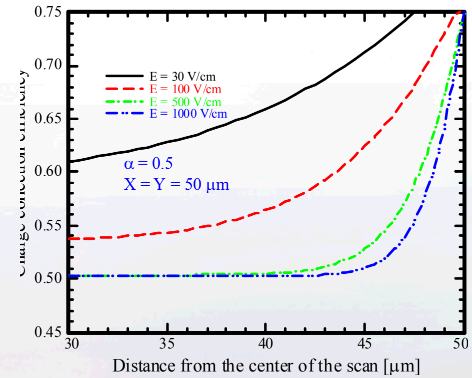
Charge collection efficiency in (x_0,y_0):

$$Q(x_0,y_0)=\frac{1}{Z}\int_0^Z F(x_0,y_0,z_0)S_e(z_0)dz_0$$



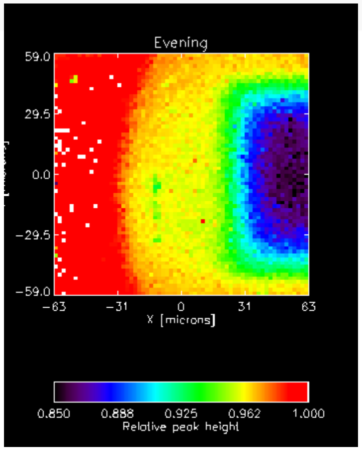


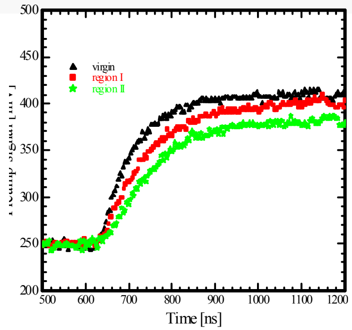




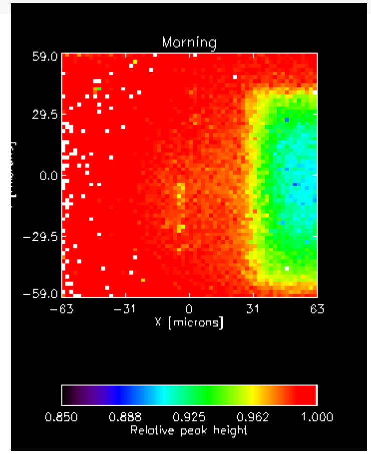
The border width depends only on the electric field

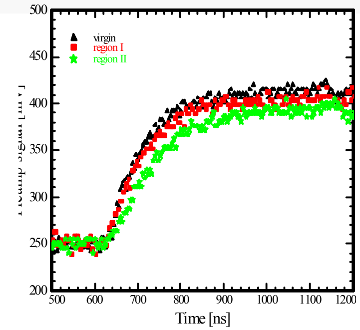
Damage experiments



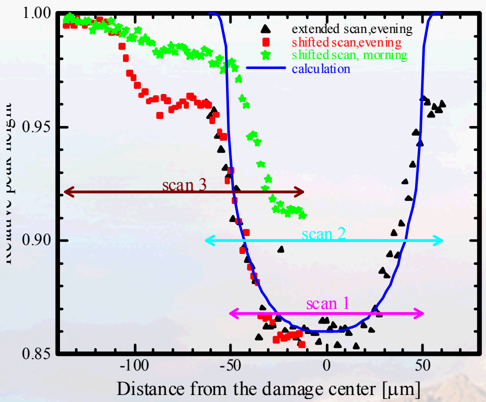


After irradiation

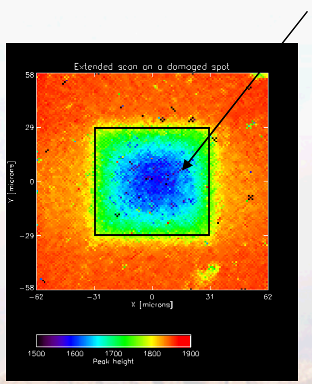




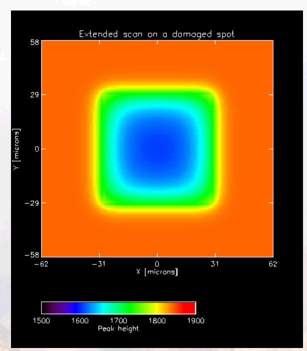
Next morning



Damaged spot



Calculation



Observations

- Longer collection time from damaged spot
- Some recovery
- Possible halo

Explanation

- Low electric field
- Charge trapping and release

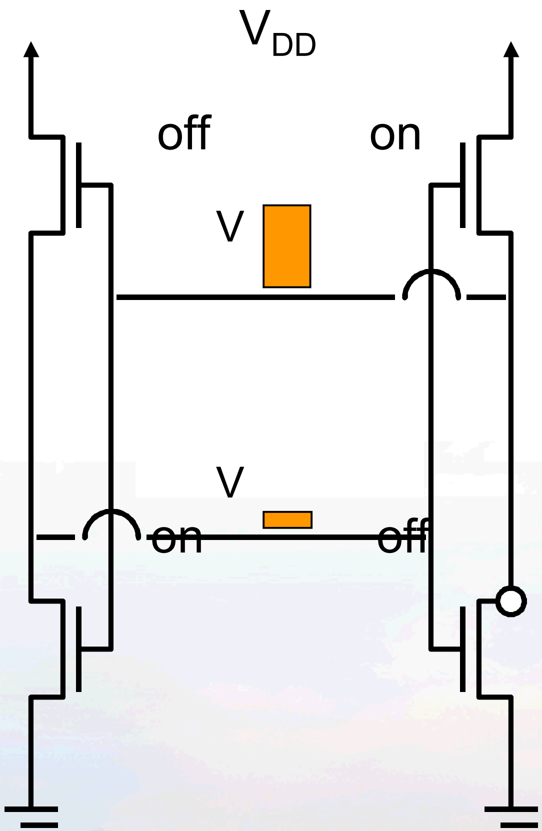
Single Event Effects (SEE)

- **Soft errors (no permanent damage)**
  - Single Event Upset (SEU) in SRAMs can occur any time, mitigation: error correction, reloading memory
  - Single Event Transient (SET) in digital logic circuits, ion has to hit at certain times, false data latched in, mitigation: voting circuits
- **Hard errors (permanent damage to device/circuit), catastrophic error, generally under high current conditions, mitigation: device/circuit needs to be replaced**
  - Single Event Latchup (SEL)
  - Single Event Burn-out (SEB)
  - Single Event Gate Rupture (SEGR)
  - Single Event Snapback (SES)

Modeling

- **Space radiation environment modeling**
- **Radiation transport: MRED = CAD+GEANT4**
- **Device modeling (TCAD): Davinci, Sentaurus, nanoTCAD**
  - Need experimental validation (IBIC, TRIBIC)
- **Circuit modeling: SPICE, Xyce**
  - Need very good device models
- **Mixed mode calculations: circuit + 1 device = Single Event Effects**

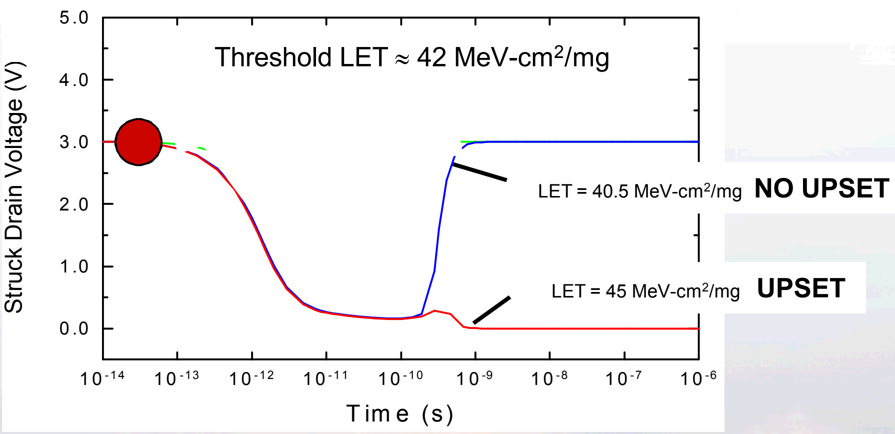
Single-Event Upset in SRAMs:



Race Condition

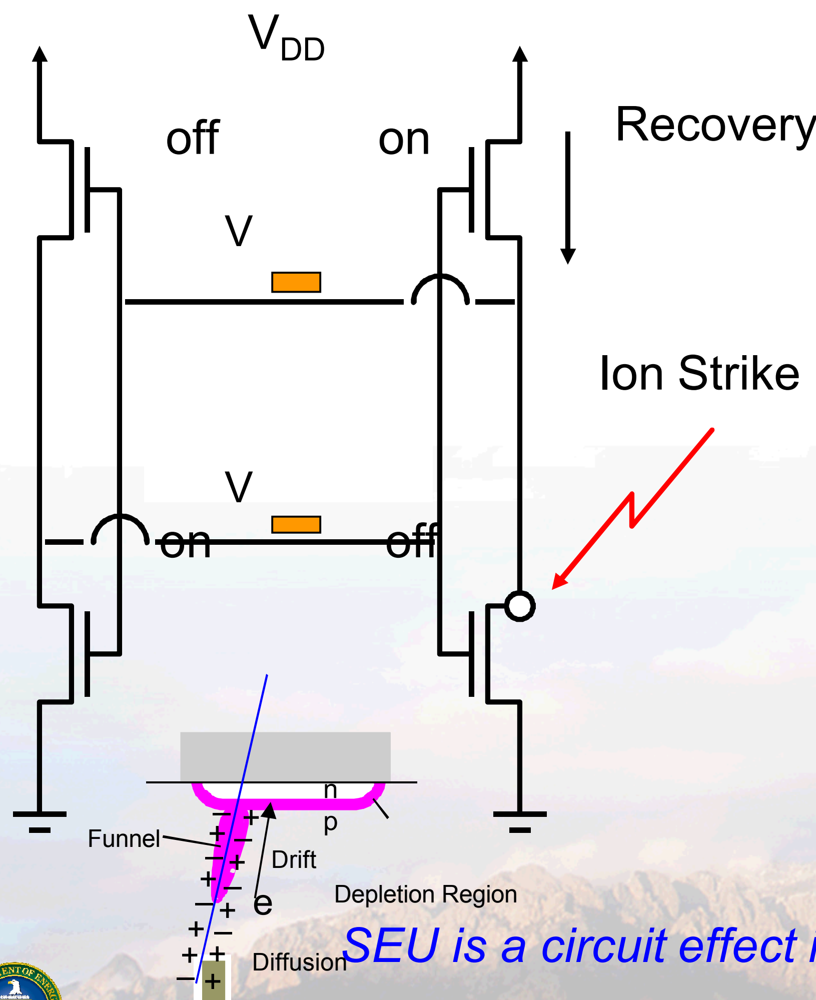
Recovery occurs before feedback:
No Upset

Feedback occurs before recovery:
Cell Upsets



SEU is a circuit effect initiated at the device level.

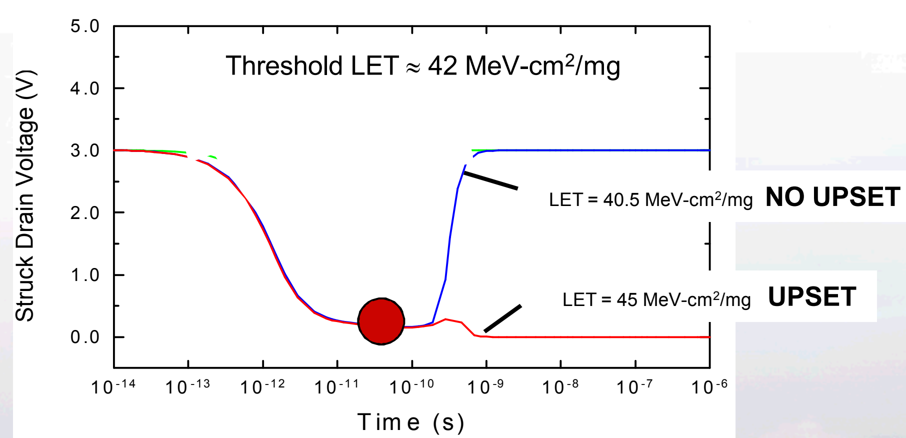
Single-Event Upset in SRAMs:



Race Condition

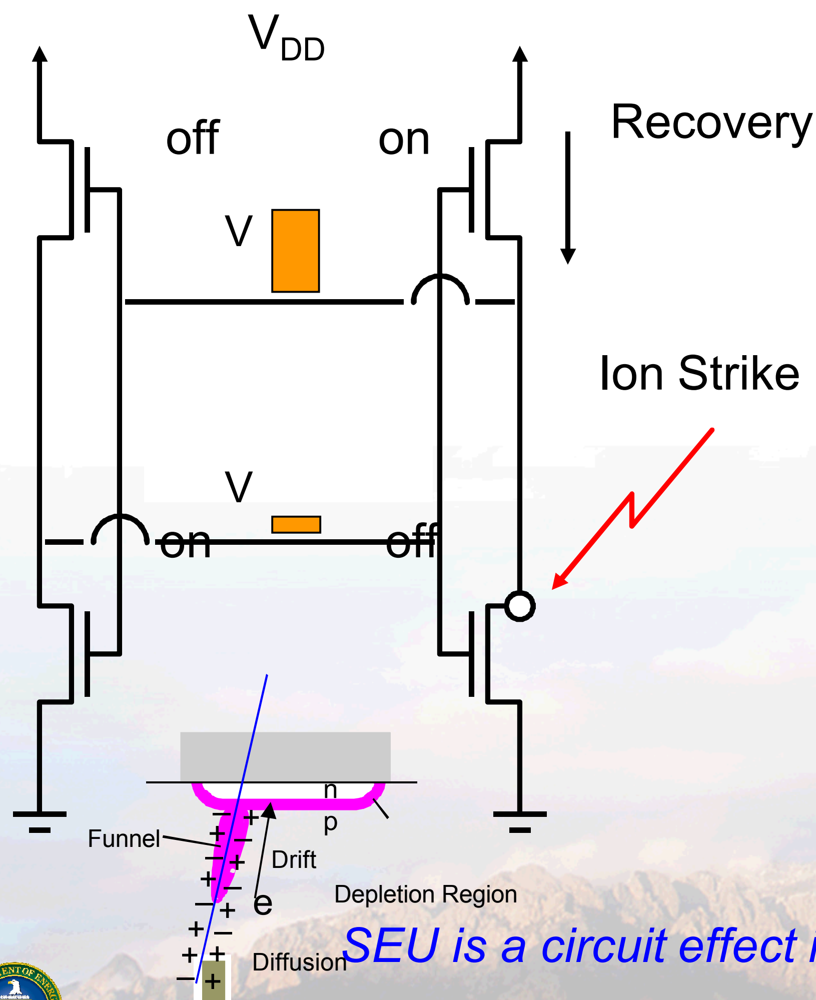
Recovery occurs before feedback:
No Upset

Feedback occurs before recovery:
Cell Upsets



SEU is a circuit effect initiated at the device level.

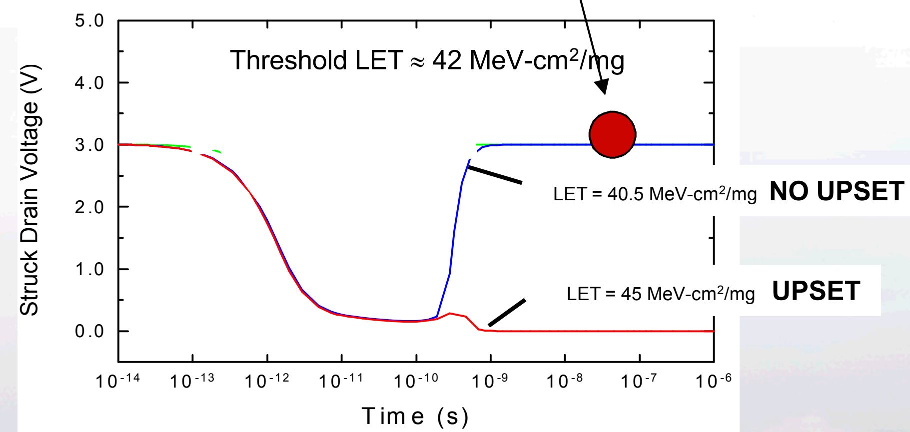
Single-Event Upset in SRAMs:



Race Condition

Recovery occurs before feedback:
No Upset

Feedback occurs before recovery:
Cell Upsets



SEU is a circuit effect initiated at the device level.

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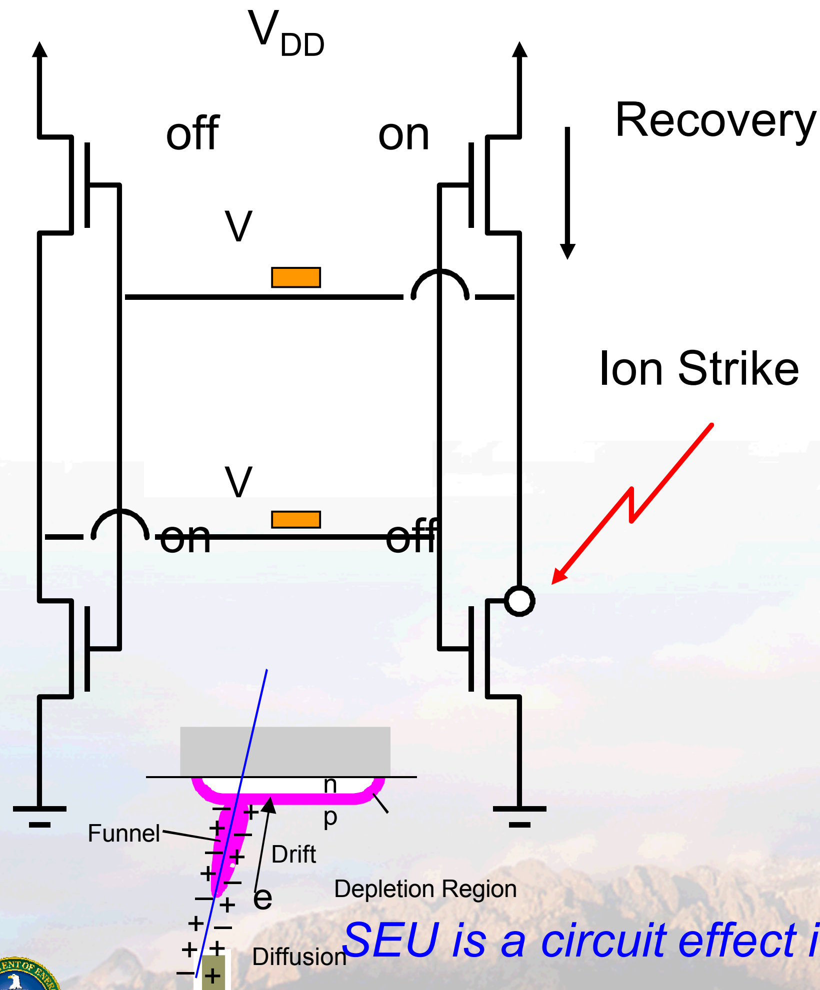
Single-Event Upset in SRAMs:



Race Condition

Recovery occurs before feedback:
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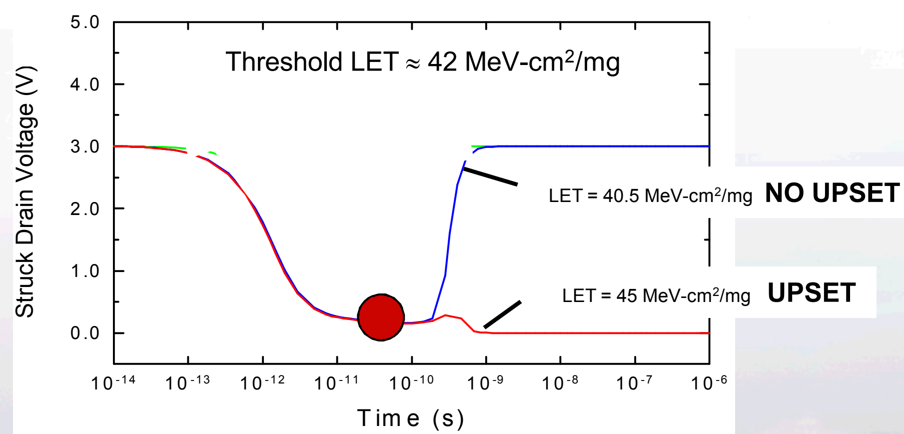
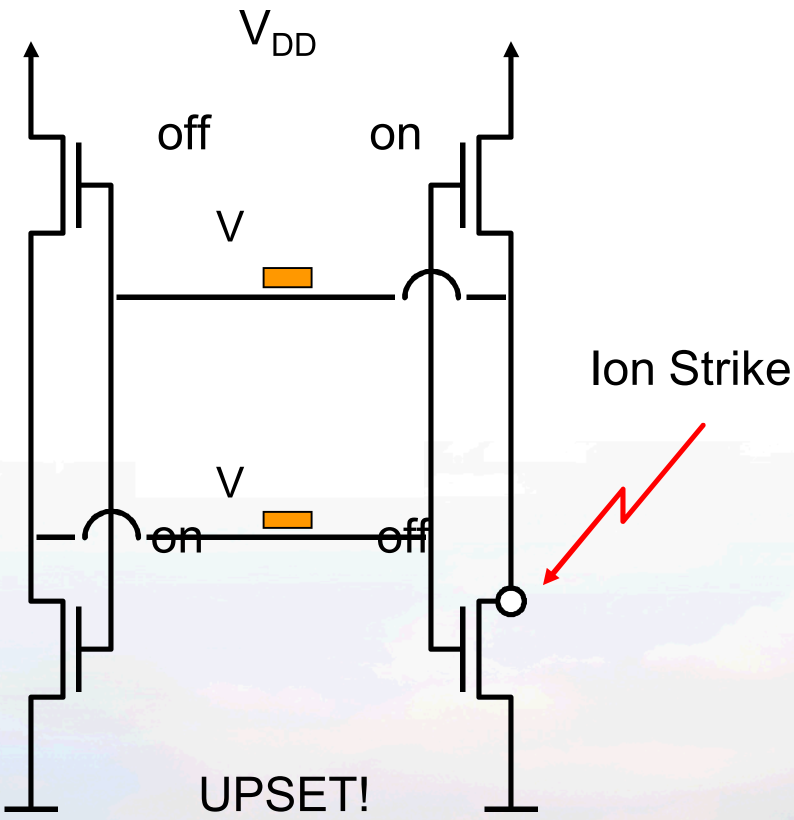
Cell Upsets



SEU is a circuit effect initiated at the device level.

Single-Event Upset in SRAMs:



Race Condition

Recovery occurs before feedback:
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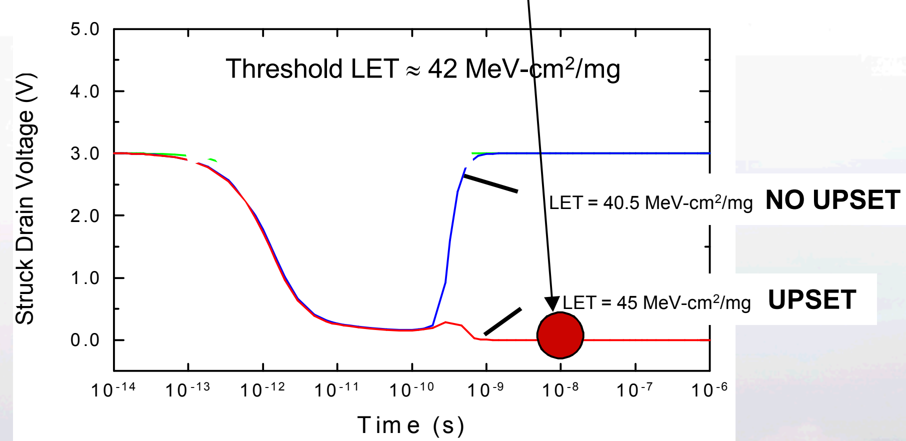
Feedback occurs before recovery:
Cell Upsets



SEU is a circuit effect initiated at the device level.

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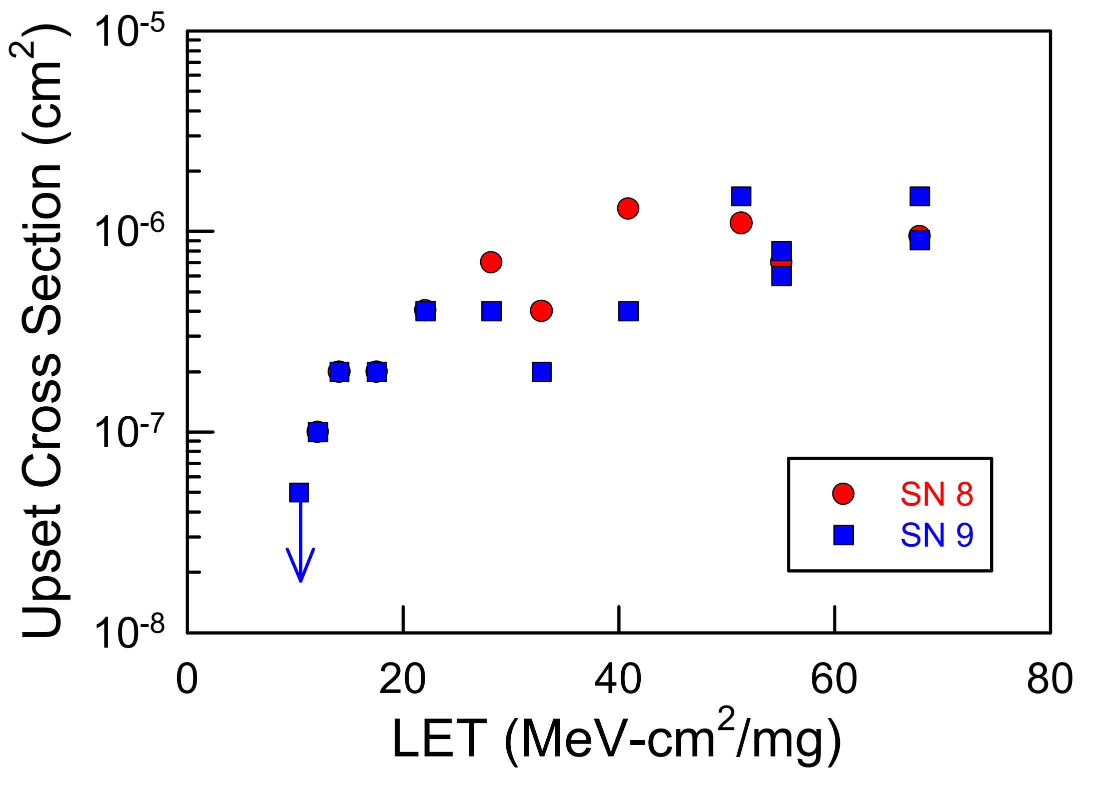
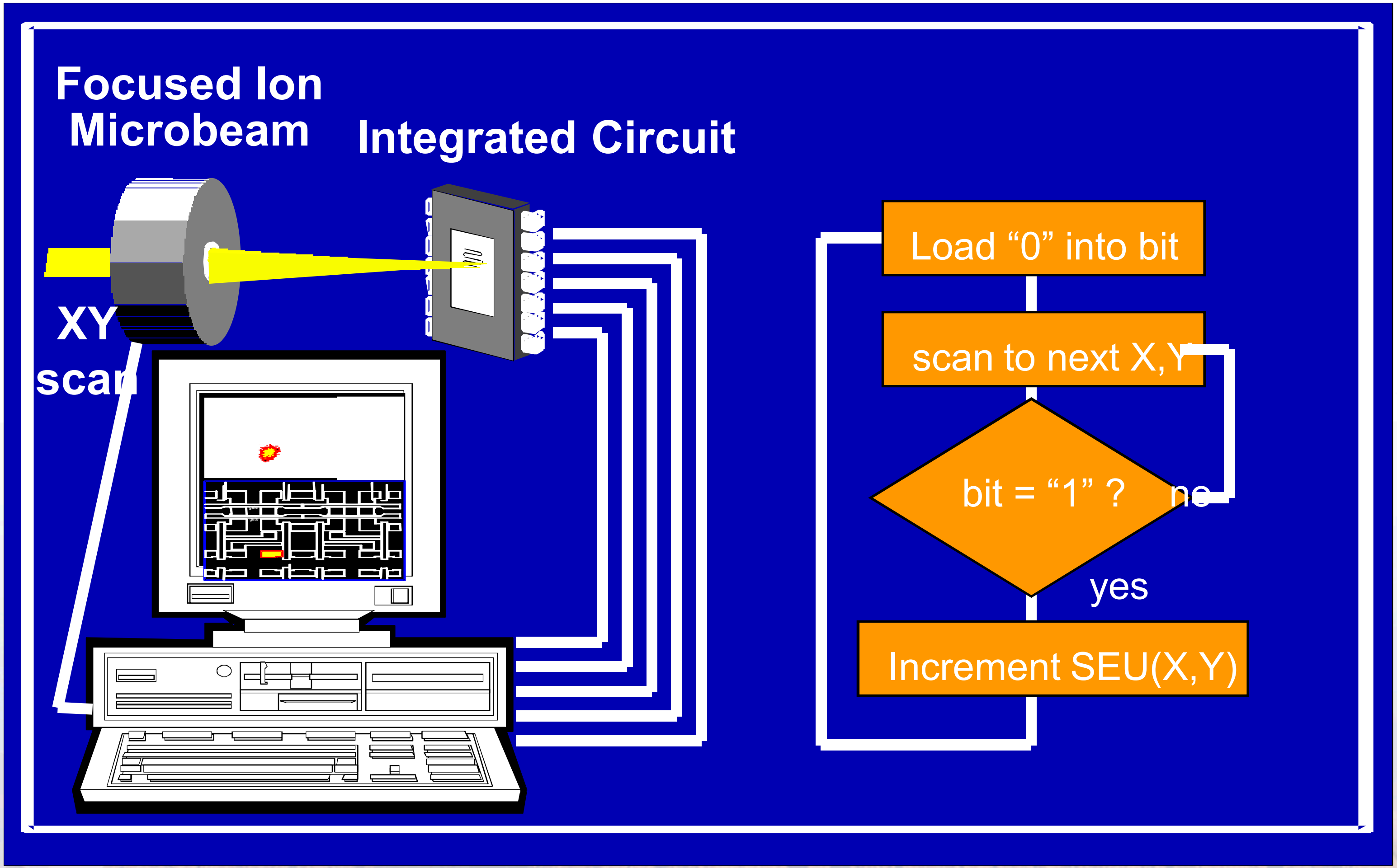
Broad beam testing: Upset cross section

- Set memory pattern
- Irradiate device (usually the whole SRAM)
- Read memory and compare to written pattern
- Count errors
- Divide by fluence



It tells you how sensitive a part is but but not which components are sensitive

Single Event Upset Imaging

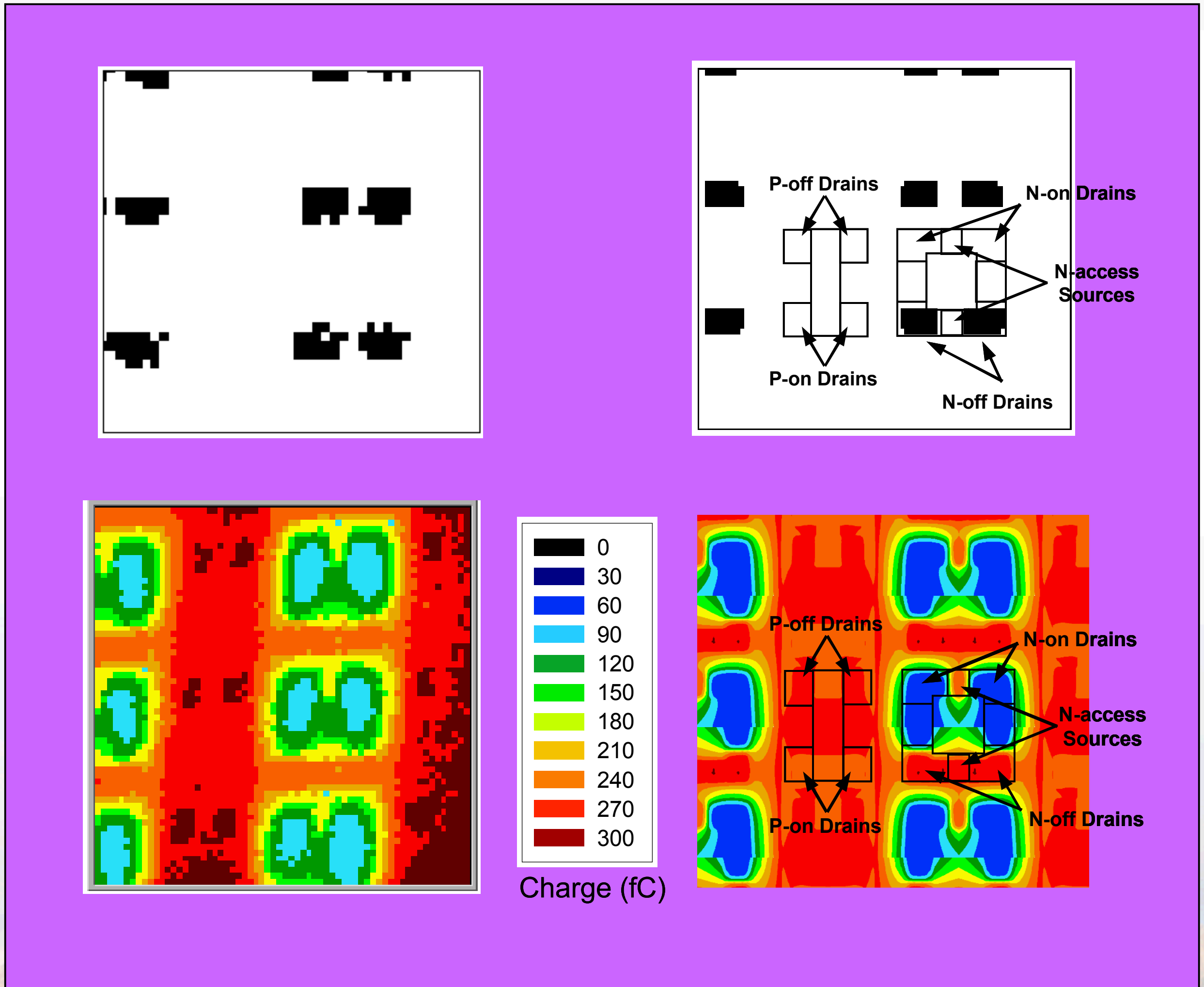


IBIC and SEU Imaging are used to observe upsets in ICs and to validate the DAVINCI model calculations of charge transport. 35 MeV Cl on SRAM

Single Event Upset Imaging

Ion Beam Induced Charge Collection

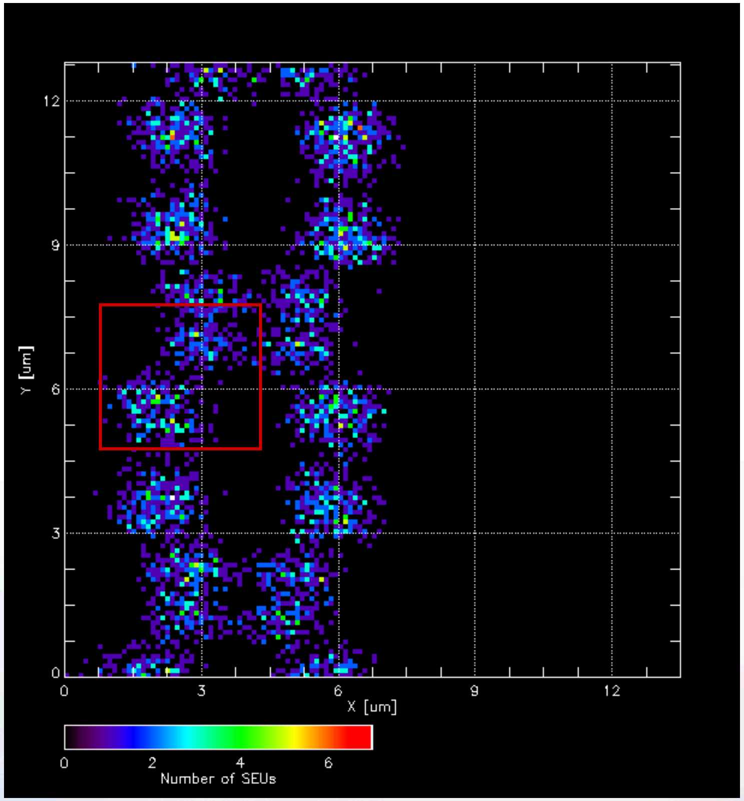
IBICC



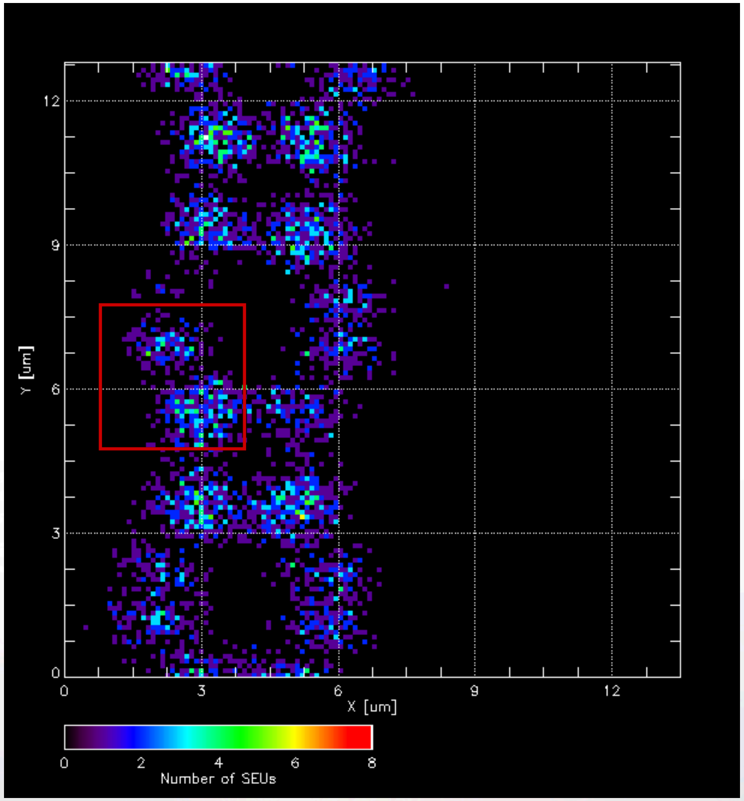
Experiment

Davinci Model

Upset depends on the content of the SRAM



All 0s



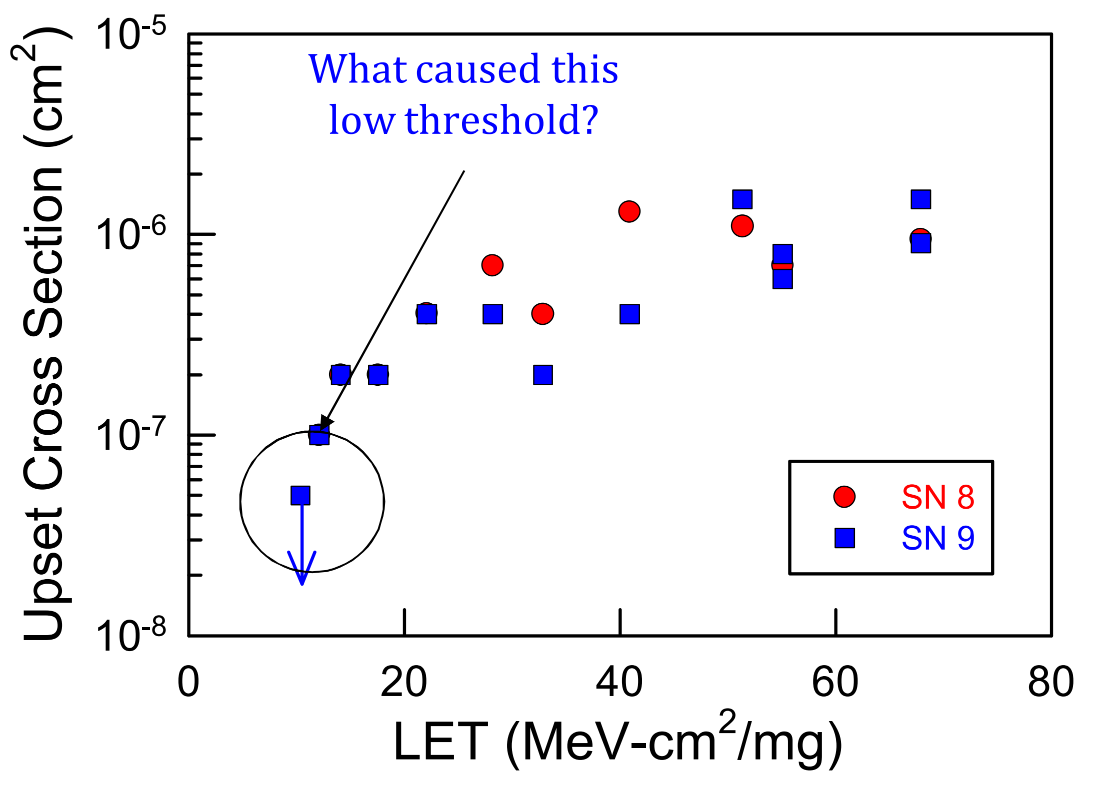
All 1s

The anatomy of device certification and failure analysis

- **Phase 0: New device design, attempt to achieve hardness by design, TCAD simulations**
- **Phase 1: Broad beam SEE cross section tests**
- **Phase 2: SEE mapping with the nuclear microprobe to validate TCAD results or pinpoint sensitive component that TCAD could not predict**
- **Phase 3: IBIC and TRIBIC on the actual device**
- **Phase 4: IBIC,TRIBIC and SEE mapping on model devices to understand the phenomenon that causes the SEE and recommend solution**

Broad-beam SEU tests of an ASIC revealed an unexpected sensitivity to low LET ions.

Phase 1



These SEUs have a very low cross section, but using the broad-beam it was impossible to pinpoint their cause. To determine that, measurements were made using REM. The SEU mapping pinpointed an area where several latches were located. (Phase 2.)

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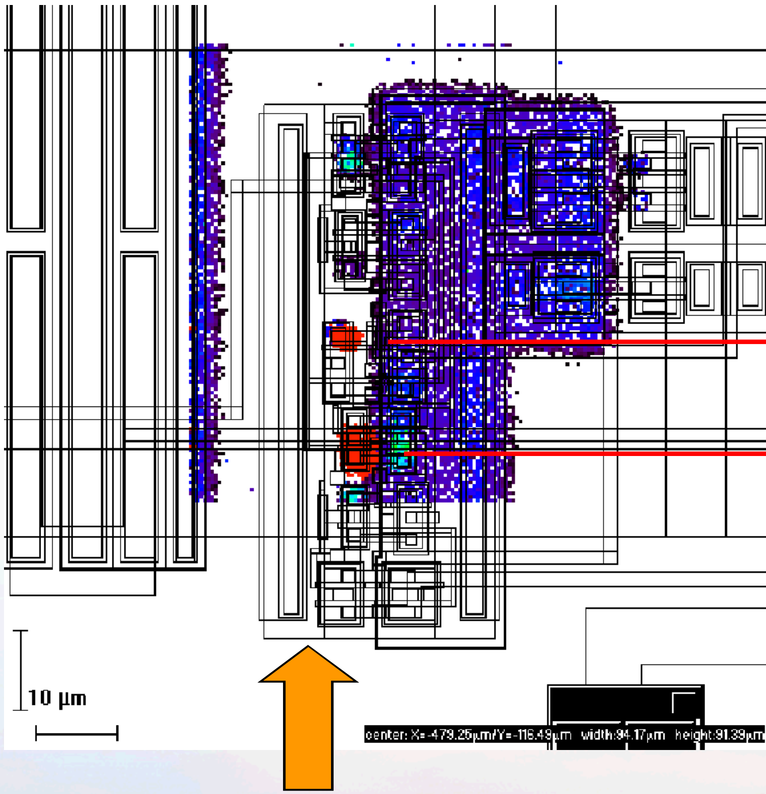
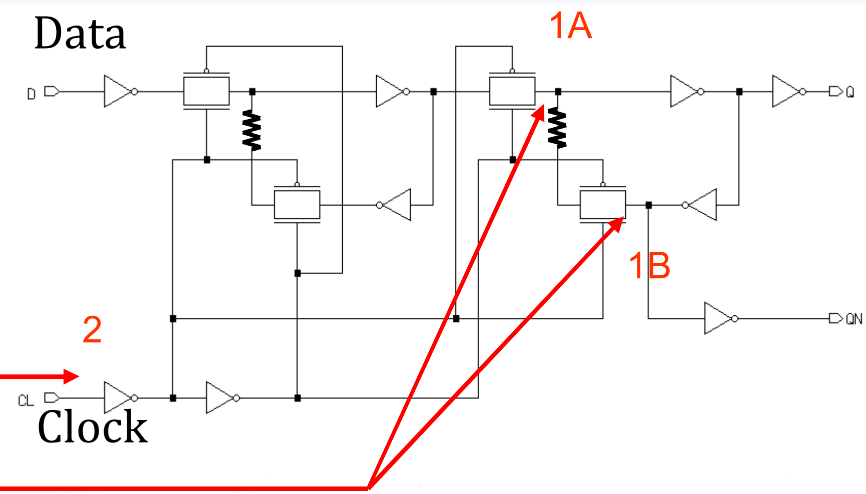
Microbeam SEU imaging confirmed suspected sensitivity of SEU (1A and 1B) and discovered another weak component (2) in test latch structures. (Phase 4)

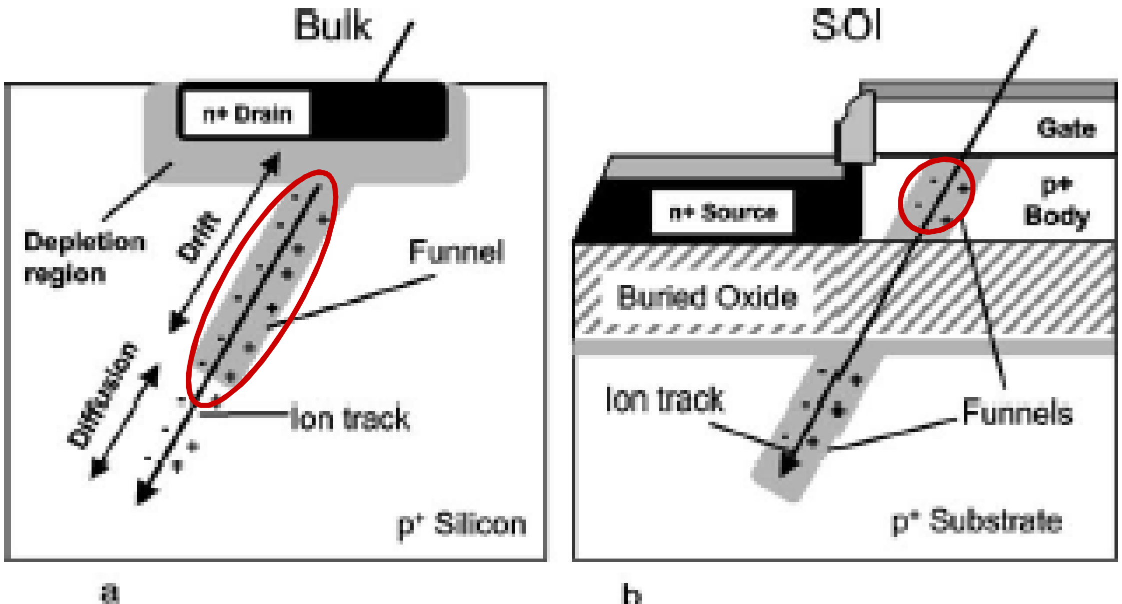




IBIC image (blue) and SEU image (red) overlaid on a GDS II map

- DAVINCI predicted the vulnerability in the transmission gates due to the resistors
- But could not predict the upsets when the clock was hit.
- After removing the resistors the transmission gate SEUs disappeared but the clock SEU remained.

SOI vs. Bulk

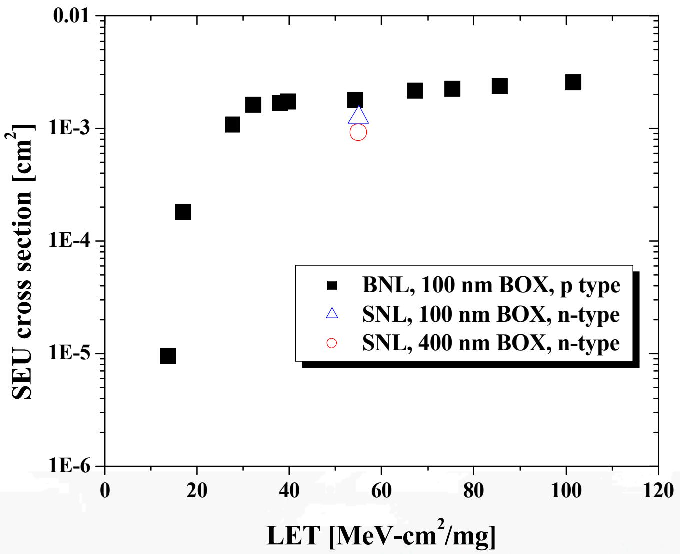


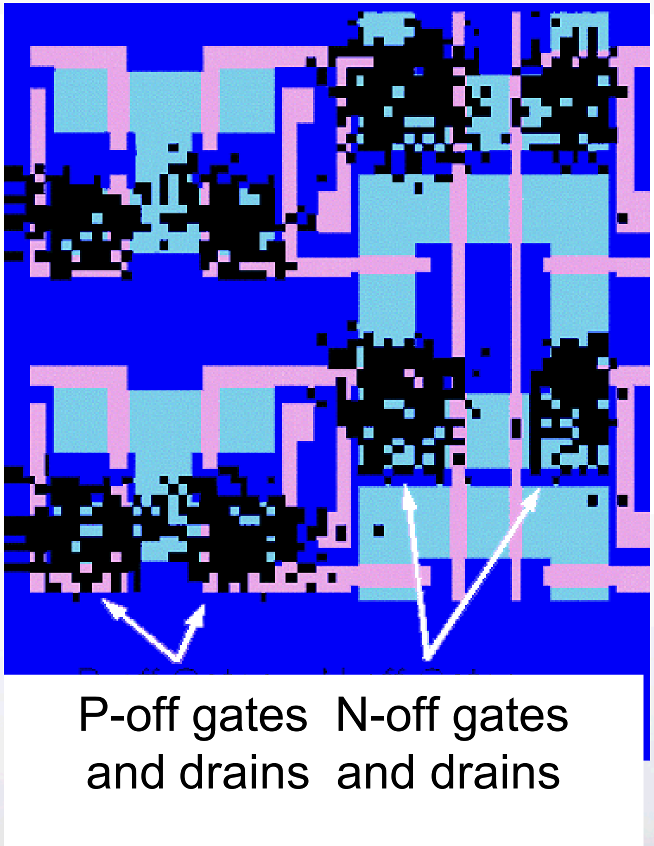
Large collection volume

Small collection volume

From D.S.Walsh et al, Nucl. Instr. Meth. B181 (2001), p 305

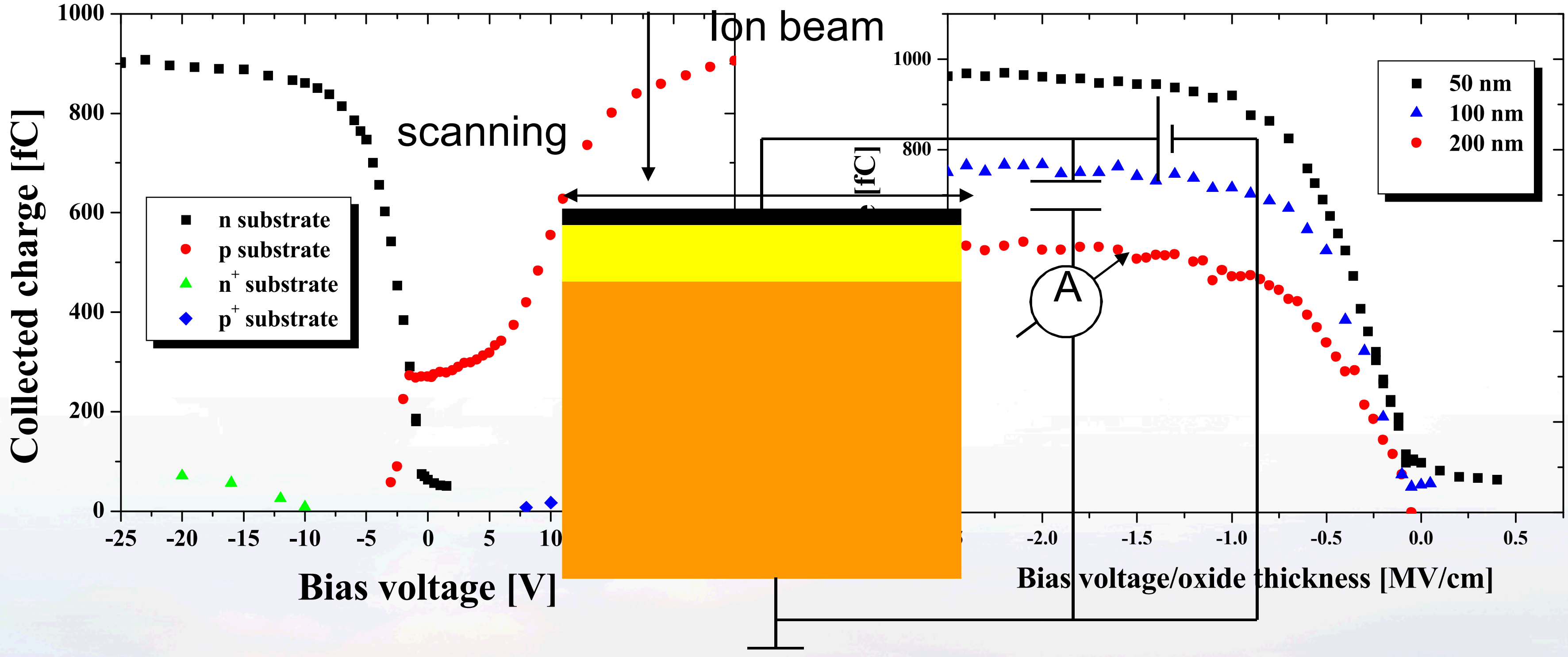
Anomalously high SEU cross section found in SOI SRAMs





- SEU cross section is closer to the combined drain – gate area than to the gate area itself.
- Charge collection occurs below the oxide.
- DaVinci (TCAD code) cannot predict it.
- Model: conducting pipe formed by the ion strike.

Charge collection in MOS structures



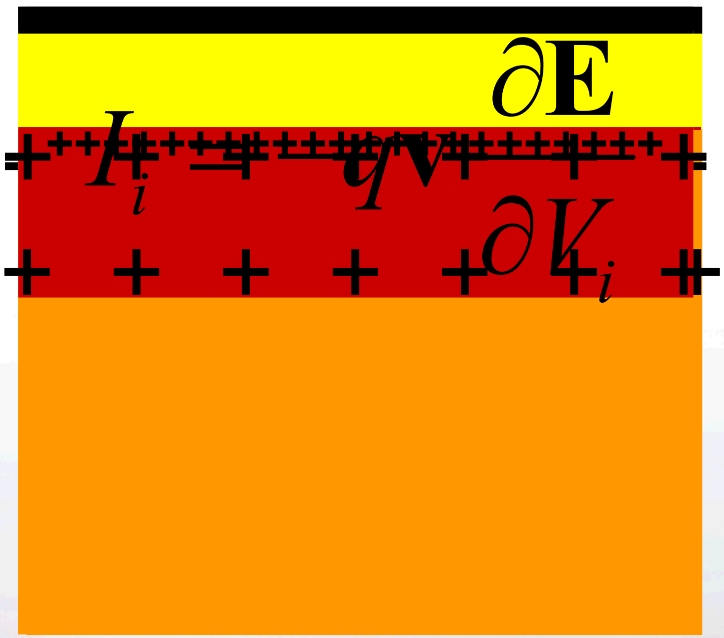
- Strong dependence on the polarity of the applied bias and the substrate doping level
- Conducting pipe model is wrong, charge collection is strongly related to the depletion layer below the oxide.

Induced charge decreases with increasing oxide thickness

Charge is never collected but induced!

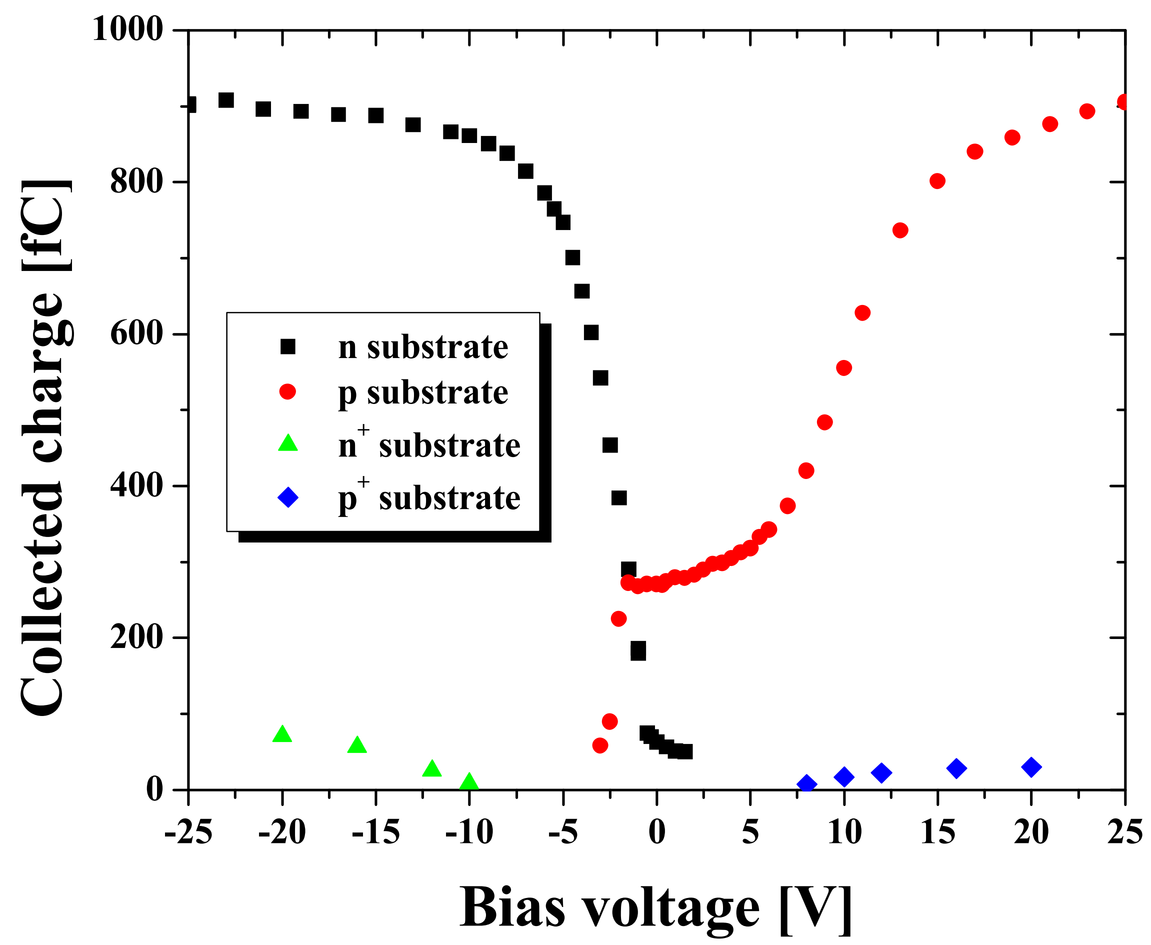
- **We do not measure the charge/current from the device but the induced charge/current**
- **Shockley-Ramo-Gunn theorem:**
- **Where is the electric field?**

$$I_i = qv\frac{\partial \mathbf{E}}{\partial V_i}$$



MOS capacitor (n-type substrate):
Accumulation mode (V>0):
majority carriers attracted
to the interface
Depletion mode (V<0):
donors/acceptors are ionized
and a depletion region is created
Inversion mode (V<<0):
minority carriers are thermally
generated at the interface but the
saturated depletion layer remains

A simple Gunn theorem of charge induction in SOI capacitors



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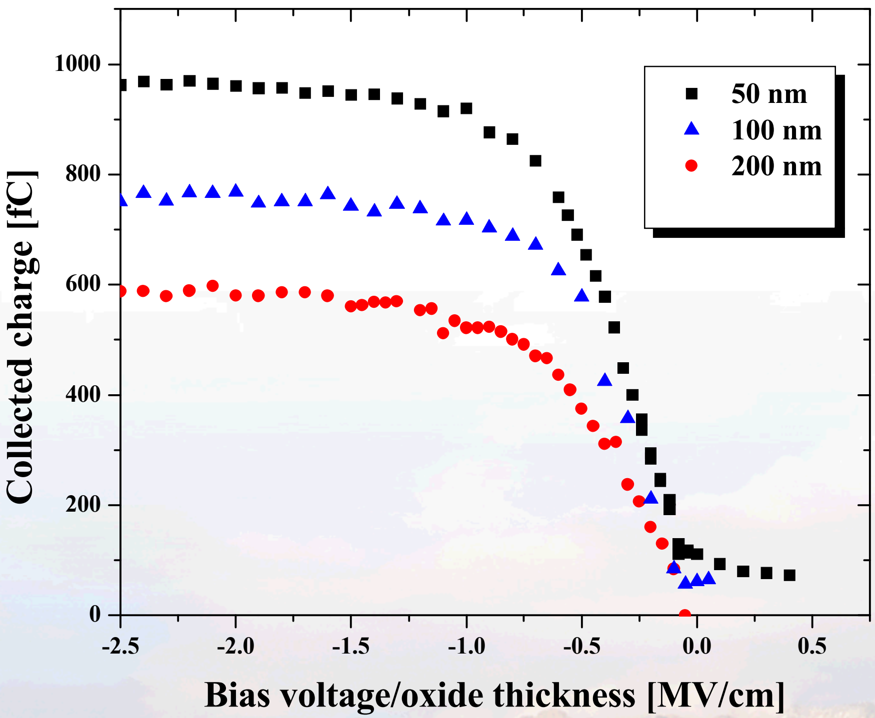
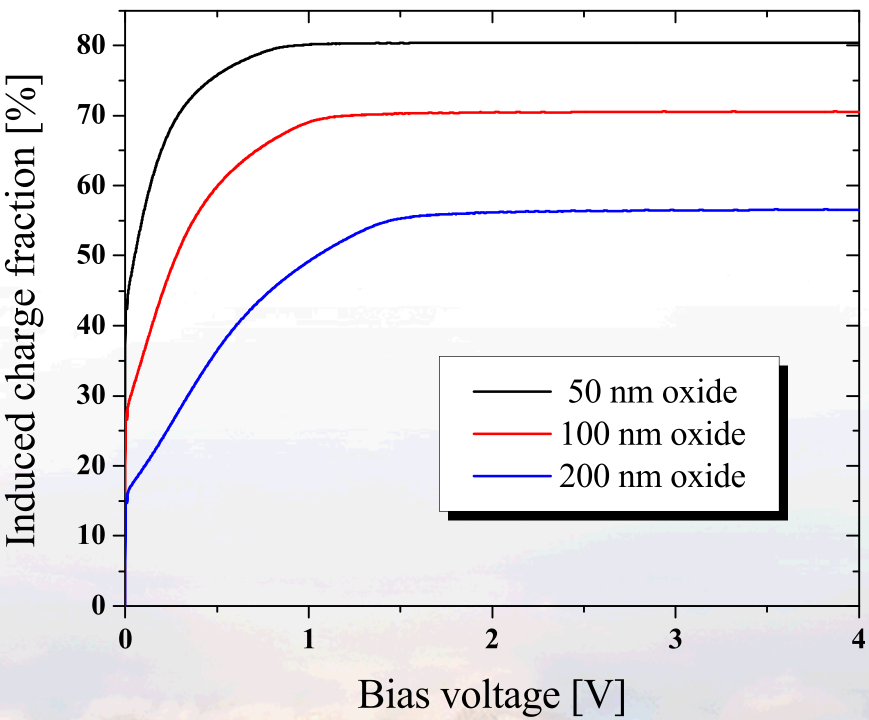
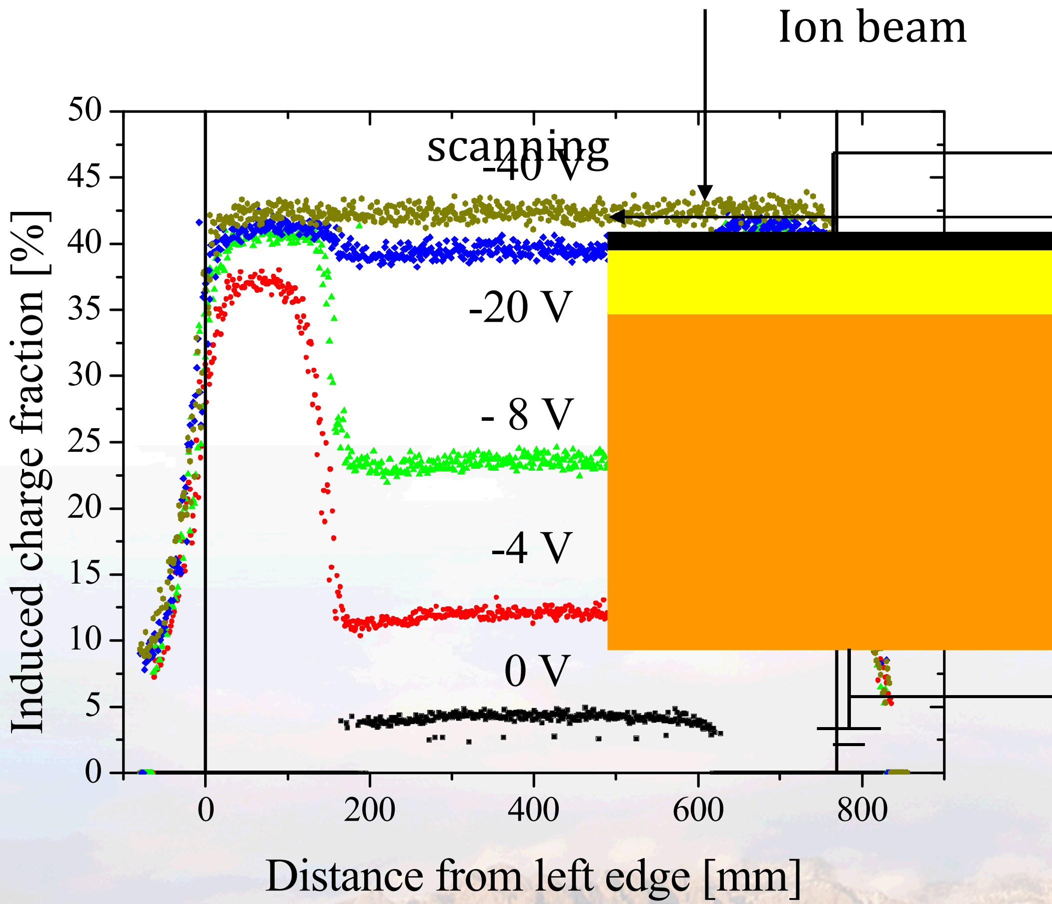
National Laboratories

Model calculations



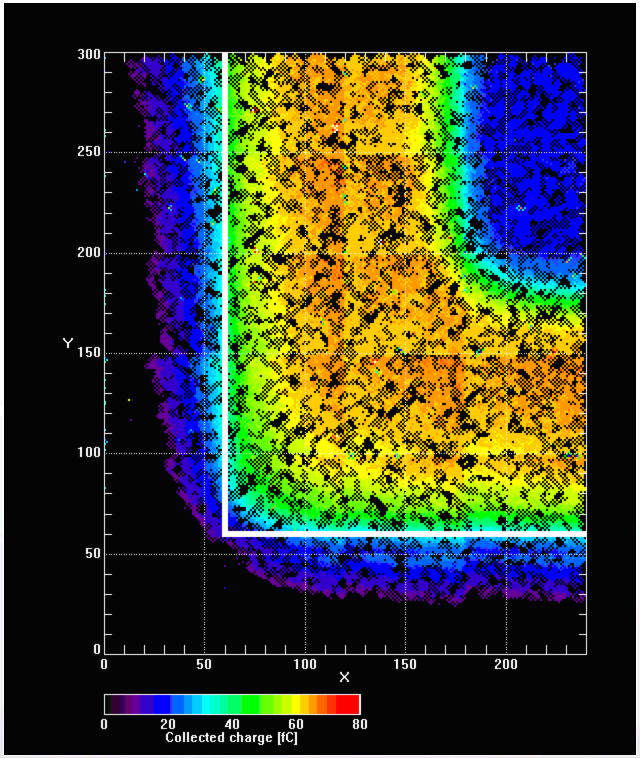


The "Rabbit Ears"

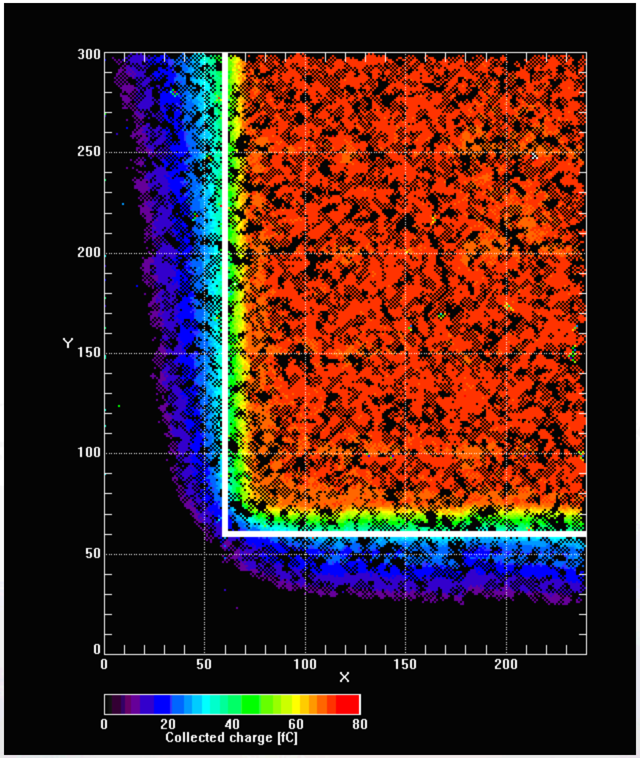


- The width of the "Rabbit ears" depends only on the oxide thickness but not on the bias or the capacitor size
- With increasing bias the "Rabbit ears" disappear

2D IBIC map of the edge of the capacitors



2 V

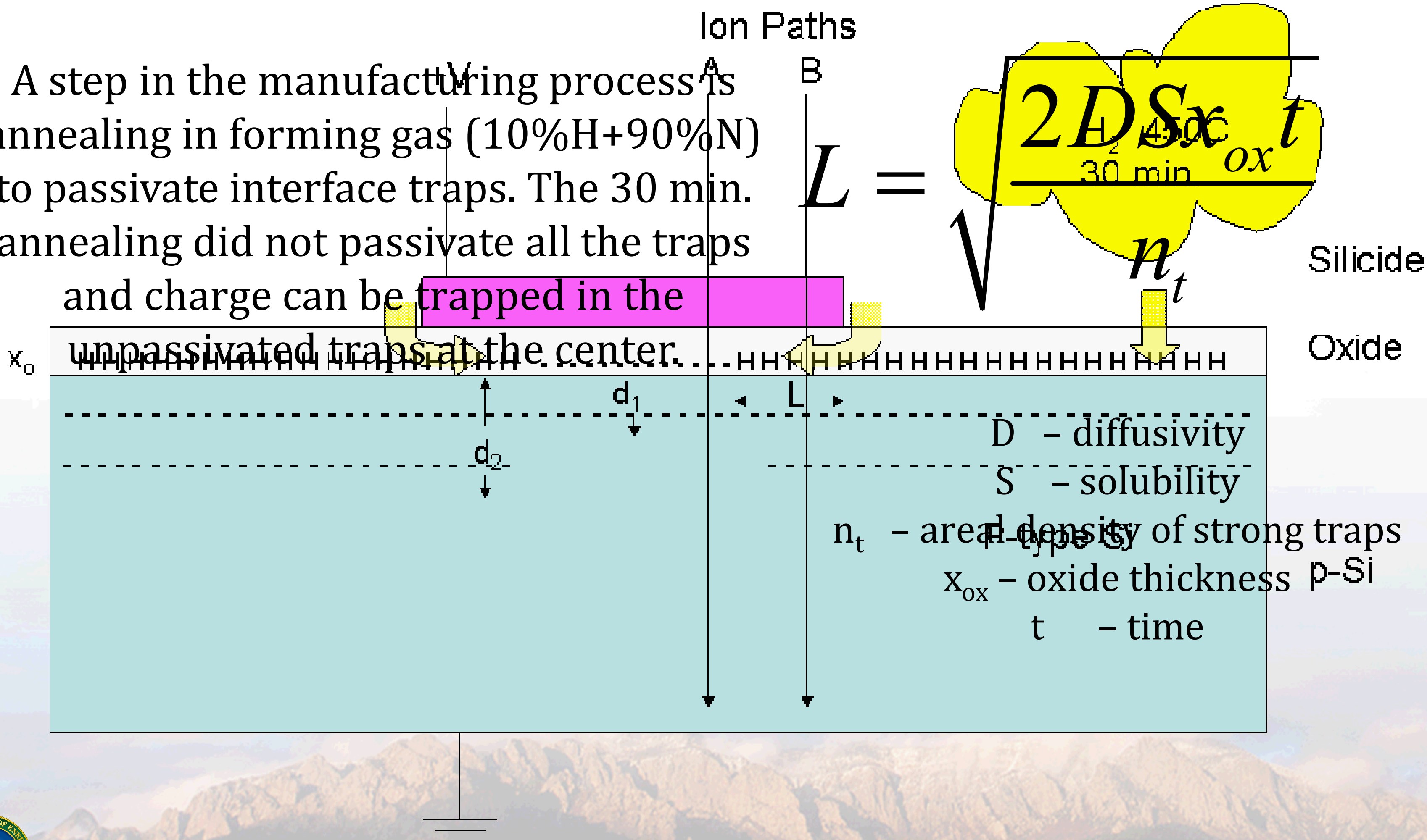


40 V

The explanation

A step in the manufacturing process is annealing in forming gas (10%H+90%N) to passivate interface traps. The 30 min. annealing did not passivate all the traps and charge can be trapped in the unpassivated traps at the center.

$$L = \sqrt{\frac{2DSx_{ox}t}{n_t}}$$



D – diffusivity

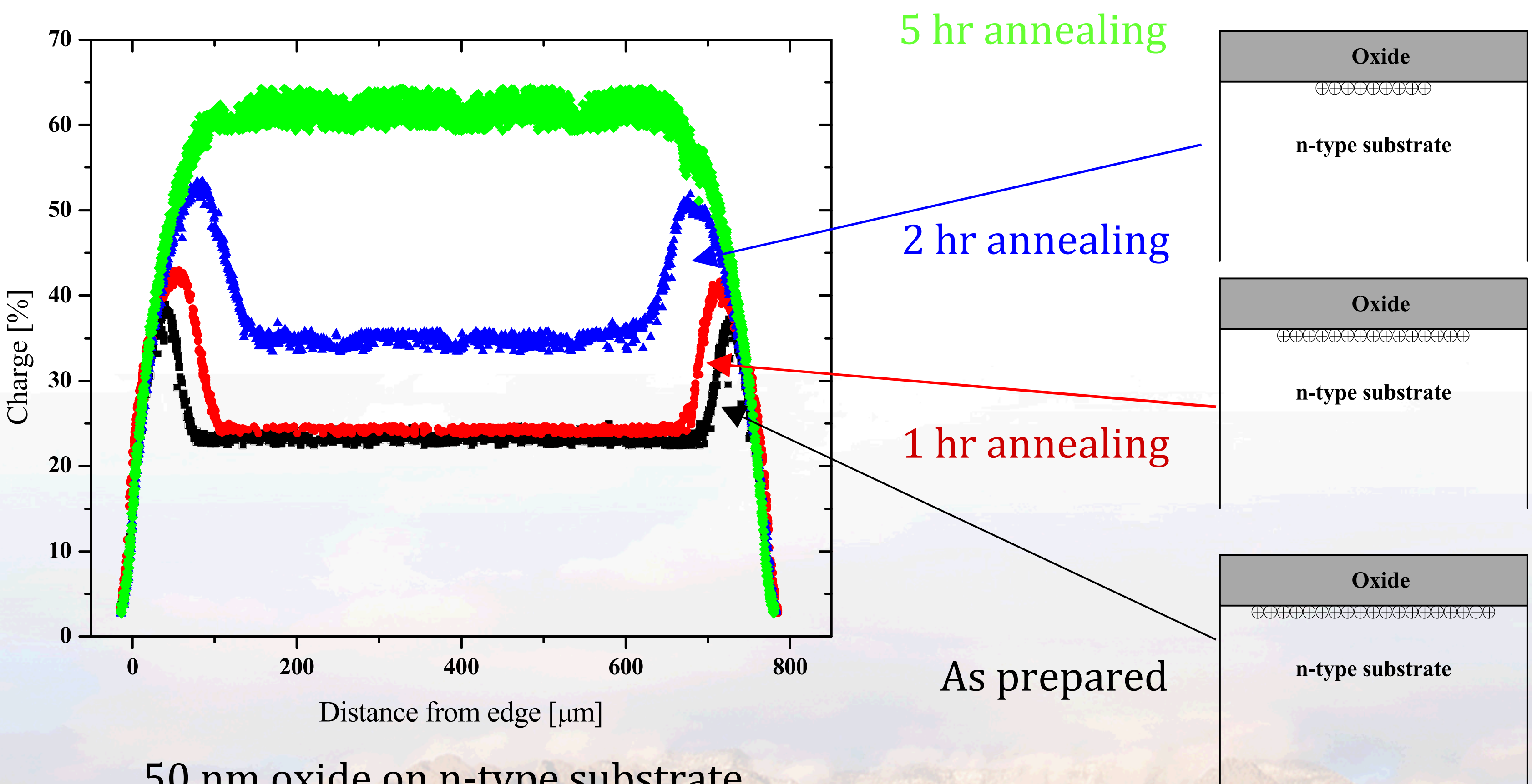
S – solubility

n_t – areal density of strong traps

x_{ox} – oxide thickness

t – time

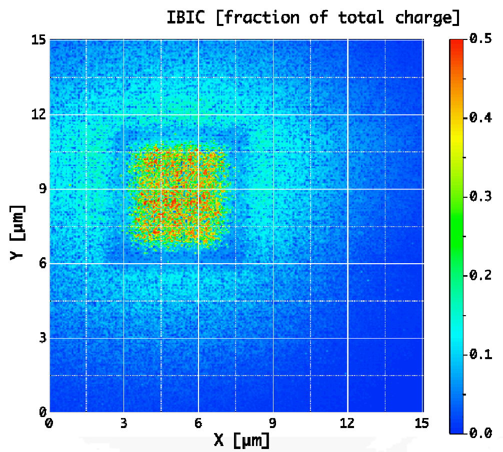
Anomalous charge collection in MOS structure is explained by insufficient passivation



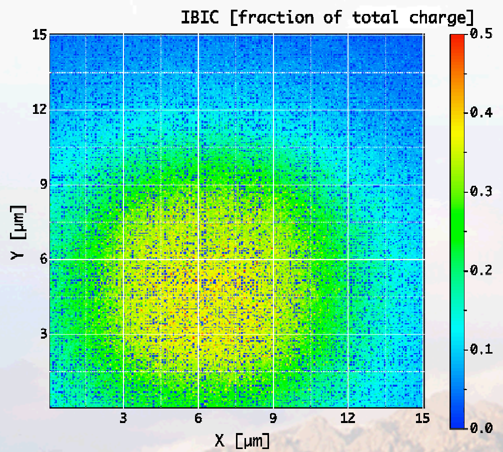
50 nm oxide on n-type substrate

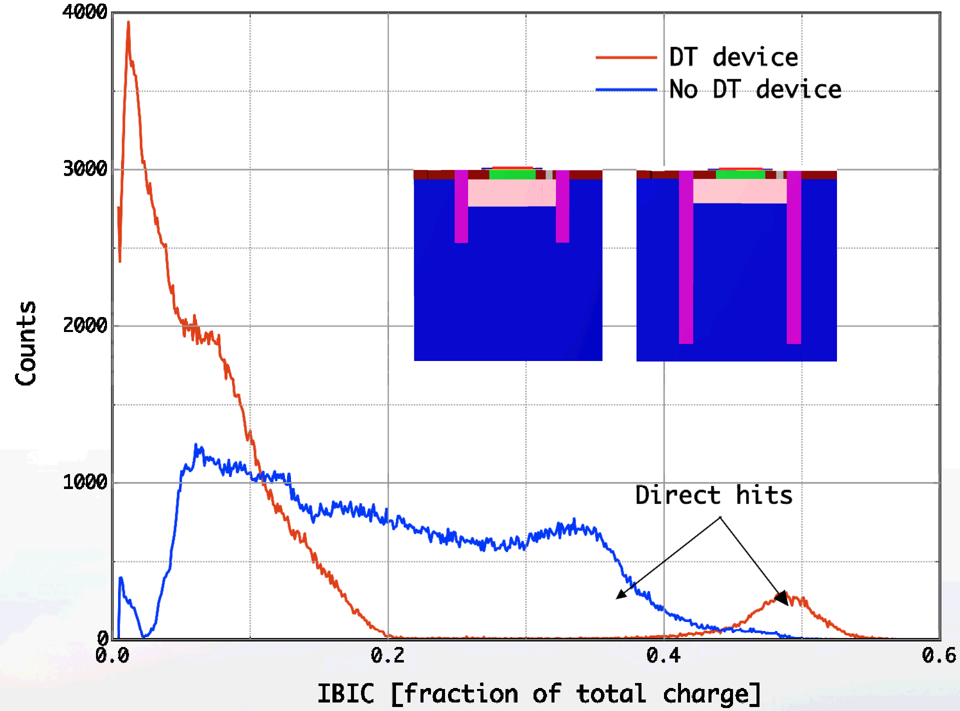
REM IBIC confirms SiGe HBT TCAD modeling

DT device



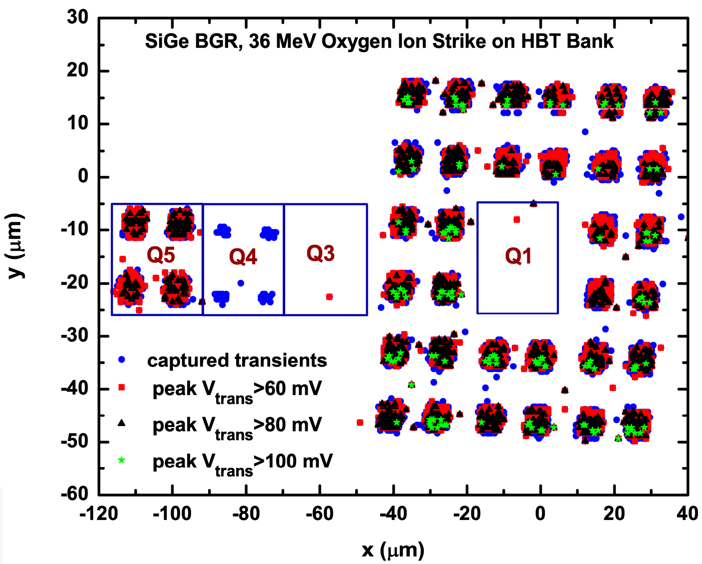
No DT device

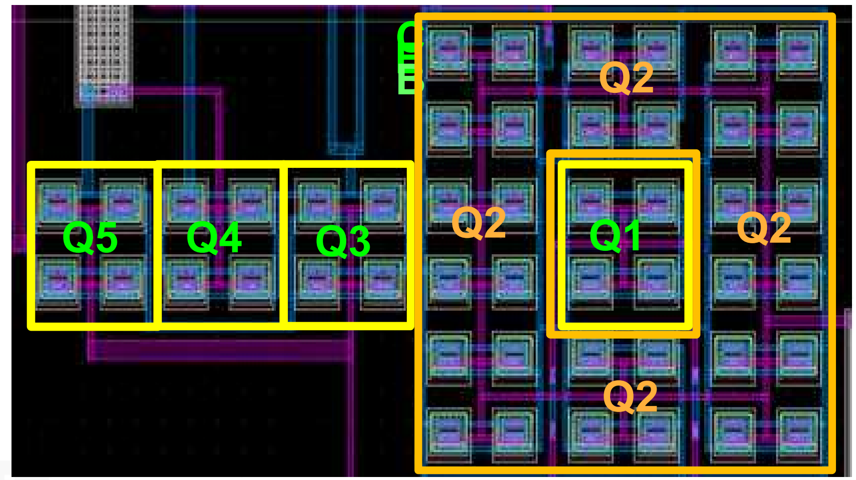


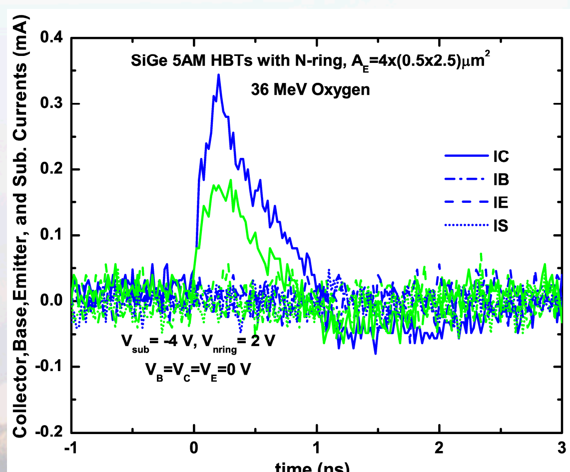


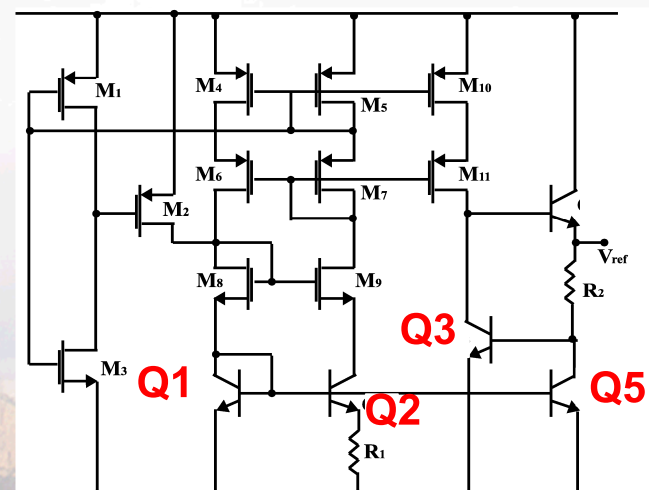
Deep trench isolation decreases the charge collection outside of the trench but increases it inside the trench. These experiments confirm TCAD modeling results.

SETs in SiGe BiCMOS BGRs









Summary

- **There are various radiation environments that affect microelectronic devices differently**
- **Ionization**
  - Total dose and dose rate effects in MOS devices
  - Single Event Effects (due to photocurrent)
- **Displacement damage**
  - Reduces lifetime, increases recombination
  - Detector efficiency degradation
  - Gain degradation in BJTs