

MICROSYSTEMS ENABLED PV

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OUTLINE

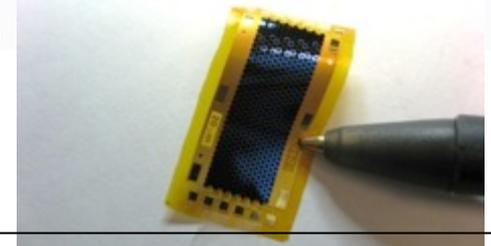
- **Technology benefits**
- Process flow/assembly examples
- Cost analysis
- From R&D to commercialization
- 3DIC/hybrid assembly and new functionality



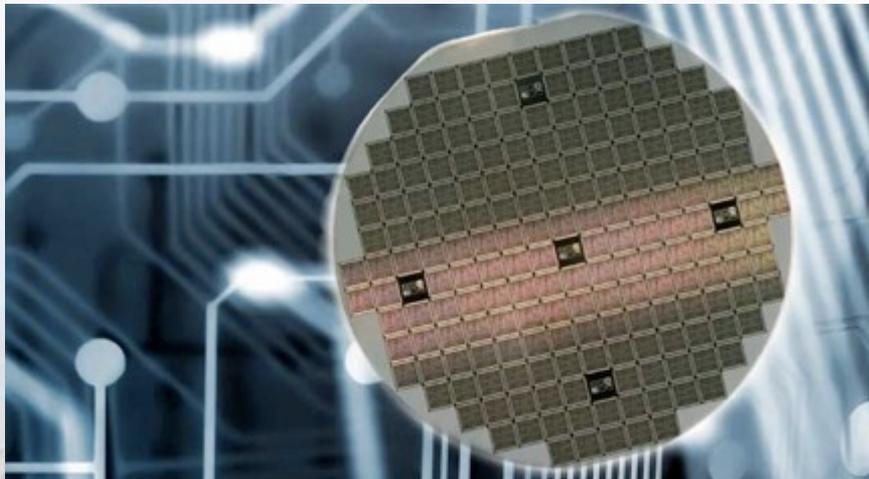
MEPV CORE COMPETITIVE ADVANTAGE

MEPV leverages concepts and technologies from existing successful microelectronics industry (IC, MEMS, LED, LCD, etc.):

- Take advantage of beneficial scaling effects
 - Improved performance
 - Reduced cost
 - New functionality
- Parallel vs. serial manufacturing
- Increased integration - system vs. cell (component) paradigm
- Utilize established manufacturing supply chain and infrastructure (reducing CapEx)



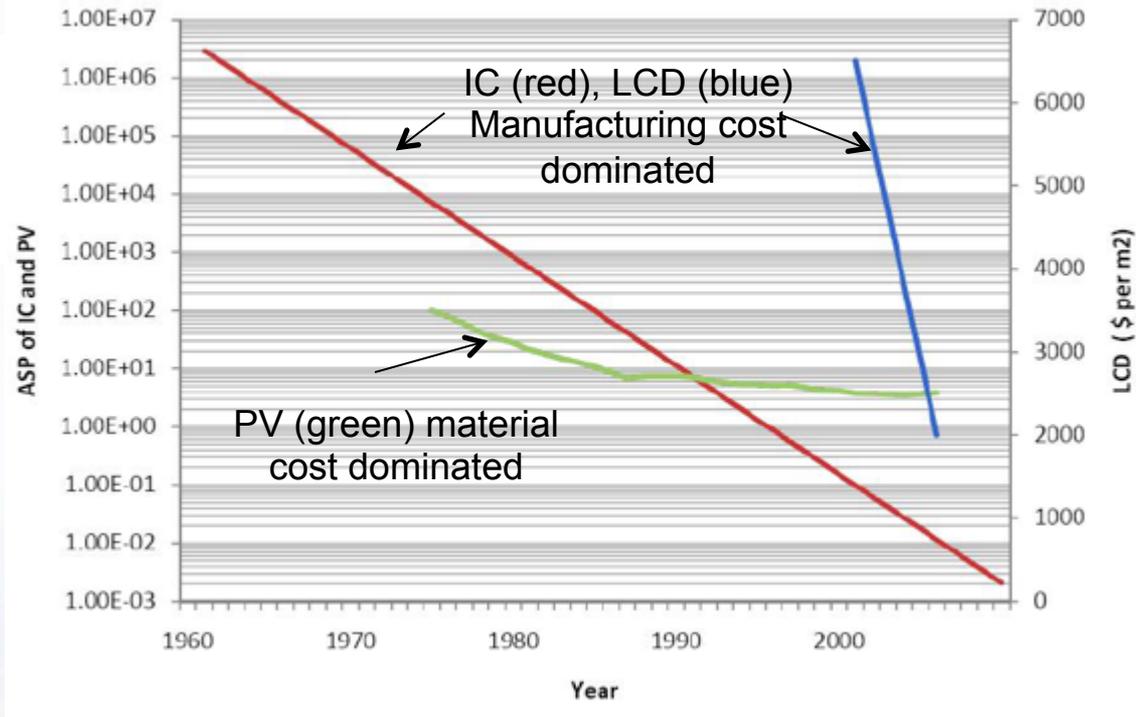
No other PV technology benefits from similar industry synergies



- *Integrated Circuit Market Size: \$300B*
- *LCD Market Size: \$102B*
- *LED Market Size: \$12.5B*
- *MEMS Market Size: \$10B*
- *PV Market Size:*



Potential for Cost Reduction



Future cost reductions are much more likely for MEPV than wafered silicon PV since manufacturing costs are a much larger component of the module costs relative to material costs. (Typically manufacturing costs are driven down more rapidly than materials costs.)

Manufacturing Tools Have Driven ~500x Price Reductions in Processed Silicon



- In 1975, the average price per transistor was ~\$0.02 (4- μm features).
- In 2008, the average price per transistor was ~\$ 5×10^{-9} (45 nm features)
- This is a 4,000,000x reduction in cost
 - Device scaling accounts for ~8,000x cost reduction (\$/transistor)
 - Manufacturing efficiencies account for ~500x reduction in the price of processed Silicon.

Scalability

Established Polysilicon supply (9-9s purity)

2010 >100,000 metric tons (Hemlock, Wacker, REC, MEMC)

2011 >120,000 metric tons

2012 - OCI (S.Korea) – 62,000 metric tons
GCL Poly (China) – 65,000 metric tons
world total > 200,000 metric tons

[Bloomberg Energy Finance]

Standard Si wafered PV

~ 5-6 grams Si/W_{peak}

MEPV - < 0.1 gram Si/W_{peak}

Silane/TCS main feedstock

10x thinner cells

no kerf loss (usually 50% for standard Si PV)

>10x optical concentration



200 MW_p/year unit line

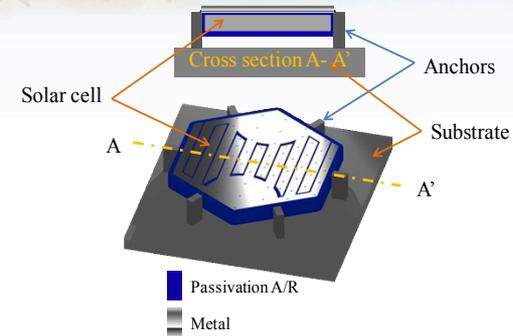
- Small IC Fab: 5,000 8" wafers/week
(@30 wfr/hr, IC industry standard = 60 wfr/hr)
- 10 pick-and-place tools: 130,000 parts/hr
- 2,900 m² PV modules produced per day
(0.7 acres)
- 200W x 2,900 = 0.58 MW_p/day

Scalability > 100GWp/year

US generation capacity ~1TW



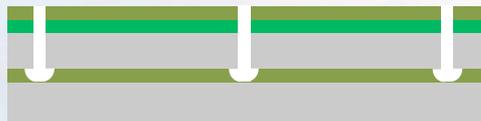
Solar Cell Fabrication: Suspended Cells



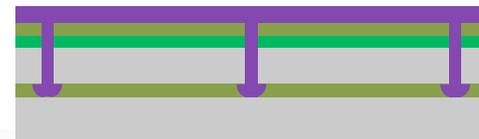
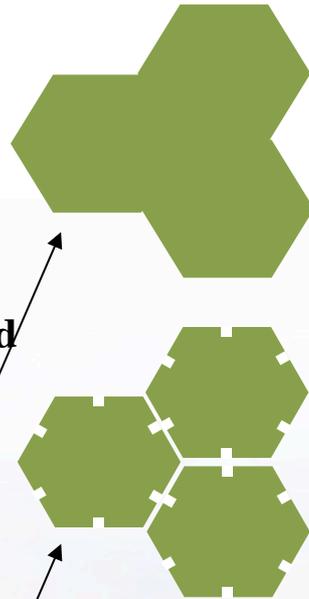
A) SOI cell with nitride and oxide



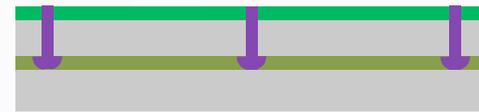
B) First deep etch reaching the BOX layer



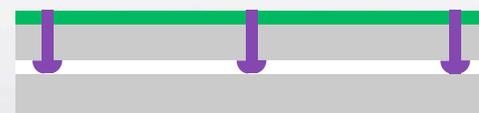
C) wet etch to reach the handle wafer



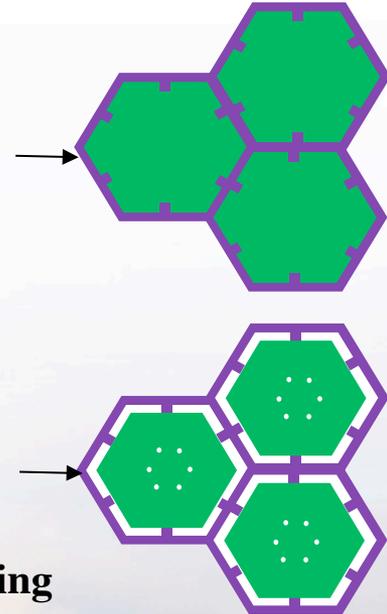
D) polysilicon fill



E) Chemical mechanical polishing

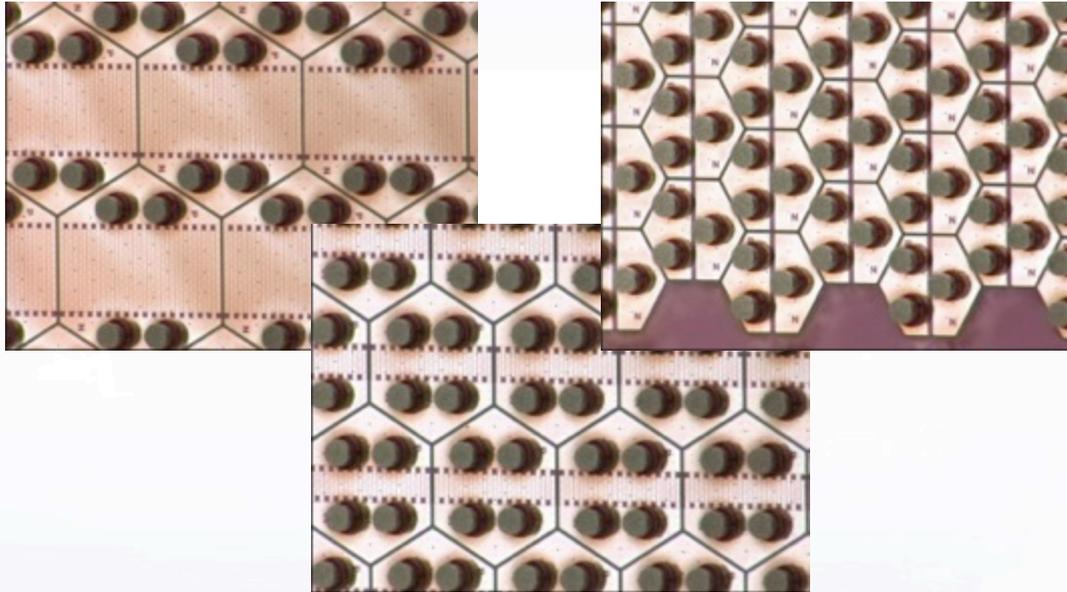


F) Second deep etch defining the cell and 2nd wet etch to suspend the cell



Assembly

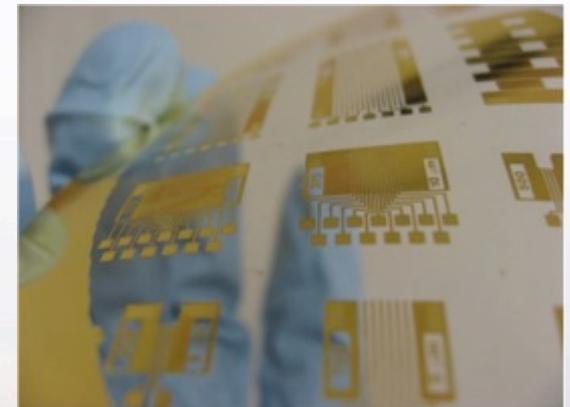
copper/solder bumps



flex receiver substrate (with cells)



pick-and-place (Universal Instruments)

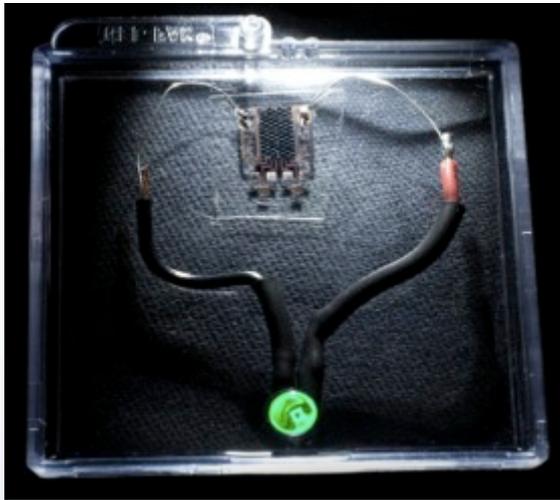


Corning® Willow™ Glass

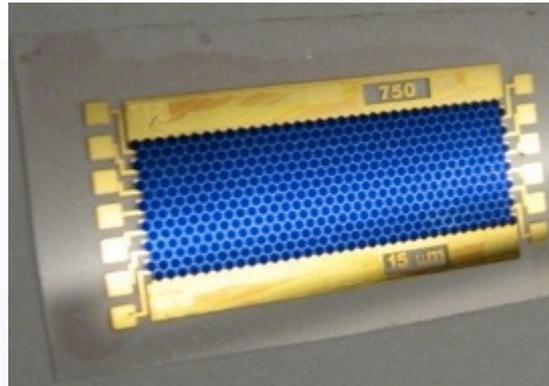


Prototype Examples

750um cell flexible prototypes on glass and polymer substrates



Corning® Willow™ Glass Substrate



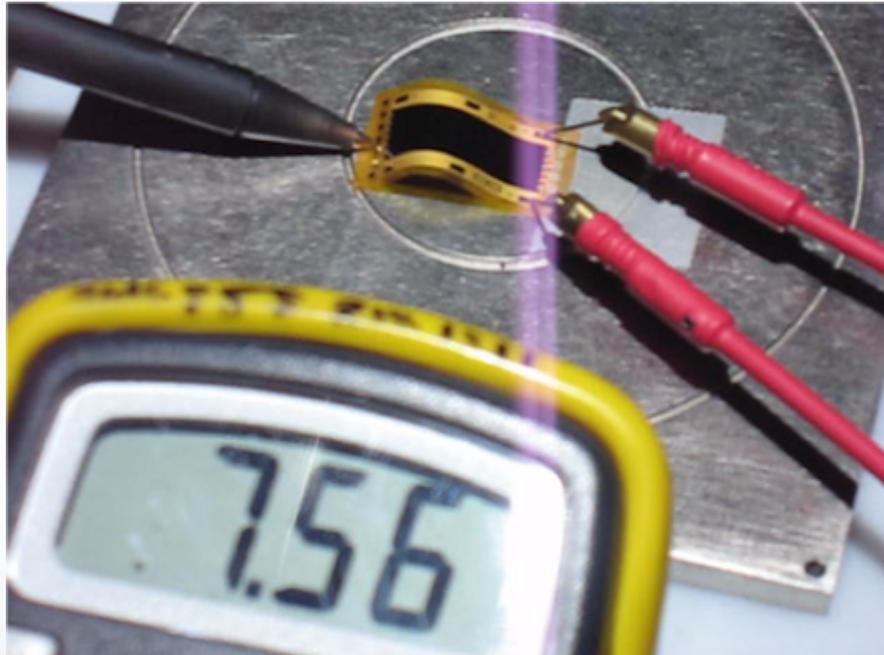
Polymer Substrate



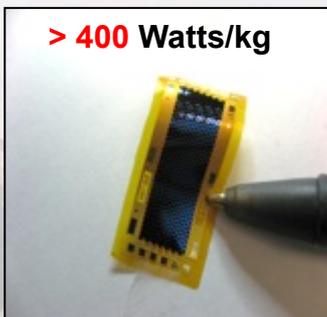
Prototype Examples

750um cell flexible prototype on polymer substrate

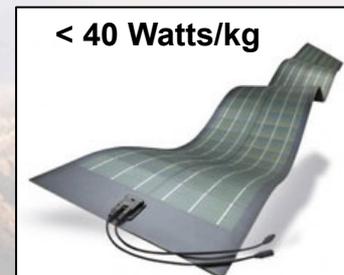
- Bend radius < 2mm without damage/ degradation.
- <100um as assembled.
- Demonstrated 14.9% array efficiency with single junction Si
 - >20% Si target
 - >35% multi-junction
- >1000 W/kg target (single junction).
- 10 kW array stowable into poster tube (“kW-in-a-can”).
- 10s of W in a pencil dimension tube.



MEPV



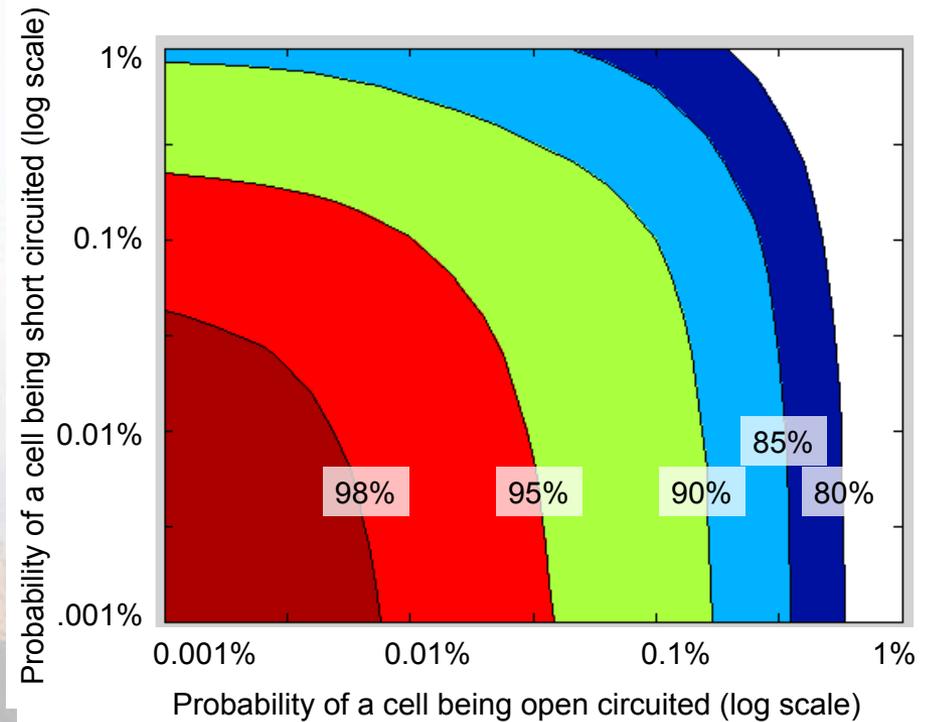
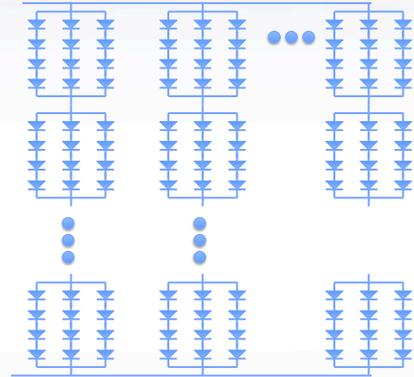
The Competition



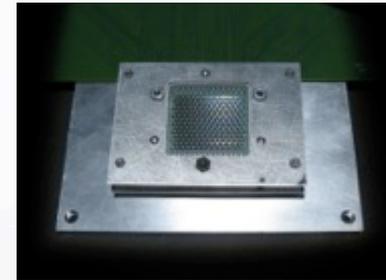
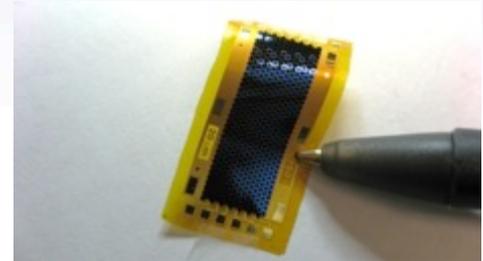
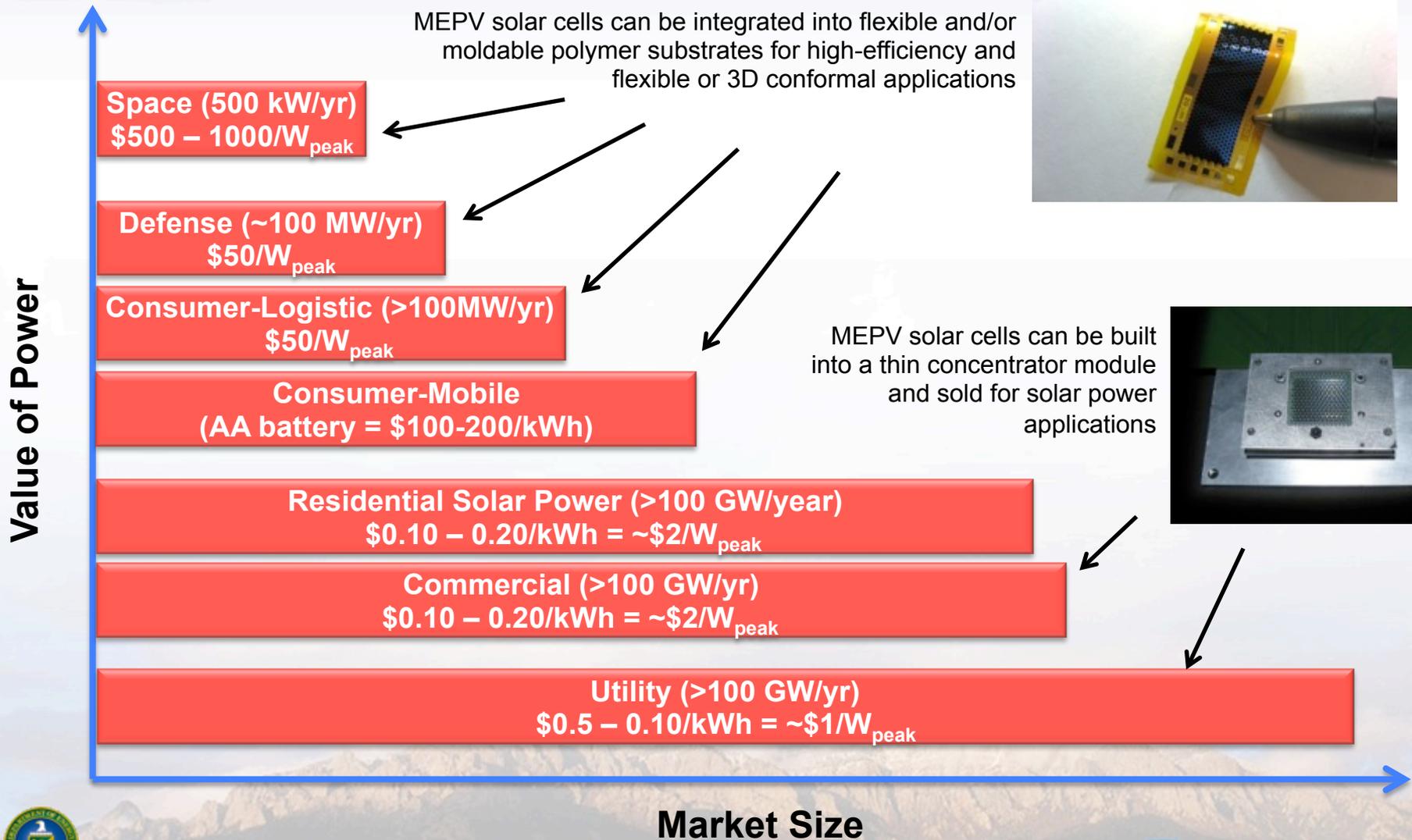
New Functionality

- Better performance in partial shading without the need for bypass protection diodes.
- Inherently robust (open/short, damage resistance).
- High-voltage DC (600 – 1000 V) in minimal footprint (5cm x 5cm).
- Integrated power management for on-the-fly optimization, voltage selection, state-of-health monitoring, logging.
- Reduced mechanical stresses and fatigue due to smaller cell/interconnect size.
- Integration of III-V layers/cells, independently connected junctions for highest performance possible.
- ...

With thousands of solar cells per square meter available, increasing levels of series-parallel-series-parallel connection networks of solar cells allow for improved performance (contour plot illustrates relative efficiency of module with different percentages of opens or shorts within the module).



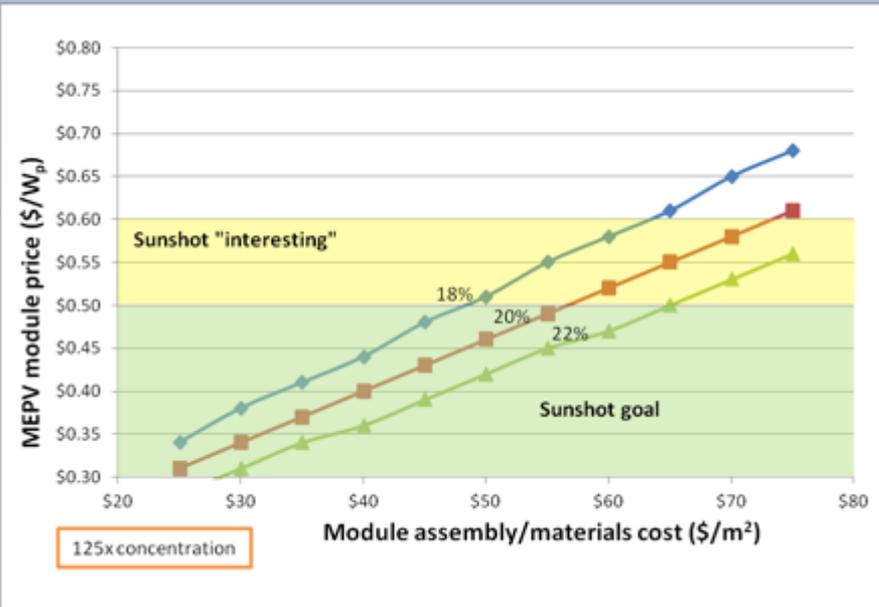
Broad Application: Power Markets



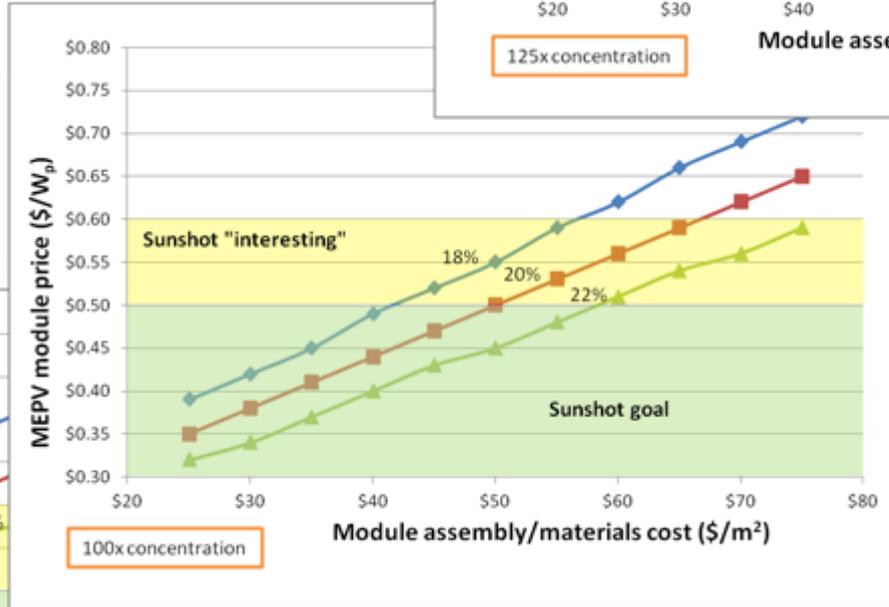
MEPV Cost Models

18% margin
200mm wafers

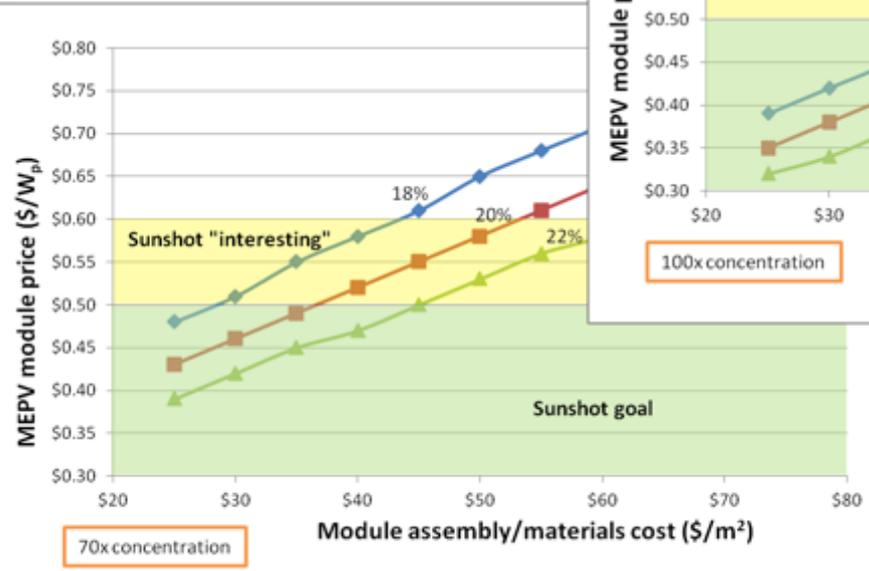
\$100/8" wafer
cell fab cost



125x



100x

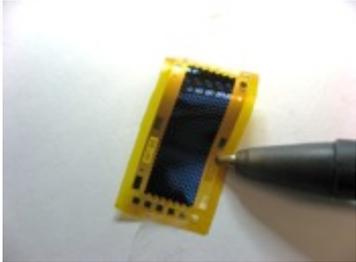


70x

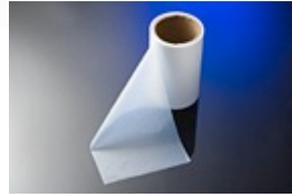
BOS costs are another $\$0.50/W_p$ –
MEPV approach has the potential to
reduce those costs as well (integrated
power management, easier install, cheaper
trackers, etc.)

Where will we be in 2 years?

Now



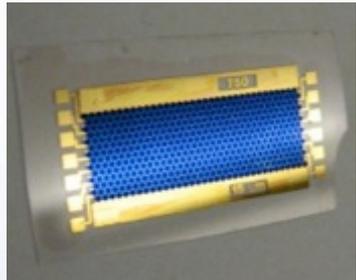
In 2 Years



Highly flexible prototype with 20% efficient, >1000 Watts/kg

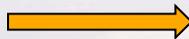
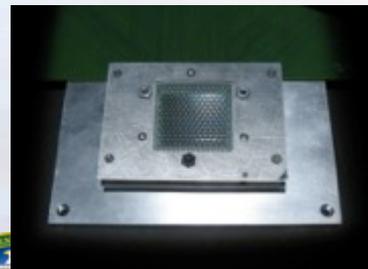
Next Steps

Identify defense systems integrators, for high margin, differentiated applications of MEPV in a flexible format



Small prototype integrated system for charging mobile devices

Identify electronics manufacturers for partnering opportunities, focused on mobile charging/energy harvesting applications. Requires either flexible or conformal MEPV capabilities with high-efficiency.



Low-Cost, High-Efficiency MEPV concentrator prototype

Continue working with solar companies: both supply chain and system integrators



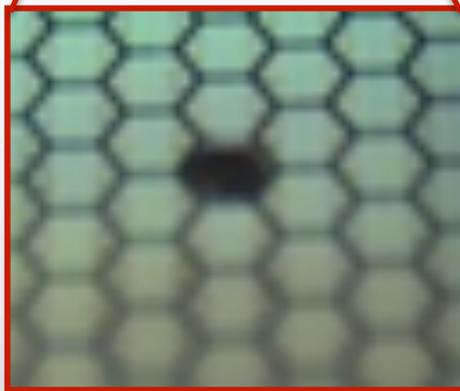
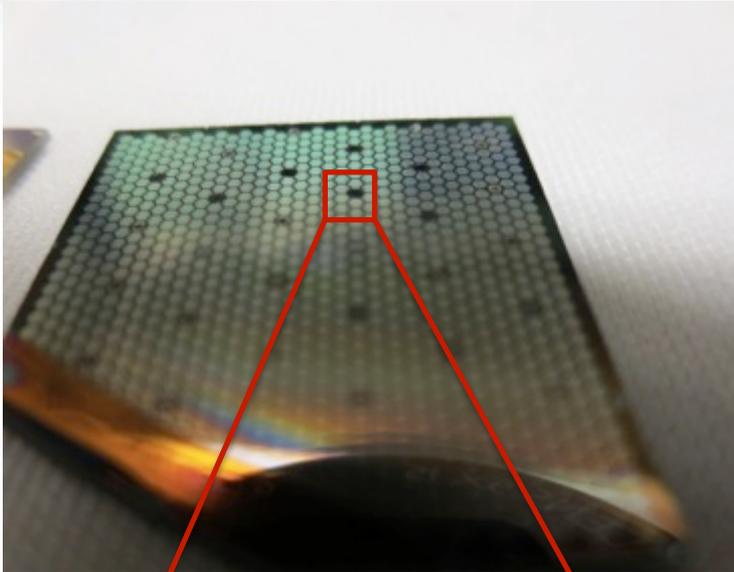


3DIC / Hybrid Integration

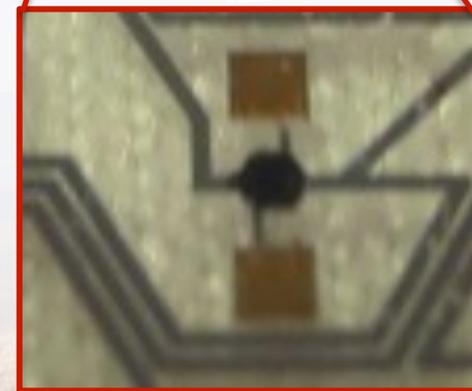
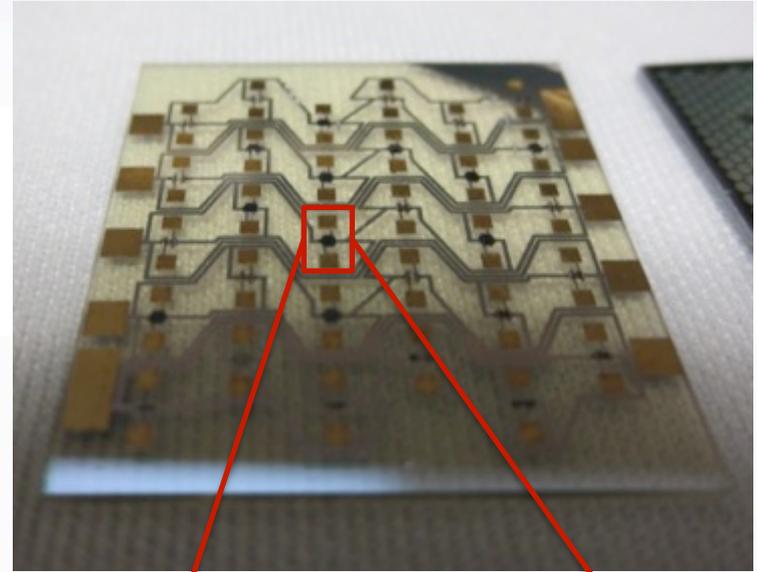
- Same technology base enables hybrid integration of dissimilar materials/processes with high throughput and high yield.
- Additional functionality integrated at chip or assembly level.
- Multiple assembly substrates possible.
- Current 3DIC approaches have significant issues with thin wafer handling, which is eliminated with this approach.



Sparse/Parallel Transfer



Donor Substrate with cells (ICs)



Receiver with cell transferred





Acknowledgements

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