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Failure Mechanisms in High Voltage Mylar Capacitors

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Abstract

Biaxially oriented polyethylene terephthalate (BO-PET/Mylar®) polymer film is commonly used as the dielectric in high-voltage, pulse-discharge capacitors because of its high dielectric strength and insulation resistance over a wide temperature range [1]. This study focuses on the use of a systematic physics of failure (PoF) approach to assess possible design and fabrication problems in BO-PET capacitors. A destructive physical analysis (DPA) procedure, which is an essential technique in understanding the failure modes and mechanisms in capacitors, has been developed through this research. Short-term breakdown (STB) testing was performed on capacitors from two independent development builds and the results are compared.

It was identified that the two primary failure mechanisms occurring in these capacitors under high voltage conditions were edge margin arc-over and dielectric punch-through. Evaluation of the electrical parameters after accelerated voltage testing revealed that the combination of lower than expected voltage breakdown values (near the voltage rating of 3.6 kV) and in-spec capacitance and dissipation factor (C/DF) values indicated an arc-over failure, while high voltage breakdown values (greater than 2.5 times the voltage rating) and out-of-spec C/DF values indicated a dielectric punch-through failure. Thick buried edges, creasing, high curvature, insufficient inactive wraps, arc spray, and inadequate edge margin were some of the modes that led to arc-over and punch-through failures. Many of these failure modes were traced back to unsuitably designed capacitors or issues with the process control during manufacturing.

Introduction

Construction of Dry Wrap and Fill Capacitors

Mylar is used as the dielectric in "dry wrap and fill" configurations. The term "dry wrap" is used because it refers to a solid dielectric, rather than liquid, where the dielectric system is comprised of air/Mylar windings, or "wraps." The ends of the capacitors are then "filled" or sealed with an encapsulating material, such as epoxy that is loaded with glass micro-balloons or mica.

The electrode configuration of these capacitors can be either extended foil or buried foil, each presenting distinct advantages and disadvantages. Extended foil capacitors provide lower electrical series resistance (ESR) and inductance (ESL), which can be useful for providing higher peak discharge currents. However, they have larger end margin requirements that call for more space in the system [2]. Increased energy density is associated with buried foil capacitors, due to the smaller end margins and hence lower volume; however, they have a higher ESR and ESL. The end margins are smaller in this design for two reasons: (i) the leads are insulated using the end potting, which electrically isolates the foils and, (ii) both foils are buried, which doubles the distance between them, in comparison to the foils in an extended foil design. The extended foil construction consists of the inner foil extending into the end margin toward one end termination, and the outer foil extending into the end margin toward the opposite end termination (*figure 1.a*). Electrical connection is achieved using solder or arc spray to connect a lead to the foils extending out of the dielectric. The buried foil construction conceals the foils between the width of the Mylar film. In this configuration, the electrical connection between the foil and leads is made through the use of one or more pairs of flag leads (tabs) that are inserted during the winding process at specific locations (*figure 1.b*).

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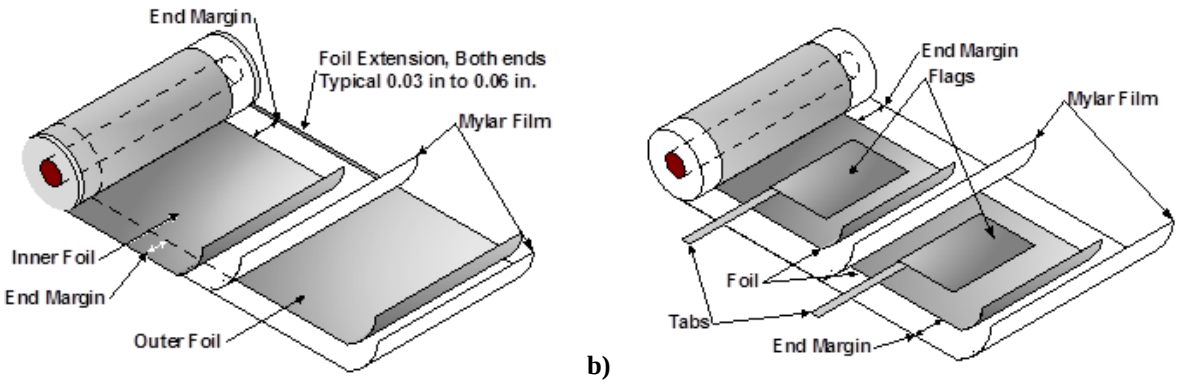


Figure 1. a) Diagram of extended foil configuration and b) diagram of buried foil configuration

Edwards [2] suggested that for dry wrap and fill capacitors used in high reliability applications, the voltage stress be limited in the margins to 4 kV/in and in the Mylar film dielectric to 2.5 kV/mil. Also, in order to keep the internal inductance low, buried foil capacitors should employ several pairs of tabs that are spaced at appropriate distances from each other.

Loescher and Sidnell [3] showed that placing opposite polarity tabs 180° apart in the winding, as was traditionally done [2], was the major source for internal inductance in buried foil capacitors because the optimal arrangement for low inductance was obtained by placing the positive and negative tabs very close to each other. Also, they determined that four to six pairs of tabs were most advantageous. Through their research, they were able to develop a capacitor that had low inductance, high voltage capabilities, and minimal volume requirements.

Destructive Physical Analysis

DPA is a procedure for the deconstruction and analysis of the capacitor after destructive testing. The process involves selecting, preparing, and unwinding the capacitors to identify and examine the failure locations. This serves as a check against major problems in the fabrication process and helps identify trends in manufacturing. Ultimately, this analysis captures the common failure modes and mechanisms and connects them to any related trends in the manufacturing/fabrication processes.

Experiment

Two development builds of extended foil capacitors rated to 3600 V were built, Build A and Build B. Both builds used similar but not identical designs and dielectric/foil stack-ups. The Mylar and foil were wound on solid mandrels, 0.5” diameter for Build A and 0.1” diameter for build B. The winding stack-ups in the active region consisted of three layers of Mylar film, one layer of 22 Gauge (G) (1 G is 0.01 mil) Al foil, three layers of Mylar film, and one layer of 22 G Al foil. Build A used 32 G Mylar films while Build B used 40 G Mylar films. As a rule, several wraps of either just Mylar or Mylar with a single layer of foil were initially wound around the mandrel. These layers are referred to as inactive or dead wraps, since the presence of both foil electrodes is required to create the active portion of the capacitor.

Two types of end terminations were used on these capacitors. Build A used solder-swage, and Build B used arc-spray. The type of solder used in the swaging process was Tin (Sn)-Zinc (Zn), and the process involved joining the electrodes that extended into the end termination together electrically by pressing them into the solder. The arc-spray material used was Babbit A, which consisted of 90% Sn, 7% Antimony (Sb), and 3% Copper (Cu). The arc-spray process involved the deposition of molten micrometer size droplets, for which the source of thermal energy was an electrical arc discharge. Lastly, polyester tape was placed around the exterior of the windings for protection on both builds.

DPA was performed on 40 capacitors from the two different development builds that had been subjected to STB testing. While both capacitor builds were rated to a voltage of 3.6 kV, they differed in end termination style, mandrel diameter, edge margin thickness, Mylar film thickness, and number of inactive wraps. Twenty capacitors from development Build A and twenty capacitors from development Build B underwent STB testing, which involved

exposure to a ramp rate of 250 V/s until a dielectric failure was detected. Failure was defined as a current draw greater than 5 mA (based on a voltage rating of 3.6 kV), which indicated a short circuit. STB measurements were made using an Associated Research, Inc. 7720 DC Withstand Voltage Tester in ambient conditions.

Table 1

	Build A	Build B
Type of Testing	STB	STB
DPA Number	20	20
End Termination	Solder Swage	Arc Spray
Mandrel Diameter (in)	0.5	0.1
Foil Configurations	Extended	Extended
Edge Margin Thickness (in)	0.28	0.218
Mylar Film Thickness (in)	0.00096 (3 x 32 G stack)	0.0012 (3 x 40 G stack)

After STB testing, the C, DF, and insulation resistance (IR) of each capacitor were measured at ambient temperature. From the parts that underwent STB testing, capacitors with the lowest and highest breakdown voltage values were selected for analysis.

Measurements made on these STB tested parts indicated that normal (in-spec) C and DF readings from the capacitance tester, along with a low STB voltage value, correlated with the arc-over failure mechanism during DPA. On the other hand, an overload reading from the C and DF measurements, coupled with a high STB voltage value, correlated with the dielectric punch-through failure mechanism. Therefore, any capacitor that had C/DF readings that measured overload and a low STB voltage value was considered an irregularity, and was selected for DPA. Since dielectric withstand voltage (DWV) screening (also called HiPot testing), which is the application of a voltage at or above the rated voltage, is considered a screening technique rather than a destructive test, any part that failed DWV was selected for DPA in order to better understand the cause of failure.

The DPA process involved first removing the outer layers of protective polyester tape to expose the inner windings and the end terminations. After removing the end termination using general lab tools, the capacitor was unwound. During the unwinding process, the sections were inspected for structural anomalies and carbon tracks. Structural anomalies included bumps, punctures, discoloration, etc. The failure sites were then documented and photographed.

Results of STB Testing

Edge margin arc-over and dielectric punch-through were the two primary failure mechanisms that occurred in these capacitors under high voltage conditions during STB testing. These failures created an electrical short between the conductive foils. Arcing occurs when air breaks down electrically and forms a pathway for the flow of electrons from one conductor to another, often resulting in visible flashes, flames and carbon charring. The pathway taken by the electrons from the negative foil to the positive foil is shown in *Figure 2.a*. The carbon traces left between the conductors increase the conductivity and provide a pathway for the continuous flow of current; however, this conduction path is not a short, so normal C and DF readings can still occur. Small irregularities/defects in either the foil or the Mylar cause electric field enhancements, which results in damage to the dielectric through the movement of normally bound charges and eventual dielectric breakdown, known as dielectric punch-through (*Figure 2.b*). Since this failure typically results in direct foil to foil contact at the failure site, overload readings are seen on the capacitance tester.

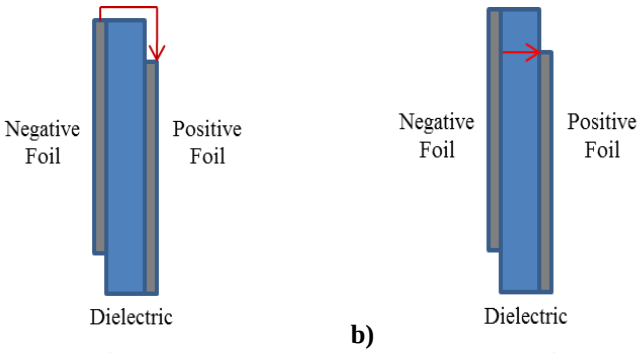


Figure 2. a) Arc-over failure diagram and b) dielectric punch-through failure mechanism

Creasing and Alignment with Thick Buried Foil Edges

Of the twenty Build A units that underwent STB testing, eighteen units failed due to edge margin arc-over and the remaining two units failed due to dielectric punch-through. However, all of the failures aligned with either a crease in the foil or a thick buried foil edge. The average edge margin arc-over failure voltage of these particular capacitors was 7.5 kV and the average dielectric punch-through failure voltage was 9.7 kV. Of the twenty Build A units that underwent STB testing, thirteen units failed due to edge margin arc-over and the remaining seven units failed due to dielectric punch-through. The average edge margin arc-over failure voltage of these particular capacitors was 4.6 kV and the average dielectric punch-through failure voltage was 6.6 kV. No failures in the capacitors from Build B were due to creasing in the windings or alignment with thick buried edges. A summary of the results from STB testing is given in *Table 2*.

Significant creasing was observed to occur in both of the electrode foils in every capacitor from Build A. This creasing had two different signatures. The first form of creasing observed appeared to have been introduced during the manufacturer's winding process. These creases were more substantial nearest the mandrel, where the windings were initially fed by hand into the winding machine. It is possible that improper tensioning during the winding process, indicative of insufficient process control, caused the occurrence of this creasing. *Figure 3* is an example of windings that appear to have bunched near the center of the mandrel, resulting in significant creasing that radiated and affected many layers. Edge margin arc-over failure occurred in this location along a crease.

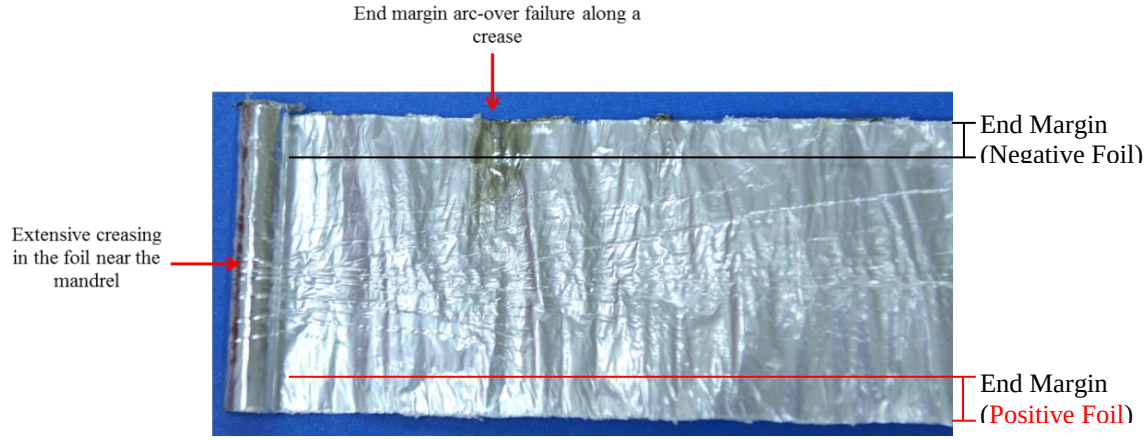


Figure 3. Creasing in the foil that led to edge margin arc-over

Figure 4 is a closer image of edge margin arc-over that occurred along one of the creases in the foil near the mandrel. Notice the physical evidence of arc-over, indicated by the carbon tracks extending to the edge of the foil and vaporized foil.

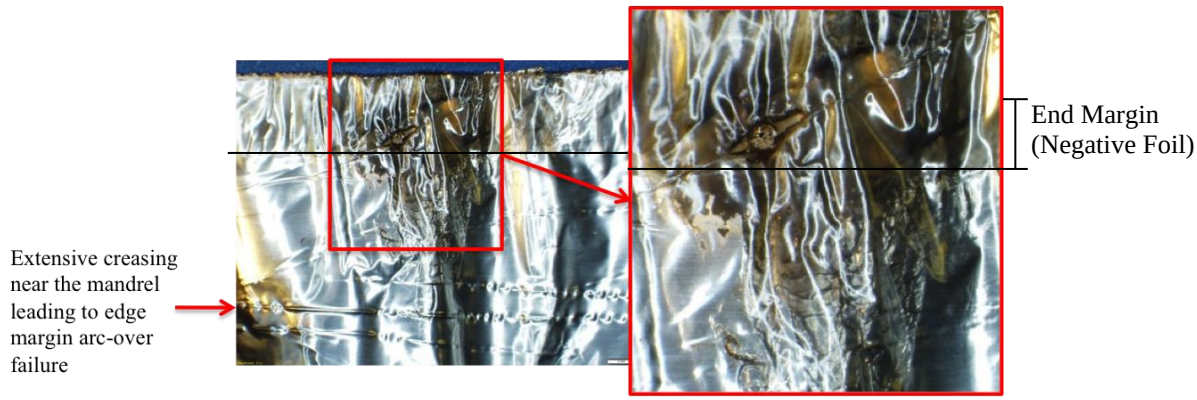


Figure 4. Crease-induced arc-over failure

Figure 5 is an image of a dielectric punch-through failure that occurred along one of the creases formed during the winding process.

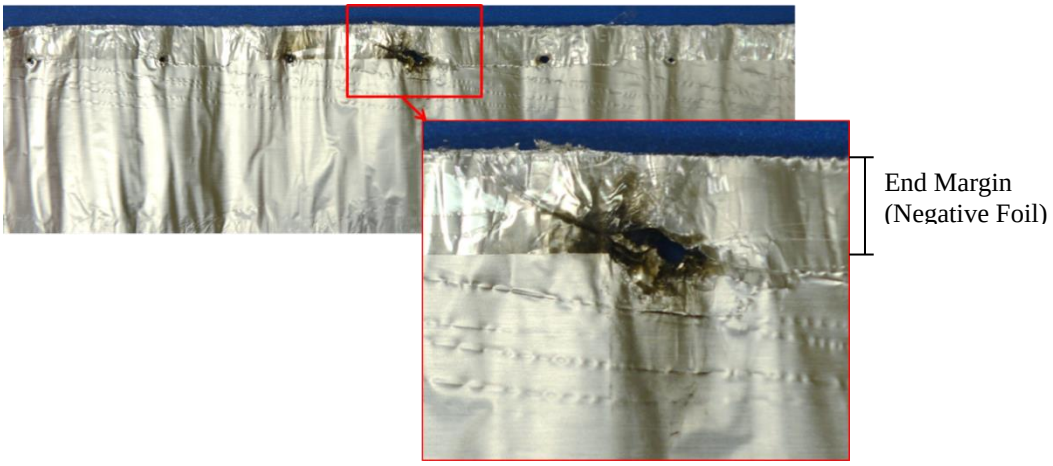


Figure 5. Crease-induced punch-through failure

Figure 6 is another example of the type of creasing that can occur due to improper tensioning during winding. Rather than creasing along the length of the windings (horizontally) as shown above, these creases run parallel to the short side of the stack (vertically).

Figure 6. Creasing due to insufficient process control (improper tensioning)

The second form of creasing was created due to thick buried edges, which we describe below. Various styles for initiating the winding around the mandrel were found to create thick buried edges and creases that affected the performance of the capacitors. Three different styles for initiating the winding within the same lot were identified for capacitors from Build A.

The first winding style consisted of a single layer of Mylar film that wrapped once around the bare mandrel, while the remaining five layers of Mylar and a single layer of Al foil were folded-over and tucked against the mandrel, creating a thick buried edge. Although each capacitor wrapped in this fashion had an average of 6.5 inactive wraps, the thick buried edge (a total of ten film layers and two foil layers) created a crease that affected as many as thirty windings. In this winding style, the inactive wraps contained a single foil, varying randomly between high voltage and ground. *Figure 7* shows the construction of the first winding style and the signature crease that is formed by a thick buried edge.

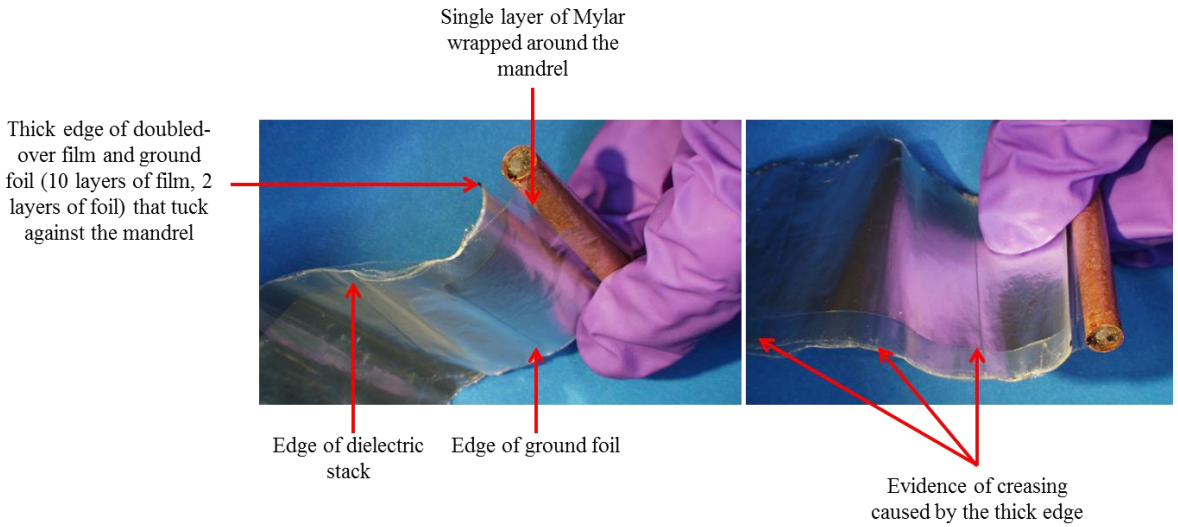


Figure 7. Construction of the first winding style

It was found that the crease created by the thick buried edge led to edge margin arc-over in several cases. *Figure 8* shows the pattern of creasing in the initial single-foil inactive area windings created by the thick buried edge. Notice that edge margin arc-over occurred along the crease at the onset of the active area.

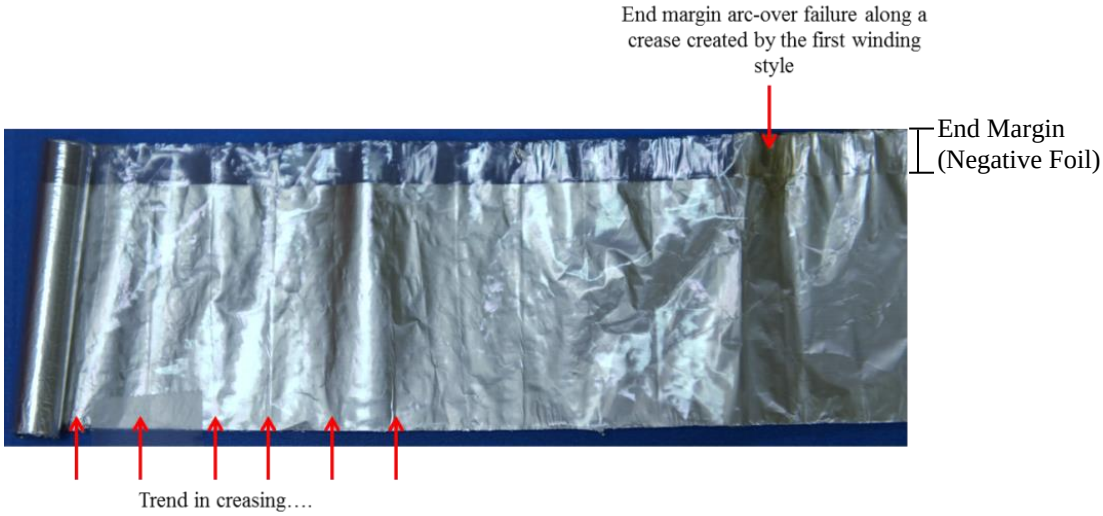


Figure 8. Creasing from thick buried edge created by the first winding style

The second winding style construction consisted of doubling over the dielectric and foil stack and aligning it directly against the bare mandrel. Similar to the first winding style, this doubled stack created twelve layers of film and two layers of foil that resulted in a thick buried edge. However, a second buried edge was created beneath the inactive-wraps by the remaining portion of the film/foil stack that folded over. The second foil was introduced after an average of 6.5 single-foil inactive wraps. *Figure 9* shows the construction of the second winding style. Several instances of edge margin arc-over were discovered to occur along the creases created by both the primary and secondary thick buried edges.

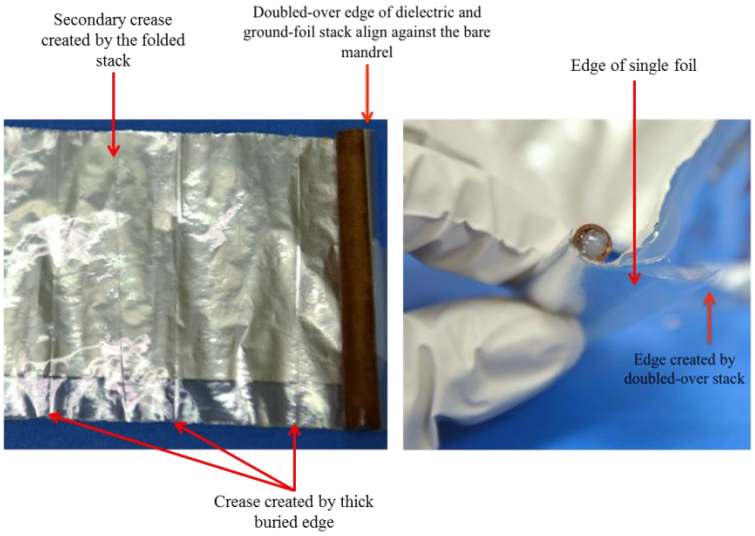


Figure 9. Second winding style

The third winding style construction consisted of the dielectric stack and a single foil wrapping around the mandrel in a "sling" fashion (*Figure 10*). This design configuration did not include any inactive wraps. Instead, the second foil was introduced directly into the folded crease against the mandrel. Therefore, in this active region, only two layers of Mylar dielectric separated the high voltage electrode from the ground electrode. Also, a thick buried edge was created against the mandrel, and in the location where the doubled stack (six layers of film and two layers of foil) ended. Every STB tested capacitor in this design failed due to edge margin arc-over that occurred along one of the thick buried edges.

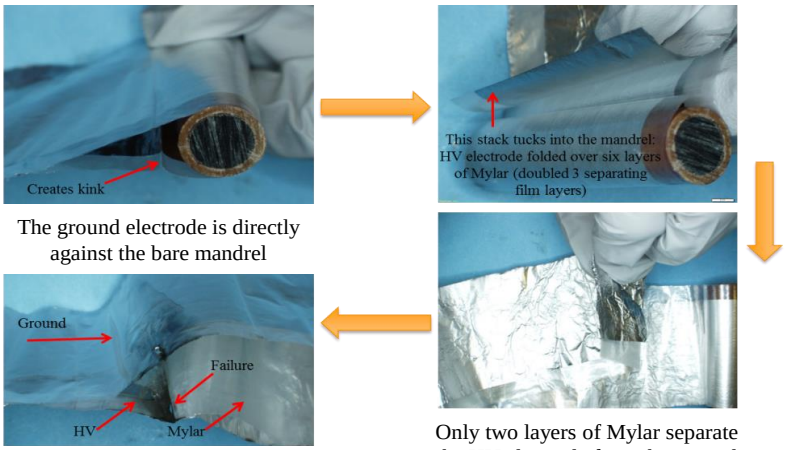
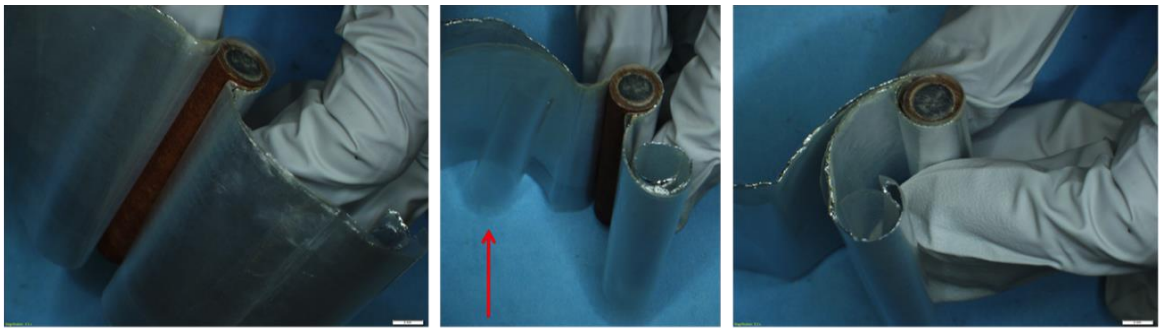


Figure 10. Third winding style

In a later lot that used the third winding style, eight inactive wraps were included. Again in this configuration, the dielectric stack and a single foil were positioned around the mandrel, creating a sling. The mandrel and stack were then wound together and the second foil was introduced after eight windings. A slight crease was created in the windings due to the sharp fold against the mandrel, however, no arc-over or punch-through failures correlated with this crease. The addition of the inactive wraps to the third winding style increased the STB failure voltage by approximately 1 kV. Also, the number of dielectric punch-through failures increased, and the number of edge margin arc-over failures were minimized. The failures that occurred in the newer design were randomly located throughout the windings. This is an improvement from the older lot, where the majority of failures were due to arc-over that occurred along the thick buried edges. *Figure 11* shows the construction of the redesigned third winding style.



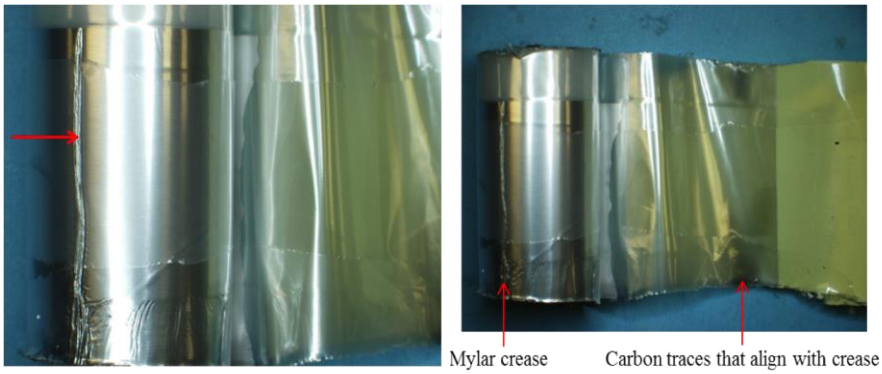
Sling-style wrapping around the mandrel similar to the third wrapping style

Mylar layer tucks into the mandrel before winding

Wound together

Figure 11. Redesigned third winding style

In some capacitors, creasing of the Mylar was detected. This creasing was correlated with failures due to edge margin arc-over (*Figure 12*).



Creasing in the Mylar

Carbon Traces Possibly from Crease-Induced Arc-Over

Figure 12. Creasing in the Mylar that led to arc-over

High Curvature

All STB tested capacitors from Build B failed due to edge margin arc-over and dielectric punch-through that occurred close to the mandrel. This development build used a split mandrel during the winding process, which was then removed and replaced with a 2.5 mm (0.1 in) diameter epoxy rod. The small diameter mandrel in these capacitors created a high curvature that increased the electric field strength in that location. Additionally, although no obvious issues were observed with the winding in this build, the failures could be correlating with the beginning of the winding. As a result, the average STB failure voltage was low, sometimes close to the rated voltage. *Figure*

13 shows this epoxy rod, as well as the windings around it and edge margin arc-over failure due to the increased electric field strength.

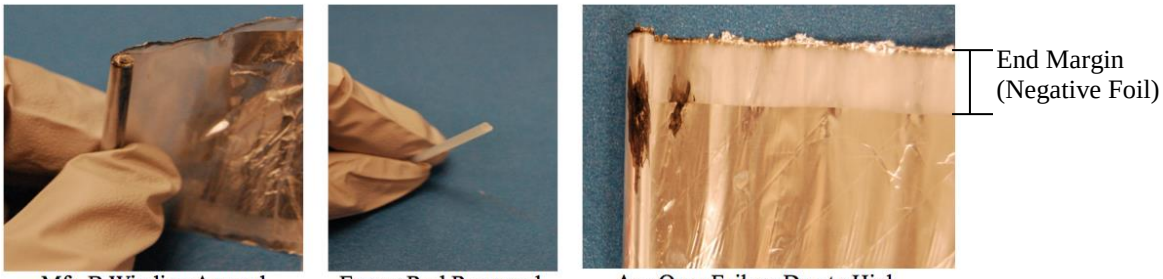


Figure 13. Epoxy mandrel rod used in Build B and the associated high curvature arc-over failure

Figure 14 shows an example of dielectric punch-through that occurred near the mandrel due to the high curvature.

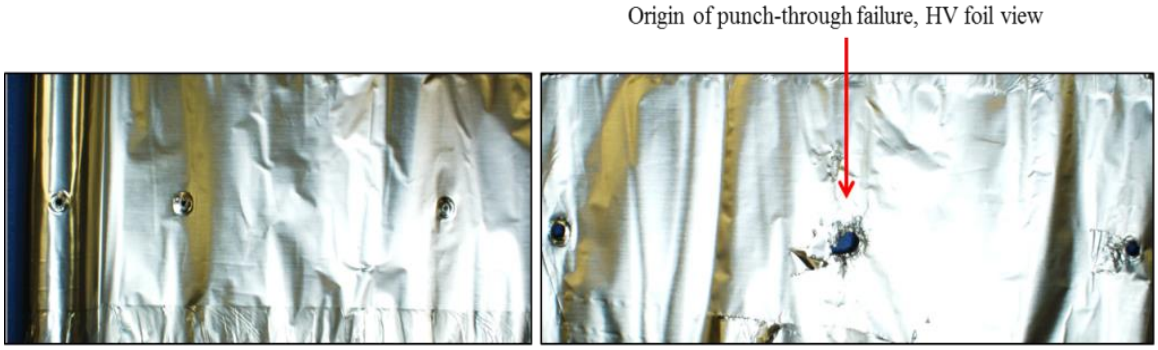


Figure 14. Dielectric punch-through failure induced by the high curvature

The capacitors from Build A were wound around a 0.5 in diameter mandrel. This helped to mitigate risks associated with increased electric field strengths due to the higher curvature.

Table 2: Summary of STB Testing Results

	Build A	Build B
Type of Testing	STB	STB
DPA Number	20	20
Average Arc-Over Voltage	7.5 kV	4.6 kV
Average Punch-Through Voltage	9.7 kV	6.6 kV

Discussion

The common failure mechanisms that occur in these capacitors under high voltage conditions are edge margin arc-over and dielectric punch-through. The failure modes found to lead to these failure mechanisms include high curvature, insufficient inactive wraps, inadequate edge margin, arc spray, and topographical irregularities such as film/foil edges, creases in the winding, tab leads and impressions. The manufacturer's selection of Mylar edge margin and film thickness, mandrel diameter, and winding process play a major role in dictating the reliability and performance of the capacitor.

Locally enhanced electric fields in the dielectric around topographical irregularities and defect sites cause arc-over and punch-through failures. Carbon tracks that have a dendritic "tree-like" morphology are left behind by the extreme heat generated by the arc, and are useful during DPA as an indicator of the failure site and short-circuit path, since the carbon tracks are conductive and allow current to flow between the electrodes. The extreme heat

during arc-over can cause the Mylar to melt and adhere to the other layers of dielectric and foil, which may create a tear during unwinding that falsely appears as a punch-through failure. The two mechanisms can be differentiated by the amount of damage produced. Arc-over damage typically affects only a few windings of film and foil due to the lesser energy at smaller voltages and the less intense dissipation over the longer breakdown path, whereas the hole and carbon charring created by punch-through can span many windings (see *figures 5* and *14*) and in certain cases create a hole or impression in the outer layer of protective polyester tape. The origin of dielectric punch-through failure is usually indicated by the greatest accumulation of damage, denoted by the site with the most significant amount of dielectric destruction and carbon residue. The significance of the damage due to dielectric punch-through is dependent on the magnitude of stored energy at which breakdown occurs.

In an extended foil capacitor, arc-over and punch-through failures will typically occur in the edge margin near the mandrel, especially in the presence of a crease or other topographical irregularity. This is because higher charge and field concentrations are generated near the foil edges and in the windings closer to the mandrel, due to the higher curvature. Coupling these factors with a topographical irregularity will usually determine the failure site. In a buried foil capacitor, the tab lead creates an irregular surface that distorts the electric field and increases its strength. Arc-over and dielectric punch-through commonly occur at the position where the tab lead crosses the edge margin in these types of capacitors.

The combination of low voltage breakdown values (near the voltage rating of 3.6 kV) and in-spec C/DF values indicate an arc-over failure. This stems from topographical irregularities creating strong concentrated electric fields from applied voltage levels that are not necessarily high, leading to electrical breakdown of the air at lower voltage breakdown values. The C/DF values remained in-spec because arcing occurs over the end margin, from one conductor to the other, and does not physically alter the Mylar or generate a short. On the other hand, high voltage breakdown values (greater than 2.5 times the voltage rating) and out-of-spec C/DF values indicated a dielectric punch-through failure. This is because a significant amount of energy, which correlates to a higher applied voltage, is dissipated in a concentrated area around an irregularity during dielectric punch-through. Since dielectric punch-through physically alters the Mylar and shorts the capacitor, the C and DF values change and result in an out-of-spec measurement reading.

During DPA of STB tested capacitors from Build A, significant creasing in the windings was observed that could be the result of insufficient process control during manufacturing, where there is too much tension on the Mylar, and too much compression on the foils. Creasing was more substantial nearest the mandrel because this was where the windings were initially placed (hand-fed) onto the mandrel before the automated winding process took control. Thick buried edges were also discovered to create creases in the windings. The severity of these buried edges varied with the winding style. Creasing in the capacitors from Build A, whether it was from insufficient process control or issues with the winding style, led to a high number of arc-over failures. In contrast, there was no creasing discovered in the capacitors from Build B, and a single consistent winding style was followed that did not create thick buried edges.

Three different winding styles were identified in the capacitors from Build A and connected to thick buried edges and creases that led to failure during STB testing. A redesign of the third winding style removed the thick buried edges from the configuration and replaced it with only a slight crease near the mandrel. Also, the redesign added inactive wraps to the configuration. The slight crease did not result in an obvious association with arc-over or punch-through failures, likely because the electric field strength was not affected significantly by this crease. The addition of eight layers of inactive wrap around the mandrel increased the diameter, reducing the electric field strength generated by the high curvature before introducing the active area. The redesigned third winding style showed that removing thick buried edges and adding inactive wraps increased the STB failure voltage by 1 kV, and shifted the failure mode towards dielectric punch-through failures. A capacitor design that fails more frequently by dielectric punch-through, rather than arc-over, is desirable because it indicates that the design is capable of handling higher levels of applied voltage. These traits denote a well-designed capacitor. The redesigned third winding style also caused randomness in the failure location, as opposed to the older design where every failure occurred in the location of the crease or thick buried edge. Randomness signifies that the location-dependent failure-causing design trend had been eliminated. Creasing that was likely caused by improper tensioning due to insufficient process

control was still observed in some of the capacitors wound with the redesigned third winding style. This creasing was correlated with arc-over and punch-through mechanisms.

The single winding process used by Build B was consistent in all of the capacitors and did not create creases or thick buried edges in the windings. However, the average STB failure voltage was still lower than that of Build A. Possible causes for this include Build B's use of an arc-sprayed end termination, a smaller end margin, and the small diameter (0.1 in) mandrel, which increases the electric field strength in the windings near the mandrel due to the high curvature. The arc-spray process can unintentionally deposit particles onto the film/foil edge margin in the active portion of the capacitor, locally enhancing the electric field strength and leading to failure. The heightened electric field strength and the enhanced possibility for arc-spray particle deposition in regions with high curvature are consistent with the fact that all STB tested capacitors from Build B failed due to arc-over or punch-through near the mandrel. This provides some perspective regarding the severity ranking of different failure modes: smaller end margins with a high curvature coupled with arc-sprayed particles in the active area of the windings cause failure at lower voltages than creasing or thick buried edges.

According to Edwards [2], the voltage stress in the edge margin should be limited to 4 kV/in and in the Mylar film dielectric to 2.5 kV/mil for high reliability applications, i.e., those that must be resilient to defects inherent in typical manufacturing processes. These capacitors have a voltage rating of 3.6 kV, meaning that the thickness of the edge margin should be at least 0.9 inches for high reliability at the rated voltage. However, the capacitors from Build A had an edge margin thickness of just 0.28 inches, resulting in an average voltage stress of 12.8 kV/in. While much less than the typical dielectric strength of air (75 kV/in), such an average voltage stress does not lead to a capacitor that is resilient to manufacturing defects such as creases in the electrode foils. Arc-over failures were thus sometimes observed to occur at voltages only slightly higher than the rated voltage where such creases were present. Furthermore, the thickness of the Mylar film used in Build A was 0.96 mil. For a capacitor rated at 3.6 kV, this leads to an average dielectric stress of 3.75 kV/mil. While much less than the advertised dielectric strength of 11 kV/mil for Mylar C [1], such an average dielectric stress does not lead to a defect-resilient capacitor as discussed above. This can lead to dielectric breakdown and result in punch-through failures at voltages below the desired multiplier over the rated voltage. The edge margin thickness of Build B capacitors was 0.218 inches, leading to a voltage stress of 16.5 kV/in, which is even higher than Build A and may be the critical factor leading to the lower voltage failures. The dielectric thickness was 1.20 mil with an average dielectric stress of 3 kV/mil, which is lower than that for Build A.

Three main failure locations were identified: (i) arc-over at the end margin, (ii) dielectric punch-through at the foil edge, and (iii) dielectric punch-through in the body of the capacitor windings. Edge margin arc-over signifies an end margin that is inadequate given topographies that may occur on the electrode edges. Dielectric punch-through, on the other hand, signifies that a high electric field was necessary to cause failure. However, punch-through in the body of the capacitor windings, where no field enhancement is expected, indicates that a weak spot was present in the dielectric. Therefore, the preferred failure mode in these capacitors is dielectric punch-through that occurs at the foil edge where the electric field strength is expected to be the highest [3], because this would result in higher breakdown values and would give credibility to our belief that the conditions that lead to failure are well defined.

Conclusions

1. DPA during the developmental stage is essential to determining which manufacturing method to use and identifying trends in the fabrication and manufacturing process that affect the reliability of the capacitor.
2. Evaluation of the electrical parameters after accelerated voltage testing revealed that the combination of low voltage breakdown values and in-spec C/DF readings indicated an arc-over failure, while high voltage breakdown values (greater than 2.5 times the voltage rating) and out-of-spec C/DF readings indicated a dielectric punch-through failure.
3. In extended foil capacitors, arc-over and punch-through typically occurred near the mandrel in the edge margin, where the electric field strength was increased due to the high curvature and topographical irregularities created by the edge, impressions, or creases in the winding. Based on prior work with buried foil capacitors, arc-over and punch-through typically occur near the tab leads, due to this topographical

irregularity distorting and increasing the electric field strength. In every case, carbon tracks indicated the blast site of punch-through and the path of arc-over.

4. Heat can cause the Mylar to melt and adhere to the other layers of dielectric and foil, which may create a tear during unwinding that falsely, appears as a punch-through failure.
5. Arc-over damage typically affects only a few windings of film and foil, whereas many windings (possibly the entire capacitor) are affected by dielectric punch-through.
6. Build A's redesigned third winding style with inactive wraps outperformed the first and second winding styles. This is because a thick buried edge was not created that resulted in creasing of the films and foils.
7. In a comparison between an older and newer lot of capacitors from Build A configured with the third winding style (without and with inactive wraps, respectively) it was found that the presence of inactive-wraps increased the breakdown voltage value by approximately 1 kV.
8. Capacitors from Build B are wound more uniformly (using an automated process, resulting in less creasing and more consistency) than Build A (using a manual process with various winding techniques resulting in extensive creasing), however, the smaller end margin and mandrel diameter, along with the arc-spray technique for Build B leads to a lower STB failure voltage than capacitors from Build A.
9. Capacitors with arc-sprayed end terminations in Build B may have unintentional deposition of particles onto the film/foil edge margin during the arc-spray process, locally enhancing the electric field strength and leading to failure. While this could be a cause for the lower voltage breakdown values, evidence of this was not observed in the DPA study and there are other factors such as end margin and mandrel diameter that could be the cause for the lower values.

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