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# A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation

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*Abstract* – **A new multilevel voltage-source inverter with separate dc sources is proposed for high-voltage, high-power applications, such as flexible ac transmission systems (FACTS) including static var generation (SVG), power line conditioning, series compensation, phase shifting, voltage balancing, fuel cell and photovoltaic utility systems interfacing, etc. The new M-level inverter consists of (M-1)/2 single phase full bridges in which each bridge has its own separate dc source. This inverter can generate almost sinusoidal waveform voltage with only one time switching per cycle as the number of levels increases. It can solve the problems of conventional transformer-based multipulse inverters and the problems of the multilevel diode-clamped inverter and the multilevel flying capacitor inverter. To demonstrate the superiority of the new inverter, a SVG system using the new inverter topology is discussed through analysis, simulation and experiment.**

## I. INTRODUCTION

### A. *Background*

With long-distance ac power transmission and load growth, active control of reactive power (var) is indispensable to stabilize the power systems and to maintain the supply voltage. Static Var Generators (SVGs) using voltage-source inverters have been widely accepted as the next generation reactive power controllers of power systems to replace the conventional var compensators, such as Thyristor Switched Capacitors (TSCs) and Thyristor Controlled Reactors (TCRs) [1–5].

Fig. 1 shows a typical 48-pulse inverter for static var generation applications. The 48-pulse inverter consists of eight 6-pulse inverters connected together through eight zigzag-connection or Wye/Delta and Delta/Delta connection transformers, in order to reduce harmonic distortion using the harmonic neutralization (cancellation) technique [1, 2]. These transformers, which are also called harmonic neutralizing magnetics,

(1) are the most expensive equipment in the system,
(2) produce about 50% of the total losses of the system,
(3) occupy up to 40% of the total system's real estate, which is an excessively large area,
(4) cause difficulties in control due to DC magnetizing and surge overvoltage problems resulting from saturation of the transformers in transient states.

To solve these problems, a diode-clamped multilevel inverter and a flying-capacitor multilevel inverter have been proposed for SVG applications [6, 7, 9, 12]. These multilevel inverters can eliminate the transformers required in an SVG using conventional 6-pulse inverters; however, they encounter new problems.

### B. *Multilevel Inverters and Their Problems*

In recent years, a relatively new type of inverters, multilevel voltage source inverters, has attracted many researchers' attention. Multilevel inverters can reach high voltage and reduce harmonics by their own structures without transformers, a benefit that many contributors have been trying to appropriate for high-voltage, high-power applications.

Fig. 2 shows the structure of a 5-level diode-clamped inverter. This inverter can reach high performance without transformers. It does, however, require additional clamping diodes. For this 5-level inverter, obviously, *D1*, *D2*, and *D3* need to block $1V_{dc}$, $2V_{dc}$, and $3V_{dc}$, respectively, assuming each dc capacitor has the same dc voltage, $V_{dc}$. When diodes are selected to have the same voltage rating as the main switching devices, *D2* and *D3* comprise two diodes in series and three diodes in series, respectively, to withstand the voltage. Therefore, the number of the additional clamping diodes is equal to (M–1)*(M–2)*3 for an M-level inverter. For example, if M=51 (for direct connection to 69 kV power

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lines) then the number of the clamping diodes will be 7350. These clamping diodes not only raise costs but also cause packaging problems and exhibit parasitic inductances; thus, the number of levels for a multilevel diode-clamped inverter may be limited to seven or nine in practical use [7, 12].

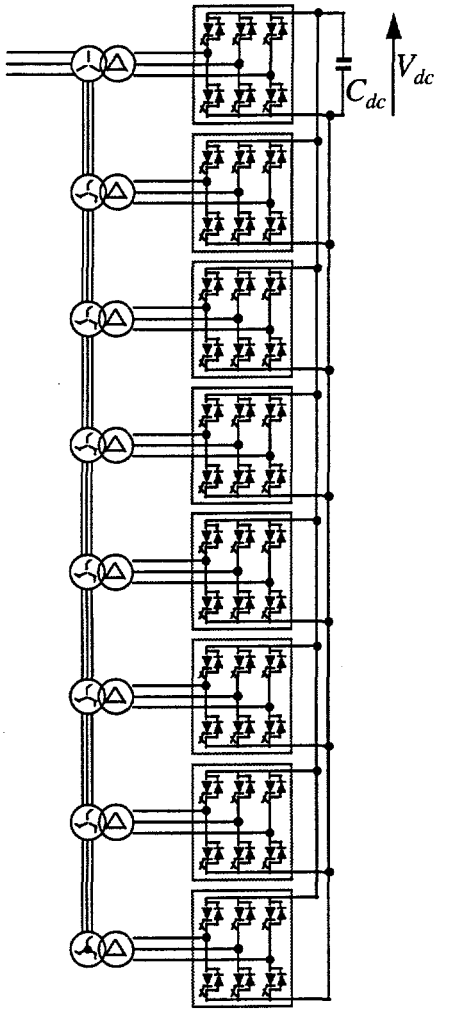



Fig. 1. Structure of the conventional 48-pulse inverter.

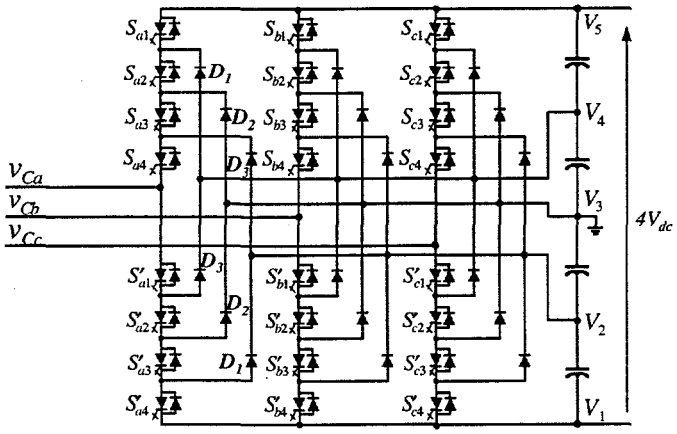



Fig. 2. Structure of the 5-level diode clamped inverter.

A relatively new structure, the multilevel flying-capacitor inverter [9], is supposed to be able to solve the voltage unbalance problem [7, 13] and excessive diode count in multilevel diode clamped inverters. Fig. 3 shows the configuration of a 5-level flying-capacitor inverter. In this inverter, however, a large number of flying capacitors are needed. The required number of flying capacitors for an M-level inverter, provided that the voltage rating of each capacitor used is the same as the main power switches, is determined by the formula, (M−1)*(M−2)*3/2+(M−1). With the assumption of the same capacitor voltage rating, an M-level diode clamped inverter only requires (M−1) capacitors. Therefore, the flying capacitor inverter requires large capacitance compared with the conventional inverter[9]. In addition, control is very complicated, and higher switching frequency is required to balance each capacitor voltage[13].

A new multilevel inverter is proposed to solve all these problems of the conventional multipulse and multilevel inverters. The new multilevel inverter eliminates the excessively large number of (1) bulky transformers required by conventional multipulse inverters, (2) clamping diodes required by multilevel diode-clamped inverters, and (3) flying capacitors required by multilevel flying-capacitor inverters. Also, it has the following features:

1. It is much more suitable to high-voltage, high-power applications than the conventional inverters.
2. It switches each device only once per line cycle and generates a multistep staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels.
3. Since the inverter structure itself consists of a cascade connection of many single-phase, full-bridge inverter (FBI) units and each bridge is fed with a separate DC source, it does not require voltage balance (sharing) circuits or voltage matching of the switching devices.
4. Packaging/layout is much easier because of the simplicity of structure and lower component count.

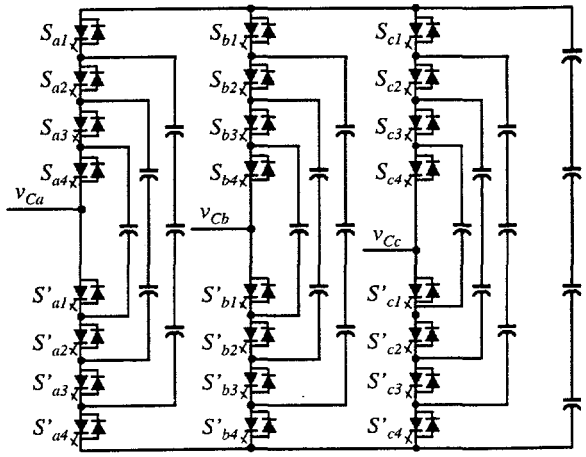



Fig. 3. Structure of the 5-level flying capacitor inverter.

## II. A New Multilevel Inverter

### A. *Inverter Structure and Operating Principle*

Fig. 4 shows the single-phase configuration of the proposed multilevel separate dc-source inverter. It consists of *(M-1)/2* single-phase FBI units connected in cascade to generate an *M* level output voltage over half fundamental cycle. Each full-bridge inverter has its own dc source. This new inverter, hereafter called a cascade inverter, does not require any transformers, clamping diodes, or flying capacitors, which are required in today's multilevel inverters.

Figs. 5 and 6 show three-phase structures of the proposed cascade inverter (level number *M=9*). Fig. 5 is used as an example to explain its operating principle. Fig. 7 shows waveforms generated by the 9-level cascade inverter shown in Fig. 5. The output phase voltage is the sum of four inverter units' outputs. That is, $v_{Can} = v_{Ca1} + v_{Ca2} + v_{Ca3} + v_{Ca4}$. Each FBI unit can generate three-level output, $+V_{dc}$, *0*, and $-V_{dc}$. This is made possible by connecting the dc-source sequentially to the ac side via the four switching devices. Note that each device is switched only once per line cycle.

Since the phase current, $i_{Ca}$ , is leading or lagging the phase voltage $v_{Can}$ by 90 degrees, the average charge to each dc capacitor is equal to zero over every half line cycle. From Fig. 7, the average charge to each dc capacitor over half cycle $[0, \pi]$, $Q_i$, can be expressed as

$$Q_i = \int_{\theta_i}^{\pi-\theta_i} \sqrt{2} I \cos\theta d\theta = 0 , \qquad (1)$$

where, $i = 1 \sim 4$; $[\theta_i, \pi-\theta_i]$ represents the time interval during which the dc capacitor connects to the ac side, and $I$ is the rms value of the line current. Because of this symmetric charge flow, voltages on all the dc capacitors remain theoretically balanced.

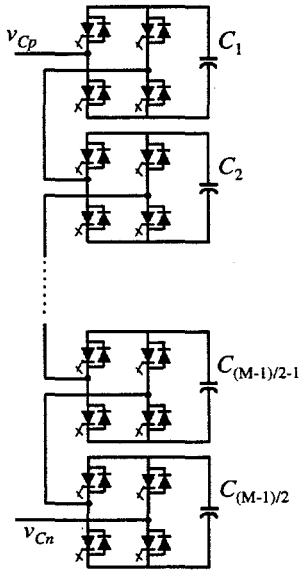



Fig. 4. Single phase structure of multilevel cascade inverter.

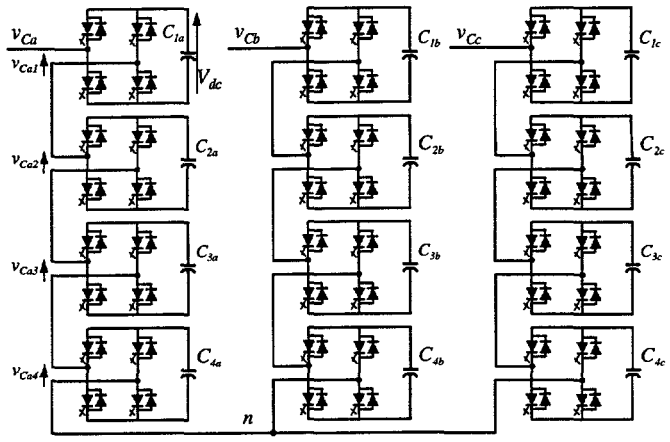



Fig. 5. Three phase Wye-connection structure of 9-level cascade inverter.

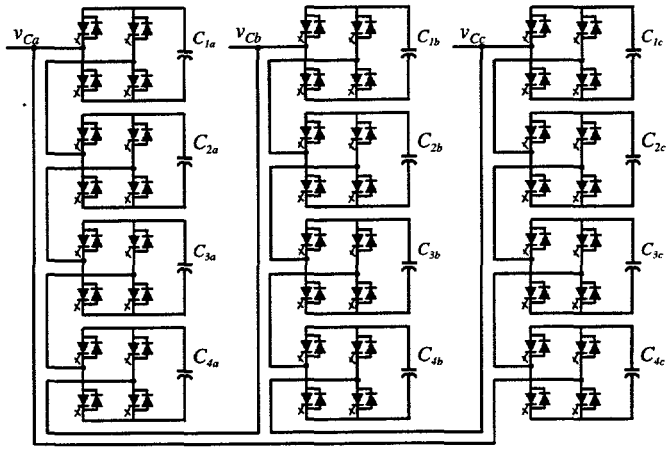



Fig. 6. Three phase Delta-connection structure of 9-level cascade inverter.

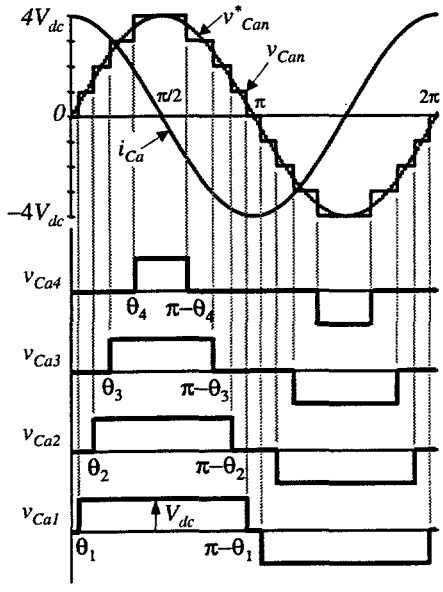



Fig. 7. Waveforms of the 9-level cascade inverter shown in Fig. 5.

### B. System Configuration and Control Scheme of SVGs

Fig. 8 shows the system configuration and control block diagram of an SVG using the new cascade inverter, where $v_S$ represents the source voltage, $L_S$ is the source impedance, and $L_C$ is the inverter interface inductance. The switching pattern table shown in Fig. 8 contains switching timings for the inverter to generate the desired output voltage as shown in Fig. 7. The switching angles, $\theta_i$ ($i$=1, 2, ···, $(M-1)/2$), are calculated off-line to minimize harmonics for each modulation index (MI), which is defined as $V_C^*/V_{Cmax}$, where $V_C^*$ is the amplitude command of the inverter output phase voltage, and $V_{Cmax}$ is the maximum obtainable amplitude, i.e., the amplitude of the phase voltage when all the switching angles, $\theta_i$, are equal to zero. As mentioned in Section II.A, the average charge on each dc capacitor will be zero if each FBI unit's output voltage, $v_{Ci}$, lags or leads the line current, $i_C$, by exactly 90 degrees as shown in Fig. 7, which means that no real power flows into the dc capacitor; however, with no power delivered to the dc capacitors, the dc capacitor voltage cannot be maintained due to switching device loss and capacitor loss. Therefore, the inverter should be controlled so that some real power is delivered to the dc capacitors. In principle, each dc capacitor voltage can be controlled to be exactly the dc command voltage, $V_{dc}^*$. The control block diagram shown in Fig. 8 includes two control loops. The outer loop controls the total power flow to all the FBI units, whereas the inner loop offsets power flow into each individual unit. The control principle can be explained with the aid of Fig. 9. In Fig. 9, $v_S$ is the source voltage, $i_C$ is the current flowing into the inverter, and $v_C$ is the inverter output voltage. If $v_C$ is controlled so that it lags $v_S$ by $\alpha_C$, then the total real power, $P_i$, flowing into the inverter is

$$P_i = \frac{V_S V_C \sin\alpha_C}{X_{Lc}}, \qquad (2)$$

where $X_{Lc}$ is the impedance of interface inductor. Since inverter devices are not ideal and have different tolerance errors, each dc capacitor voltage may not be exactly balanced with the outer loop only. If the $i$th FBI unit's output voltage, $v_{Ci}$, is as shown with the light wider line in Fig. 9, then the average charge into the dc capacitor over each half cycle, the area shown by the lighter shadow, will be almost zero. However, if $v_{Ci}$, is shifted ahead by $\Delta\alpha_{Ci}$ as shown by the darker line waveform in the figure, then the charge shown by the darker area can be expressed as

$$Q_i = \int_{\theta_i-\Delta\alpha_{Ci}}^{\pi-\theta_i-\Delta\alpha_{Ci}} \sqrt{2}I\cos\theta d\theta = 2\sqrt{2}I\cos\theta_i \sin\Delta\alpha_{Ci}, \qquad (3)$$

which is proportional to $\Delta\alpha_{Ci}$ when $\Delta\alpha_{Ci}$ is small. Therefore, each FBI unit's dc voltage can be controlled by slightly shifting the switching pattern. The magnitude of this shift is usually much smaller than $\alpha_C$. For high voltage high power applications, the total power loss of the inverter is typically less than 1%, thus $\Delta\alpha_{Ci} \ll \alpha_C < 0.01$ *rad.*

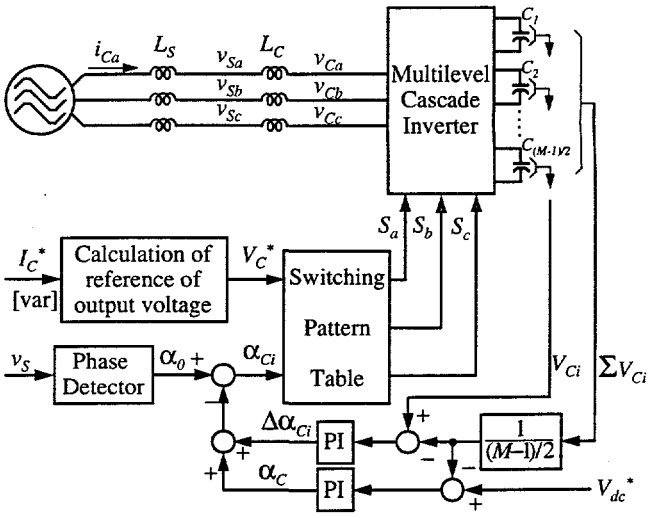



Fig. 8. System configuration of an SVG using the cascade inverter.

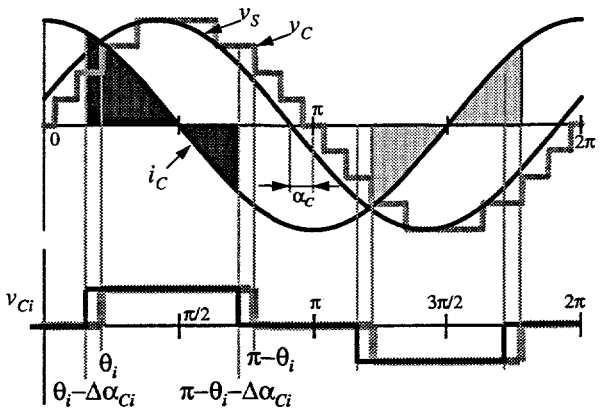



Fig. 9. Control principle of each dc capacitor voltage.

## III. Required Capacitance of DC Capacitors

The above description has shown that the proposed cascade inverter has the simplest structure and least components, compared with the conventional multipulse inverter, the diode-clamped multilevel inverter, and the flying capacitor multilevel inverter. However, the new inverter's capacitor requirements are higher than the conventional multipulse inverter and the diode-clamped multilevel inverter. Here, the required capacitance of the cascade inverter will be formulated and compared with that of the conventional multipulse inverter.

### A. For the Conventional Multipulse Inverters

It is generally required that an SVG has the capability to generate 100% negative-sequence var for unbalanced loads or in case of phase fault. Therefore, the required capacitance, $C_{dc}$, of dc capacitors used in the conventional inverter shown in Fig. 1 should accommodate this generation of 100% negative-sequence var and can be expressed as

$$\frac{1}{2}C_{dc}(V_{DC\max}^2 - V_{DC\min}^2) = \int_0^{T/4} Q_{\text{var}} \sin 2\omega t dt, \quad (4)$$

or

$$C_{dc} = \frac{2Q_{\text{var}}}{\omega(V_{DC\max}^2 - V_{DC\min}^2)} = \frac{Q_{\text{var}}}{2\omega\varepsilon V_{DC}^2}, \quad (5)$$

where $V_{DCmax}$ and $V_{DCmin}$ represent the maximum and minimum values of dc voltage, respectively, $Q_{var}$ is the var rating, $T$ is the line period, and $\omega$ is the line frequency. $V_{DC}$ is the average dc voltage, $V_{DC}$=( $V_{DCmax}$ + $V_{DCmin}$)/2. $\varepsilon$ is the regulation factor of dc voltage, $\varepsilon$ =( $V_{DCmax}$ − $V_{DCmin}$)/(2$V_{DC}$). Therefore, given an allowable regulation factor $\varepsilon$, average dc voltage $V_{DC}$, and var rating $Q_{var}$, one can obtain the required capacitance, $C_{dc}$, from (5).

### *B. For the Cascade Inverters*

For the proposed cascade inverter, since each phase has its own separate dc capacitors, calculation of the required capacitance of each FBI unit's dc capacitor is straightforward and automatically covers both positive-sequence and negative-sequence reactive power. The required capacitance, $C_i$, can be formulated from Fig. 7 as

$$C_i = \frac{\Delta Q_i}{\Delta V_{dc}} = \frac{\int_{\theta_i(t)}^{T/4} \sqrt{2} I \cos\omega t dt}{2\varepsilon V_{dc}} = \frac{\sqrt{2} I(1-\sin\theta_i)}{2\omega\varepsilon V_{dc}}, \quad (6)$$

where $I$ is the current rating of the inverter ($I$=$I_{SVG}$ for the Wye structure, and $I$=$I_{SVG}/\sqrt{3}$ for the Delta structure, $I_{SVG}$ is the current rating of the SVG), and $\theta_i$ is the switching timing angle of FBI unit $i$ as shown in Fig. 7. Therefore, the total required capacitance for a three phase $M$-level inverter, $C$, is

$$C = 3\sum_{i=1}^{(M-1)/2} C_i. \quad (7)$$

As mentioned before, $\theta_i$ is calculated for each MI value. To generate $\pm Q_{var}$ reactive power, MI would change between $MI_{min}$ and $MI_{max}$, where the SVG produces $+Q_{var}$ at $MI$=$MI_{max}$ and produces $-Q_{var}$ for $MI$=$MI_{min}$. For $MI$=$MI_{max}$, $\theta_i$ becomes minimum, and for $MI$=$MI_{min}$, $\theta_i$ becomes maximum. Therefore, we can use $\theta_i|_{at\ MI=MImax}$ in (6) to calculate the required capacitance so that the dc voltage ripple will not be larger than the given regulation factor, $\varepsilon$, for all loads.

### *C. Comparison of the Required Capacitance*

Now, a comparison will be made between two example systems. An experimental prototype of Fig. 8 has been built to demonstrate the validity of the new inverter. This SVG system uses 5 FBI units per phase to form an 11-level Wye-connected cascade inverter. The system parameters are shown in Table I. The switching timing angles, $\theta_i$ ($i$=1, 2, ···, 5), are specially calculated to minimize harmonics (under 25th order) of voltage and stored in the switching pattern table of Fig. 8 as shown in Table II.

TABLE I
SYSTEM PARAMETERS OF EXPERIMENTAL PROTOTYPE

| | |
|---|---|
| Source Voltage Rating $V_S$ | 240 V |
| Var Rating $Q_{var}$ | ± 1 kvar |
| Current Rating $I$ | 2.4 A |
| DC Voltage $V_{dc}$ | 40 V |
| DC Voltage Regulation factor $\varepsilon$ | ± 5% |
| Interface Inductance $L_C$ | 20% (32 mH) |
| Source Impedance $L_S$ | 3% (0.03 *pu*) |
| Modulation Index [$MI_{min}$, $MI_{max}$] | [0.615, 0.915] |

TABLE II
SWITCHING PATTERN TABLE OF 11-LEVEL CASCADE INVERTER

| Modulation Index | Switching Timing Angles [rad.] | | | | |
|---|---|---|---|---|---|
| $MI$* | $\theta_1$ | $\theta_2$ | $\theta_3$ | $\theta_4$ | $\theta_5$ |
| 0.615 | 0.4353 | 0.7274 | 0.8795 | 1.0665 | 1.2655 |
| ... | ... | ... | ... | ... | ... |
| 0.915 | 0.0687 | 0.1595 | 0.3124 | 0.4978 | 0.7077 |

* The resolution of $MI$ equals to 0.01 in the experimental system.

Using the parameters of Tables I and II and (6) and(7), we get $C_1$=2.1 mF, $C_2$=1.89 mF, $C_3$=1.56 mF, $C_4$=1.18 mF, $C_5$=0.79 mF, and the total capacitance $C$=22.56 mF. For a comparable conventional multipulse inverter, the required capacitance is, $C_{dc}$=16.6 mF, according to (5). Therefore, the required capacitance of the 11-level cascade inverter is 1.36 times of that of the conventional multipulse inverter.

Actually, when the number of levels is increased for high-voltage applications, the required capacitance of the cascade inverter will approach that of the conventional multipulse inverter, that is, the ratio $C/C_{dc}$ will approach one as a limit. For example, consider an SVG system using the Delta structure of a 21-level (10 FBI units per phase) cascade inverter connected directly to a 13 kV power system. The SVG capacity is ± 50 Mvar. $I_{SVG}$=2.22 kA (the current rating of inverter, $I$=1.282 kA), $L_C$=3%, $MI$=[0.6385, 0.8054], $V_{dc}$=2 kV and $\varepsilon$=±5%=±0.05. At the rated load of +50 Mvar, [$\theta_1$, $\theta_2$, ···, $\theta_{10}$]=[0.0334, 0.1840, 0.2491, 0.3469, 0.4275, 0.5381, 0.6692, 0.8539, 0.9840, 1.1613] [rad.]. For this SVG system, the total required capacitance of dc capacitors can be calculated as $C$=370 mF. The required capacitance for a comparable conventional multipulse inverter will be $C_{dc}$=332 mF. Therefore, the ratio, $C/C_{dc}$, is 1.11, which is approaching 1.0 as stated.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

To demonstrate the validity of the new inverter, an SVG prototype using an 11-level Wye-connected cascade inverter was built. Fig. 8, Table I, and Table II show the system configuration and the corresponding parameters. For the dc voltage control loops, only $C_1$ and $C_5$'s voltages of phase 'a' are detected and controlled directly. The control of $C_2$, $C_3$, and $C_4$'s voltage uses interpolating values of $\Delta\alpha_{C1}$ and $\Delta\alpha_{C5}$.

Figs. 10 ~ 12 show experimental results when the SVG generates +1 kvar. Fig. 13 shows experimental results at zero var output. Figs. 14 and 15 show the case of −1 kvar output.

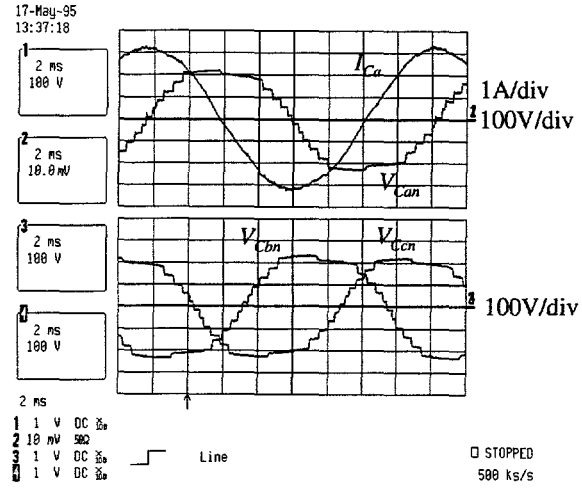



Fig. 10. Experimental results showing phase voltages of the inverter, $V_{Can}$, $V_{Cbn}$, and $V_{Ccn}$, and the line current, $I_{Ca}$, at +1 kvar output.

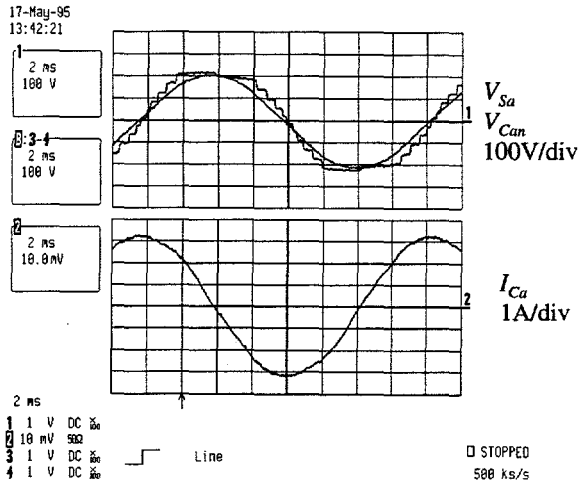



Fig. 11. Experimental results showing phase voltages of the source and the inverter, $V_{Sa}$, and $V_{Can}$, and the line current, $I_{Ca}$, at +1 kvar output.

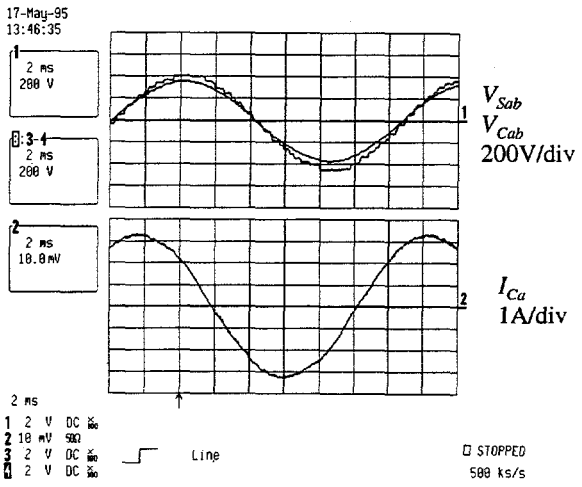



Fig. 12. Experimental results showing line-to-line voltages of the source and the inverter, $V_{Sab}$ and $V_{Cab}$, and the line current, $I_{Ca}$, at +1 kvar output.

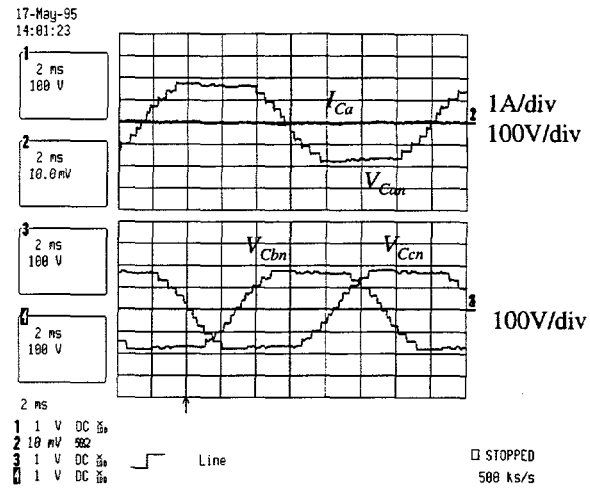



Fig. 13. Experimental results showing phase voltages of the inverter, $V_{Can}$, $V_{Cbn}$, and $V_{Ccn}$, and the line current, $I_{Ca}$, at zero var output.

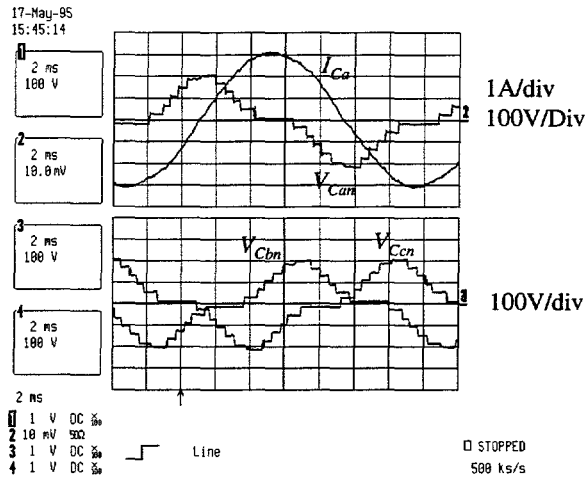



Fig. 14. Experimental results showing phase voltages of the inverter, $V_{Can}$, $V_{Cbn}$, and $V_{Ccn}$, and the line current, $I_{Ca}$, at −1 kvar output.

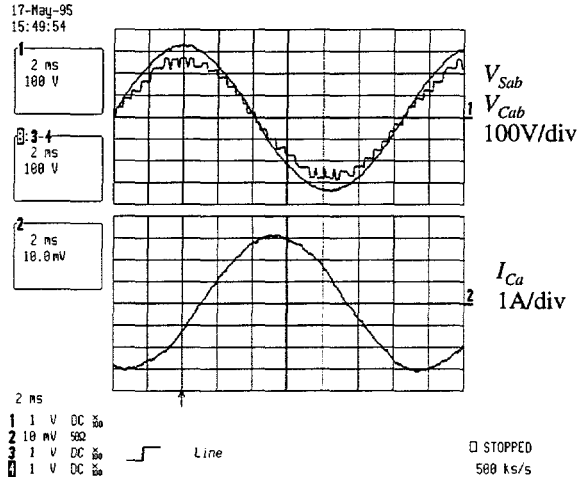



Fig. 15. Experimental results showing line-to-line voltages of the source and the inverter, $V_{Sab}$ and $V_{Cab}$, and the line current, $I_{Ca}$, at −1kvar output.

In the experimental system of Fig. 8, a Proportional and Integral (PI) controller was used for the dc voltage control loops. The PI gains of the controllers were $K_P$=0 and $K_I$=0.1 [rad./volt].

Figs. 10, 11, and 12 show that the inverter output phase voltage is an 11-level step-like waveform, and the line-to-line voltage is a 21-level step-like waveform over one half cycle. Each step has the same span, indicating that the voltage of each dc capacitor is well controlled and balanced. The command dc voltage, $V_{dc}^*$, was 40V, $\alpha_C$=0.08 [rad.], $\Delta\alpha_{C1}$=0.002 [rad.], $\Delta\alpha_{C5}$=–0.003 [rad.], and the modulation index was the maximum, *MI=0.915*, in this case.

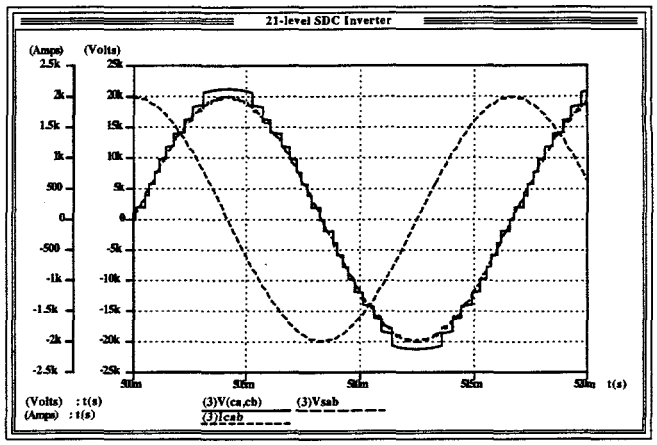
As is well-known, to regulate the output voltage one can simultaneously and independently control either the modulation index or the dc voltage. Fig. 13 shows the experimental waveforms that generate zero reactive power or zero current with the same modulation index as in Figs. 10, 11, and 12, but with a different dc voltage. In this case the dc voltage of each dc capacitor was controlled to be 34V, that is, $V_{dc}^*$=34 V. Lowering the dc voltage can reduce the inverter losses. However, a step change of the dc voltage is impossible. Therefore, the MI regulation is usually used to get a desired step change of the output voltage, whereas the dc voltage control is suitable for slow response to improve the inverter efficiency.

In Figs. 14 and 15, *MI* was *0.615*, and $V_{dc}^*$ was 40 V. The inverter generates −1kvar of reactive power, that is, the current, $I_{Ca}$, lags the voltage, $V_{Sa}$, by 90 degrees.

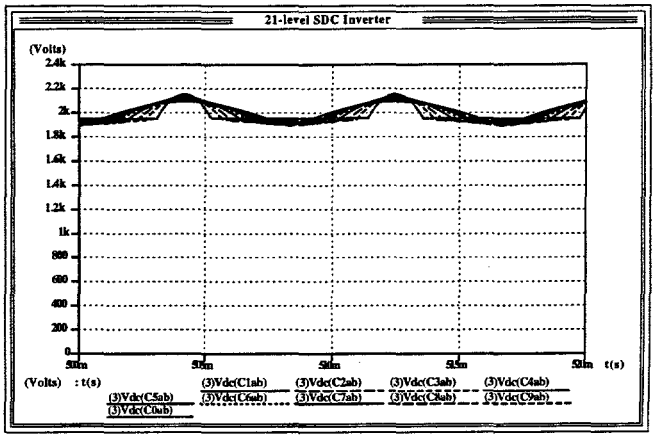
The above experimental results show that voltages of all the dc capacitors are well balanced even with only two sensed voltages, although each dc voltage can be independently controlled by detecting all the dc voltages. The results also show that a pure sinusoidal current can be obtained with only a total 23% (0.23 *pu*) impedance on the ac side.

From the structures of the multilevel cascade inverter, Figs. 4, 5, and 6, we can see that each phase can be controlled independently. Therefore, each phase of the inverter behaves just like an actively controlled inductance or capacitance as long as its voltage and current have a 90 degree phase difference. This feature makes it possible for the Delta structure of Fig. 6 to furnish both positive- and negative-sequence reactive power [14, 15], thus behaving like a controlled ideal source of reactive power. Negative-sequence reactive power is necessary for phase balancing and power-factor correction of unbalanced (unsymmetrical) loads.

Fig. 16 shows simulation results of an SVG, in which a 21-level Delta structure cascade inverter is used to connect directly to a 13 kV power line. The corresponding parameters have been mentioned in Section III.C. The capacitances for the ten FBI units' dc capacitors are [$C_1$, $C_2$, ···, $C_{10}$]=[23.2, 19.6, 18.1, 15.8, 14.0, 11.7, 9.11, 5.91, 4.01, 1.98]mF, respectively. In Fig. 16(a), *V(ca,cb)* is the output voltage of phase *ab* of the inverter. It shows a step-like waveform with 21 levels over a half cycle. It is seen that the current, *Icab*,




(a) Source voltage, inverter voltage, and inverter current




(b) Voltage of each dc capacitor of phase *ab*

Fig. 16. Simulation results of an SVG using a 21-level Delta-connected cascade inverter.

leads the phase voltage by 90 degrees and is purely sinusoidal, and the source voltage, *Vsab*, is almost distortion-free even with a small interface inductance ($L_S$=3.5%, $L_C$=3%). Fig. 16(b) shows waveforms of dc capacitor voltages of phase *ab*, where the voltages are maintained at a constant value, 2 kV, within ±5% ripples.

## V. CONCLUSIONS

A new multilevel voltage-source cascade inverter has been proposed. The new inverter has many features, including the least component count, as well as easy modularity and packaging, which solve the major problems of the conventional multipulse inverter, the diode-clamped multi-level inverter, and the flying capacitor multilevel inverter. The cascade inverter is specially suitable for FACTS

applications including static var generation, power line conditioning, series compensation, phase shift, and voltage balancing, because each dc capacitor voltage can be self-maintained and independently controlled without additional dc sources. The superiority and validity have been demonstrated through experimental and simulated results. It has also been shown that the required capacitance of dc capacitors is almost the same as that of the conventional inverter for practical SVG applications.

This cascade inverter topology can be easily adapted to other applications such as fuel cell and photovoltaic utility interface systems where the sources are originally isolated dc sources. For these niched applications, it is expected that the cascade inverter will become widespread.

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