Electromagnetic Isolation Solutions in Low Temperature Cofired Ceramic (LTCC)

Daniel Krueger[1*], Ken Peterson[2], and Laurie Euler[1]
[1]NNSA's Kansas City Plant, Kansas City, MO USA
*Phone: 816-997-2701 Email: dkrueger@kcp.com
[2]Sandia National Laboratories, Albuquerque, NM, USA,

Abstract

Low Temperature Cofired Ceramic (LTCC) is a commercial ceramic-glass multilayer technology with compelling advantages for microelectronics, microsystems and sensors. High frequency applications require good electrical properties such as low dielectric los,s and newer applications require extreme isolation from electromagnetic interference (EMI) that is even difficult to measure (-150db). Approaches to providing this isolation, once provided by via fences, have included sidewall coating and full tape thickness features (FTTF) that have been introduced by the filling of slots with via-fill compositions. Several techniques for creating these structures have been modeled for stress and temperature effects in the face of other necessary attachments, such as metallic seal frames. The relative effects of attachment media, FTTF geometry, and alternative measures will be reported. Approaches for thick film and thin film implementations are described.

Key Words: Low temperature cofired ceramic (LTCC), electromagnetic interference (EMI), micro-milling

I. Introduction

Low temperature cofired ceramic (LTCC) is a laminate technology based on unfired ('green') layers of ceramic-glass tape which are structured with screen-printed conductive traces, filled conductive z-axis vias, and a range of other components. The layers are collated, laminated, and cofired to yield a monolithic system. Because of the unique structural possibilities, LTCC has found a niche in non-microelectronics applications, microsystems, and sensors in addition to multichip modules (MCM). [1,2] Radio frequency (RF) MCMs benefit from low dielectric losses and high metal conductivities designed into these material systems. [3] An increasingly common way to build a multichip module is to use surface mounted components for miniaturization and function, and subsequently combine this partially assembled board with chip and wire hybrid techniques wherein RF integrated circuits (IC) are mounted and wire/ribbon bonded directly into the circuit. All of these components are typically enclosed inside a hermetic enclosure constructed in part with a metallic seal frame and lid as per industry practice. [4]

In RF MCMs, is the concern for the effects of electromagnetic interference (EMI) between individual sections of the module requires consideration. This has historically been provided by exotic techniques or external packaging such as discrete cans and shields. [5] The metallic seal frame is very useful to this endeavor, but additional structure is required in the LTCC. This has been accomplished in a variety of ways—most usually by rows of via fences which block line of sight radiation and mitigate interference. [6] In our experimental prototypes, better solutions are required, and we have worked with rows of slot vias, and ultimately with full tape-thickness feature (FTTF) solid walls in the LTCC. Sidewall coating is also feasible, and has been treated in literature. [7] Most recently, the older technique of green-state-machining, or micro-milling [8] has been developed for this purpose. These unusual structures could be expected to lead to mechanical integrity issues—especially when seal frames are mounted above them. These structures were modeled in order to sort out stress effects as affected by temperature.

Designers have been intrigued at this point with the isolation provided, so techniques for solid EMI structures persist. Certainly LTCC is a study in

discontinuities, every tape sheet having originally been separate. Furthermore, the common practice of punching and filling vias creates more potential mechanical discontinuities. Certainly, in view of structural interactions with strength and material parameters, such discontinuities must be stable. Were it not possible to 'heal' these discontinuities with sintering, LTCC would never have succeeded. Shown in Fig. 1, in a cross sectional view, are original discontinuities that routinely heal in common applications.

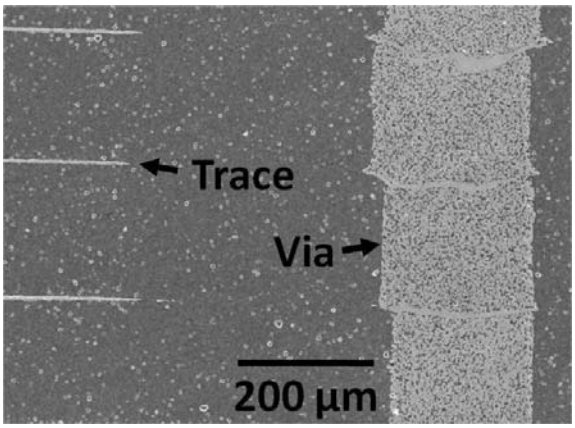

Figure 1. Discontinuities and potential stress concentration points that have healed by sintering.

II. Background

An MCM configuration of interest is commonly described in the literature. (e.g.,[9]) It consists of an LTCC body which incorporates critical functions with high conductivity metallization traces and vias. To this body, or substrate, are added : (i) a seal frame for hermetic enclosure of individual circuits, (ii) soldered discrete devices for miniaturization and circuit performance, (iii) chip-and-wire assembled devices and an assortment of other components, and (iv) a lid, which is seam-welded into place following a suitable bake and back-filling.

The LTCC substrate is a conventional multi-layer board fabricated using commercial tapes, pastes, and industry standard processing techniques, except for Faraday slot related processes. Vias are filled with a specified via-fill material, and thick film internal traces are screen-printed on unfired LTCC tapes. Extensive trade-offs exist in the decisions on how to use cavities, in view of flatness and dimensional requirements. Thick film techniques for the surface metallization have previously been the norm. For triple printed-dried-fired solderable metallization and associated dielectrics, and brazed seal frames on a double sided board, the special processing could require as many as 12 post-firing steps at 850°C. Post fired metallization using thick film is difficult in cavities, particularly when solderable compositions are desired.

Multiple approaches were created to evaluate the Faraday cage structure in LTCC for EMI shielding. Traditional via fences, elongated discontinuous slots, and finally continuous slots have all been evaluated for EMI shielding, structural interactions, and manufacturability. Continuous slots can be formed in LTCC as full tape thickness features (FTTFs), but require multiple layers of tape and progressive operations on those layers to completely form. These features have demonstrated very high isolation levels empirically. [7] Due to the success of the high isolation achieved with FTTFs, but also because of the structural interactions, additional approaches have been developed. These include open recesses that reach the ground plane where the recess and exposed ground plane are metallized using thin film. This permits the seal frame to accomplish the EMI protection required. Each method will be reviewed here.

Via fences (Figure 2) are typical structures used to create isolation of RF signals in LTCC structures. [design guides from Sea Ceramics, Natel, Anaren, etc.] These via fences are straightforward to fabricate by mechanically punching a series of vias that are staggered around a die that requires RF isolation, and then those vias are filled with standard composition via fill materials. In our application via fences do not provide sufficient isolation.

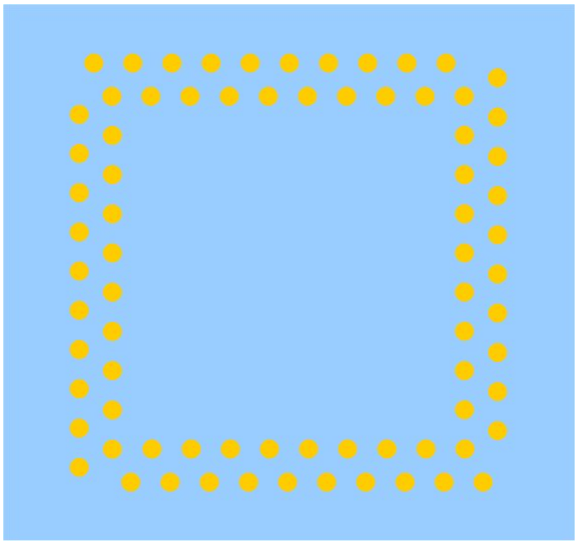

Figure 2: Typical Via Fence Configuration

An approach using staggered, discontinuous, elongated vias or slots (Figure 3) is another approach that has been used to create higher levels of RF

isolation than via fences. Even these, however, do not completely isolate die or selected components from causing or being affected by EMI. [4] High concentrations of closely spaced, large volume features such as these are also problematic to form, and can result in cracks forming between the filled slots in the LTCC.

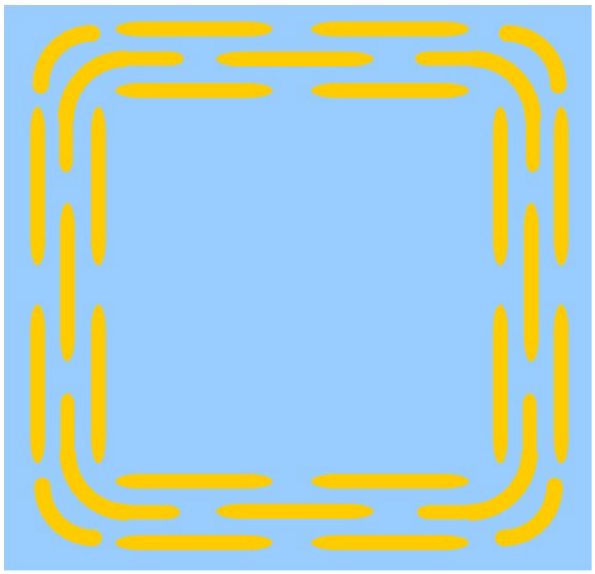

Figure 3: Staggered "racetrack" slot configuration.

Circuits have previously been fabricated using a technique for continuous wall formation (Figure 4) in individual layers of tape. This involved partial lamination and staged segmental punching and filling of continuous wall features. Advantages of this technique included fabrication by layer as is the case with conventional LTCC. Disadvantages included the fact that in handling, the partially constructed, unfired solid wall structures were fragile, and seemed to show cracking due to solvent-tape interactions. Also, the sequential lamination is beneficial to the support required for the end result, but became cumbersome with its own logistics due to controlling expansion.

It was realized that green-state machining permits a stack to be constructed in a relatively simple manner, followed by machining of a 'trench' to the ground plane, which, when subsequently filled, becomes an FTTF solid wall, connected to the ground plane of the module. Electrical conductivity sense-mode machining permits milling to a locally thickened ground plane without perforating it. Table 1 compares the progressively punched FTTF formation method and green machining. The green machining method provides a more straightforward approach with less potential for handling damage than the progressively punched method.

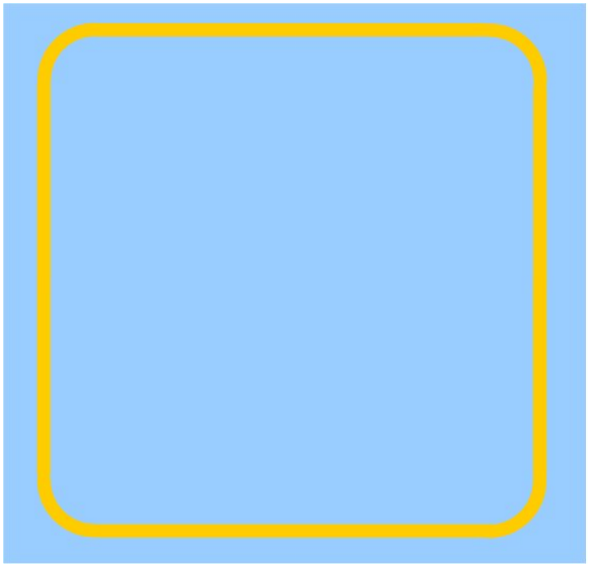

Figure 4: FTTF forming continuous isolation structure.

Because the original implementation of the punched solid wall features were showing defects and cracking related to punching and filling operations, concern mounted over further attaching a seal frame to this region of the circuit. If this situation were modeled, it would be possible to understand the stress developed, and what the effects of adding a seal frame and the assembly over temperature ranges would be. Also, lower stress implementations were envisioned, but required other logistics to be solved as well.

The Faraday structures we are employing are taxing the properties of the constituents. Mismatches that may exist between LTCC and via-fill materials are mitigated in vias where dimensions are small, and resulting mismatched displacements are also small. By constructing these via-like structures over considerably longer distances, we are susceptible to larger mismatched displacements. Furthermore, although soldered seal frames are quite common, there are geometries wherein these mismatches (sometimes due to non-linear CTE behavior) can be problematic. A recent publication shows cracking that appears to be related to such logistics. [9] Also recently, modeling has been performed on the MCM structure in the absence of the faraday structures during assembly. [10]

Table 1. Comparison of progressive punching vs. green machining for Faraday structure formation.

MECHANICAL PUNCHING METHOD	GREEN MACHINING METHOD
CONDITION TAPE	CONDITION TAPE
PUNCH VIAS	PUNCH VIAS
PRINT/DRY VIA FILL	PRINT/DRY VIA FILL
PRINT/DRY CONDUCTORS	PRINT/DRY CONDUCTORS
PUNCH SLOT/WEBBING (TOP LAYER)	COLLATE & LAMINATE ALL LAYERS
-	GREEN MACHINE SLOTS
PROGRESSIVELY LAMINATE TOP 2 LAYERS	FILL SLOT/WEBBING LAYER
PUNCH PROGRESSIVELY LAMINATED SLOT LAYERS	-
FILL PROGRESSIVELY LAMINATED SLOT LAYERS	-
COLLATE & LAMINATE REMAINING LAYERS WITH SLOT LAYERS	-
BURNOUT & COFIRE	BURNOUT & COFIRE
PRINT/DRY/FIRE CONDUCTORS/DIELECTRIC/ PASSIVES	PRINT/DRY/FIRE CONDUCTORS/DIELECTRIC/ PASSIVES
SINGULATE	SINGULATE

III. Results and Discussion

The role of various components of the MCM system (i.e. seal frame, presence of filled slot, location of the seal frame, solder composition, seal frame composition, etc.) were analyzed in multiple models to understand the impact of each one on the system stress. The modeling started by looking at structures independently of how they had been fabricated. However, it was noticed that fabrication technique influenced the type of failure that could be generated. Using green-machining, for instance, fewer defects were seen in cross-sections.

One limit of the model would look at direct attachment of the seal frame to the LTCC—providing a worst-case analysis. The attachment material, however, is real and finite, and plays a significant role on the result due to its individual mechanical properties. The processing ease dictated that Sn-Pb solder would be used for seal frame attachment. In industry, Au-Sn attachment of seal frames is a standard process. Similarly, one could wonder if the use of a very compliant solder (Pb-In) could help in the mechanical behavior of the connection. In this vein, multiple materials were modeled in attachment of the seal frames to the LTCC.

Also, because Kovar has a CTE that varies significantly over temperature, other materials, such as titanium, were considered. Modeling has been pursued to evaluate the effect of the seal frame on the LTCC and the effect of the solid wall feature and its potential replacements on the big picture. The interest in modeling was accentuated by early observations of cracking in punched and filled FTTF structures as shown in Figure 5.

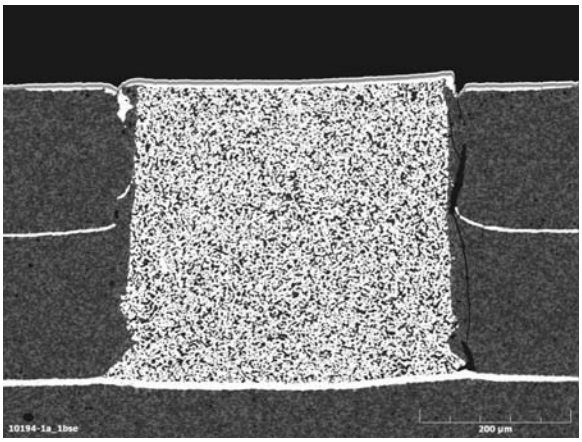

Figure 5. Crack accompanying FTTF structure.

A study of the effect of various solder fillets on the seal frame provided stress estimates. The study shows the need for mechanical properties of the via fill compositions. The sintering shrinkage is

closely matched with the LTCC tape for success in via formation.

Figure 6. shows the results of an analysis of the effect of seal frame width. This is an axisymmetric plane strain analysis, using the commercial product ABAQUS[11], showing the maximum principle stress. The axisymmetric axis was selected to be representative of the 1.7" part. The solder volume was fixed, which permitted the fillet to become more step for the wider seal frames. The steeper fillet is primarily responsible for the increase of stress seen here. The materials are assumed to be stress-free at the soldering temperature (181°C).

Because the seal frame and joint materials are selectable, various combinations were considered as shown in Figure 7and Figure 8 below. The effect of the width on the maximum stresses in the LTCC was considerably more if Au-Sn joint materials were selected. This is an industry standard for applications such as this. A corresponding effect is seen in Figure 8 below, where the maximum strain in the solder foot is considerably greater in the case of the Sn-Pb joint materials.

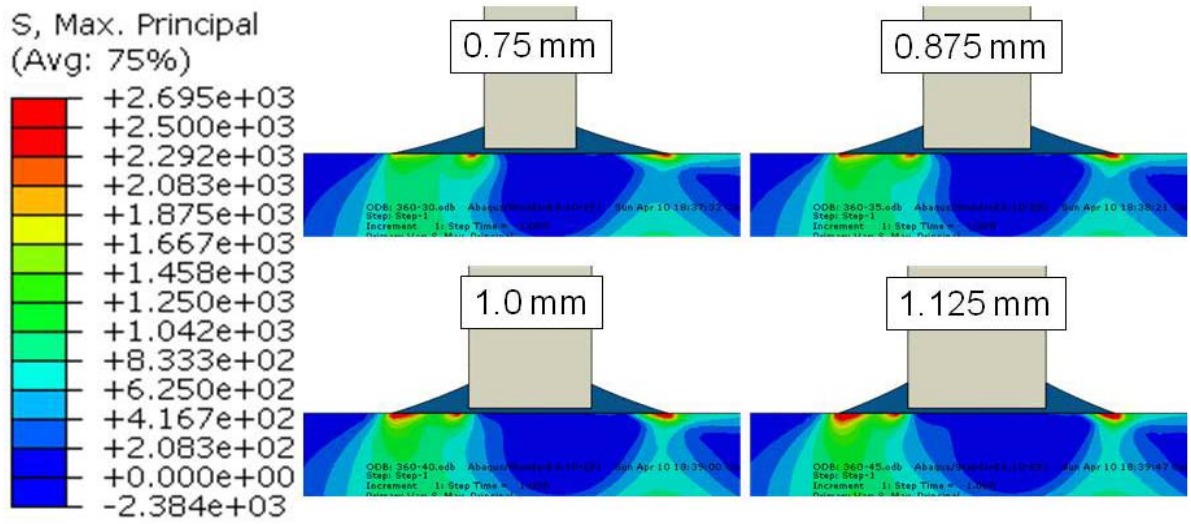

Figure 6. The increased stress in the ceramic at the foot of the solder joint is mainly due to solder geometry. (Kovar seal frame, 181°C to -55°C)

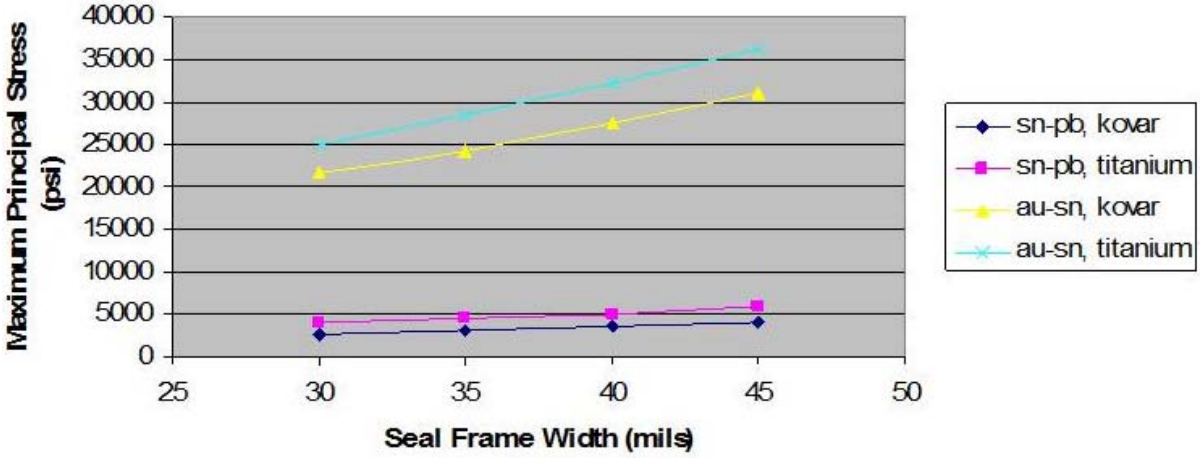

Figure 7. Maximum stress effects are considerably higher for Au-Sn joining materials than for Sn-Pb.

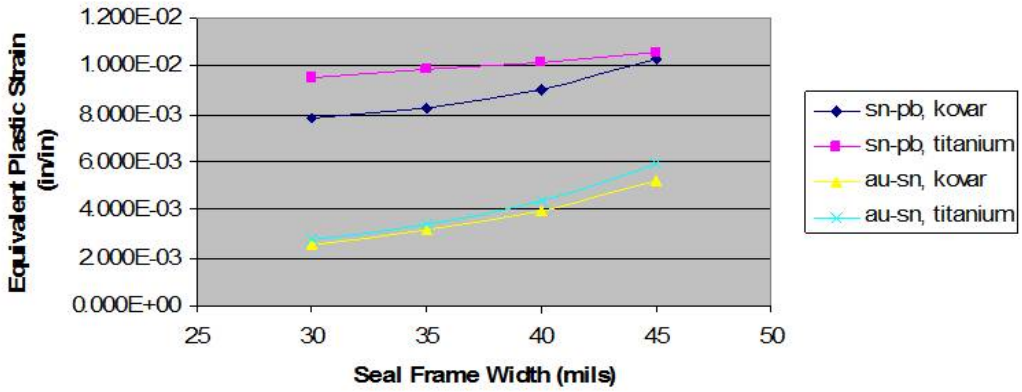

Figure 8 Maximum strain effects are considerably higher for Sn-Pb joining materials than for Au-Sn.

A few different cases of interest are illustrated in Figure 9. The properties of pure gold and LTCC were used interchangeably for the material in the slot. A test of the thermal expansion coefficient of the via fill material showed it to be essentially the same as gold. This sample was constructed and fired but was not in contact with the LTCC tape during firing. A technique that completes the Faraday cage without a via-fill material is shown in Figure 9a for a thin film implementation. The machined and filled FTTF with square corners is shown in Figure 9b. This does not differentiate whether this is done via punching or machining, but punching introduces additional factors that need to be considered. In Figure 9c, a modified geometry that can result from milling is shown and is seen to reduce the stressed area in the LTCC. The via filled areas in Figure 9b and Figure 9c would show no color unless stressed in this map, and the fact that the stress is high is important. However, to look more meaningfully at the stress inside the via-fill, a Von Mises criterion would be more appropriate. For the moment, we are more interested in the stresses in the ceramic because the fractures are in the ceramic.

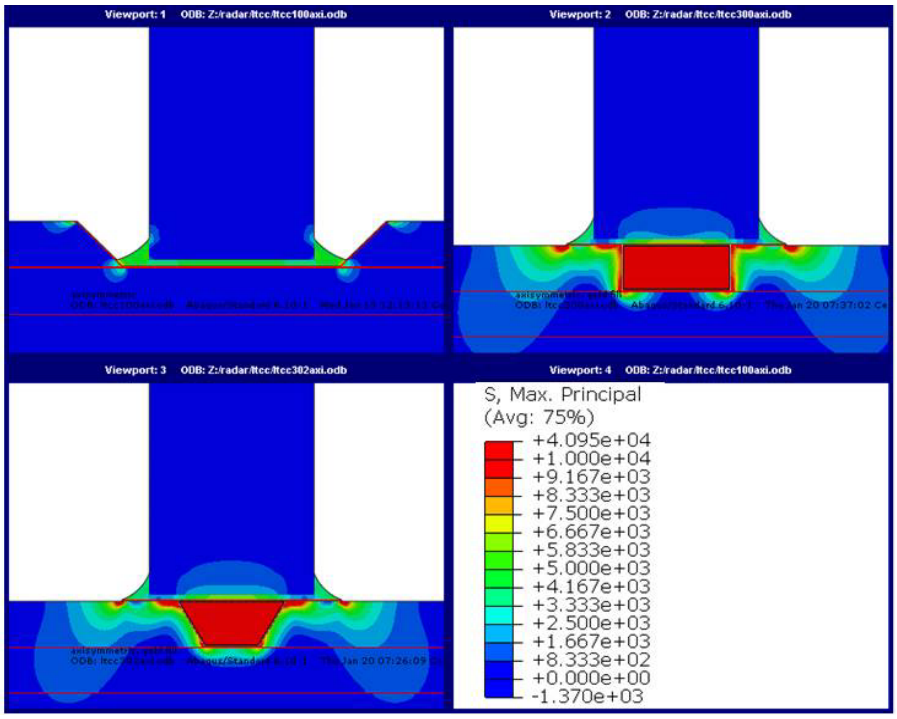

Figure 9. A plane strain analysis of the stress in solder and LTCC for several schematic isolation techniques.

An implementation of the FTTF with a seal frame is shown in a cross-sectional view in Figure 10. In this case, the metallization is a multilayer metal thin film.

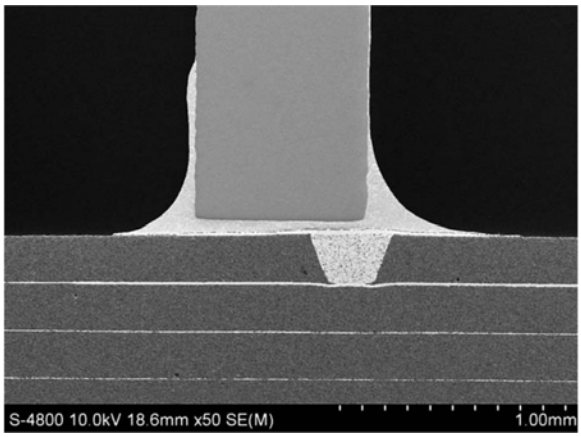

Figure 10. Cross sectional view of a seal frame soldered to a thin film covering a FTTF solid wall structure used in a prototype.

An actual implementation of the concept previously shown in Figure 9a is shown in a cross-sectional view in Figure 11. This involves a 'trench' to the ground plane that was machined in the green state, cofired, and subsequently coated with a thin film metal multilayer stack. The seal frame is then soldered into this trench with SnPb solder. Modeling indicated comparatively low stresses for this geometry. Various environmental tests are being completed for this design.

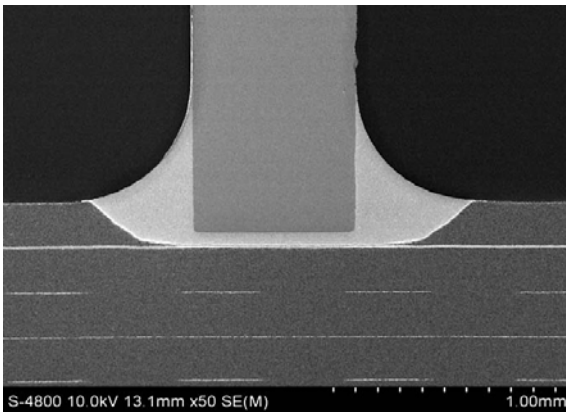

Figure 11: SEM Micrograph of cross sectioned green machined, open recess with seal frame soldered into recess.

IV. Summary

Modeling has shown that the existence of the slot feature under the seal frame does increase the stress to a point that it needs to be addressed for reliability in the face of material properties for the LTCC. Naturally, removing the slot material from the slot reduces the stress state in the substrate (LTCC). The shape of the slot is not major player (for the shapes analyzed here) being secondary to the volume of slot fill material. Geometries used in practice avoid sharp features that might serve as stress concentration points. Modeling showed that solder (and particularly, solder geometry) is the second largest contributor to final stress. Furthermore, steep solder fillet angles impart higher stress on LTCC at toe than lower angles, as expected. Cross sections of actual prototypes have confirmed the results. Cross sectioning was viewed as critical since removal of the slot would not necessarily resolve cracking due to the solder/seal frame arrangement, as also shown in literature. Finally, in an examination of different solder materials, AuSn solder was seen to predict higher stress in the LTCC than the SnPb solder.

V. Acknowledgements

The authors wish to acknowledge valuable assistance from Mike Girardi, Dave Stockdale, Jim Mahoney, and many others.

Notice: This manuscript has been authored by Honeywell Federal Manufacturing & Technologies under Contract No.DE-NA-0000622 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a nonexclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

VI. References

[1] M.R. Gongora-Rubio, P. Espinoza-Vallejos, L. Sola-Laguna, J.J. Santiago-Aviles, "Overview of low temperature co-fired ceramics tape technology for meso-system technology," Sensors and Actuators A 89 (2001) 222-241.

[2] L.J. Golonka, “New application of LTCC technology,” Proc. 28th Int. Spring Seminar on Electronics Technology, (2005) 148-152.
[3] C.R.S. Needes, D.I. Amey, and S.J. Horowitz, (Cost effective solutions for high density interconnect and RF modules using low temperature cofired ceramic materials,” IMC/IEMT Conference, April 2000.
[4] Integrated brazed LTCC packages, A.L. Kovacs and D. F. Elwell, Proceedings of the 1994 International Conference on Multichip Modules, Denver, CO, April 13-15, 1994, pp. 591-596.
[5] Innovations in QFN Packaging Targeting RF and Image Sensor System-in-Package Andrew Holland RF Module & Optical Design Limited Farfield Innovation Centre Albert Road Cambridge UKEmail:aholland@rfmod.com.
[6] G.E. Ponchak, D. Chun; J.-W. Yook; L.P.B Katehi, “Experimental verification of the use of metal filled via hole fences for crosstalk control of microstrip lines in LTCC packages,” IEEE Trans: Advanced Packaging, Volume 24, Issue 1, Feb 2001, 76 – 80.
[7] K. Peterson, G. Barner, F. Smith, R. Knudson, B. Duverneay, M. Johnson, “Improved Isolation for LTCC Transceiver Modules using Full-Tape-Thickness Features, Proceedings of the Ceramic Interconnect and Ceramic Microsystems Technology, CICMT 2009, IMAPS-ACerS, Denver, CO, April, 2009.
[8] U. Partsch, A. Goldberg, M. Ihle, G. Hagen, D. Arndt, “Novel Technology Options for Multilayer-Based Ceramic Microsystems,” 7th International Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT), San Diego, USA, pp. 166-171, April 5-7, 2011.
[9] R. Monti, F. Coppola, P. Gasbarri, U. Lecci, “Residual stress brazing process induced in hybrid package for ISP applications,” Acta Astronautica 66 (2010) 897–913.
[10] N. Young, J. Massad, and K. Ewsuk, “An assembly-based structural model for LTCC package design and reliability,” Proceedings of the 7th CICMT International Conference and Exhibition, IMAPS/ACerS, San Diego, April 5-7, 2011, pp. 59-63.
[11] www.simulia.com