FINAL REPORT

Solar Cell Nanotechnology

Award Number : DE-FG36-08GO88010

by

Biswajit Das
University of Nevada, Las Vegas

EXECEUTIVE SUMMARY

The objective of this project is to develop a low cost nonlithographic nanofabrication technology for the fabrication of thin film porous templates as well as uniform arrays of semiconductor nanostructures for the implementation of high efficiency solar cells. Solar cells based on semiconductor nanostructures are expected to have very high energy conversion efficiencies due to the increased absorption coefficients of semiconductor nanostructures. In addition, the thin film porous template can be used for optimum surface texturing of solar cells leading to additional enhancement in energy conversion efficiency. An important requirement for these applications is the ability to synthesize nanostructure arrays of different dimensions with good size control. This project employed nanoporous alumina templates created by the anodization of aluminum thin films deposited on glass substrates for the fabrication of the nanostructures and optimized the process parameters to obtain uniform pore diameters. An additional requirement is uniformity or regularity of the nanostructure arrays. While constant current anodization was observed to provide controlled pore diameters, constant voltage anodization was needed for regularity of the nanostructure arrays. Thus a two-step anodization process was investigated and developed in this project for improving the pore size distribution and pore periodicity of the nanoporous alumina templates.

CdTe was selected to be the active material for the nanowires, and the process for the successful synthesis of CdTe nanowires was developed in this project. Two different synthesis approaches were investigated in this project, electrochemical and electrophoretic deposition. While electrochemical synthesis was successfully employed for the synthesis of nanowires inside the pores of the alumina templates, the technique was determined to be non-optimum due to the need of elevated temperature that is detrimental to the structural integrity of the nanoporous alumina templates. In order to eliminate this problem, electrophoretic deposition was selected as the more appropriate technique, which involves the guided deposition of semiconductor nanoparticles in the presence of ultrasonic energy to form the crystalline nanowires. Extensive experimental research was carried out to optimize the process parameters for formation of crystalline nanowires. It was observed that the environmental bath temperature plays a critical role in determining the structural integrity of the nanowires and hence their lengths. Investigation was carried out for the formation of semitransparent ohmic contacts on the nanowires to facilitate photocurrent spectroscopy measurements as well as for solar cell implementation. Formation of such ohmic contacts was found to be challenging and a process involving mechanical and electrochemical polishing was developed to facilitate such contacts.

The use of nanoporous alumina templates for the surface texturing of mono- and multi-crystalline solar cells was extensively investigated by electrochemical etching of the silicon through the pores of the nanoporous templates. The processes for template formation as well as etching were optimized and the alumina/silicon interface was investigated using capacitance-voltage characterization. The process developed was found to be viable for improving solar cell performance.

Introduction

Nanotechnology based solar cells can provide very high energy conversion efficiency and is considered to be a serious candidate for future PV technology. The large energy conversion efficiency arise from the following effects: (a) nanostructure *crystallite sizes* are comparable to the *carrier scattering lengths*, this significantly reduces the scattering rate, thus *increasing the carrier collection efficiency*; and (b) nanostructures have *strong absorption coefficient* due to increased density of states. In addition, by varying the size of the nanostructures, the band gap can be tuned to absorb in a particular photon energy range. However, to achieve these advantages at non-cryogenic temperatures, it is necessary to fabricate periodic arrays of individual nanostructures with a uniform size below 20 nm. A major impediment to the development of a nanostructure-based PV technology has been the inability to fabricate large arrays of nanostructures with the required periodicity and size control at low cost. The conventional nanofabrication techniques of epitaxial material growth, electron-beam lithography and reactive ion etching are not suitable for photovoltaic applications due to their prohibitively large manufacturing costs. A number of alternative nonlithographic fabrication techniques have been investigated, such as deposition from a colloidal suspension of particles, incorporation of semiconductor clusters in organic polymers, incorporation of semiconductor microcrystallites in glass matrices, strain-induced self-organized growth, etc. However, most of these techniques lack the necessary control over nanostructure size distribution, periodicity and the flexibility regarding the choice of semiconductor material. We have developed a unique low-cost nanogrowth technology for the fabrication of periodic arrays of semiconductor nanostructures with very good size control (±10%) and a high degree of periodicity. This technique uses electrochemical synthesis of semiconductor nanostrucutres on a preformed template that is created by electrochemical anodization of aluminum. Since this technique uses methods that are of widespread use in the commercial electrochemical manufacturing industry, it is inexpensive, reliable, suitable for mass production, and in addition allows the use of a wide range of substrate and semiconductor materials. This technology is also ideally suited for the formation of multijunction structures, which can further increase the photo-conversion efficiency. The objective of this project is to utilize this nonlithographic method to develop a low cost technology for the implementation of high efficiency solar cells.

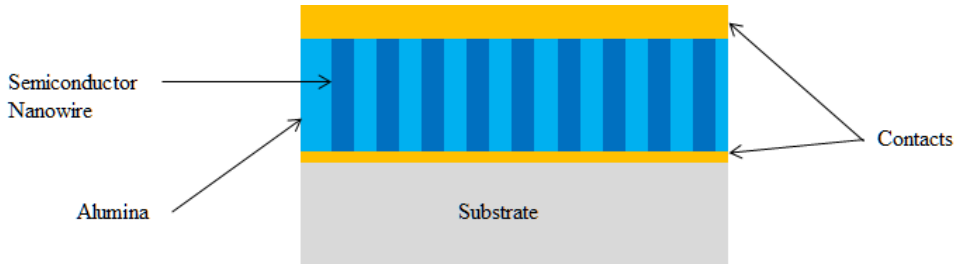


Figure 1. Schematic diagram of the nanostructure based solar cell

A schematic diagram of the nanostructure based solar cell is shown in Figure 1. The structure consists of semiconductor nanowires embedded in an alumina matrix grown on a substrate containing the bottom electrical contact for the solar cells The nanowires are contacted at the top to form the other electrical contact. The substrate is glass and the top contact is formed with a transparent conductor so as to allow full absorption of the solar radiation. In addition, the bottom contact is also preferred to b formed using a transparent conductor so as to allow future implementation of multijunction solar cells. The photons from the solar radiation are absorbed by the nanowires at relatively high efficiency due to the increased density of states of the lower dimensional structures. The built-in electric field separates the electron-hole p[airs created due to photon absorption which are collected by the bottom and top electrical

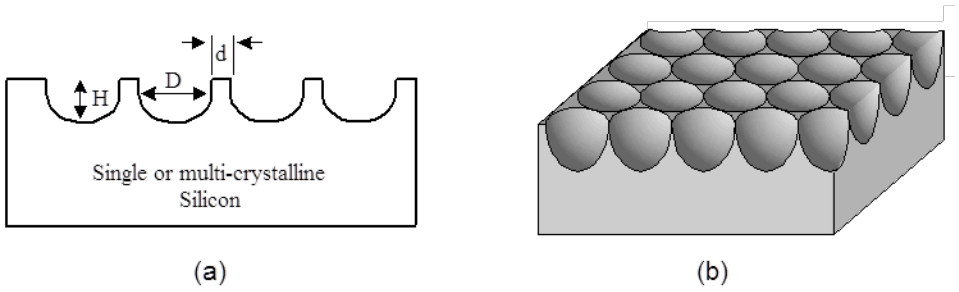
contacts. Due to the nanoscale dimensions of the active material, it is expected that the built-in electric field produced inside the nanostructures due to Fermi level pinning at the surface will be sufficient to separate the electron-hole pairs generated by the optical absorption process, thus eliminating the need for PN junction formation. However, if the built-in electric field proves to be insufficient, then PN junctions can be created by adding the appropriate dopant materials during synthesis.

Another component of this project is to use the thin film nanoporous alumina templates to develop the technology for the creation of optimum surface texturing for the increased efficiency of mono and multicrystalline solar cells. Surface texturing is commonly used in crystalline silicon photovoltaic cells to improve light absorption and therefore total cell efficiency. In this approach, multiple reflections off of the textured silicon surfaces increase the probability of photon absorption in the active silicon material. When combined with suitable anti-reflection coating, this approach has been demonstrated to significantly enhance the efficiency of crystalline silicon photovoltaic cells. Techniques for surface texturing for both mono- and multi-crystalline silicon have been an active area of research. For the case of mono-crystalline silicon, the use of an anisotropic etch that is selective to crystal orientation is commonly used. This approach has evolved from the use of etched square-based pyramid structures in the early COMSAT cells, to the inverted pyramid structure used in the high efficiency PERL cells. In addition, lithographic processes have been developed for surface texturing in high efficiency mono-crystalline PV cells. For the case of multi-crystalline silicon devices, anisotropic etch techniques are not appropriate due to the lack of well-defined crystal planes. The use of random texturing has been developed for multi-crystalline silicon, however a large percentage (28 %) of the incident light is reflected from these randomly textured surfaces.

Since the use of multi-crystalline silicon PV devices appears to be increasing, it is appropriate to investigate alternative texturing approaches that are suitable for these devices. Several different approaches have been previously investigated to provide surface texturing for multi-crystalline silicon, including mechanical grooving, defect etching with acidic solutions, reactive ion etching (RIE), and lithographic surface patterning. However, each of these techniques presents several problems for commercial manufacturing. While considerable work has been done on mechanical grooving, low-cost metallization on the deeply grooved surfaces is difficult. Defect etching requires the use of a large amount of proprietary acidic solutions. RIE is a relatively slow vacuum process that can also induce unwanted damage to the silicon surface. Finally, the use of lithographic processes for texturing is not cost-effective due to equipment expense and low throughput. As a result, it is important to develop a low cost, manufacturable surface texturing technique that can provide control over pore shape and dimension, and is applicable for both mono- and multi- crystalline silicon.

One of the objectives of this project is to develop an electrochemical technique for surface texturing that is applicable for both mono- and multi- crystalline silicon PV cells. This approach can *non-lithographically* reproduce the “honeycomb” structures however with significantly reduced flat surface area and therefore improved device performance. With this approach, the pore density, diameter, and separation can be independently controlled to produce optimum light trapping for a given cell design. In addition, this approach is based on well-established industrial processes and is suitable for high-throughput manufacturing. Finally, the etched structures can be used as a getterning site to reduce the crystal defect density in the active regions of the device.

The surface texturing technique developed in this project is based on guided *electrochemical etching* of silicon through the pores of an alumina template formed by the anodization of a thin film of aluminum deposited on the substrate. Two views of the proposed silicon surface structure are shown in Figure 2.



1Figure 2: (a) Cross-sectional and (b) Perspective view of the silicon surface texturing technology to be developed in this project. The height (H), diameter (D), and spacing (d) can be independently controlled with the proposed technique.

Formation of Nanoporous Alumina Templates

The fabrication technique used in this project is based on electrochemical synthesis of semiconductor on a preformed template. When aluminum is anodized in a suitable oxidizing acid (e.g.sulphuric acid), a two-dimensional hexagonal lacework of Al_2O_3 cells with uniform tubular pores is formed as shown in Figure 3. The pore diameter and the cell wall thickness depend on the anodization conditions, such as type and pH of the anodizing acid, and the anodizing current density, and can be precisely controlled over a wide range. The technique can be used to create templates with pore diameters ranging from 4 to 200 nm, pore length from 10 to 1000s of nm, and pore density in the $10^9 - 10^{11}$ cm^{-2} range. In addition, such templates can be created on aluminum substrates, silicon substrates and glass (soda lime) substrates, and a pore diameter variation of ±10% can be achieved. In recent years, researchers have reported self-organized pore growth leading to a nearly perfect, densely packed hexagonal pore structure for a narrow set of processing parameters. A systematic investigation suggests that the cause of this self-ordering behavior is mechanical stress which leads to a repulsive interaction between neighboring pores . Such self-organized pore growth allow even more stringent control over the diameters of the nanostructures.

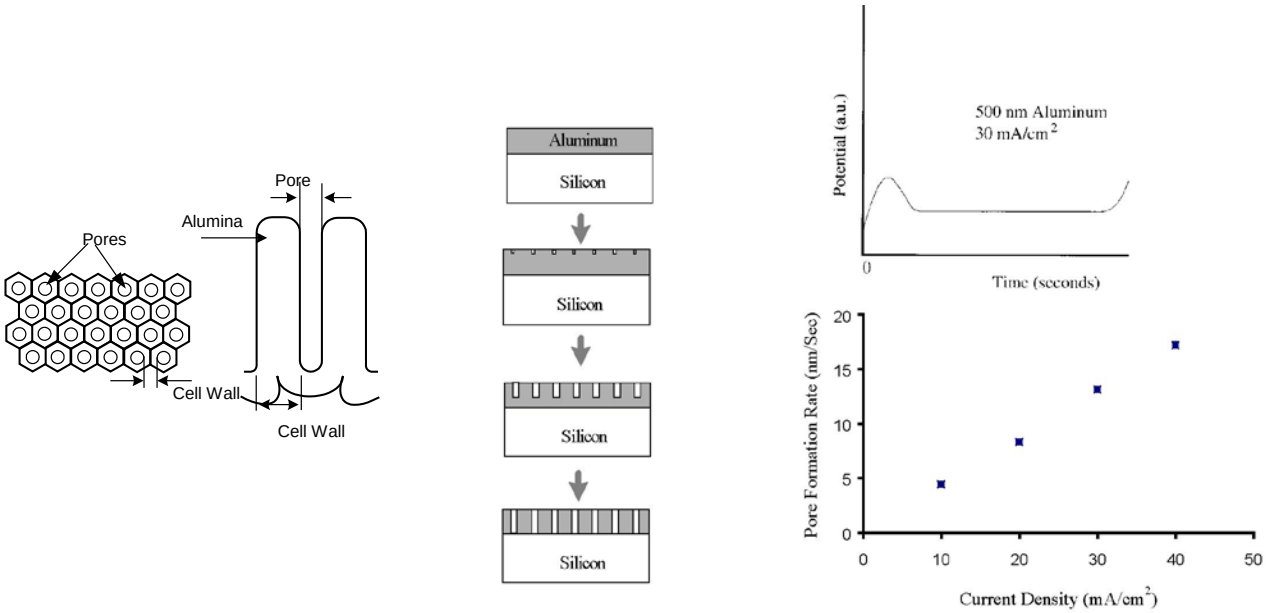


Figure 3. Schematic top and cross-sectional views of pores formed by anodization of aluminum. Pore formation steps and concurrent potential-time characteristics providing an insight into pore formation process for thin films of aluminum. The potential-time curves and the aluminum film thickness can be used to determine the pore formation rate which is experimentally determined to be proportional to the anodization current density.

Although the pore formation mechanism is not yet fully understood, it is believed to take place in the following steps. During the first 3-5 s of anodization, a thin non-porous layer of alumina (Al_2O_3) is formed on top of the aluminum layer. As anodization is continued, an array of pores develops on the alumina layer, and grow in diameter until reaching the final dimension determined by the anodization conditions. Once the final diameter is reached, the diameter of the pores do not increase any further, and as the anodization is continued, the depth of the pores increase in proportion to the anodization current. While most of the work in this area has been restrictd to bulk aluminum, we have extended this technique to create Al_2O_3 templates on silicon and glass substrates through the deposition of an aluminum thin film. This approach provides the possibility of nanostructure integration on silicon substrates, and provides us with a tool for precisely controlling the nanostructure depth by monitoring the voltage-time characteristics during anodization, as shown in Figure 3. During anodization, the potential increases initially during the formation of the top layer of Al2O3 , then decreases during pore widening, and then levels of at the onset of pore propagation. Next, when the pores propagate through the complete layer of aluminum film, and contacts the silicon substrate, the potential rapidly increases. Since the thickness of the aluminum fillm is accurately known, and the time from the beginning to the end of pore formation can be determined from the potential profile, the pore formation rate can be precisely determined in this system. Therefore, in addition to providing control over the diameter of the pores, our approach also provides precise control over the length of the pores.

Fabrication Process Development

One of the requirements for the implementation of high performance solar cells using this technology is the formation of semiconductor nanowires with very small size variation and of high degree of periodicity. Due to quantum confinement, the absorption spectrum of a nanowire is determined by its diameter, thus a variation in the diameter can result in shifts in the absorption spectra. While such shifts can be advantageously used to cover a broader range of the solar spectra, a large variation in the dimensions can eliminate the benefits of quantum confinement effects such as increased absorption due to higher density of states. As a result, a good control over the nanowire diameter is necessary. To identify the desired size variation of the nanowires, the results from an earlier theoretical modeling was used in this project. The theoretical model was developed for cadmium sulfide, which has very similar properties as cadmium telluride with a somewhat larger band gap. The simulation results shown in Figure 4 demonstrate that a size variation of over 30% can wash out the effect of quantum confinement.

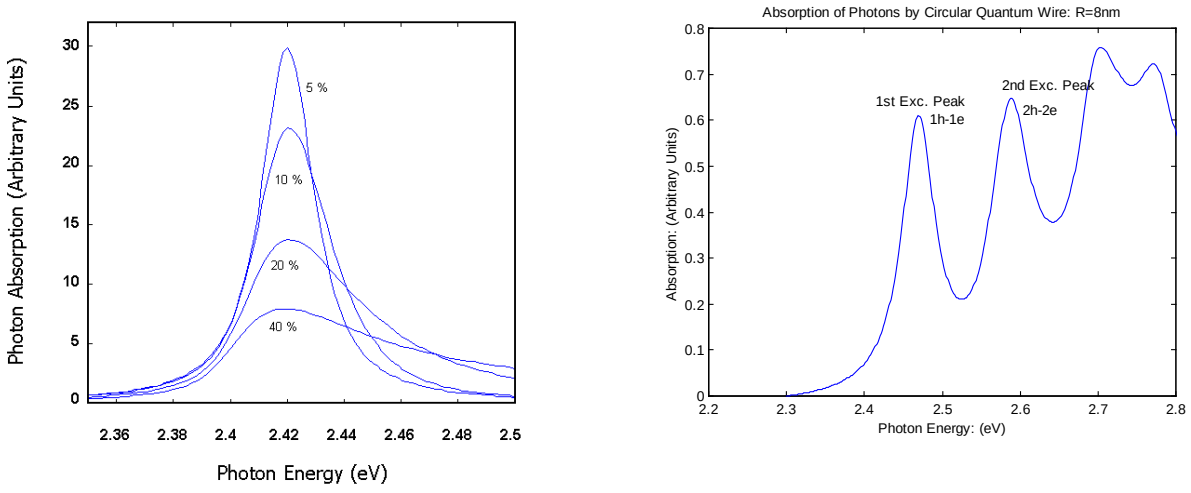


Figure 4. Simulation results for the dependence of absorption spectra on nanowire size variation and the absorption spectra showing the different excitonic peaks for a 16 nm diameter nanowire.

Simulation was used to confirm the quantum confined nature of the absorption spectra from the excitonic absorption peaks shown in Figure 5. It was determined that the size variation of the nanowires will need to be kept belo 30%, and preferably betwe3n 10-20%. This will require the pore size variation of the nanoproous alumina template to be within the 10-20% range. While the spatial distribution of the nanowires do not directly affect the absorption spectra, a template with low degree of pore periodicity can adversely affect the solar cell performance as two closely located pores can fuse to form a larger pore, which has been often observed. Thus, another requirement for this project is to develop the process for the formation of nanoporous alumina templates with good degree of pore periodicity. The fabrication process in this project consisted of : (i) the development and optimization of the anodization process, (ii) the development and optimization of the nanowire synthesis process, (iii) fabrication process development for the formation of ohmic contacs, and (iv) process development for the surface texturing of solar cells.

The first phase of the project consisted of the development and optimization of the process parameters for the fabrication of nanoporous alumina templates with good pore size uniformity and high degree of pore periodicity. This objective was accomplished by optimization of the thin film structure for the creation of uniform arrays of nanostructures, the optimization of aluminum deposition process, identification of any buffer materials needed, optimization of aluminum layer thickness, as well as the investigation and development of the two-step anodization process. The process development was initially carried out on silicon substrates and once optimized was transferred to ITO coated glass substrates. The silicon substrate was an ideal platform for the development of the process due to its extremely smooth surface profile. Silicon substrates were first summa-cleaned, then immersed in a 1% HF bath, rinsed, and dried in N_2. Then, a 100 nm layer of Al was sputter deposited on the back of the wafer, followed by annealing at 450^o C for 30 minutes to form an ohmic back contact. Next, a 100 nm layer of Al was deposited on the top of the wafer, which was then annealed at 400^o C for 30 minutes to ensure good adhesion. The wafers were then anodized in 20% sulfuric acid at different current densities. Some of these wafers were then pore widened in 5% phosphoric acid for either 3 or 6 minute durations.

A picture of the anodization apparatus is shown in Figure 5, which also shows a close-up of the sample holder. The sample is mounted on the chamber so as to be liquid sealed; the chamber is cooled using a water bath circulating around it that is pumped through the pump. This ensures a constant temperature of the anodization bath as the porosity can be adversely affected by varying bath temperatures. All anodizations in this project were carried out at a constant temperature of around 10^{o}C.

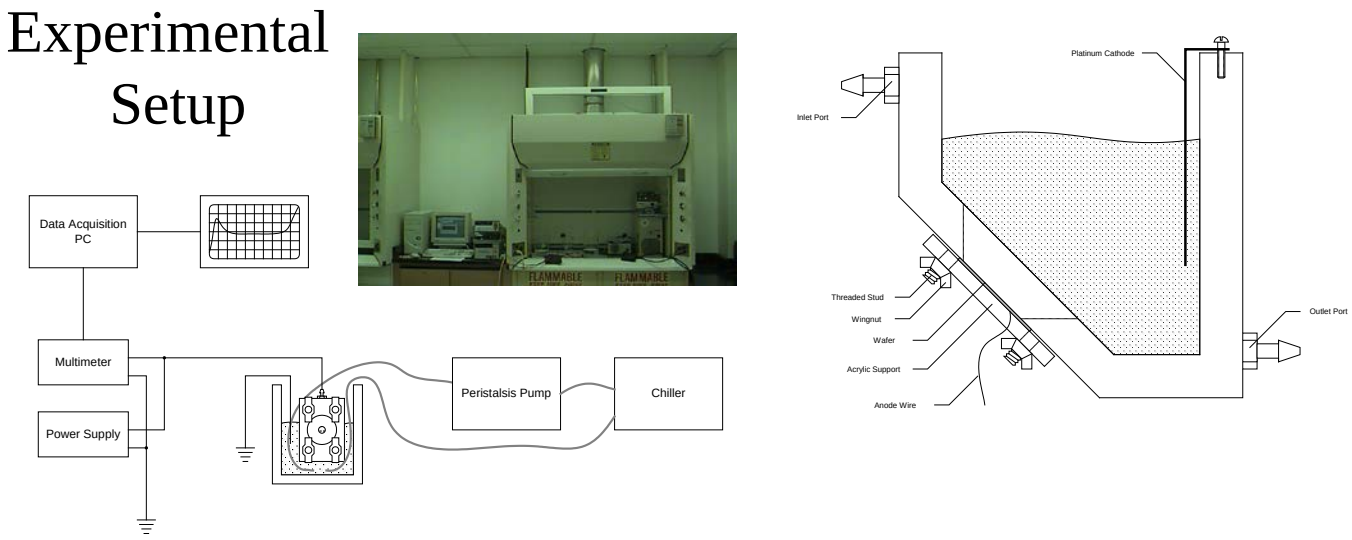


Figure 5. Anodization apparatus and chamber showing details of the sample holder

During andization, the voltage-time characteristics is monitored to obtain an insight into the anodization process and also to obtain an end point for the anodization process. Figure 6. Shows a typical voltage-time characteristics obtained during anodization. The voltage-time characteristics show the steps of pore initiation, pore formation, pore propagation and termination of the pores on the substrate.

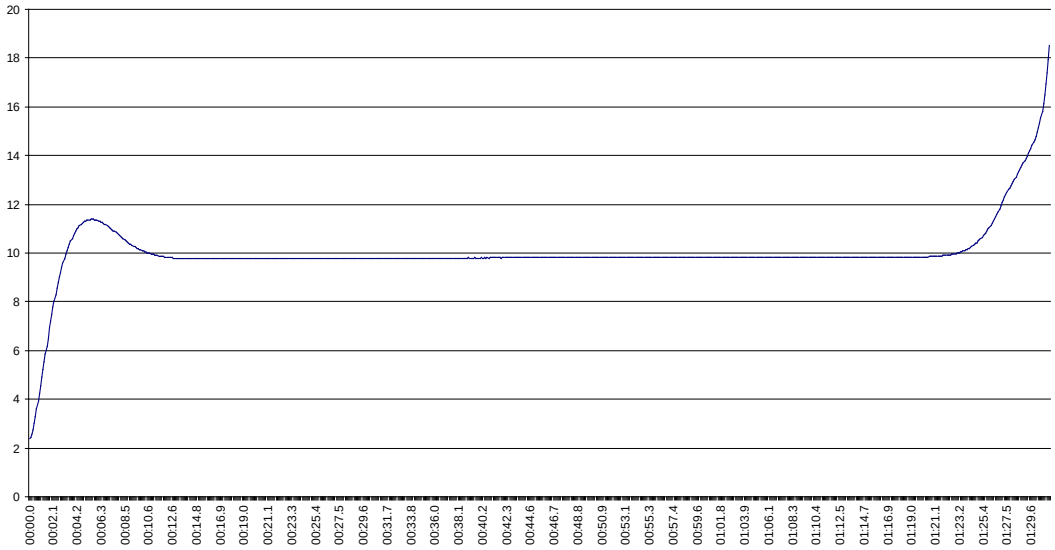
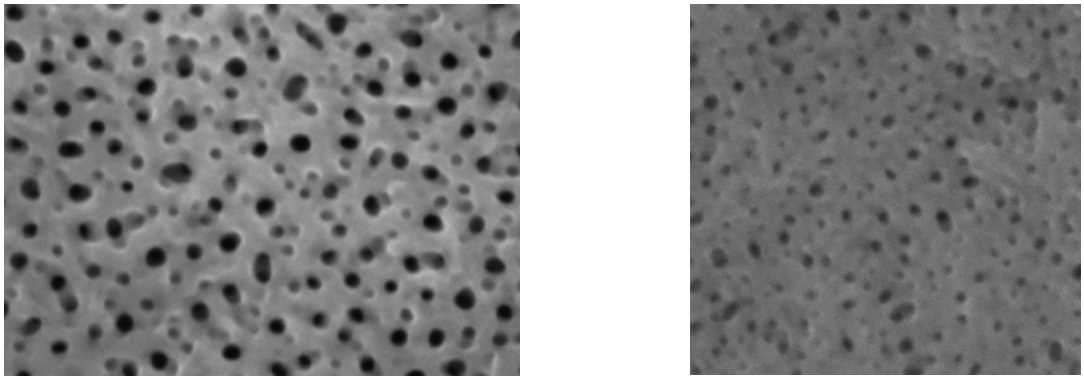


Figure 6. Typical voltage-time characteristics obtained during the anodization of aluminum under constant current condition.

One of the first tasks in this project was to identify the aluminum deposition process and also the thickness of the aluminum layer as the final thickness of the nanowire will be determined by the thickness of the nanoporous alumina template. Based on our investigation and calculation it was determined that a thickness of 100 nm of aluminum would be sufficient for this project. Two different techniques for the deposition of aluminum was investigated : sputtering and electron beam evaporation. While sputtering has the benefit of providing faster deposition rate and is a manufacturing process, electron beam evaporation was found to provide improved film quality and better anodized layer. Figure 7 shows the scanning electron microscope images of the surface of anodized layers for aluminum deposited by sputtering and electron beam evaporation, which clearly show the benefit of the latter process. One of the problems with obtaining top views of the pores was the high resistivity of alumina which caused charging during electron microscopy.



Figue 7. Scanning electron microscope images of the surface of alumina template created from sputter deposited and electron beam evaporated aluminum.

In order to identify the optimum anodization parameters, a detailed investigation was carried out on the structural dependence of the nanoporous alumina on the different anodization parameters such as the current density, electrolyte temperature, voltage and anodization time. In particular, a special protocol was developed to identify the end of anodization of the thin film. On silicon substrates such end-point determination is accomplished through observation of a significant rise in voltage due to oxidation of the silicon substrate. For thin film aluminum deposited on glass substrate, such determination is more complicated since at the aluminum-glass interface, the voltage-time behavior is complex. The pattern of voltage-time was monitored for a number of samples and the common component was identified. Such end-point determination is very important to control the pore size of the nanoporous alumina template.

Initial process development for optimization of the nanoporous alumina films was carried out on silicon substrates due to the flat surface properties of silicon substrates as well as the ability to make a back contact on the silicon substrate for the anodization process. Since metallic aluminum does not have good adhesion to silicon, a layer of platinum or tantalum was typically deposited first. Once the process was optimized, it was transferred to glass substrates as well as ITO coated glass substrates. The problem with using aluminum directly deposited on glass was that the full thickness of aluminum could not be anodized as the aluminum layer is also used as the anode. Process development was also carried out on ITO-coated glass substrate which have the benefit that the ITO layer could be used as the back contact for anodization as well as for solar cell contact. A specialized sample holder was designed and developed for the anodization of aluminum layers deposited on both glass and ITO-coated glass substrates as the contact had to be made from the front and not from the back. Figure 8 shows the schematic of the sample holder developed as well as a typical voltage-time characteristics obtained during the anodization of aluminum deposited on ITO-coated glass. This special sample holder was also used for the electrochemical deposition of CdTe inside the pores of the alumina templates.

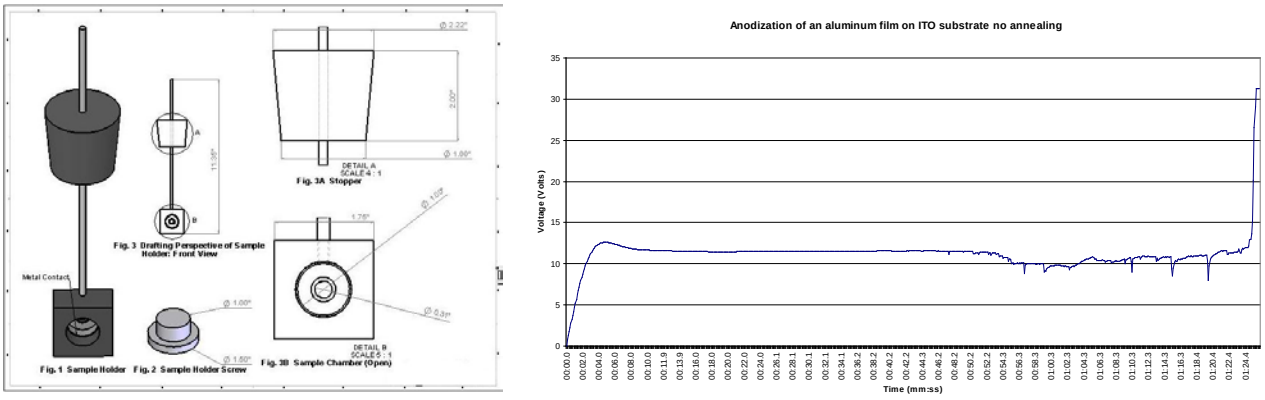


Figure 8. Special holder developed for the anodization of aluminum deposited on glass and ITO-coated glass substrates. Right hand side figure shows a typical voltage-time characteristic obtained during the anodization of aluminum deposited on ITO-coated glass.

The voltage-time characteristics for glass and ITO-coated glass substrates show similar characteristics with a rapid rise when the substrate is reached due to oxidation of the substrate by the anodizing solution. To remove the oxidation, a tin film of platinum was initially deposited on the ITO-coated glass, however, it was found that the end-point determination was more difficult. It was determined that the oxide at the bottom could be removed by carrying out a pore widening step in phosphoric acid.

During anodization process development, it was observed that while the anodization current density had a greater impact on the pore diameter, the anodization voltage played a crucial role on the pore size uniformity. For solar cell implementation, since the template pore size and uniformity determine the nanoparticle size and uniformity, it is necessary to control the dimensions as well as the pore size uniformity. Since either constant current anodization or constant voltage anodization will not provide control over both parameters, a combination of constant-current and constant-voltage anodization is needed. Towards this goal, a two-step anodization process was investigated and developed. Two-step anodization is typically performed on bulk aluminum samples where the aluminum thickness is in mm dimensions. The first anodization step is carried out for over a period of 10 to 20 hours, when 100s of microns of aluminum is anodized. The anodized alumina is then etched off and the second anodization step is carried out. The 'foot prints' left behind by the first anodization step provides seed points for the pore initiation providing more pore size periodicity and uniformity. For thin film aluminum samples such as in our case, such two-step anodization is very challenging since the total thickness of aluminum film is less than a micron. Thus, special process steps, more precise compared to bulk samples, needed to be developed for the two-step anodization of aluminum thin films. Since the quantum wire diameter in this project is determined by the pore diameter of the nanoporous alumina template, hence the need for the optimization of the process parameters for various pore diameters in the two-step anodization process. The specific parameters that were determined are the voltage to be used for the first anodization step, anodization time for the first anodization step, etching time, etchant concentration, etch time, current density for second anodization step, and second anodization time. It was noted that as the anodization voltage was varied for the first anodization step, the concentration of the etchant had to be modified to carry out the etching with the necessary thickness control. This was complicated by the fact that different anodization acids were used to obtain different pore diameters. Towards this goal, anodization of aluminum thin films were carried out at different voltages covering the range around 15 nm that were estimated to be needed for this project. For 15 nm pore diameter, it was decided that phosphoric acid is the most suitable anodization acid. For pore diameters in the range of 15 -20 nm, the optimum parameters were determined to be as follows. The first anodization step was carried out for 30 seconds, followed by an etching step. The second anodization was then carried out under a constant current density of 30 mA/cm^2 to obtain the desired pore size.

Synthesis of nanowires

The active nanowires in the solar cells are implemented by guided synthesis using the nanoporous alumina templates. Two different synthesis techniques were investigated in this project, specifically electrochemical synthesis technique and electrophoretic synthesis technique as described below.

In electrochemical synthesis technique, the semiconductor nanoparticles are synthesized inside the pores of the nanoporous alumina templates using an electric current. Electrochemical synthesis is an inexpensive technique for semiconductor synthesis and a suitable one for solar cells. However, electrochemical processes need to be optimized to produce highest quality semiconductors. The quality of semiconductor material depends on electrochemical parameters such as electrical current, electrolyte composition and electrolyte temperature. An extensive literature search was carried out to determine the most appropriate synthesis technique for solar cell applications. An important requirement for solar cells is improved crystalline quality of the material. For the electrodeposition of CdTe inside the pores of the anodized alumina templates, the following electrochemical solutions were used : $3CdSO_4.8H_2O$ (25.6 g L^{-1}), TeO_2 (1.6 g L^{-1}), and H_2SO_4 (98 g L^{-1}). A 9-V battery was used as the power source, a platinum mesh was used as the anode, and the template as the cathode. The reaction follows the kinetics as below :

$HTeO_2^+ \ 3H^+ \ +4e^- \rightarrow Te + 2H_2O$

$Cd^{2+} + Te \ + 2e^- \rightarrow CdTe$

$Cd^{2+} + 2e^- \ \rightarrow \ Cd$

Using the above process, CdTe was electrochemically deposited inside the pores of the alumina template. A systematic study was first carried out to determine the optimum process parameters for the deposition of CdTe inside the pores. A number of samples were prepared using the above process and the samples were characterized for structural characteristics and material composition. The CdTe nanowires were characterized using EDS to determine the composition of the CdTe materials and the ratio was found to be 50:50 confirming the presence of CdTe. Figure 9 shows the cross-sectional scanning electron microscope image of a typical structure showing the growth of CdTe inside the pores of a nanoporous alumina template.

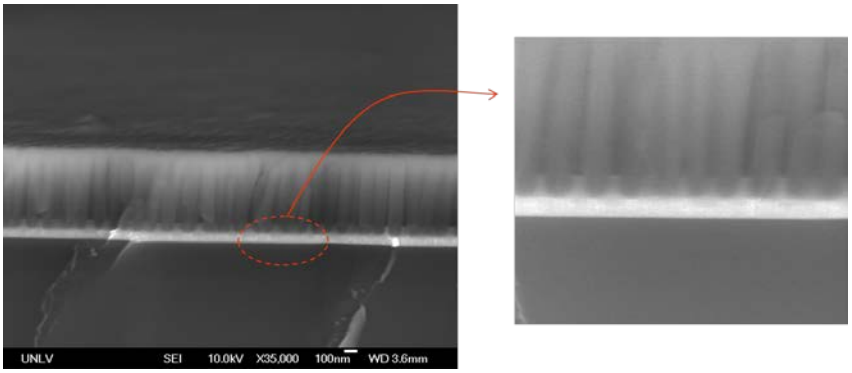


Figure 9. Cross-sectional scanning electron micrograph of CdTe formed inside the pores of a nanoporous alumina template

One of the problems encountered with electrochemical synthesis is that the growth rate was very low at room temperature. Another concern was the quality of the crystals formed at lower temperatures. The growth rate and the crystalline quality of the nanowires can be increased by carrying out synthesis at elevated temperatures, however, such an environment was found to be detrimental to the integrity of the nanoporous alumina templates. To address these issues, in this project a new technique, namely electrophoretic method, was investigated and developed for the synthesis of CdTe nanowires. This new technique involves the synthesis of nanowires through electrophoretic deposition of pre-synthesized nanoparticles in the presence of ultrasonic energy; the ultrasonic energy fuses the nanoparticles into a crystalline material inside the nanoporous template. This technique is promising for the creation of high crystalline quality nanowires with very high aspect ratio. High crystalline quality of the nanowire is important for efficient collection of the photo-generated carriers. On the other hand, increased nanowire length is required to increase the photocurrent. In the traditional electrochemical synthesis of nanowires, it has been found that the defect density increases with increasing thickness of the nanowires.

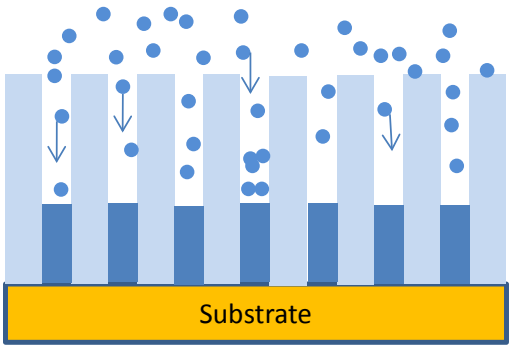


Figure 10. Schematic representation of the electrophoretic deposition process and the ultrasonic equipment used for the deposition.

The electrophoretic synthesis process is schematically shown in Figure 10. Pre-synthesized nanoparticles, typically crystalline in nature, are guided inside the pores of the nanoporous template through the application of an electric field. The guided nanoparticles are fused together by the ultrasonic energy which is applied during the deposition process. As mentioned earlier, one of the advantages of this technique is that the nanoporous alumina film is not exposed to the electrochemical synthesis process which can often involve elevated temperatures. To provide the directed electric field, the special sample holder developed for the anodization of aluminum films deposited on glass substrates was used. Towards the development of the fabrication process, gold nanoparticles were initially used as the nanoparticle material. Gold nanoparticles synthesized by the electrophoretic technique inside the nanoporous alumina templates in the presence of ultrasonic energy were investigated for different ultrasonic energies and duration. While collection of gold nanoparticles inside the pores could initially be observed, the complete fusion of the nanoparticles required extensive process optimization and fine tuning. The ultrasonic energy was varied over a wide range. It was observed that the samples with very high ultrasonic energy showed some damages to the template structure and while some of the gold nanoparticles show agglomeration, many of them were scattered and the confinement was lost. This was not unexpected. In the lower energy range, the samples showed agglomeration, but not complete fusion. It was necessary to determine the window of ultrasonic energy for which complete fusion of the nanoparticles may be obtained without damaging the structure of the nanotemplate. Once the process was developed, the synthesis of CdTe nanowires using the electrophoretic technique was investigated. The window of ultrasonic energy for this material was found to be different than that of gold nanoparticles, as expected. Extensive investigation was carried out to optimize the process parameters, however, complete fusion of the nanoparticles and breakdown of the nanoporous structure was common. Figure 11 shows the image of such a structure with disintegration of the nanoporous template and fusion with the nanoparticles.

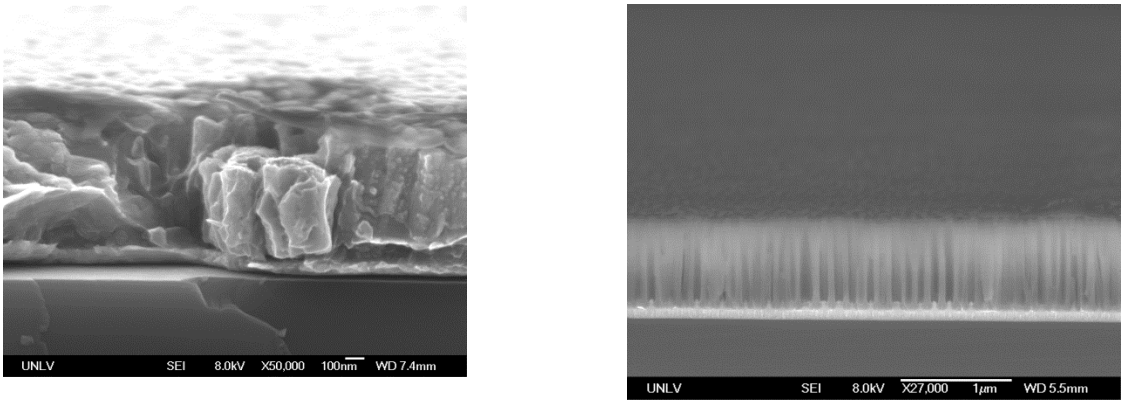


Figure 11. Left : an example of disintegrated template with fused nanoparticles during electrophoretic synthesis of CdTe. Right : Cross-sectional structure showing formation of CdTe nanowires.

One of the problems encountered with electrophoretic synthesis was the smaller length of the nanowires. For longer deposition time needed for longer nanowires, it was observed that the nanoporous template would disintegrate and fuse with the nanoparticles as described earlier. The samples that were created using increased ultrasonic energy to reduce longer deposition times showed discontinuity in the wires. Based on our analysis, it was determined that a lower temperature bath could mitigate some of the negative effects of the higher ultrasonic energy and provide superior quality films. Further investigations were carried out by fabricating additional samples using similar ultrasonic energy, however, in a lower temperature environment and good results were obtained as shown in Figure 12.

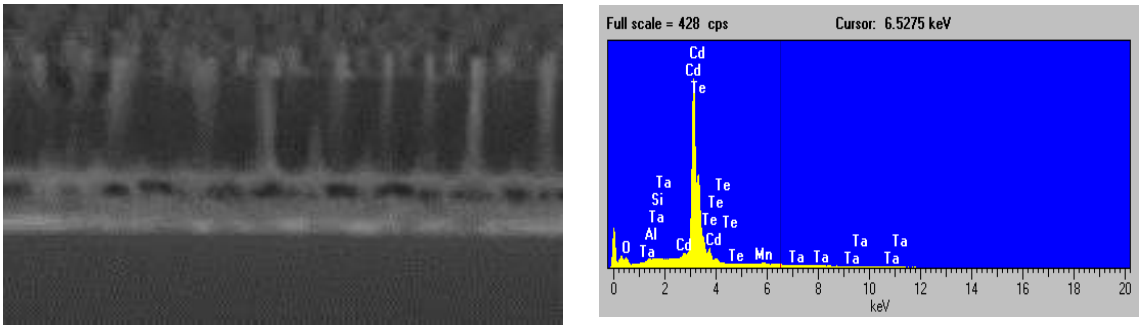


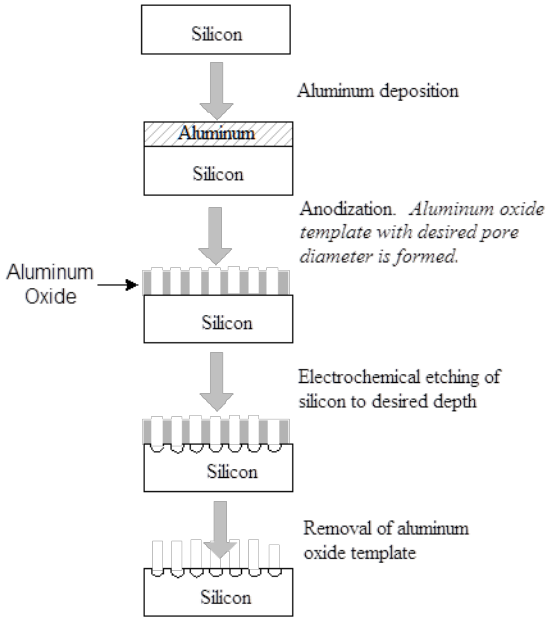
Figure 12. CdTe nanowires synthesized by guided synthesis through alumina template. Right : EDS spectra confirming correct composition of the deposited CdTe.

Ohmic contact formation

The CdTe nanowires fabricated inside the pores of the nanoporous alumina template form the active material of the nanostructure based solar cells. While the scanning electron microscope characterization demonstrated the formation of the CdTe nanowires, it was determined that photocurrent spectroscopy was required to provide information on the absorption properties of the nanowires. Such data can also provide valuable insight in the collection efficiency of the photogenerated carriers inside the nanowires. Formation of an ohmic contact on top of the nanowires is required for such measurements, the substrate underneath can provide the additional contact. Such ohmic contact formation is also an important step in the fabrication of solar cells. It was decided that both metal thin films and ITO films would be investigated for the formation of the ohmic contacts. As a first step towards this objective, thin gold films were identified to be used as the top contact layer. Gold films of thickness less than10 nm are routinely used for such test purposes, which can provide good electrical contacts as well as sufficient optical transparency. Gold thin films approximately 6 nm thick were deposited on the top surface of the nanowires using electron beam evaporation technique. A glass slide was also coated during the same deposition to measure the optical transparency, which showed 60% transparency. Electrical characterization of the ohmic contacts was carried out by using a 4 terminal resistance measurement apparatus. However, all the ohmic contacts were found to be non-conducting. Upon closer investigation it was observed that the metal layer was discontinuous due to uneven lengths of the nanowires from surface. While some of the metal penetrated the pores to contact the nanowires, there were obvious breakage all over the samples. To address this issue, it was determined that the surface needed to be polished to expose all the nanowires to the surface to enable improved contacting. Since the samples were only a few microns thick, it was critical to control the polishing process. Initially such polishing was carried out in a mechanical polishing device. However, since the samples were only a few microns thick, it was observed initially that the nanowire layers were almost completely removed. To address this, further polishing studies were carried out with more control on the polishing speed. However, upon further analysis and investigation, it was determined that a combination of mechanical and electrochemical polishing would be needed to provide better control on the polishing end point. The polishing process was further investigated and a combination of mechanical and electrochemical polishing process was developed to allow better contacting of the nanowires. While the nanowires could be electrically contacted using the thin gold films, the photocurrent spectroscopy proved to be difficult to measure using the equipment available due t the small volume of the active material.

Surface Texturing using nanotemplates

As described earlier, the nanoporous template provides an avenue to create uniform surface texturing features on solar cells for improved performance. While the technique can be used for both monocrystalline and multicrystalline silicon, the technique developed in this project will be most beneficial for the latter. The technique was first developed and optimized on single crystal silicon and was then transferred to multicrystalline silicon. The process steps involved (i) fabrication of thin film nanoporous alumina templates on silicon layers, (ii) characterization of the silicon/template interface using capacitance-voltage characteristics, (iii) etching of silicon through the template, and (iv) characterization of the textured surface. The process flow is schematically shown in figure on the left.



The process development was initially carried out on monocrystalline silicon; doped p-type silicon wafers were selected to provide better insight into the capacitance-voltage characteristics. A number of aluminum/porous alumina/p-Si MIS capacitors were fabricated using the following technique. P-type silicon substrates were first summa-cleaned, then immersed in a 1% HF bath, rinsed, and dried in N_2. Then, a 100 nm layer of Al was sputter deposited on the back of the wafer, followed by annealing at 450^o C for 30 minutes to form an ohmic back contact. Next, a 100 nm layer of Al was deposited on the top of the wafer, which was then annealed at 400^o C for 30 minutes to ensure good adhesion. The wafers were then anodized in 20% sulfuric acid at different current densities. Some of these wafers were then pore widened in 5% phosphoric acid for either 3 or 6 minute durations. The purpose of pore widening is to remove any remaining barrier layer (alumina) at the alumina/silicon interface, as well as to remove impurity ions left over from the anodization process. Next, metal contacts were created on top of the alumina templates created on silicon; the size and the shape of the metal contacts were controlled by the shadow masking technique. The metal contacts were circular in shape of approximately 1 mm in diameter. The schematic structure of the MIS capacitor structure is shown in Figure 13.

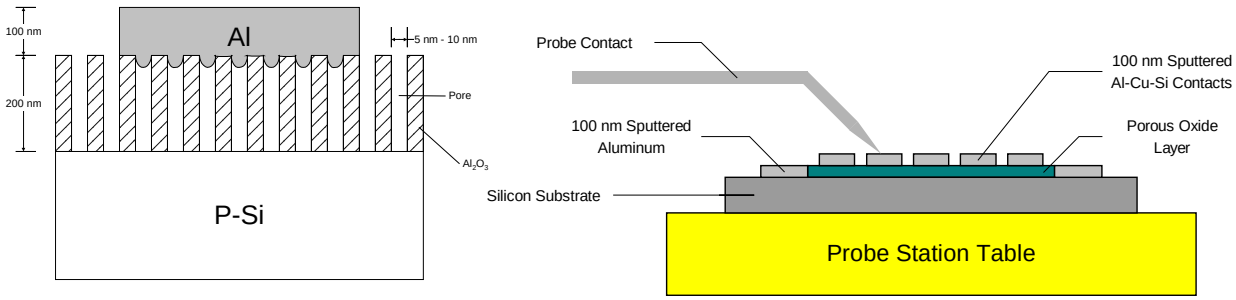


Figure 13. Schematic of the MIS device structure and the experimental setup for capacitance-voltage characterization.

Since capacitance-voltage characterization of the silicon/template interface can provide valuable information regarding the interface quality, specifically electrical properties of the interface, such

characetristics were measured on a number of samples fabricated using different current densities. Towards this goal, current-voltage (IV) measurements were performed on each capacitor sample to determine the range of bias voltages to be used for CV measurements. A typical current-voltage result is shown in Figure Y. On each wafer, the devices with the lowest leakage currents were selected for CV measurements. Capacitance-voltage measurements were performed at a frequency of 1.0 MHz. The bias voltage was varied between–5 VDC to +5 VDC. For each of the selected devices, multiple CV scans were taken and the data were averaged to provide a characteristic profile for a single device. The CV measurements were carried out in the dark to avoid photocurrent effects. Figure 14 shows the typical C-V

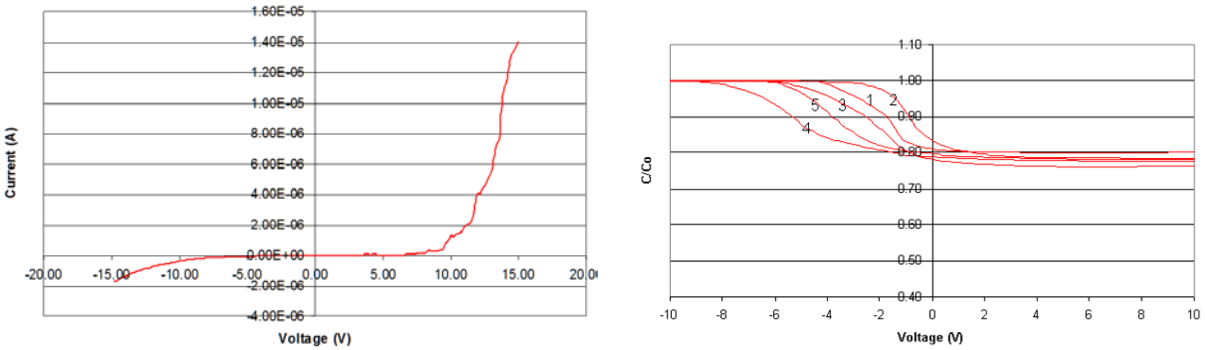


Figure 14. Typical current-voltage and capacitance-voltage results for MIS structures fabricated on monocrystalline silicon.

characteristics obtained on an MIS structure fabricated on a monocrystalline silicon wafer, which shows the alumina/silicon interface to be of good quality as indicated by the formation of accumulation, depletion and inversion layers, as expected for an MIS structure. This is encouraging for the application of this technique for performance improvement of solar cells. . The CV data were analyzed to calculate device parameters such as theoretical carrier density, threshold voltage, and flatband voltage. The carrier density of the substrate was calculated and compared with the known substrate density for verification, which matched very well.

The threshold voltages for each capacitor were obtained from the CV data using the relationship:

$$V_{TH} = V\ (C_{inv} + (C_0 - C_{inv}).0.05);$$

this is the voltage at which the capacitance drops to 5% of the difference between its maximum and minimum values. For each anodization current density, the threshold voltages are obtained for different capacitor pad of the various samples. The CV data was also used to calculate the flat-band voltages using the expression:

$$V_{FB} = V\ (C_0 - (C_0 - C_{inv}).0.05);$$

this is the voltage at which the capacitance drops to 95% of the difference between its maximum and minimum values. Although the flatband voltage showed a large distribution, an average value for the samples was calculated to be –3.29 V.

After considering C_o of each capacitor, it is simple to calculate the dielectric constant for each sample using the following relationship:

$$\varepsilon = \frac{C_0 \cdot t_{ox}}{\varepsilon . A}$$

where C_o is the oxide capacitance (F), t_{ox} is the oxide thickness (m), and A is the area of the top contact (m^2); the results obtained matched well with published data, which further confirmed the validity of our analysis. While cross-sectional imaging of the samples was made difficult by the small dimensions of the pores, and the very high resistivities of the alumina layers (which caused charging during scanning electron microscopy), we have carried out the following analysis that provide some insight into the characteristics of the porous alumina layer. Although the thin film alumina template is a complex porous structure, the total accumulation capacitance C_o may be approximated as two capacitances in parallel:

$$C_0 = C_{air} + C_{al}$$

where C_{air} is the capacitance due to the air-filled pores, and C_{al} is the capacitance due to the porous alumina layer. Since the walls are constructed of alumina, with a dielectric constant of approximately 9.7, and the pores are filled with air, which, by definition, has a dielectric constant of 1.0:

$$C_o = \frac{\varepsilon_{air} \cdot \varepsilon_o \cdot A_{air}}{t_{air}} + \frac{\varepsilon_{al} \cdot \varepsilon_o \cdot A_{al}}{t_{al}}$$

It is known that the porosity, P (ratio of pores to total area), is quite high. It is also known that the thickness of the alumina layer after anodization (t_{al}) is at least 200 nm from fabrication parameters. And finally, it is known that the thickness of the air layer should be less than that of the alumina layer. If these three quantities are considered across a short range, viable measurements of pore dimensions may be estimated using the above relationship. From these calculations, the porosity of the samples was found to be around 80%, which is close to what is expected for the anodization parameters used. It is also interesting to note that, as the thickness of the alumina is increased, the thickness of the air layer approaches an asymptote near 100 nm. Therefore, regardless of the actual porosity, the air layer is at least 100 nm thick. It may thus be inferred that the aluminum top contact, which is sputter deposited on top of the pores, enters the pores by no more than 100 nm.

Following the encouraging results, the process developed on monoicrystalline silicon was then transferred to multicrystalline silicon. Multicrystalline silicon was prepared by sputter deposition of silicon on a glass substrate.. Fabrication of multicrystalline silicon by sputter deposition is an established process and parameters from the literature were used for this project. Before the deposition of the silicon, a thin layer of aluminum was deposited on the glass substrate to provide an ohmic contact for anodization. The silicon was then coated with a layer of aluminum about 100 nm thick. Sputter deposited aluminum was initially used, however, as they did not show good uniformity, electron beam evaporation was used for further deposition. It may be noted that the aluminum was deposited on silicon in situ without breaking vacuum. The aluminum was then anodized using the process parameters developed previously and the samples were characterized using cross-sectional imaging and C-V characterization. While the C-V data did not look as precise as the results for monocrystalline silicon and showed lareg sample-to-sample variation, however, the low leakage current in the structures and the presence of some C-V variation confirmed the high quality of the alumina silicon interface. In order to achieve texturing of the multicrystalline silicon surface, the silicon was next etched through the pores in the anodized alumina template. Instead of conventional chemical etching, it was decided to use electrochemical etching as the etch rate is faster and creates structures with improved side walls. A solution of HF and H_2O_2 was used in an electrochemical cell to perform the electrochemical etching. A current density of 90 mA/cm^2 was used for the first run; however, SEM data showed that while the silicon was etched through the template, the template was also

partially etched. In order to prevent template etching, three different current densities were used to etch a number of samples and 85 mA/cm^2 was determined to provide the optimum results. An scanning electron microscope top view image of the etched sample is shown in Figure 15. It may be noted that he pore size uniformity is degraded by the etching process indicating further precise tuning of the process.

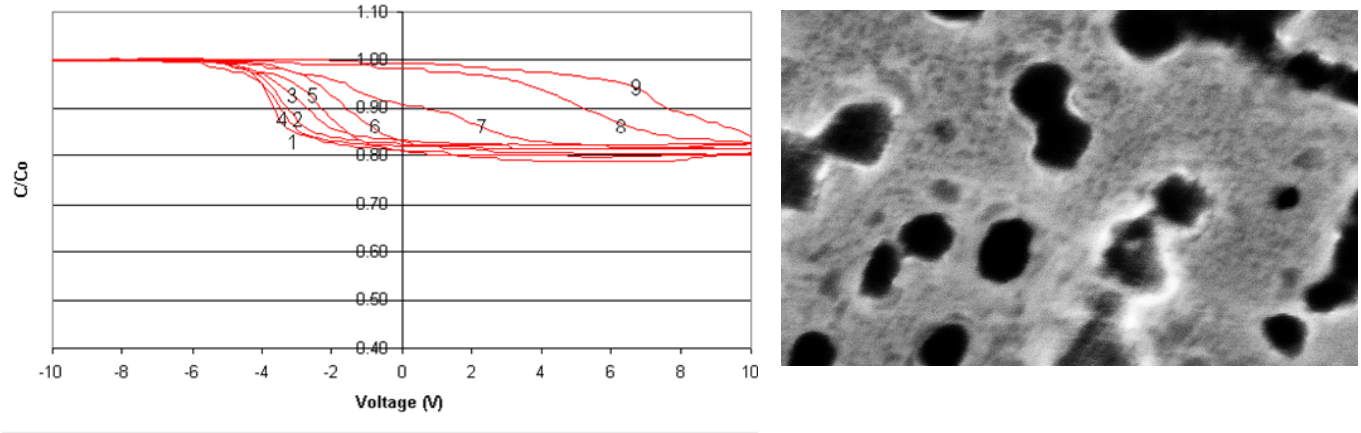


Figure 15. Left : typical capacitance-voltage characteristics of an MIS structure fabricated on multicrystalline silicon. The C-V characetristics show more variation due to non-crystalline nature of the material. Right : Scanning electron microsope image of silicon etched through the nonporous alumina layer.