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Ultrafast Power Processor for Smart Grid

Power Module Development

EP-P37924-C17010

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Technical Update, December 2012

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ABSTRACT

This project's goal was to increase the switching speed and decrease the losses of the power semiconductor devices and power switch modules necessary to enable Smart Grid energy flow and control equipment such as the Ultra-Fast Power Processor. The primary focus of this project involves exploiting the new silicon-based Super-GTO (SGTO) technology and build on prototype modules already being developed. The prototype super gate-turn-off thyristor (SGTO) has been tested fully under continuously conducting and double-pulse hard-switching conditions for conduction and switching characteristics evaluation. The conduction voltage drop measurement results indicate that SGTO has excellent conduction characteristics despite inconsistency among some prototype devices. Tests were conducted with two conditions: (1) fixed gate voltage and varying anode current condition, and (2) fixed anode current and varying gate voltage condition. The conduction voltage drop is relatively a constant under different gate voltage condition. In terms of voltage drop as a function of the load current, there is a fixed voltage drop about 0.5V under zero current condition, and then the voltage drop is linearly increased with the current. For a 5-kV voltage blocking device that may operate under 2.5-kV condition, the projected voltage drop is less than 2.5 V under 50-A condition, or 0.1%. If the device is adopted in a converter operating under soft-switching condition, then the converter can achieve an ultrahigh efficiency, typically above 99%. The two-pulse switching test results indicate that SGTO switching speed is very fast. The switching loss is relatively low as compared to that of the insulated-gate-bipolar-transistors (IGBTs). A special phenomenon needs to be noted is such a fast switching speed for the high-voltage switching tends to create an unexpected C·dv/dt current, which reduces the turn-on loss because the dv/dt is negative and increases the turn-off loss because the dv/dt is positive. As a result, the turn-on loss at low current is quite low, and the turn-off loss at low current is relatively high. The phenomenon was verified with junction capacitance measurement along with the dv/dt calculation. Under 2-kV test condition, the turn-on and turn-off losses at 25-A is about 3 and 9 mJ, respectively. As compared to a 4.5-kV, 60-A rated IGBT, which has turn-on and turn-off losses about 25 and 20 mJ under similar test condition, the SGTO shows significant switching loss reduction. The switching loss depends on the switching frequency, but under hard-switching condition, the SGTO is favored to the IGBT device. The only concern is during low current turn-on condition, there is a voltage bump that can translate to significant power loss and associated heat. The reason for such a current bump is not known from this study. It is necessary that the device manufacturer perform though test and provide the answer so the user can properly apply SGTO in pulse-width-modulated (PWM) converter and inverter applications.

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1
INTRODUCTION

Power electronics technologies are critical to the success of the smart grid. Inverters are required to interface photovoltaic and storage with the grid. Large converters are required as part of the transmission infrastructure build out for strategic HVDC links. Static compensators are needed at both the transmission and distribution levels to help manage the system voltage, improve power flow capability of the infrastructure, and assure system stability. Brand new technologies are also likely to play an important role. One of these technologies is the "Intelligent Universal Transformer" proposed by EPRI to provide a flexible interface to customers, distributed generation, renewable, distributed storage, and electric vehicle chargers. All of these technologies for the smart grid have one thing in common – they need new solid state switch devices that have better switching characteristics and lower losses.

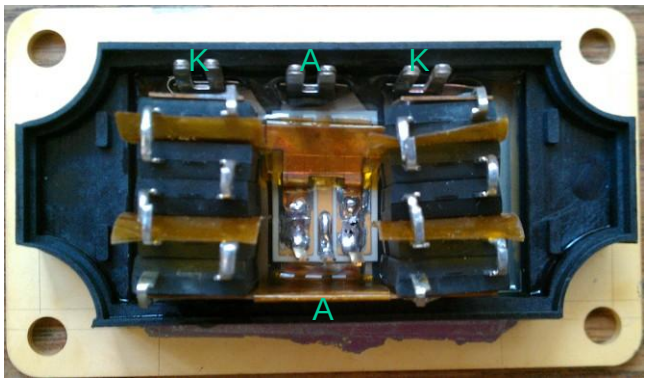
This project focused on the development and testing of an advanced switch developed by Silicon Power called the Super Gate Turn-Off (SGTO) switch. The overall goal for advanced switch development was to increase the switching speed and decrease the losses of the power semiconductor devices and power switch modules necessary to enable Smart Grid energy flow and control equipment. The primary focus involves exploiting the new silicon-based Super-GTO (SGTO) technology and builds on prototype modules already being developed.

Project Objective

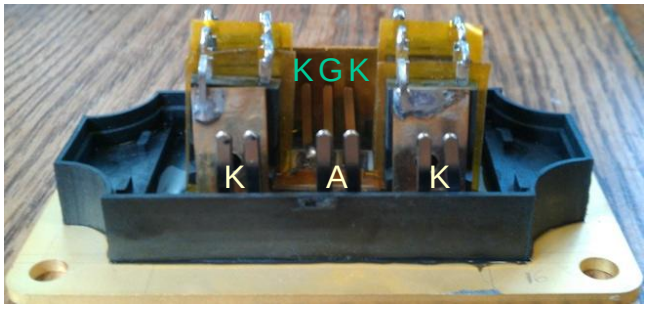
The objective of this project is to characterize the switching behavior of the newly developed super gate-turn-off thyristor (SGTO) module under the conventional hard switching condition. In addition, comparison of the SGTO against available IGBT-based (prior art) modules will be made to quantify the switching speed and efficiency improvement

The SGTO module contains one phase leg of SGTO devices and anti-paralleled diodes. The module has been characterized under soft-switching condition and demonstrated in pulse power applications [1–8].

Figures 1-1(a) and 1(b) show the top view and front view of the photograph of the SGTO module to be characterized. The SGTO chip is rated 3.6kV peak [1]. Due to unavailability of the matched high-voltage ultrafast reverse recovery diode, the SGTO chip is anti-paralleled with series stacked commercially available 1.2-kV silicon diodes.



(a)



(b)

Figure 1-1: Photograph of the SGTO module to be tested: (a) top view and (b) front view.

To verify performance, the testing of the SGTO modules were carried out at two independent locations

- Silicon Power Corporation (SPCO) facility in Malvern PA
- Enertronics facility in Blacksburg VA

References

[1] HB-INC-5N01 Power Semiconductor Half-Bridge Module™ Data Sheet (Rev 0 - 02/06/09), Silicon Power, Feb. 2009.

[2] HB-HVI-5N002 Power Semiconductor Half-Bridge Module™ Data Sheet (Rev 0 - 02/06/09), Silicon Power, Feb. 2009.

[3] V. Temple, " 'Super' GTO's Push the Limits of Thyristor Physics," in *Proc. of 35th IEEE Power Electronics Specialists Conference*, Aachen, Germany, June 20-25, 2004, pp. 604–610.

[4] T.F. Podlesak, R.L. Thomas, F.M. Simon, "Preliminary evaluation of super GTOs in pulse application," *IEEE Transactions on Plasma Science*, Vol 33-4, pp. 1235-1239, August 2005.

[5] R.L. Thomas, H. O'Brien, W. Shaheen, and S.B. Bayne, "Evaluation of a 7kV, 80 kA SGTO Module," in *Proc. of 15th IEEE International Pulsed Power Conference*, June 13-17, 2005, pp. 916 – 918.

[6] K. Brandmier, “SolidtronTM CCSTA14N40 N-Type, ThinPakTM Preliminary Data Sheet,” Silicon Power Corp., Malvern, PA, 2005.
[7] H. O’Brien, et al., “Evaluation of Advanced Si and SiC Switching Components for Army Pulsed Power Applications,” *13th EML Symposium*, unpublished.
[8] H. O’Brien, W. Shaheen, T. Crowley, and S.B. Bayne, “Evaluation of a 10 kV, 400 kA Si SGTO at High dI/dt,” *IEEE Power Modulator Symposium*, May 2006, pp. 236 – 239.

2
DESIGN OVERVIEW

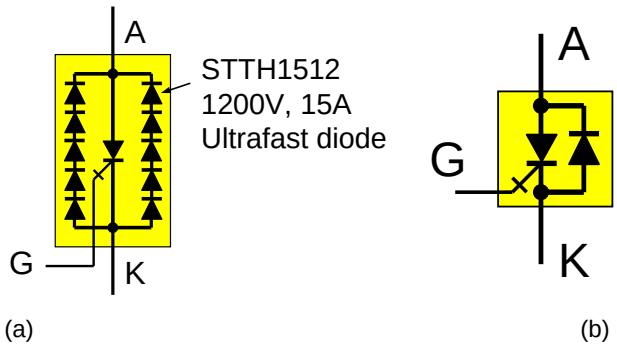
Previous design attempts generated an integrated half-bridge module inclusive of an upper/lower SGTO/w anti-parallel series connected Si-diodes and associated optically/electrically isolated gate drivers. Some of the short comings of this design direction were difficult thermal management, electrical isolation, voltage breakdown of parts as well as dielectrics. The modules were also difficult to scale for voltage and current requiring different modules for the AFE/RFE topologies.

The design philosophy for this project includes:

- Separate out the major functions, to allow for easier access, measurement and characterization of the device and module's operational parameters and to establish device/module benchmark tests necessary to guarantee performance in the AFE/RFE applications
- Make a universal module that could be easily series and/or parallel connected for higher voltage and current
- Allow for various thermal management alternatives (forced air/thermal electric coolers/heat pipes/liquid cooled/refrigerants)
- Arrive at a scalable isolated power supply system that would allow easy powering of the high/low-side power stage gate drivers
- Allow for some level of diagnostics and easy replacement in the event that became necessary

The main objective of this project is to characterize the SGTO module under two-pulse hard-switching condition to verify its di/dt capability and to find the switching energy under turn-on and turn-off conditions. The results will be compared with those of silicon insulated-gate-bipolar-transistor (IGBT) and silicon carbide (SiC) metal-oxide-semiconductor-field-effect-transistor (MOSFET). Their switching energy will be used to estimate the power conversion system efficiency under different switching frequency conditions.

Figure 2-1(a) shows actual internal circuit of the SGTO module. There are two sets of series stacked diode in parallel to increase the current rating of the diode. Each series stack consists of five 1200-V, 15-A rated ultrafast reverse recovery diodes. The simplified SGTO module symbol can be represented in Figure 2-1(b), which is a standard module symbol with three terminals: anode (A), cathode (K), and gate (G).



(a) (b)

Figure 2-1: Symbols showing SGTO and diode combined module: (a) actual internal circuit of the module and (b) simplified SGTO module symbol.

3
MODULE CHARACTERIZATION PLAN PERFORMED AT SPCO LABORATORY

This test will be performed using a high voltage pulse tester (as shown in Figure 3-1 below) and with an inductive load. A matched diode must be used across the device to evaluate the switching characteristics. In general, in the case of an SGTO/IGBT, the switching speed is fast, but the high-voltage diode is very slow in reverse recovery. When the switch is turned on, it needs to turn off the freewheeling diode, and a slow reverse recovery diode will cause large recovery related turn-on loss. Hence, the diode is an important part of this test setup. The choice of the diode is up to Silicon Power.

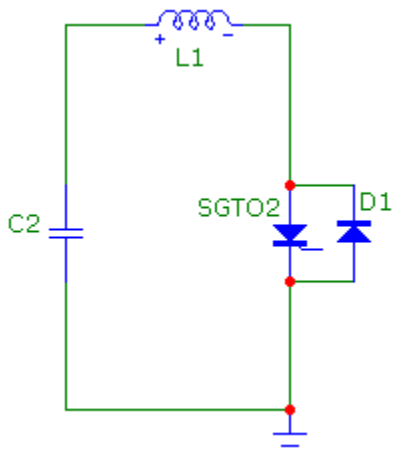


Figure 3-1 Module Test Circuit

Device Loss Evaluation

The objective of this test is to evaluate the losses of the SGTO and compare their performance with a comparable IGBT. The testing is organized as follows:

Evaluation of losses

1. Each device is subject to a pulse test. From the waveform recorded, the following are calculated:
    a. Turn-on loss (mJ): E_{on}
    b. Turn-off loss (mJ): E_{off}
    c. Conduction loss: E_{cond}
    d. Total loss per pulse/cycle: $E_{total} = E_{on} + E_{off} + E_{cond}$

2. Repeat above test for anode/collector current in 10% increments up-till rated current.
3. Plot the following charts

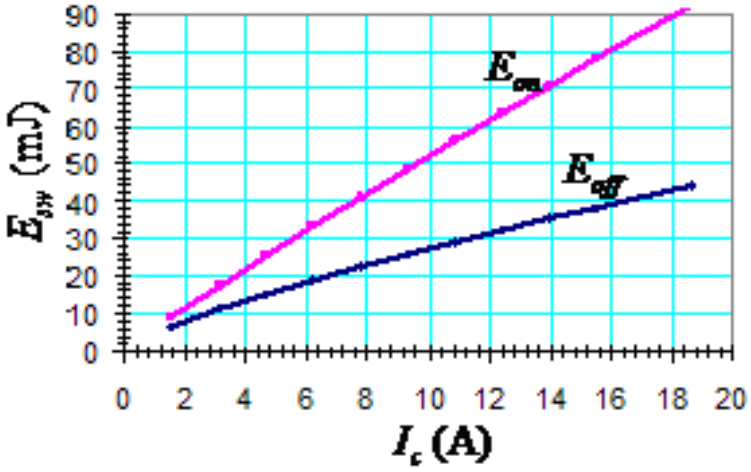


Figure 3-2: Sample Plot Energy vs. Current (Hard Switching HV IGBT-FZ200R65KF1 Switching Energy Projected at 3.75kV Condition)

Suitability for Continuous Switching Frequency Applications

1. Using the data obtained above, evaluate power loss for simple half bridge circuit operating at various switching frequencies (up-to what is deemed as maximum for the device).
2. Plot Efficiency vs. Rated Converter Power Output chart

Thermal Characteristics

The device junction temperature can be estimated using the sum of conduction and switching losses and the respective thermal resistances. The junction temperature of the device is evaluated using a thermal model and the loss data recorded earlier. Using a thermal model with known thermal coefficients (R_{jc}, R_{ha}), the junction temperature is evaluated. In lieu of this, other direct measurements wherever available can also be used to predict the junction temperature. At a minimum the case and heat sink temperatures must be monitored.

A basic thermal model for the SiC Diode SGTO module shall be submitted after evaluation.

Static Voltage-Current Characteristics

This test plots the standard V-I characteristics of the device. An example of a static V-I curve for a thyristor is shown as follows:

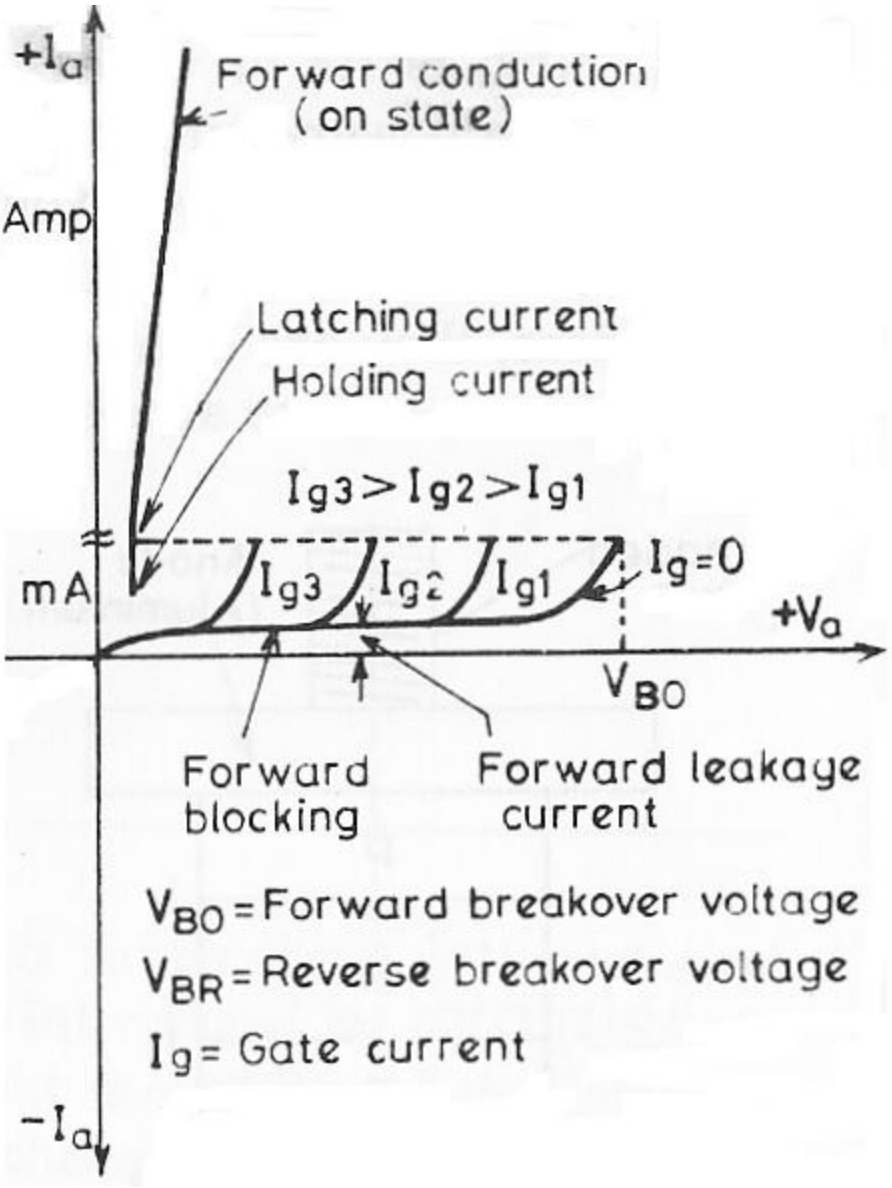


Figure 3-3: Sample V-I Curve with definitions

Waveform Analysis

As part of this test, the turn-on and turn-off behavior of the device is captured on a high-bandwidth oscilloscope. Each device is subject to a single pulse test. The waveforms are captured at rated (18-20A), 90% rated, and 10% rated current at 3500V blocking voltage. The following parameters are recorded:

- Voltage across SGTO/IGBT: V_{AK} / V_{CE}
- Current through SGTO/IGBT: I_A / I_C
- Gate voltage: V_G
- Gate current: I_G

Typical examples of these waveforms are shown in Figure 3-4.

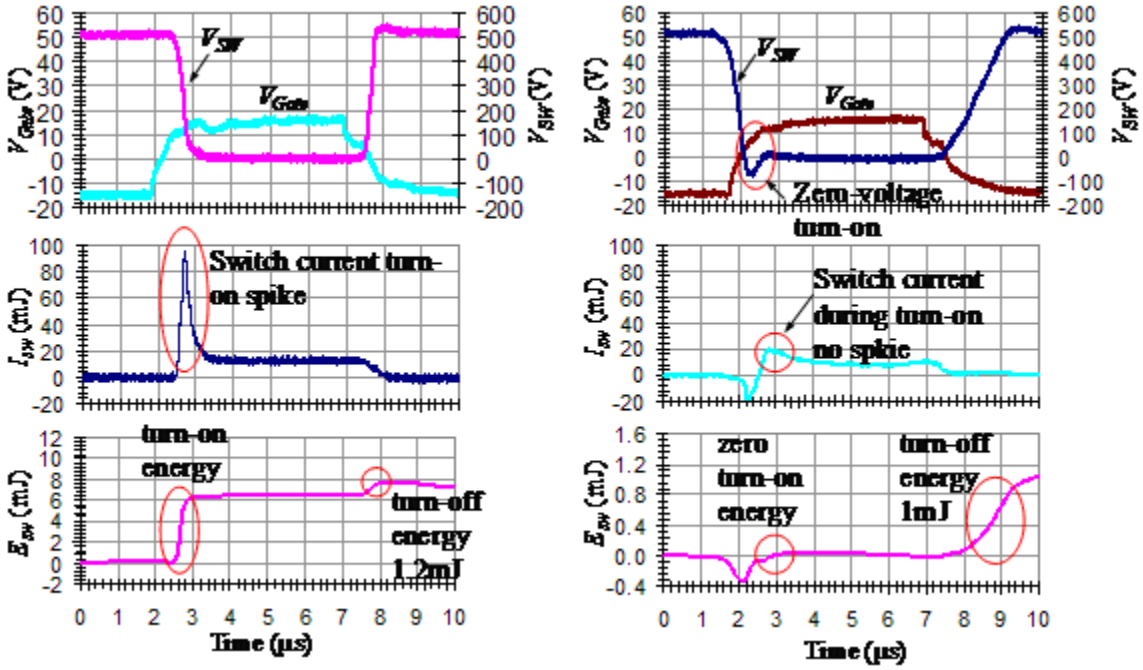


Figure 3-4: Typical waveforms from 6.5KV 200A Infinion IGBT

Figure 3-5 through Figure 3-113 shows the characterization of the Si SGTO modules. Figure 3-5 and Figure 3-6 are snapshots (survey shots) of the waveform captures that were recorded during testing.

Figure 3-5 is the survey shot that is used for deriving gate energy and conduction loss Figure 3-7 and Figure 3-8. The conduction losses reported in Figure 3-8 is about 4.048MW/sec.

Figure 3-6 is the survey shot that is used for deriving turn-on losses, turn-off losses, fall time, storage time, time delays which are shown in Figure 3-9 through Figure 3-13. The turn-on and turn-off losses captured were 38µJ and 3.8mJ, respectively. The fall time and storage time is 40nsec and 1.84µs. The time delay (10% of the gate to 90% of when the voltage collapses) is 152nsec. The current value in Figure 3-5 through Figure 3-13 is about 36A.

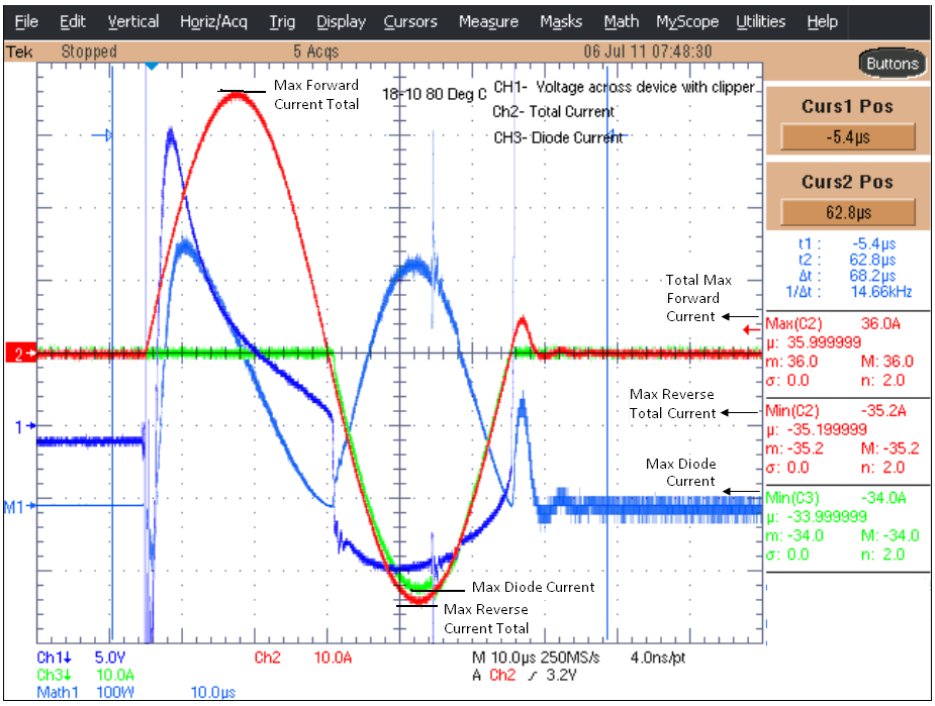


Figure 3-5: SGTO Si-Module -Setup 1 –Screen Survey Shot

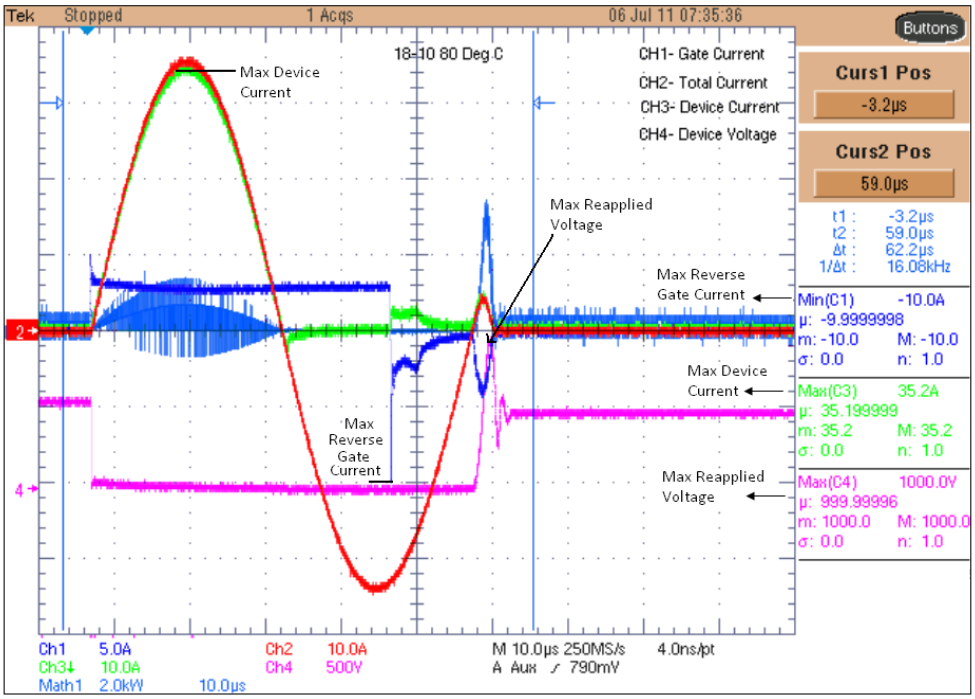


Figure 3-6: SGTO Si-Module -Setup2 –Screen Survey Shot

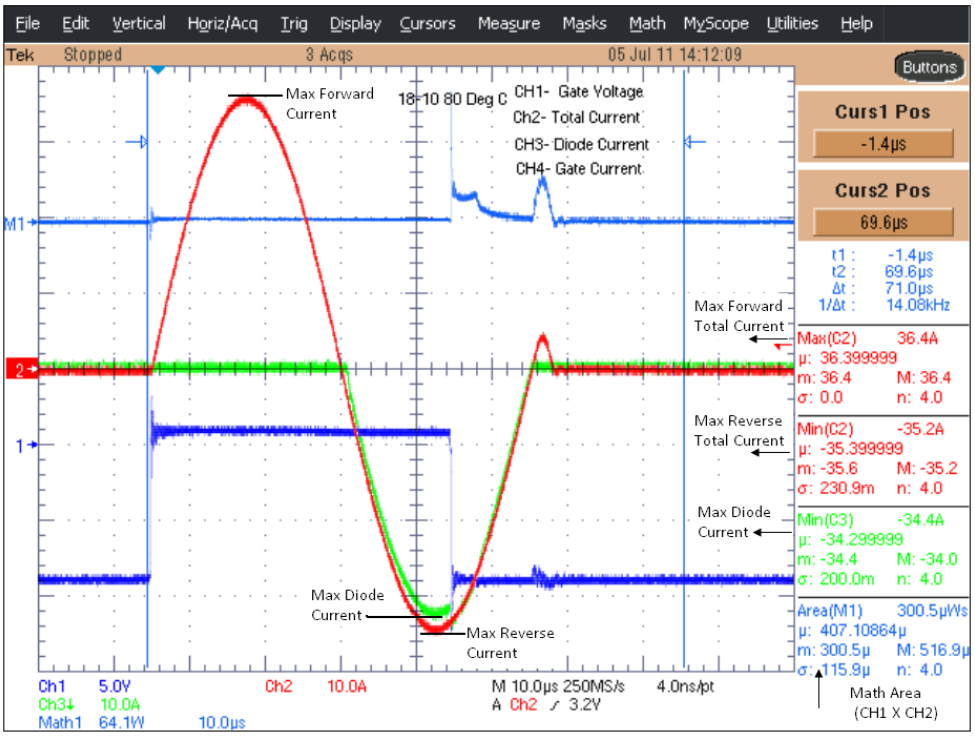


Figure 3-7: SGTO Si-Module -Setup3– E_g (Gate Energy trace labeled "M1")

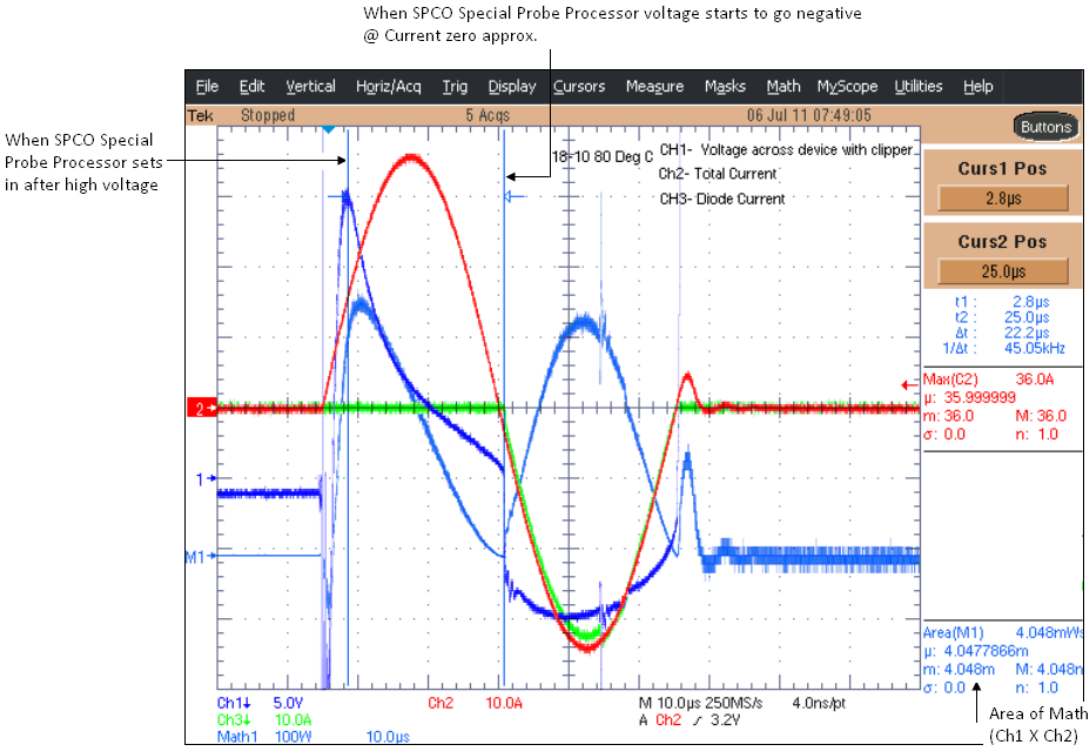


Figure 3-8: SGTO Si-Module -Setup4– E_{cond} (Conduction Losses)

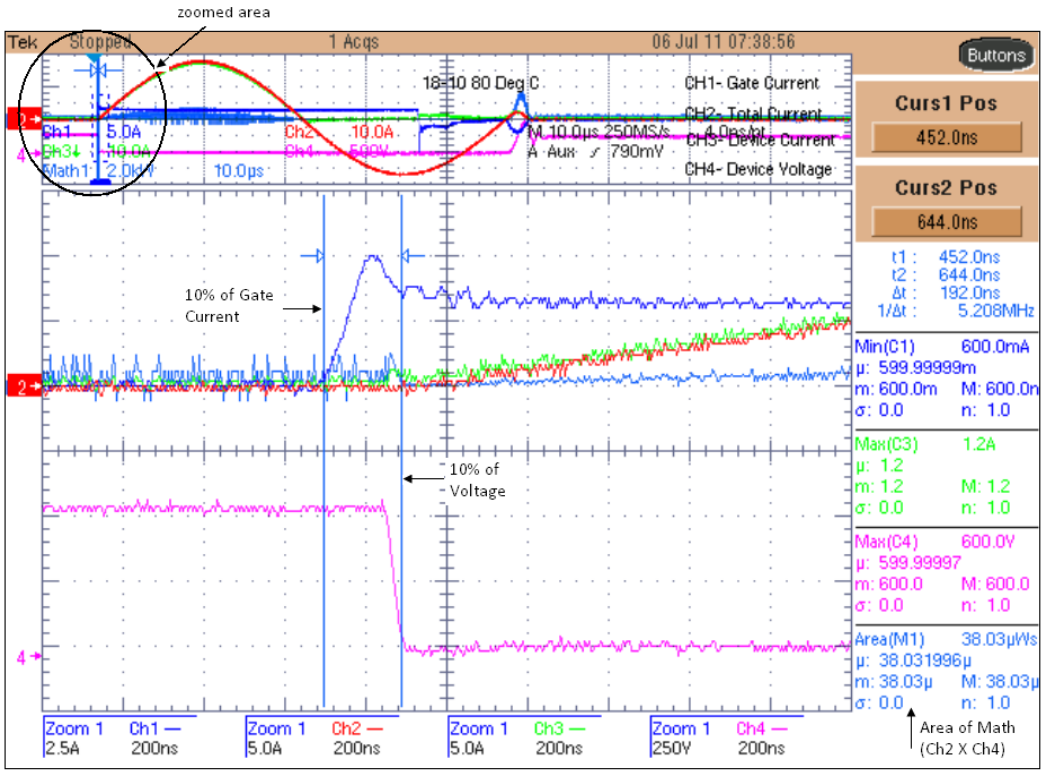


Figure 3-9: SGTO Si-Module -Setup5– E_{on} (Turn-on Losses)

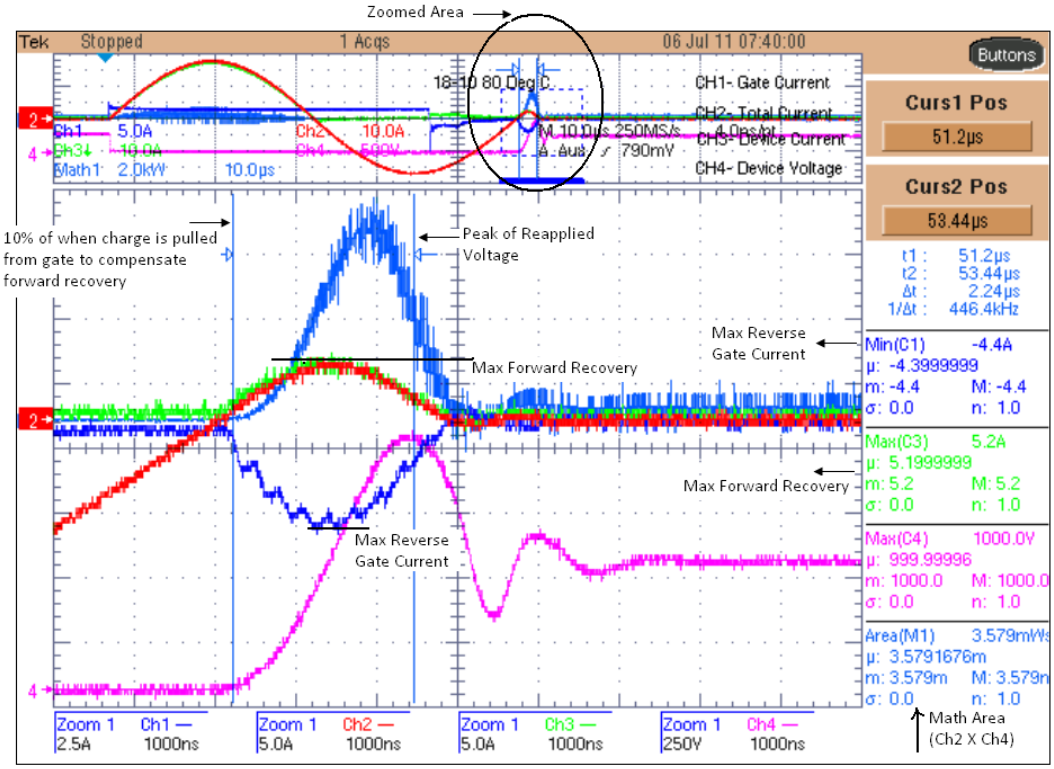


Figure 3-10: SGTO Si-Module -Setup6 - E_{off} (Turn-off Losses)

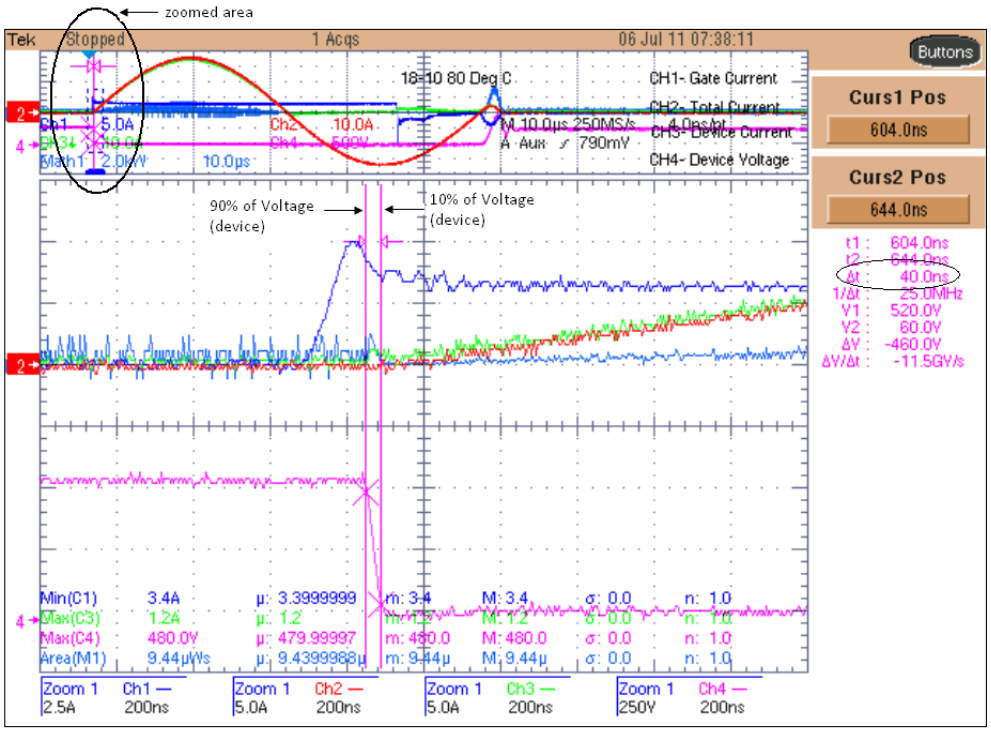


Figure 3-11: SGTO Si-Module -Setup7– Fall Time

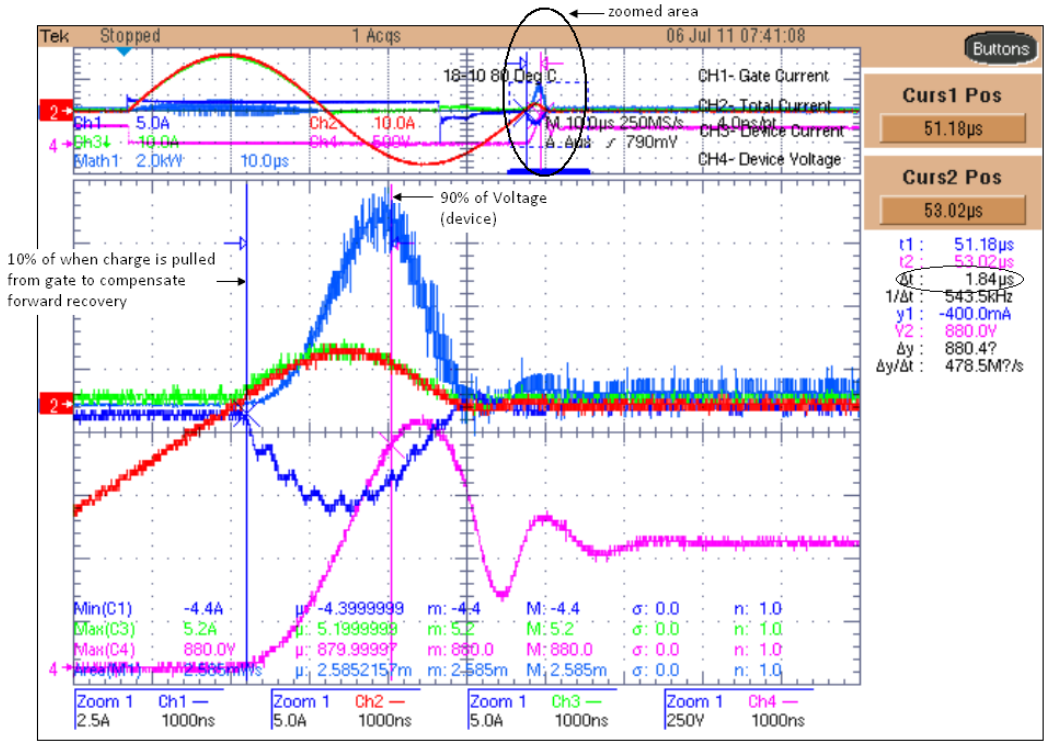


Figure 3-12: SGTO Si-Module -Setup8– Storage Time

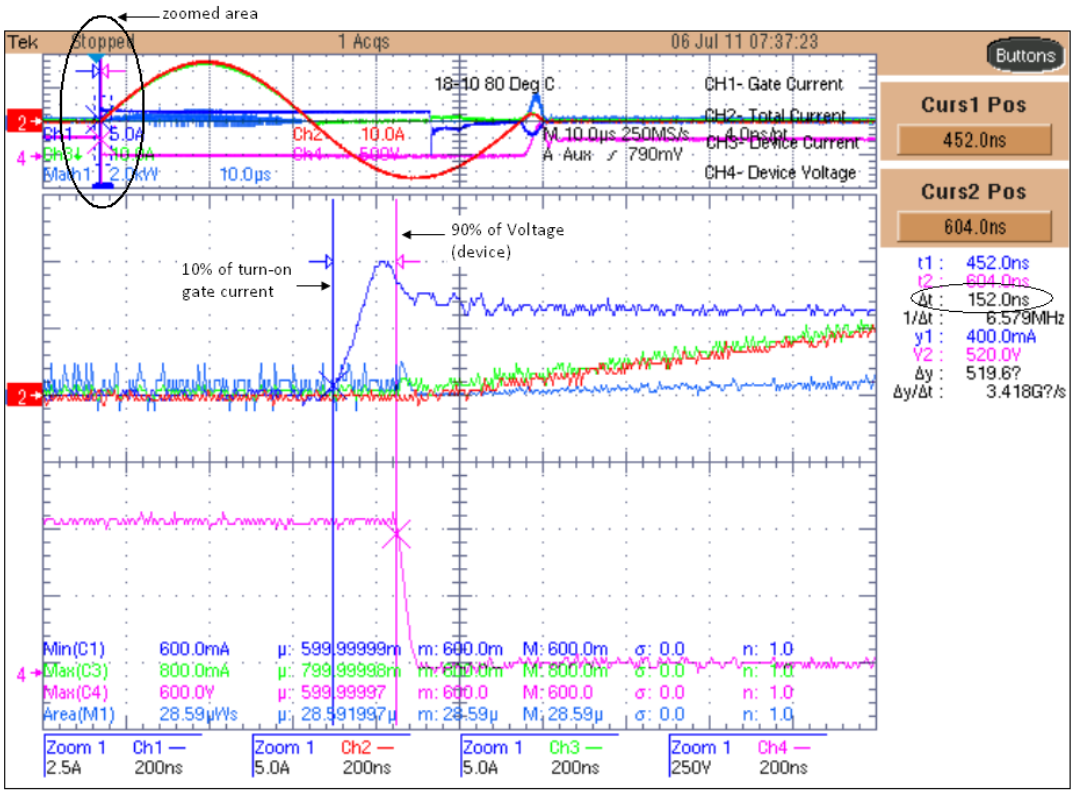


Figure 3-13: SGTO Si-Module -Setup9– Time Delay

4

SI-DIODE/SGTO BASED MODULE TEST RESULTS PERFORMED AT SPCO LABORATORY

This chapter presents the data obtained from the tests conducted at Silicon Power facility in Malvern, PA. The Si-diode version of the SGTO modules underwent various tests for characterization; a summary is presented below.

The following results are presented in this section:

1. Hard Turn-off Test
2. Soft/Resonant Turn-off Test
3. Thermal Model
4. V-I Characteristics

Module Test Circuit

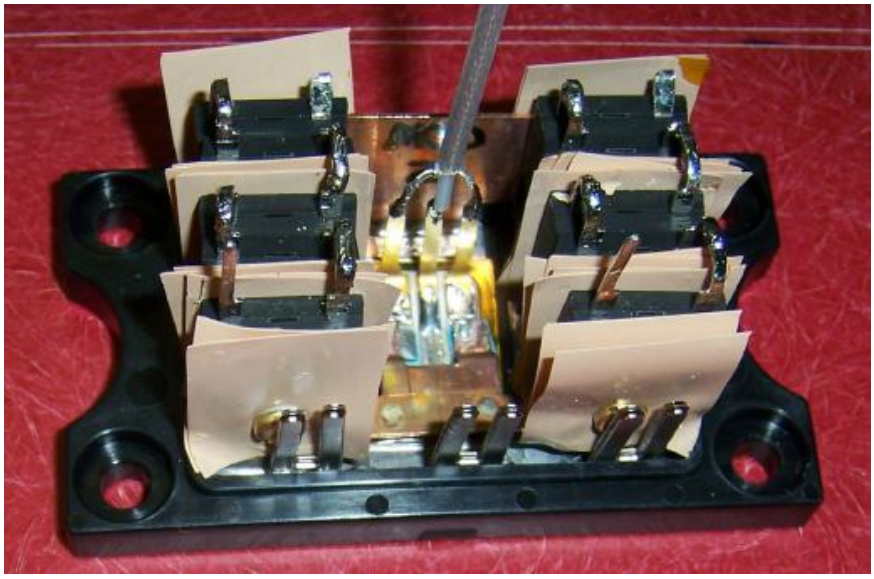


Figure 4-1: Si-diode/SGTO based module

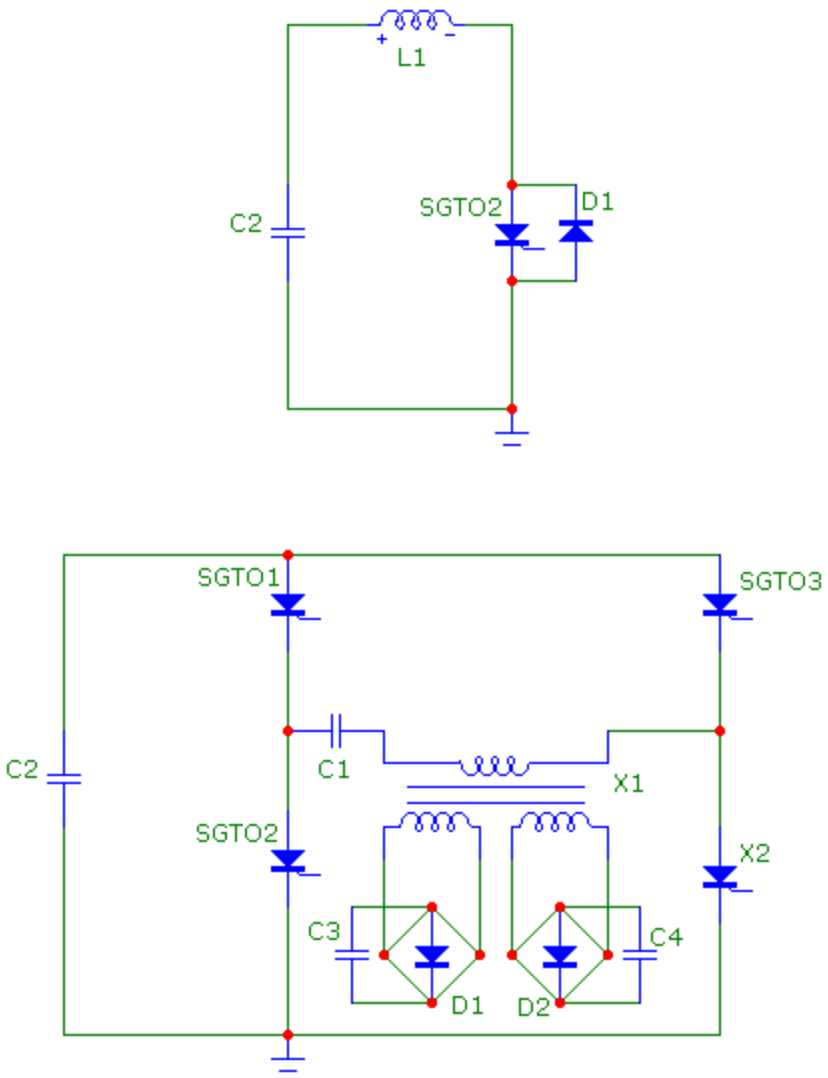


Figure 4-2: Module Test Circuits

Hard and Resonant Switching -Module Test Results

The SGTO modules with Si Diodes were tested using the circuits above. The following section presents the data set and the curves (for hard switching) for the turn-off energy and turn-on energy tested as per the test plan presented in the previous section.

Test Data for Turn-off Energy - Module#18

Table 4-1 and 4-2 present the data set for the hard turn-off and soft/resonant turn-off for representative module #18 respectively.

Table 4-1: Hard turn-off data at 30ºC for Module #18

Hard Turn off-30°C		
Current Apk	**Reapplied Voltage, Vpk**	**Turn-Off Energy mJ**
15.2	3800	44.25
20	3860	47.96
30	4040	45.55
40	4260	49.13

Table 4-2: Soft/Resonant Turn-off at 30ºC for Module #18

Capacitance, uF	Turn-off Time, us	Reapplied Voltage, Vpk	Current, Apk	Turn-Off Energy, mJ
.05uf	16	3500	20.49	2.858
.1uf	24	3500	28.81	2.701
.15uf	29	3500	34.8	2.119
.3uf	42	3500	48	1.062
.45uf	51	3500	56	0.6363
.6uf	60	3500	64.8	0.461

The following graph (Figure 4-3) shows the turn-off energy vs. peak current under both hard turn-off and resonant turn-off type topology for module#18.

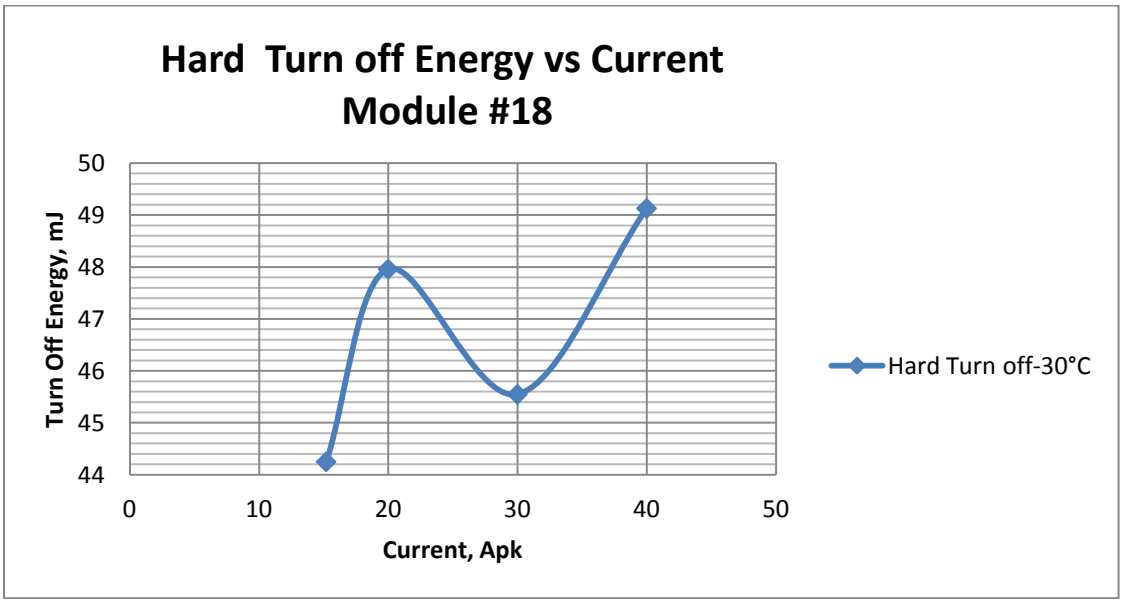


Figure 4-3: Hard and Resonant Turn-off Energy Curves – Module #18

Test Data for Turn-on Energy- Module#18

Table 4-3 shows the data obtained while testing module #18. The turn-on losses were captured for a rated current of 20A (28A peak). On further investigation, we found that turn-on energy is so small that it is negligible compared to rest of the losses and we are exceeding the instrumentation capabilities. New set-up for measurement is in the process of being developed.

Table 4-3: Turn-on Energy at 30ºC for Module # 18

Reapplied Voltage, V	3500
Time Delay, nsec	184
Fall Time, nsec	92
Eon, mJ	0
Current, A	30

Test Data for Turn-off Energy- Module#11

Table 4-4 and 4-5 present the data set for the hard turn-off and soft/resonant turn-off for representative module #11 respectively.

Table 4-4: Hard turn-off data at 30ºC for Module #11

	Hard Turn off-30°C	
Current Apk	**Reapplied Voltage, Vpk**	**Turn-Off Energy mJ**
18.4	3500	31.3
20	3560	33.4
33	3680	47.2
40.8	3760	62.3

Table 4-5: Soft/ Resonant Turn-off at 30ºC for Module #11

	Resonant Turn off-30°C			
Capacitance, uF	**Turn-off Time, usec**	**Reapplied Voltage, Vpk**	**Current, Apk**	**Turn-Off Energy, mJ**
.05uf	16	3300	22	20.02
.1uf	24	3480	30.4	26.35
.15uf	29	3500	37.6	24.68
.3uf	42	3540	52.8	19.49
.45uf	51	3500	64	14.93
.6uf	60	3520	74.4	12.94

The following graph (Figure 4-4) shows the turn-off energy vs. peak current under both hard turn-off and soft turn-off type topology for module#11.

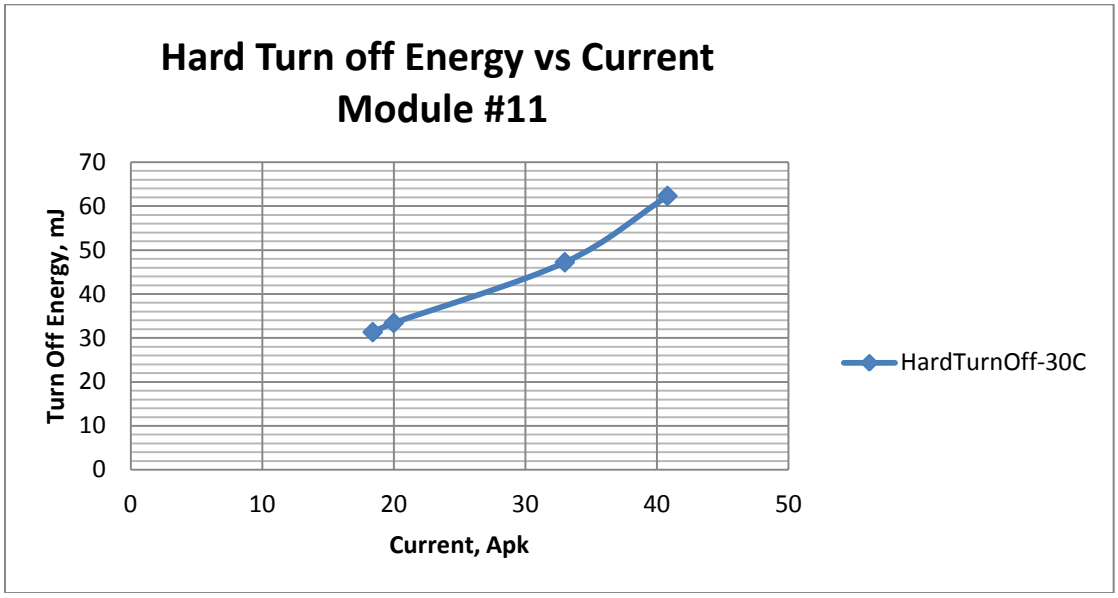


Figure 4-4: Hard Turn-off Energy Curves-Module#11

Test Data for Turn-on Energy- Module#11

Table 4-6 shows the data obtained while testing representative module #11. As stated in the EPRI report – SGTO Device Characterization, the turn-on energy obtained was very low about 2.99mJ.

Table 4-6: Turn-on Energy at 30ºC for Module # 11

Reapplied Voltage, V	3500
Time Delay, nsec	200
Fall Time, nsec	124
Eon, mJ	2.99
Current, A	30

Thermal Characteristics/Analysis

Simulated Data

- Power dissipation
    - 16 W per each Si diode
    - Total power for analysis=80W.

Assumption:

- Module is mounted on to a heat sink base which is maintained at an average temperature of 20C.

- Half Model analysis since the module is symmetric along YZ plane.

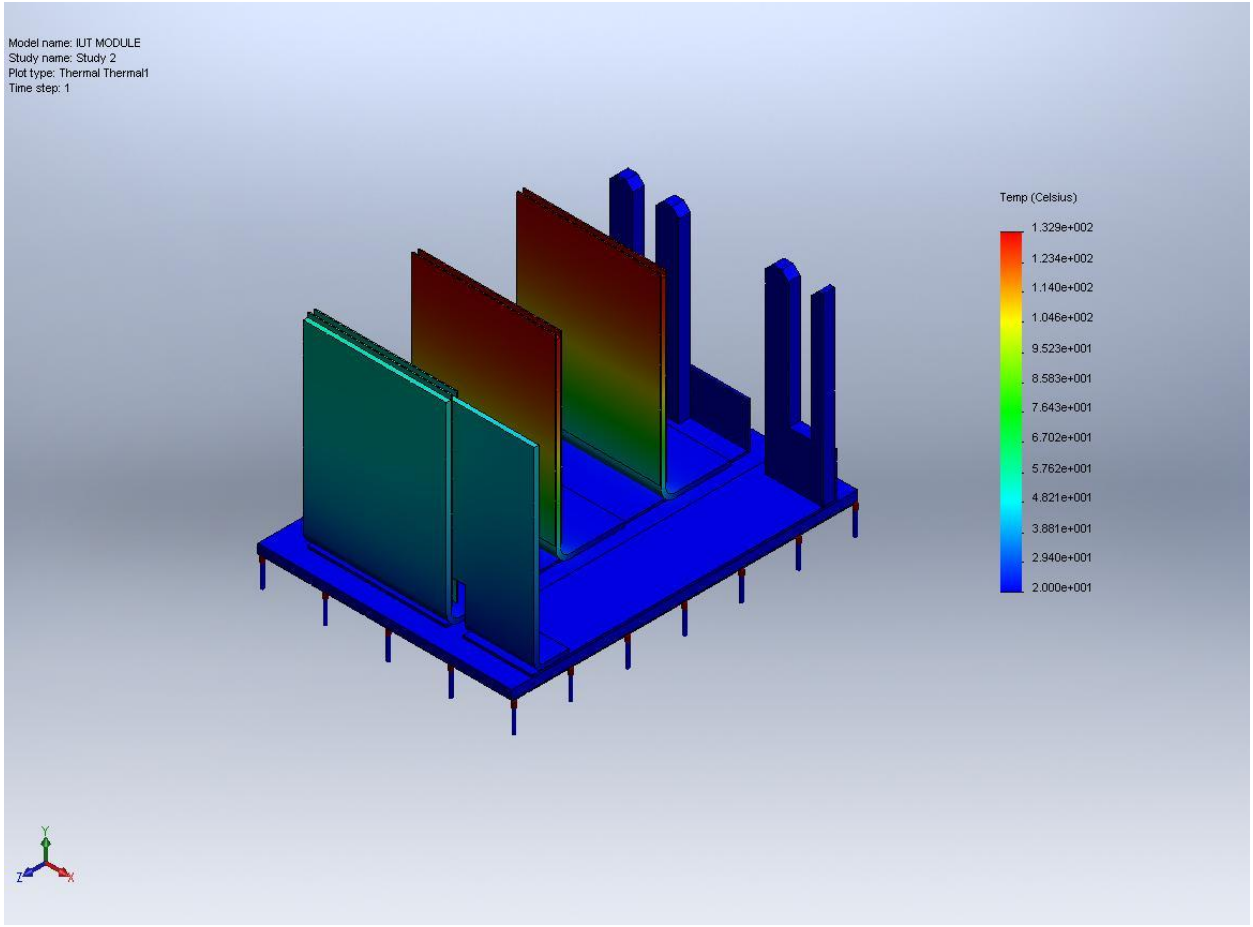


Figure 4-5: Steady State Thermal analysis on Si module

Results

A maximum temperature of 132C was observed for the Si diodes. This is the temperature of the copper strap to which the diodes are clamped for thermal path. The junction of the diodes will be higher than 132C depending on the thermal resistance of the Diode.

The base of the module has a uniform temperature, assuming the heat sink base onto which this module is mounted will have a steady average temperature of 20C.

The outer copper strap has lower temperature profile compared to inner. This is because inner copper straps are shared by 2 diodes each compared to outer one onto which only 1 diode is clamped. Also the outer copper strap has higher thermal mass compared to inner ones.

To determine the thermal resistance junction to case the continuous 5A DC current test was running for IUT modules. Forty five minutes test results:

T ambient = 21.4C, Tdevice = 40.1C,

Average forward voltage drop Vaverage = 4.98V,

average power Paverage = 24.9W,

thermal resistance Rth = (40.1 – 21.4)/ 24.9 = 0.751004 C/W.

Voltage-Current Characteristic for Varying Gate Currents

Figure 4-6 provides the V-I Characteristics with different gate current for the Asymmetric (No Reverse breakover voltage) SGTO device. The test was run in 6 steps by varying the gate current and can be tabulated in Table 4-7. The following V-I characteristics were obtained using a Tektronics 370A (CT-1) Programmable Curve Tracer S/N: J303170 and a picture of the screen was taken for documentation purposes.

Table 4-7: V-I Curve Step Tabulation

Forward Breakover Voltage(V)	Gate Current(mA)
2000	0
1200	0.5
850	1
600	1.5
400	2.0
250	2.5

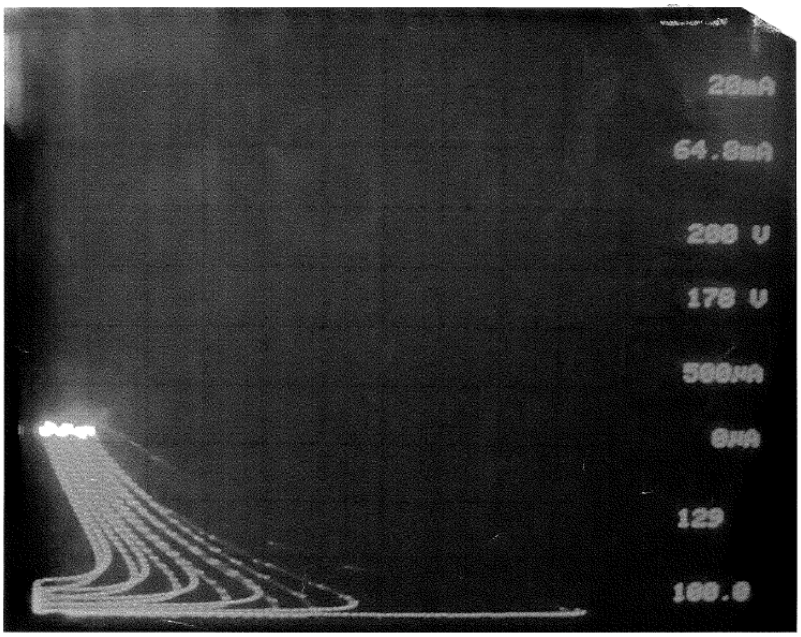


Figure 4-6 V-I Characteristics for a SGTO 250Vdc to 2000vdc

5
HALF BRIDGE TESTING PERFORMED AT SPCO LABORATORY

Figure 5-1: Half Bridge Configuration

Figure 5-1 shows the half bridge test configuration (top left: forced air heat sinks/w fans; top center: half-bridge, bus capacitor, HV differential and thermal probes, resonant transformer, Thermal electric coolers/w power supplies and fans; top right: thermal electric coolers/w fans and powered isolated gate drivers (blue lights); lower left: pulse generators; bottom right: additional support instrumentation.

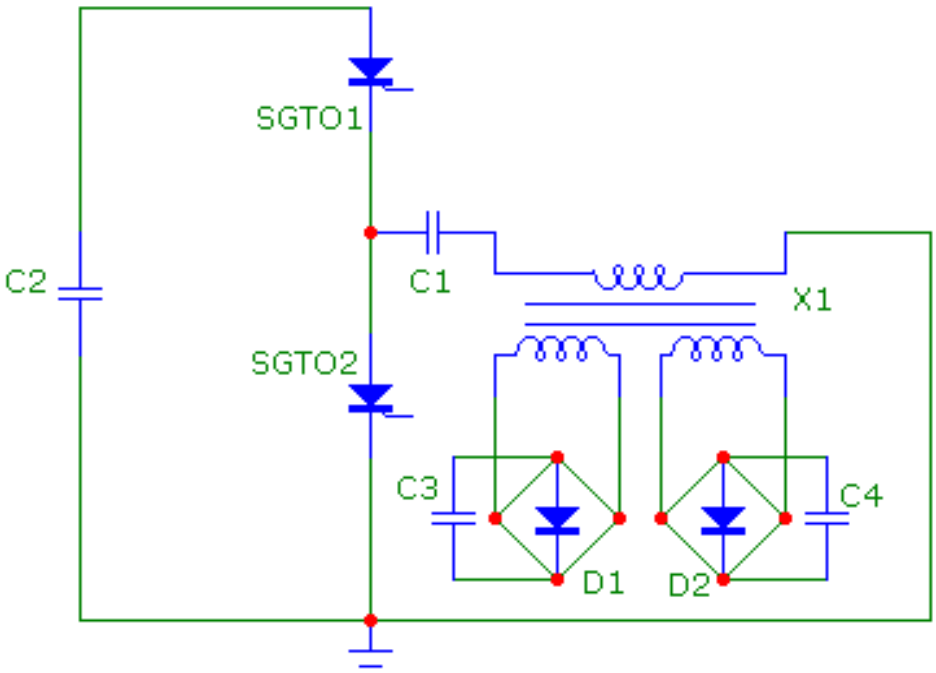


Figure 5-2: Half Bridge Test Circuit

Half-Bridge Test Waveforms

These waveforms are used to show the measurement location on the waveform; exact set-up of the cursors and math functions for the particular measurement will depend on the user's available equipment and functional enhancements of their equipment.

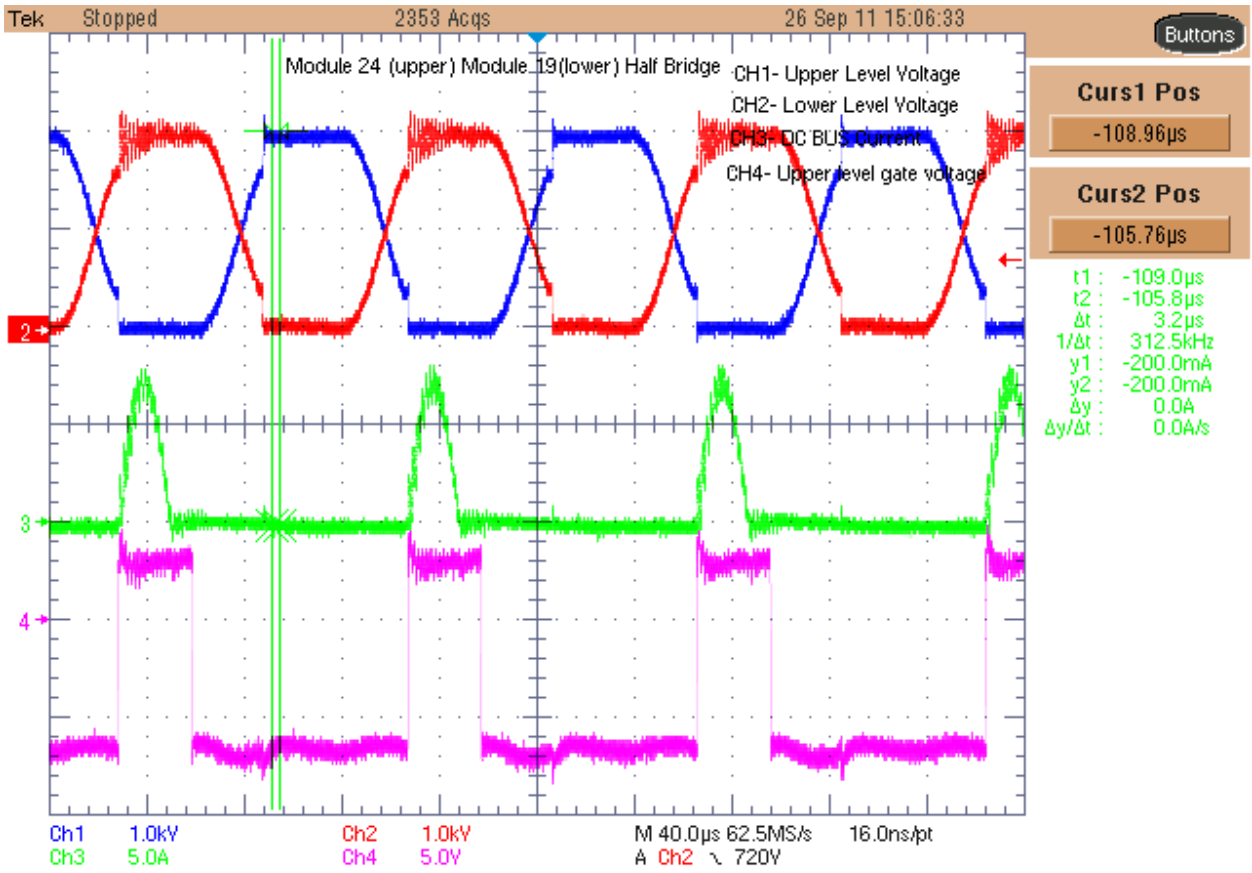


Figure 5-3: 2000V Continuous Operation

The above figure shows the initial measurements made with the half bridge circuit. The high (upper) side and low (lower) side voltages are about 2000V and the current through the high side SGTO is about 8A. The switching frequency is 10 kHz.

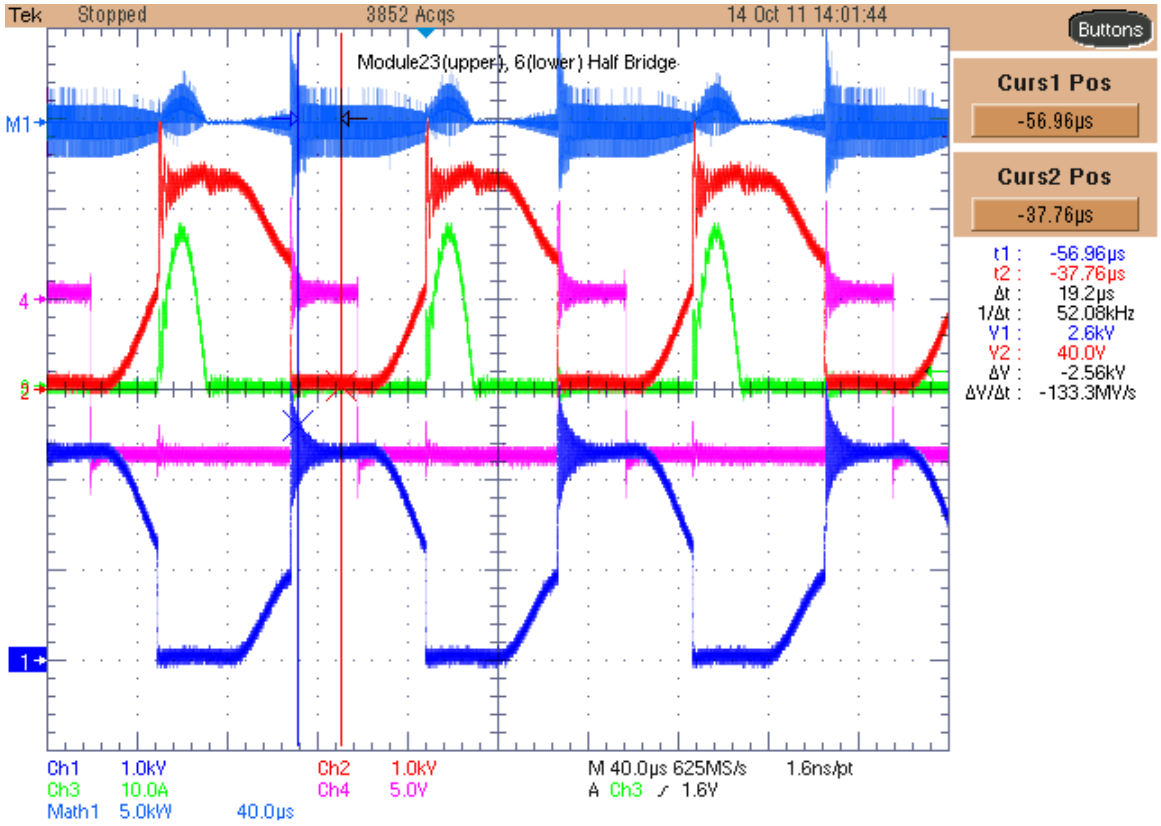


Figure 5-4: 2500V Continuous Operation

Figure 5-4 shows the waveform at 2500V, 18A peak with the circuit running at 10 kHz. Channel 1 represents the high side SGTO voltage, Channel 2 represents the low side SGTO voltage, Channel 3 represents the bus current and Channel 4 represents low side gate signal. M1 on this waveform represents loss computations for the high side SGTO.

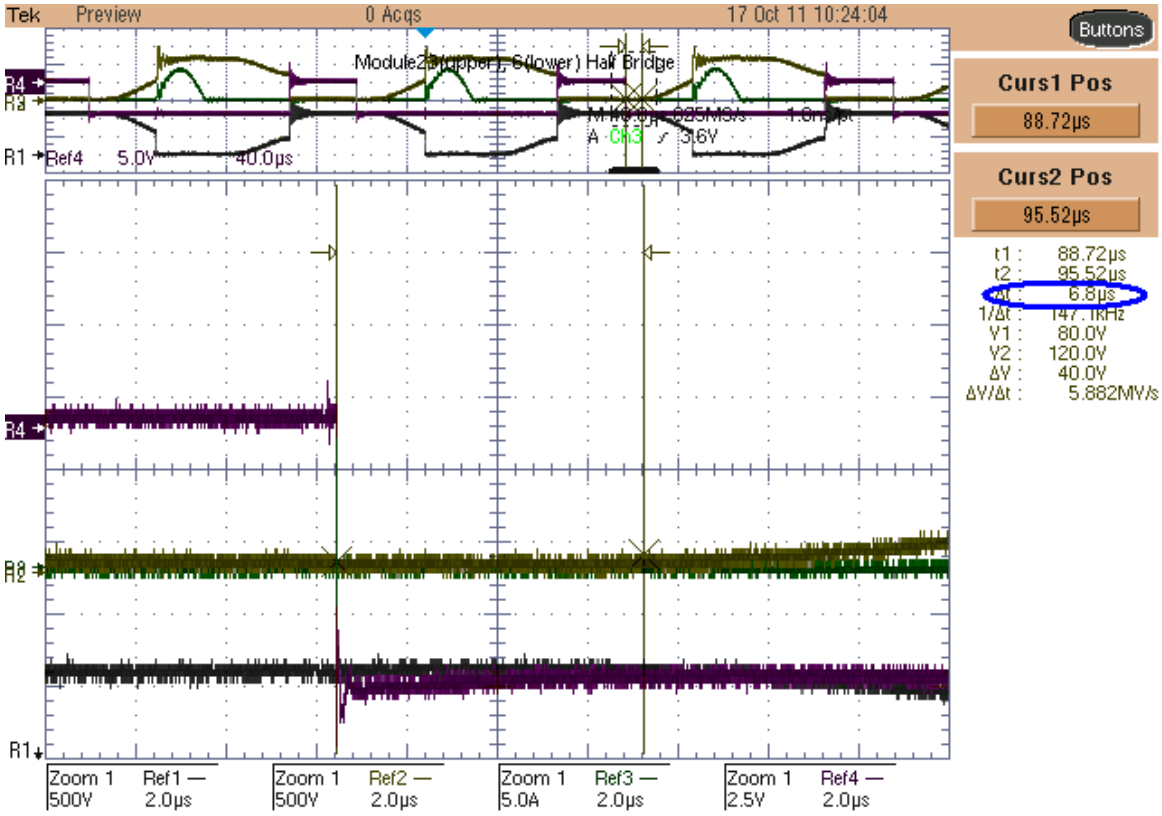


Figure 5-5: 2000V Continuous Operation@8A – Storage time

The above waveform is a screenshot for the measurement of storage time. In this particular case the storage time was measured to be 6.8us.

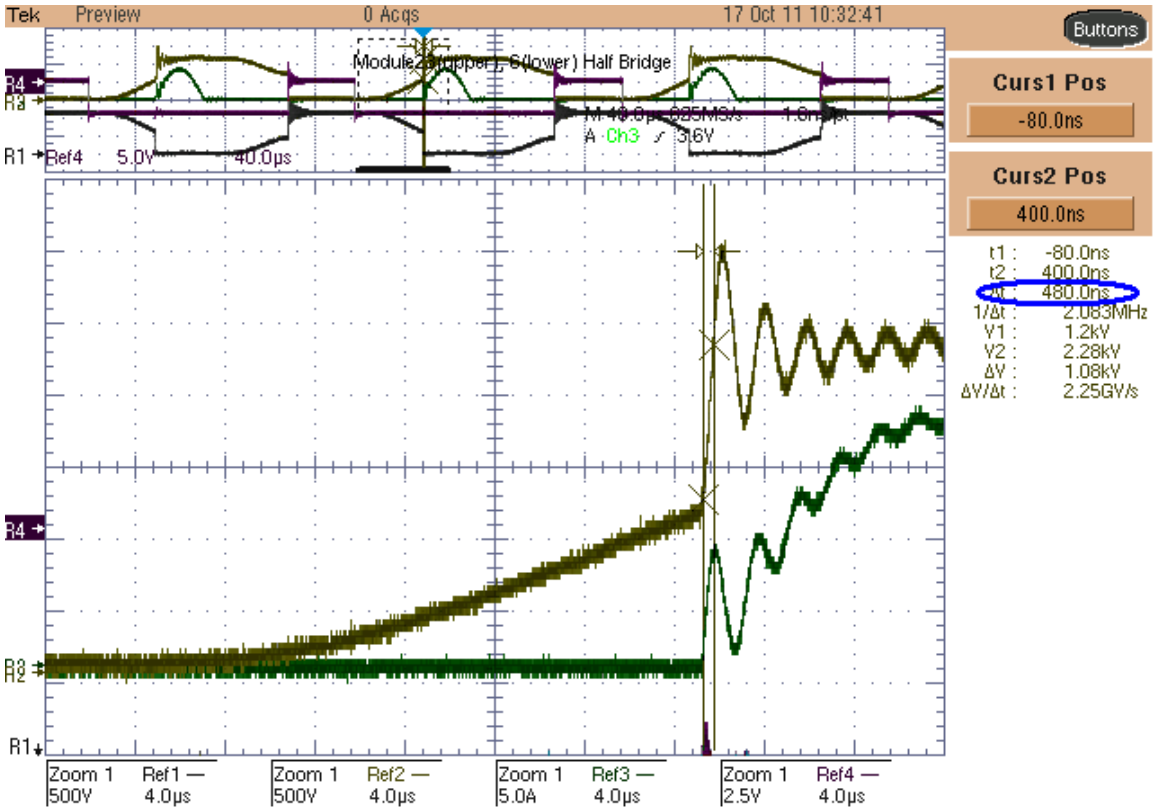


Figure 5-6: 2000V Continuous Operation@8A – Rise Time

The above waveform is a screenshot for the measurement of Rise Time. In this particular case the rise time was measured to be 480ns.

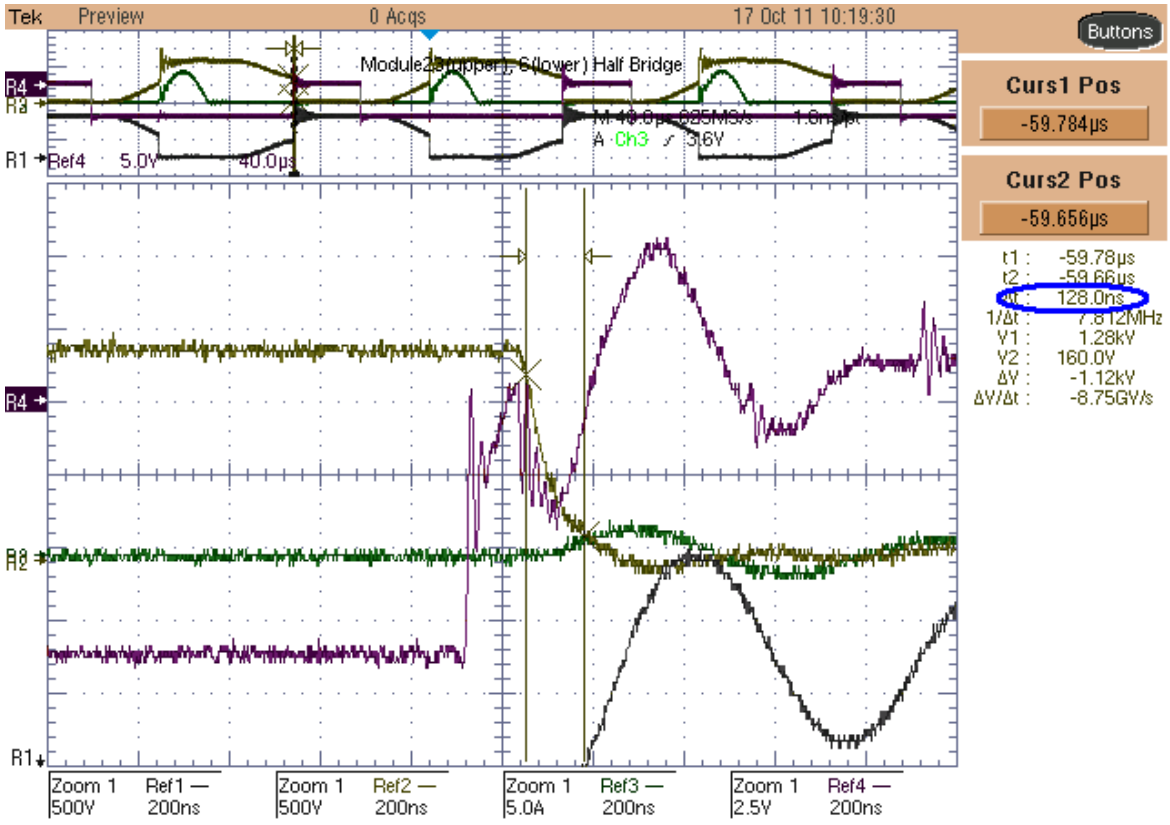


Figure 5-7: 2000V Continuous Operation@8A – Fall Time

The above waveform is a screenshot for the measurement of fall time. In this particular case fall time was measured to be 128ns.

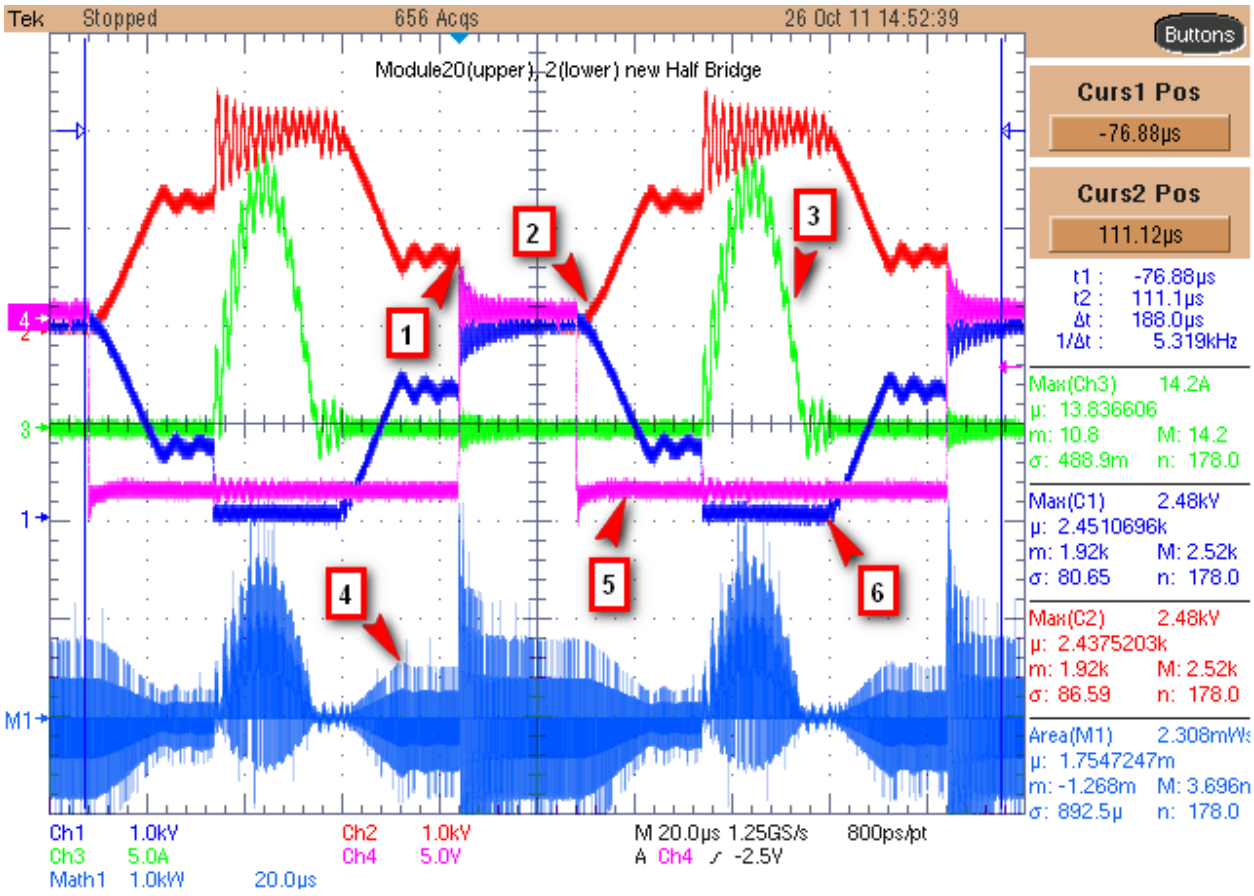


Figure 5-8 3080V Turn-on, Turn-off.

Where:

1. Upper level module turn-on.

2. Point where upper level module turn-off process starts.

3. Upper level current.

4. Energy.

5. Synchronous pulse.

6. Lower level module voltage.

Table 5-1 Summarizing the overall Results from Half-Bridge Testing

Half-Bridge Module	Output Resistive Load Value		
Parameters	**10.5Ω**	**12.7Ω**	**15Ω**
Voltage DC Power Supply, Vdc	2513	2513	2513
Current DC Power Supply, Adc	4.71	3.80	3.39
Pin (Power Supply), KW	11.84	9.55	8.52
Vout, Vdc	328.1	329	330
Iout, Adc	35.95	29.00	25.5
Pout, KW	11.78	9.54	8.42
Resonant Current RMS, Arms	13.19	10.68	9.76
Resonant Current, Apk	18.65	15.1	13.8
*Rise Time, Tr, nsec	60.96	69.28	69.12
*Fall Time, Tf, nsec	60.96	69.28	69.12
Storage Time, Ts, nsec	1720	1210	1140
Time Delay, Td, nsec	112.5	114.1	112.6
E_{on}, mJ	.01689	.01796	.01423
E_{off}, mJ	1.103	.7998	.8264
E_{cond}, mJ (computed from measured data)	4.382	3.346	2.883
E_{total}, mJ (computed from measured data)	5.502	4.164	3.724
Efficiency, % =Pout/Pin	99.5	99.9	99.0

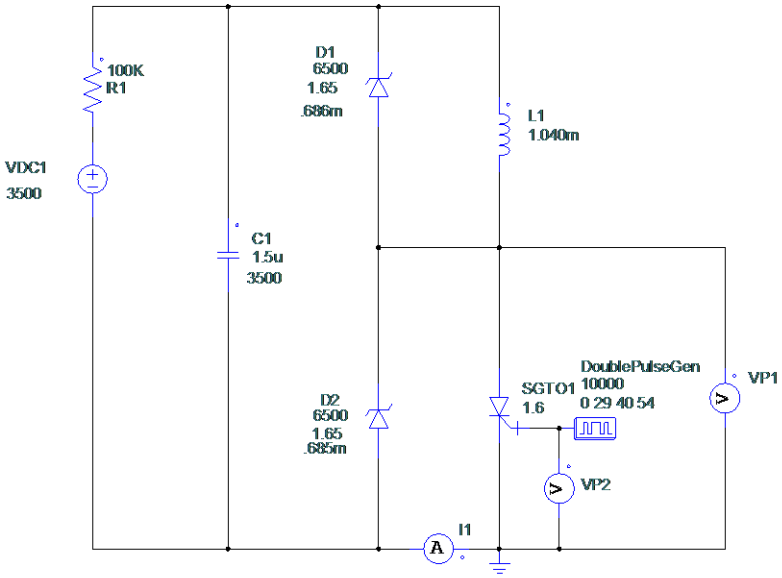
The above tables summarize the available results obtained from the half-bridge testing so far. Although the conduction losses and total losses are not able to be extracted directly at this time due to limitations of instrumentation (scope and HV differential probes: Technical discussions with the instrumentation vendor has validated this fact; there is also the loading effects of the HV differential probes and their capacitive AC ground limitations that will limit their use in these higher voltage bridges and especially in the cascaded system), SPCO has used an alternate method for extraction of E_{cond} and E_{total} data and although derived from indirect measurements, it

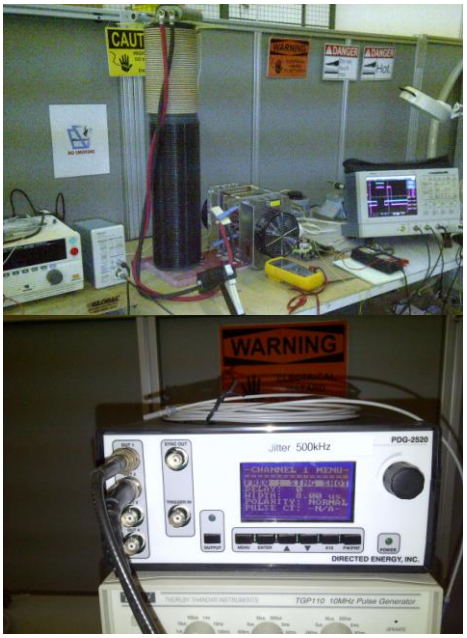
does offer a reasonable result for benchmark comparison, until a more reliable direct measurement approach can be implemented.

Table 5-1 details the different parameters that were measured as part of the half-bridge testing. One of the key conclusions that can be reached is that is that the turn-on losses for the Si-SGTO is negligible as compared to the 6.5KV IGBTs. Total losses appear to be comparable with the 6.5KV Si-IGBT. However, we need to evaluate the findings from the full-bridge testing.

6 DOUBLE PULSE TESTING PERFORMED AT SPCO LABORATORY

Double- Pulse Test Circuit and Results





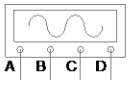
Equipment Used for this Test
Directed Energy (DoublePulseGen)
Model: PDQ-2520
S/N:06-0520

Tektronix
Model: TCPA300 Current Amplifier
S/N: B025344

Model: TCP303 Current Probe (Measured I1)
S/N: B013699

Model: P5210 High Voltage Differential Probe (Measured SGTO1 Anode-Cathode Voltage
S/N: B015865

TDS5034B
Digital Phospher Oscilloscope (Displays CHA(1)-I1, CHD(4)-VP1, CHB(2)-VP2,
CHC(3)-DoublePulseGen, tdon, tdoff and Computes Eon, Eoff
350MHz-5GS/s
S/N: B052823



TE Technology
CP-200HT
S/N: 0076-2010-3-15
S/N: 0075-2009-6-10

PTI Plasma Technics
Model: SSD-110/15
S/N: SSD-110-0310-989

Hewlett-Packard
Model:
4000VDC @ 0-50ma
S/N: 1146401020

D1- 5X-STTH-1512W
D2- 2-5X-STTH-1512W in parallel

Figure 6-1: Simplified Double-Pulse Circuit and Actual Test Set-up

Double-Pulse Test Purpose (reference Figure 6-1)

The configuration of Silicon Power's Double-Pulse Test set-up consists of a variable high voltage dc power supply, air core load inductor with a freewheeling diode to shunt the inductor and the module under test. A pulse generator capable of programmable double pulse generation to drive the gate driver board used to control the device under test. Instrumentation used to measure the peak current and voltage through and across the module respectively and to compute and display turn-on/off characteristics in a snubberless hard switched configuration. The inductance used was selected to limit the overall current between 18Apk (1st Pulse @ 2500Vpk) to 40Apk (2nd Pulse @ 3500Vpk). The test set-up was also implemented to minimize stray inductance effects as evident by minimal ringing on the waveforms.

Double-Pulse Simulation

Simulation shows agreement with the measured response for the circuit shown under double-pulse excitation. The spike at the beginning of the 2nd pulse is associated with the D1 diode reverse recovery charge and test circuit total parasitic capacitances.

Simulation Results

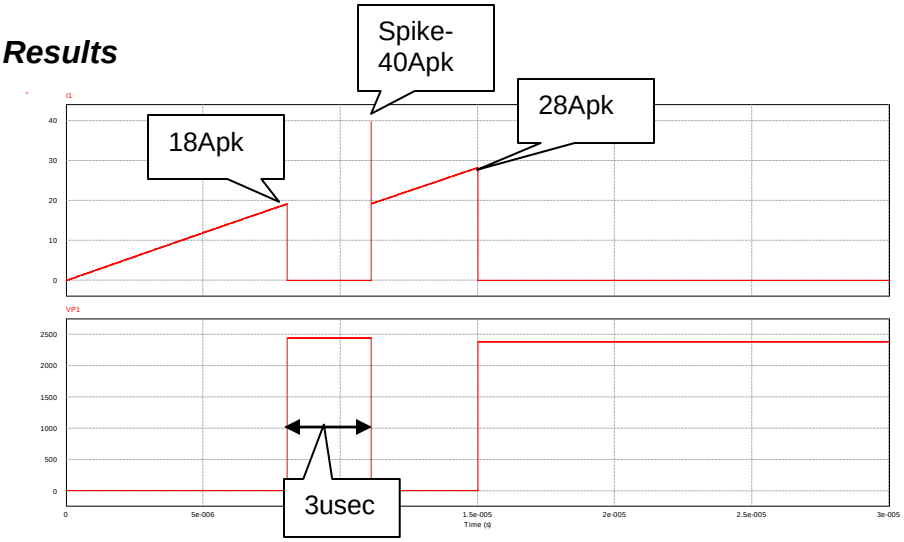


Figure 6-2: Module Simulated Double-Pulse at 2500Vpk

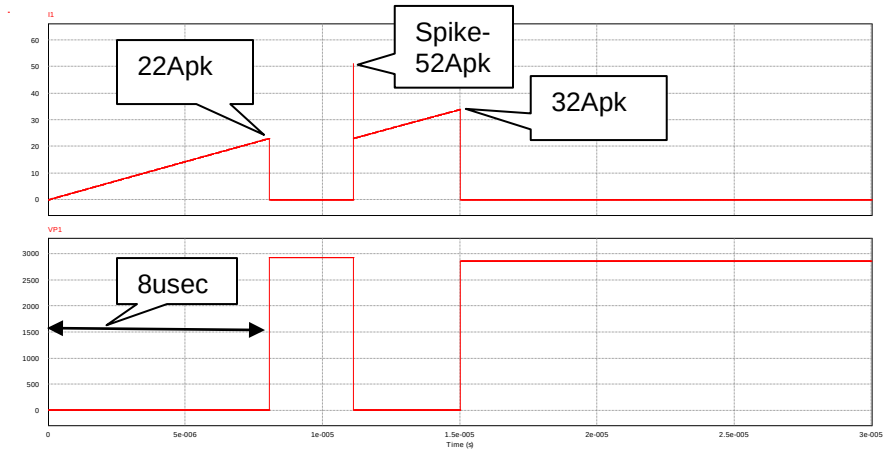


Figure 6-3: Module Simulated Double-Pulse at 3000Vpk

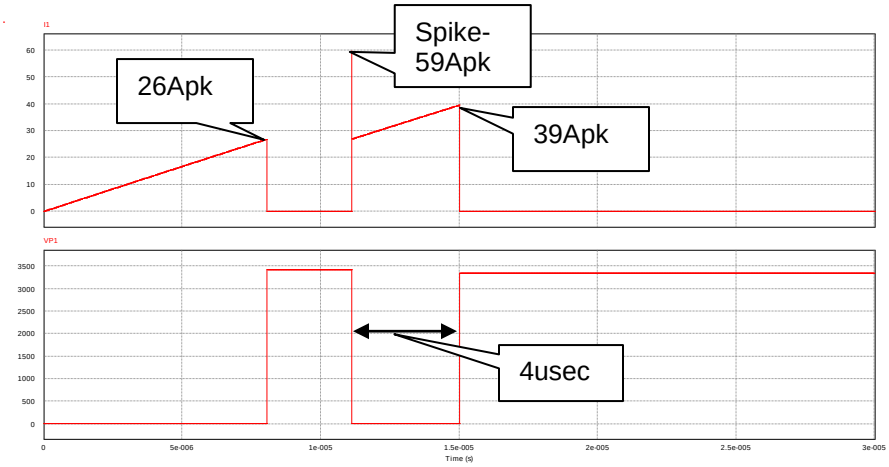


Figure 6-4: Module Simulated Double-Pulse at 3500Vpk

Table 6-1: Actual Measured Module Double-Pulse Test Data Summary

Test Parameter	Pulse Position	Mod 4-Driver 23			Mod12-Driver 23			Mod 14-Driver 23		
		2500Vpk	*3000Vpk*	*3500Vpk*	*2500Vpk*	*3000Vpk*	*3500Vpk*	*2500Vpk*	*3000Vpk*	*3500Vpk*
tdon, nsec	1	34	38	36	54.4	44	48	34	40	40
tdoff, nsec	1	416	420	428	450	456	464	432	436	448
Eon, uJ	1	8.22	70.33	110.6	643.3	746.9	936.6	0.8038	2.212	20.57
Eoff, uJ	1	15340	26150	37300	11080	18100	30030	12310	18140	24870
I, Apk	1	22	26	31	22	26	30	18	22	26
tdon, nsec	2	94	120	116	116	128	106	144	148	168
tdoff, nsec	2	416	412	424	422	436	464	428	440	460
Eon, uJ	2	6588	10030	13360	7790	10750	14710	6155	9316	11900
Eoff, uJ	2	12120	27900	43240	8295	24830	29940	15080	21640	27220
I, Apk	2	33	39	45	33	39	45	27	32	38

Module 1 was tested up to 2500Vpk and demonstrated excessive noise above this level. It was determined to be caused to internal partial discharge and was not included as part of this data set (the data and screen shots at 2500Vpk are available for this module). Also the current range variation between module 14 and modules 4 and 12 are due to changes in the geometric position of the series equivalent inductance, L1 (actually made up of 119uH, 163uH, 260uH and 498uH in series) that occurred during the changing of the modules in preparation for testing within the test circuit. Other sources of this error were considered such as jitter of the signal source and device turn-on/turn-off delays; however, they were dismissed as sources of the error due to their insignificant contribution to the error.

The following graphs were plotted to give visual significance to the above data and to give some indication to the trends of this data. The data set was taken for the 1st and 2nd pulses representing a dynamic range of performance. No abnormal operation of the modules were anticipated or observed except what was previously mentioned for Module 1

Table 6-2: Module Double-Pulse 1st Approximation Ramp Currents

	Mod14								
	2500V			3000V			3500V		
	Calculated	Actual	%Err	Calculated	Actual	%Err	Calculated	Actual	%Err
1st-Ramp Current, Apk	19.2	18	6.6	23	22	4.5	26.9	26	3.5
2nd-Ramp Current, Apk	28.8	27	6.6	34.5	32	6.8	40.4	38	6.3

Double Pulse Data Graphs 1st/2nd Pulse Comparisons between Modules

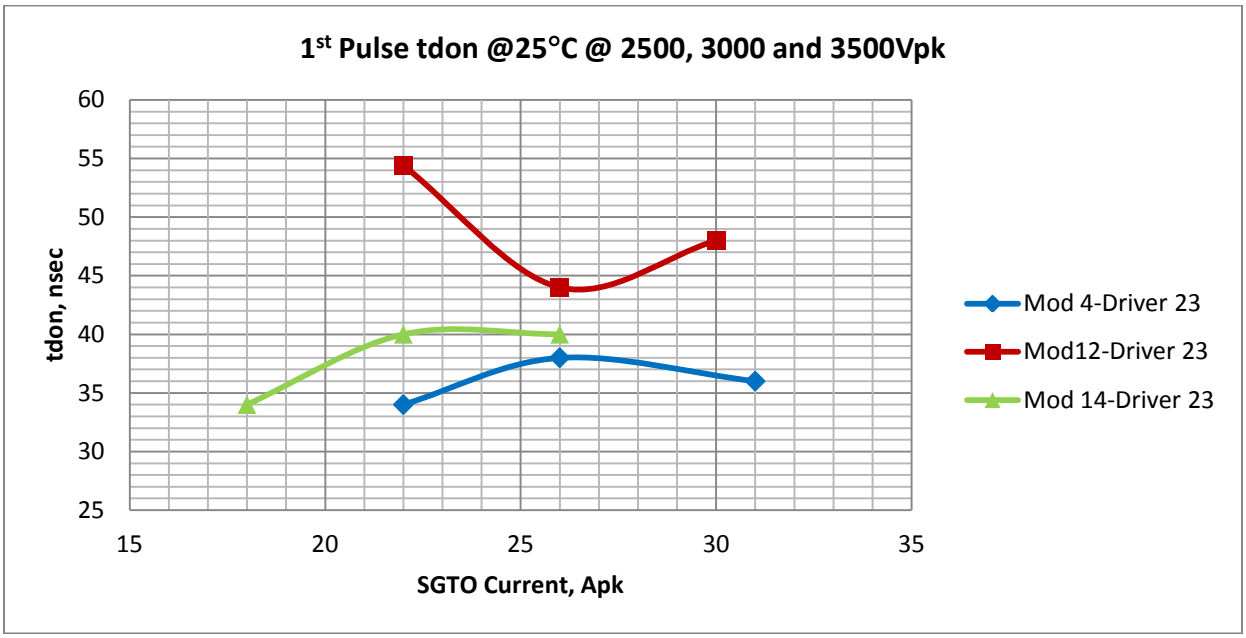


Figure 6-5: Turn-on 1st Pulse

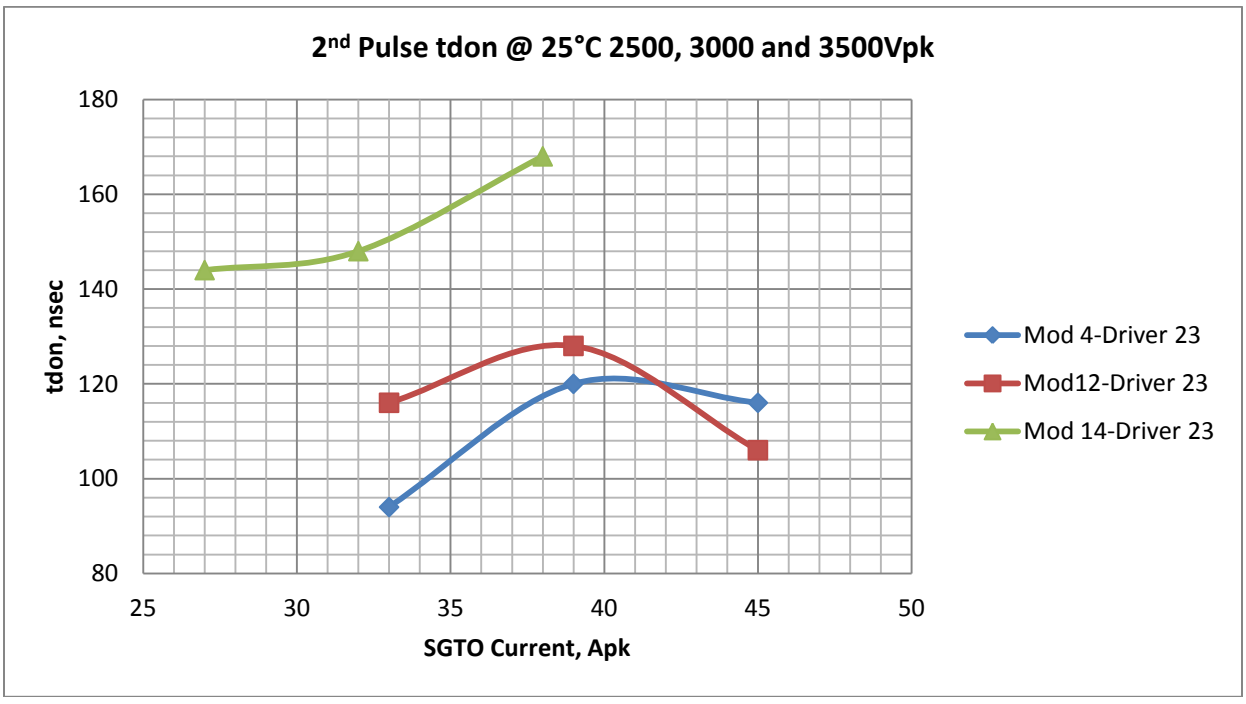


Figure 6-6: Turn-on 2nd Pulse

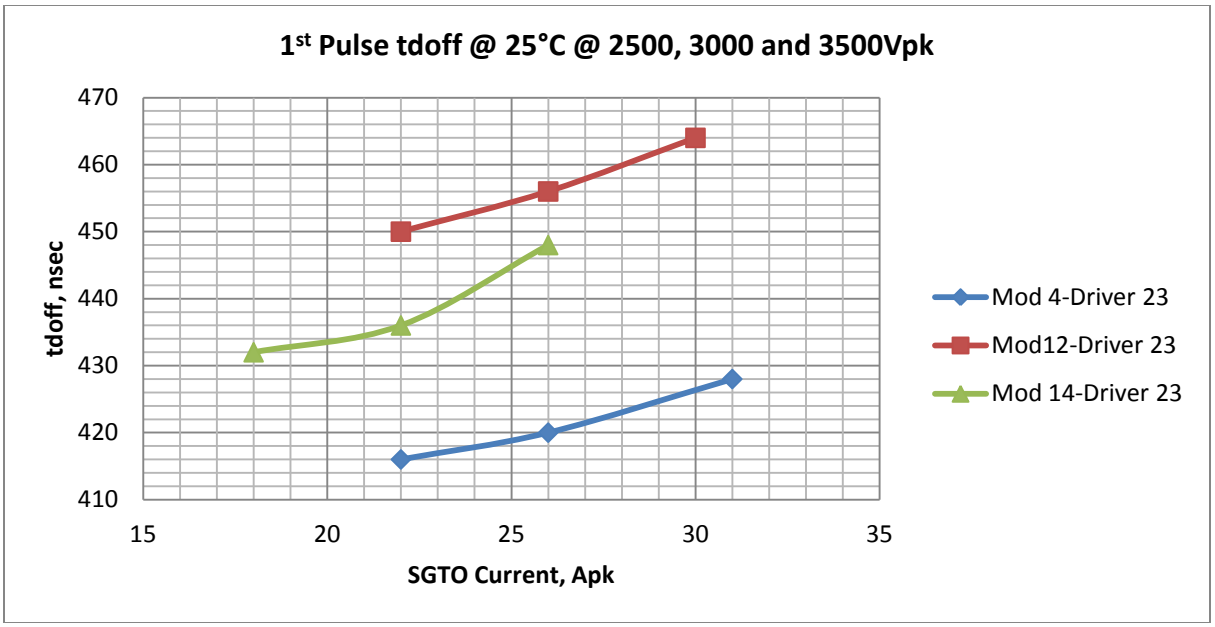


Figure 6-7: Turn-off 1st Pulse

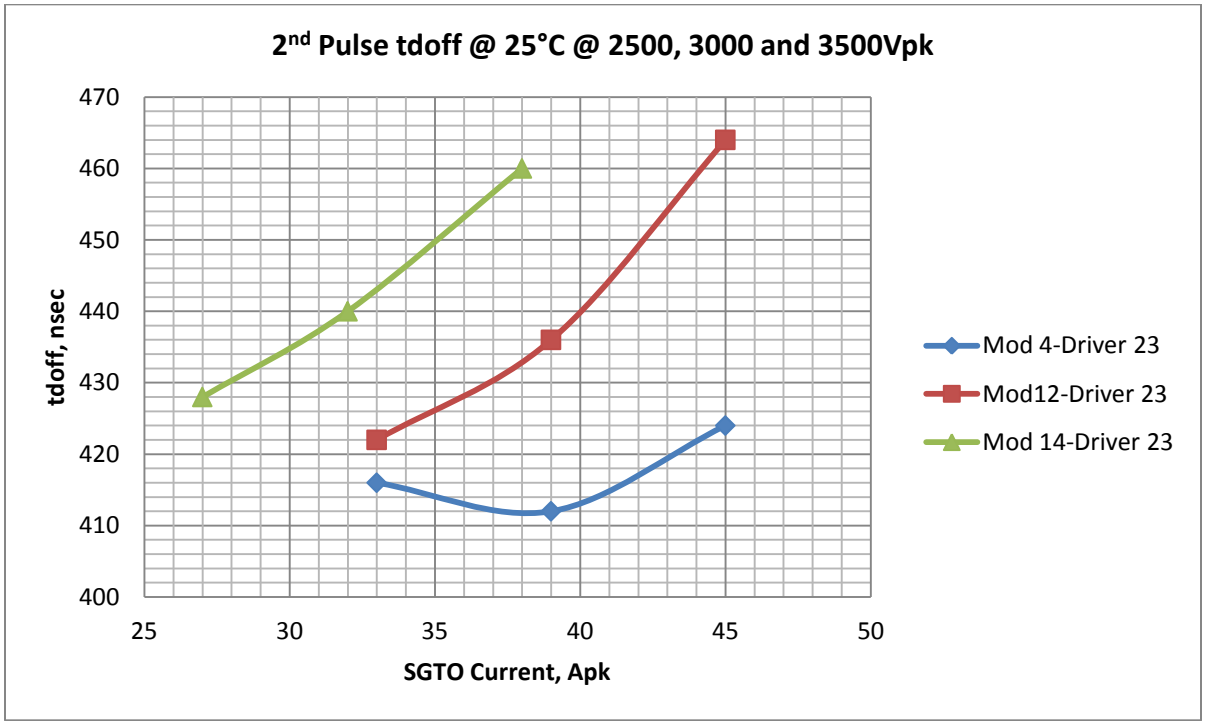


Figure 6-8: Turn-off 2nd Pulse

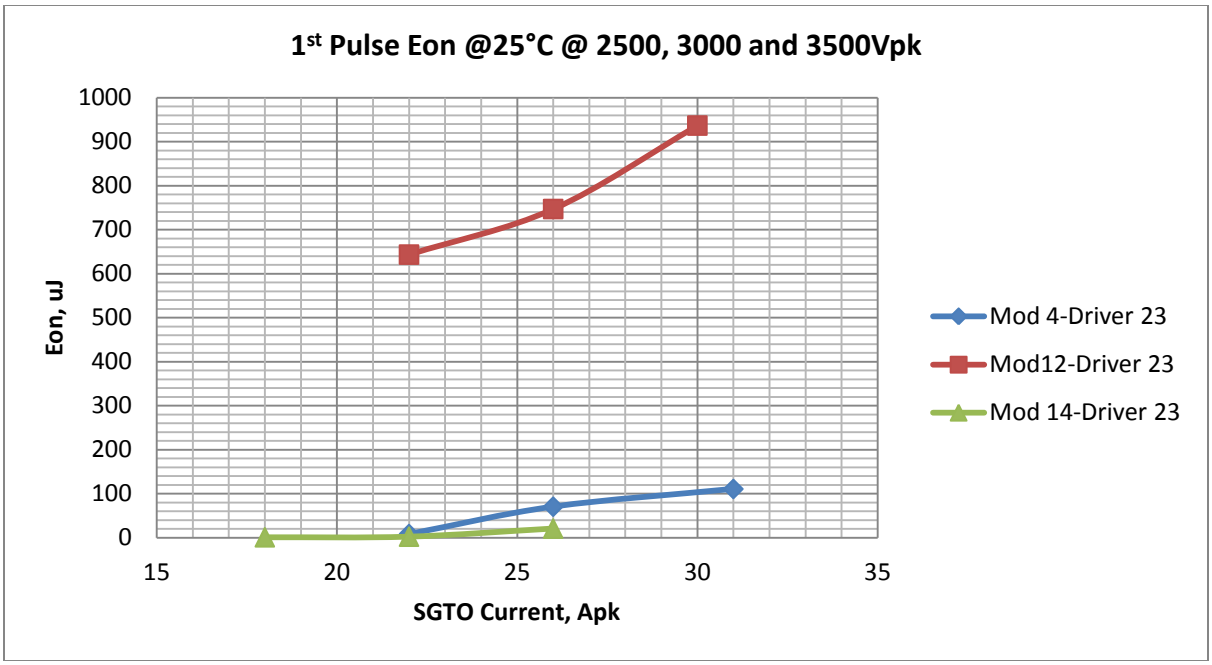


Figure 6-9: Turn-on Energy 1st Pulse

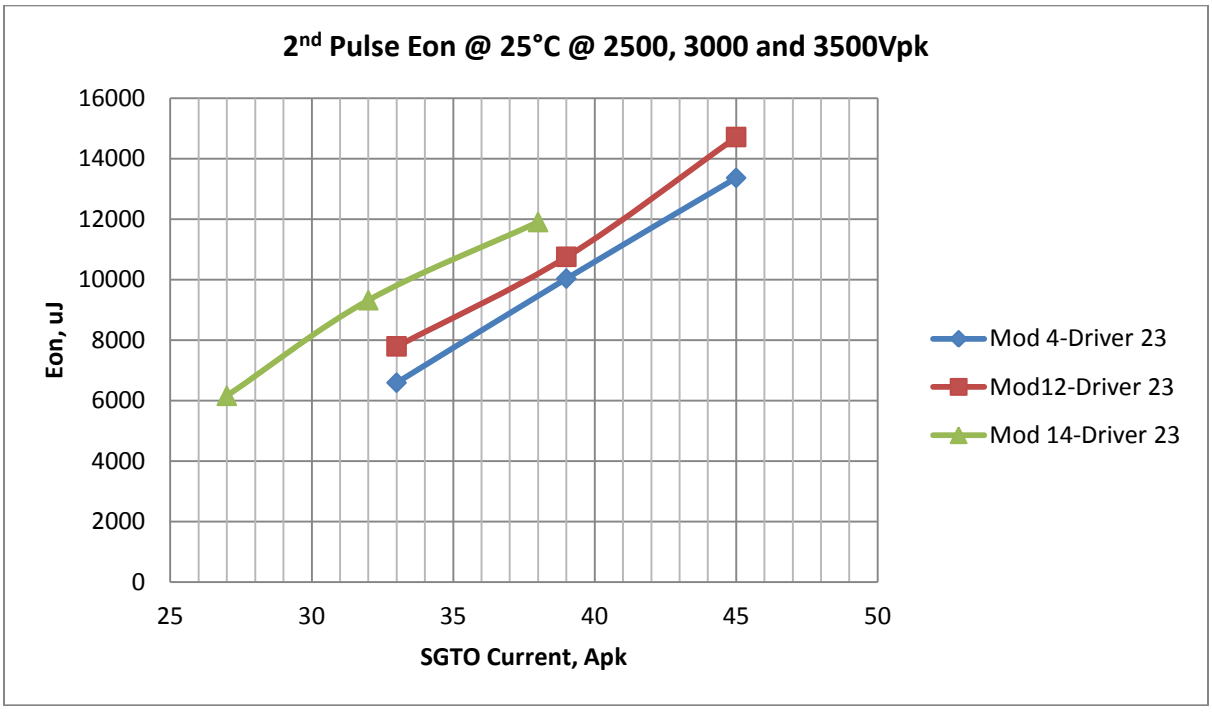


Figure 6-10: Turn-on Energy 2nd Pulse

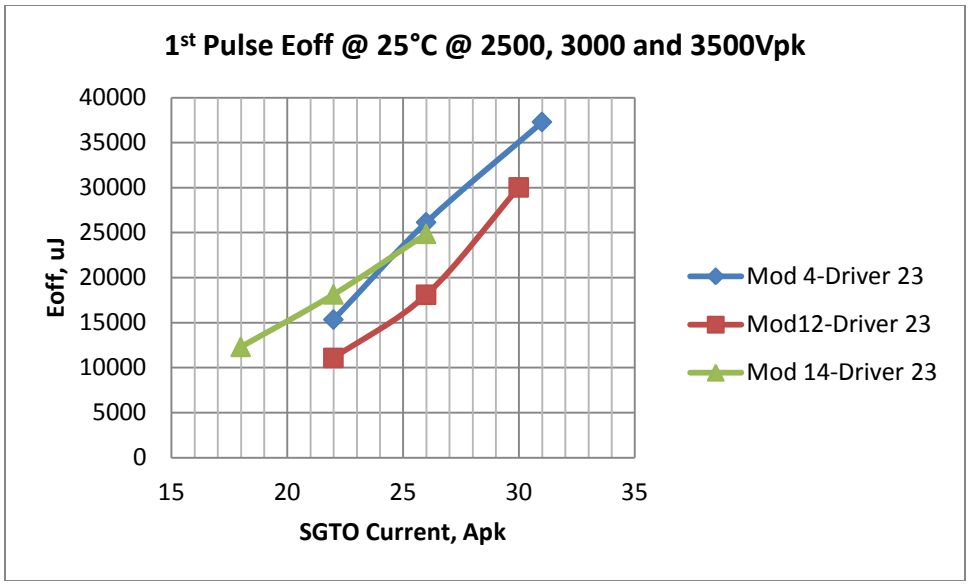


Figure 6-11: Turn-off Energy 1st Pulse

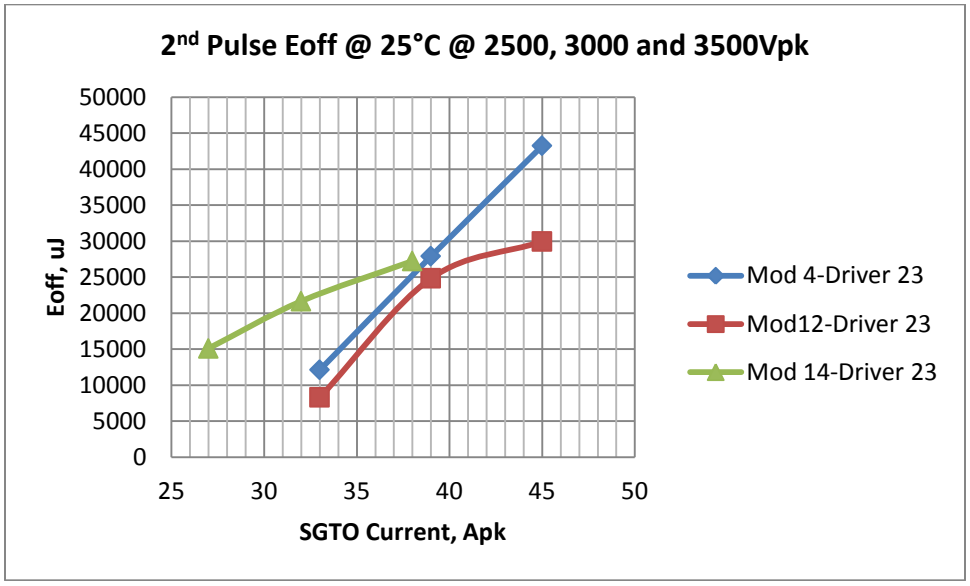


Figure 6-12: Turn-off Energy 2nd Pulse

Scope Screen Shots used to Extract Measurements

(Module 14 @ 3500Vpk used for reference)

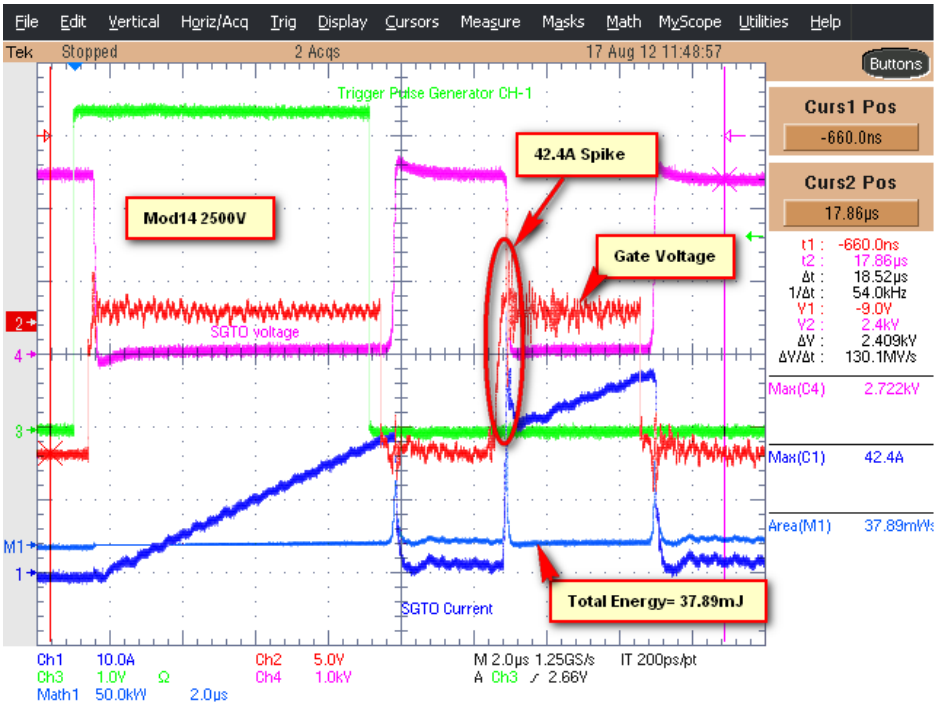


Figure 6-13: Double-Pulse @ 2500Vpk

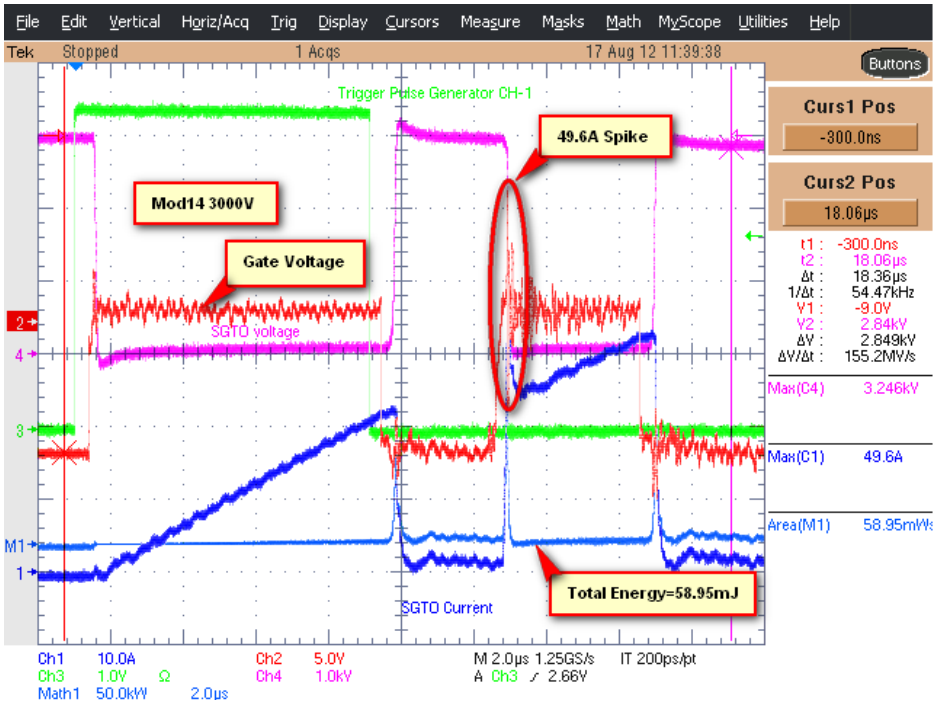


Figure 6-14: Double-Pulse @ 3000Vpk

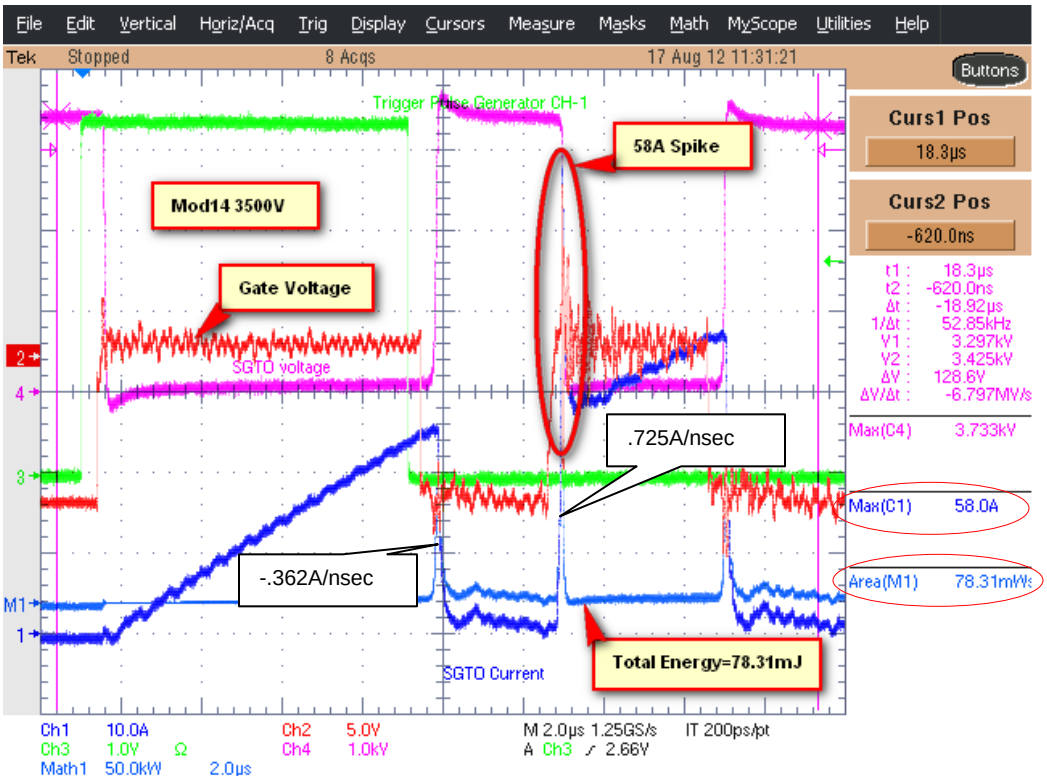


Figure 6-15: Double-Pulse @ 3500Vpk

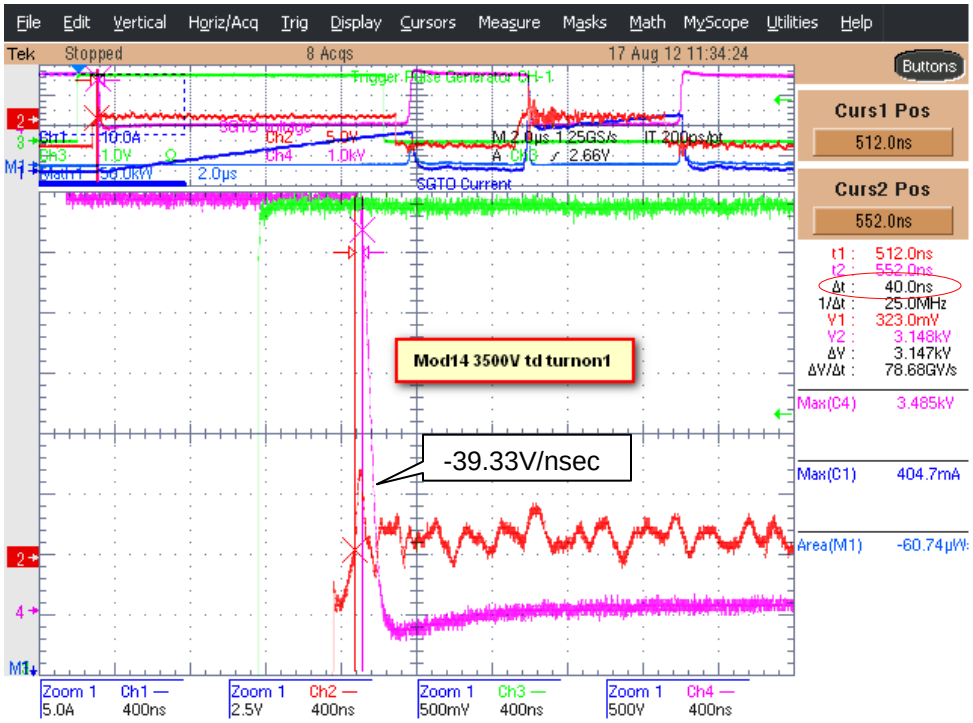


Figure 6-16: Turn-on Time 1st Pulse

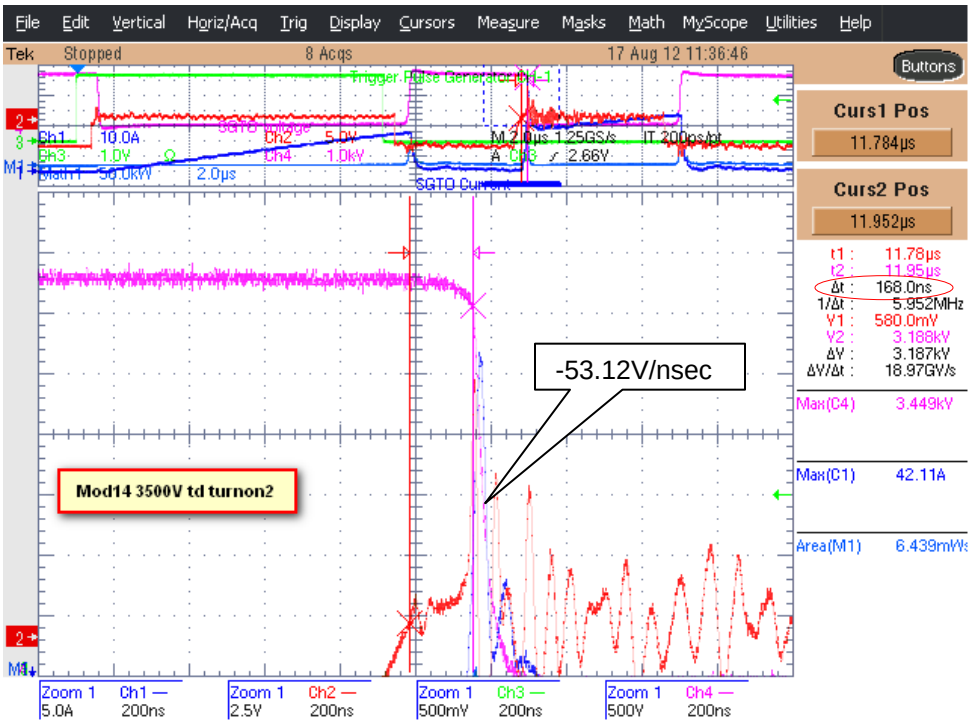


Figure 6-17: Turn-on Time 2nd Pulse

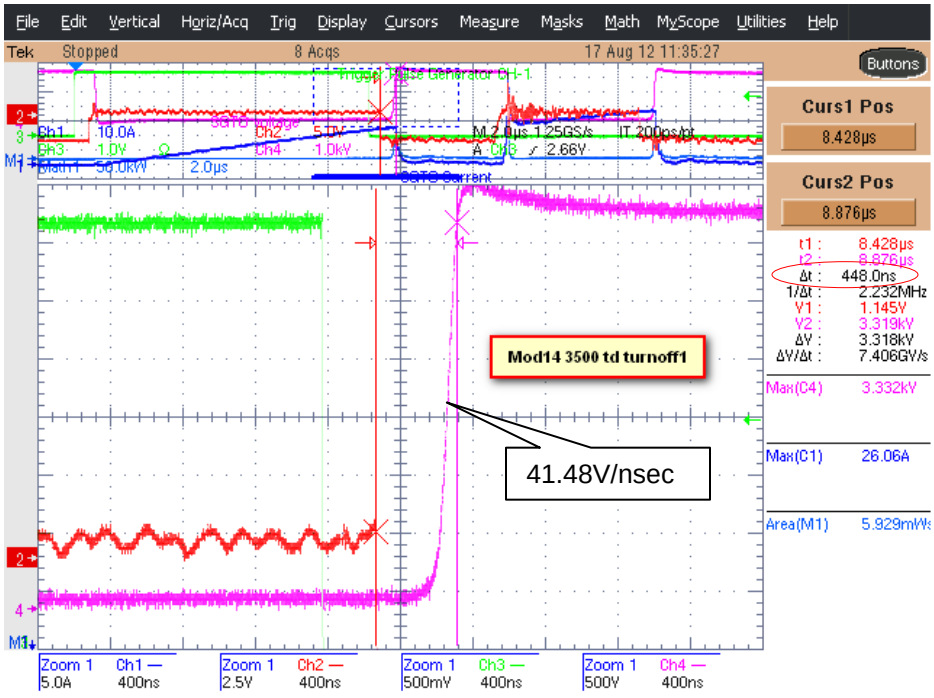


Figure 6-18: Turn-off Time 1st Pulse

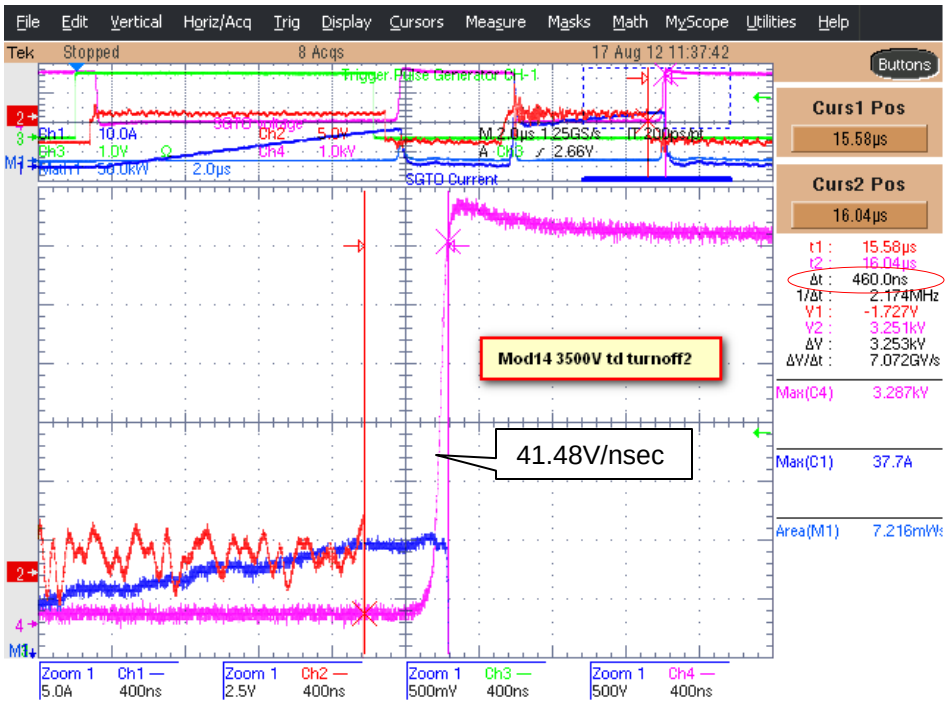


Figure 6-19: Turn-off 2nd Pulse

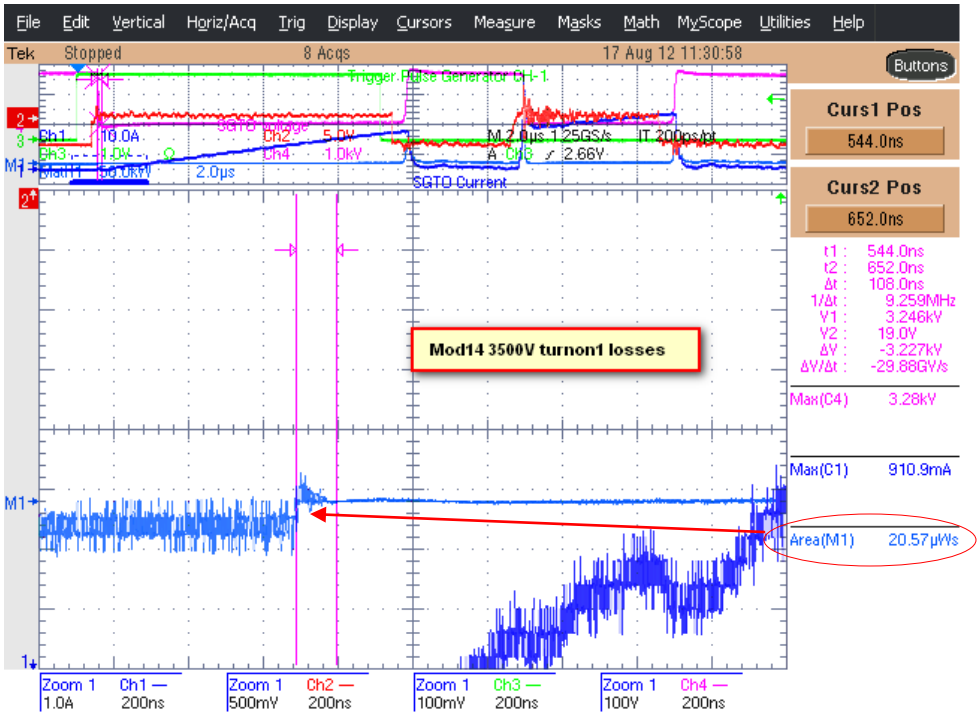


Figure 6-20: Turn-on Energy 1st Pulse

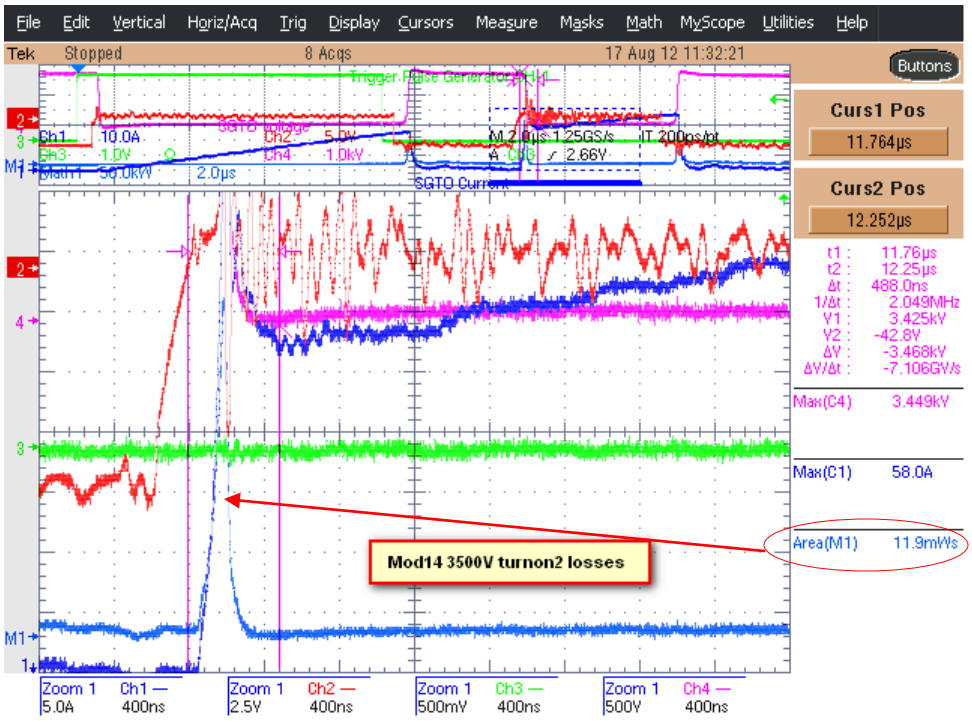


Figure 6-21: Turn-on Energy 2nd Pulse

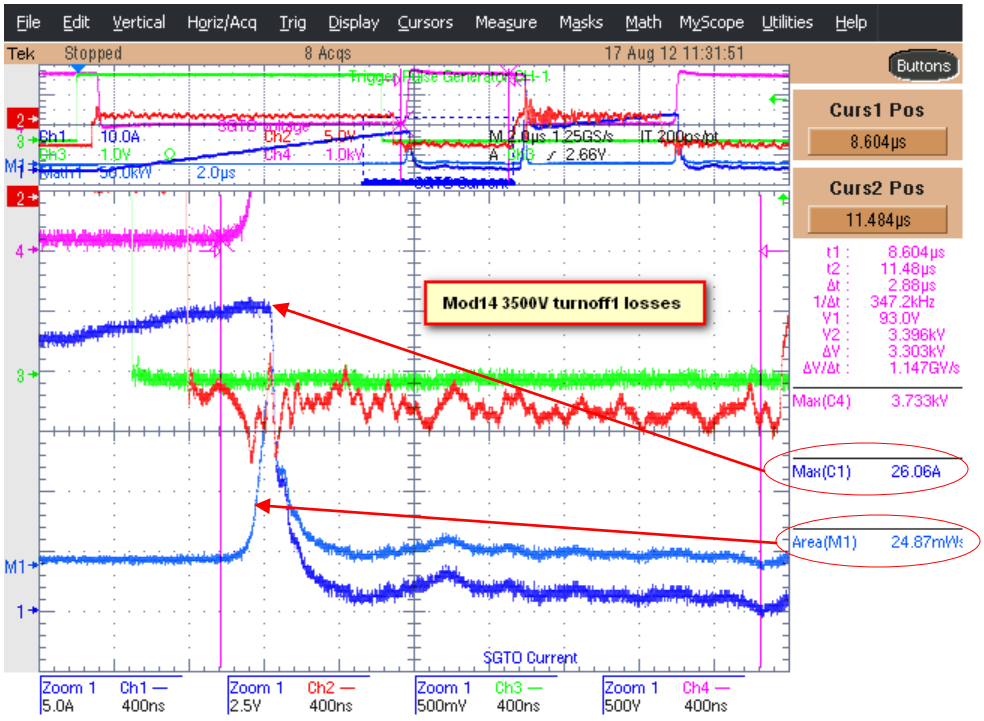


Figure 6-22: Turn-off Energy 1st Pulse

Figure 6-23: Turn-off Energy 2nd Pulse

Snubberless Hard Switched Double-Pulse Waveform Analysis:

The module 14 waveforms (figures 6-13 to 6-23) describe the representative captured waveforms for the various measurements made during the double-pulse test of the Silicon Power SGTO modules. The data and waveforms were collected for the 1st and 2nd pulses.

Waveforms, figures 6-13 to 6-15, are the composite double-pulse waveform at 2500/3000/3500Vpk volts respectively. The SGTO voltage has a slight voltage rise at turn-off most likely due to the stray inductances and possible instrumentation contribution of voltage probe compensation. The current ramps are calculated to a 1st approximation as linear ramps due to the minimal decay of the voltage/current over the double-pulse time region. The current spikes at the on-set of the 2nd pulse are attributed to the net charge of the free-wheeling diode stray capacitances (including the load inductor's parasitic capacitance) and the dv/dt of that voltage edge. The SGTO adds a decreasing dynamic capacitance to the existing parasitic contributions during this voltage edge excursion, but its major effect on the spike magnitude is at the first 63% of the dv/dt excursion (faster the SGTO, that is a higher dv/dt and the larger the parasitic capacitance a larger generated current spike). It is interesting to note that this was predicted by simulation done by increasing the net parallel capacitance across the load inductance and the free-wheeling diode, and a small capacitance representing the decreased dynamic capacitance of the SGTO during the dv/dt excursion and the results track nicely as the Vpk across the device is increased (causing an increase in the available current; this was done to generate a trend in the effect). If all the parasitic elements are known or at least can be assigned reasonable values a reasonably accurate response could be generated and easily evaluated via simulation or classical analysis.

A key point to remember with all thyristor based devices once they are commanded to turn-on/off there is no means to control their switching speeds other than through the use of external current limiting and snubber/clamping circuitry which tend to introduce other response anomalies and losses.

Waveforms, figures 6-16 to 6-17, are the turn-on times at 3500Vpk for the 1st and 2nd pulses. Turn-on dv/dt ranges between 39 to 53V/nsec between the 1st and 2nd pulses. Even with these fast rise times the modules behaved with minimal ringing and disturbance to the waveforms except for the current spikes on the start of the 2nd current ramps (previously explained).

Waveforms, figures 6-18 to 6-19, are the turn-off times at 3500Vpk for the 1st and the 2nd pulses. Turn-off dv/dt ranges around 40V/nsec for both 1st and 2nd pulses. The disturbances to the waveforms are minimal considering the fast switching at these voltages and currents.

Waveforms, figures 6-20 to 6-21, are the turn-on energies at 3500Vpk for the 1st and 2nd pulses. The turn-on switching energies (Eon is .02 to .9mJ for the 1st pulse and 11.9 to 13.3mJ for the 2nd pulse) attest to the efficient switching of the modules at elevated voltages and currents (3500Vpk/26-31Apk 1st pulse to 38-45Apk 2nd pulse).

Waveforms, figures 6-22 to 6-23, are the turn-off energies at 3500Vpk for the 1st and 2nd pulses. The turn-off switching energies (Eoff is 24.8 to 37.3mJ for the 1st pulse and 27.2 to 43.2mJ for the 2nd pulse) are impressive at the elevated voltage and current (3500Vpk/26-31Apk 1st pulse to 38-45Apk 2nd pulse).

Table 6-3: Module External Static Terminal Capacitance Measurement at VAK=0 (measured w/Fluke Model: 289; a semiconductor parametric analyzer may be a better instrument for this type evaluation or dynamic measurement)

	Capacitance, nF				
Measured Parameter	Mod1	Mod4	Mod12	Mod14	Average
C_{GK}	73.1	73.1	75.2	73.8	73.9
C_{GA}	65	22	298	500	221.3
C_{KA}	21.5	18.4	18.8	22.4	20.3

Summary

Some of the lessons learned:

- Controlling the turn-on/turn-off speeds of the SGTO-based modules (usually by external circuitry means, such as inductance and or snubber/clamp if necessary.
- Instrumentation measurement of conduction/switching losses and key points to consider and address if a contributor of error:
    - HF probe compensation
    - Differential and common mode specifications
    - Degaussing/Re-setting
    - De-skewing
    - HF bandwidth limitations
- Instrumentation, high voltage limitations, as higher voltage/current limits are required.

- Internal module design for better reliability/quality becomes more difficult and taxes the isolating/conducting materials and manufacturing processes' regarding degree of contamination introduction /control as higher voltage/current limits are sought.
- Power flow/capacitive/magnetic coupling effects must be considered at the module design and during testing.
- Proper attention to good HV practices must be adhered to during the design phase if the proper and reliable operation of the module is to be achieved:
    - Minimize high electric field regions (no sharp edges/corners) this helps to mitigate corona inception.
    - Proper choice of insulation systems/inter-connects and attention to dielectric constant/loss tangent of the insulating materials to minimize unexpected creation of parasitic capacitances in critical regions of the module.

- Optical sensitivity of the SGTO requires the module to be designed with an opaque covering to mitigate this effect.

The double-pulse testing allowed for a more detailed switching evaluation for the hard switched, snubberless configuration. The differences between previous test results for the hard switching done at the module level were due to the sinusoidal verses double-pulse, wafer and minor device irradiation differences. The instrument and probe resolution still is an issue and requires great care in compensating measurements properly to get the most accurate and repeatable results especially at these elevated operating voltages and currents.

ABB HV 6.5KV soft recovery die diodes were considered for the resonant application however, they were not available during the scheduled project time. The ST TO247 packaged ultra fast diodes were lower voltage but, were fast and available in sufficient quantity to allow very close matching. This close matching negates the need for matching resistor/capacitor networks (there is a stringent set of parameters associated with passives used to compensate the diodes: non-inductive, high SRF, and power rating). The use of two sets of diodes offered some advantages 1) double the current capability of a single string of diodes, 2) reduce the loop inductance by a factor of two due to the fact that the diode strings are in parallel, 3) reduced power dissipation made diodes less susceptible to temperature effects 4) balance the current through each of the cathode terminals of the SGTO. ST's surface mount version caused real estate issues regarding connection and isolation complications. SemiSouth SiC diodes were also considered in the configurations, but for the resonant configuration it would offer no significant advantage when paired to the SGTO.

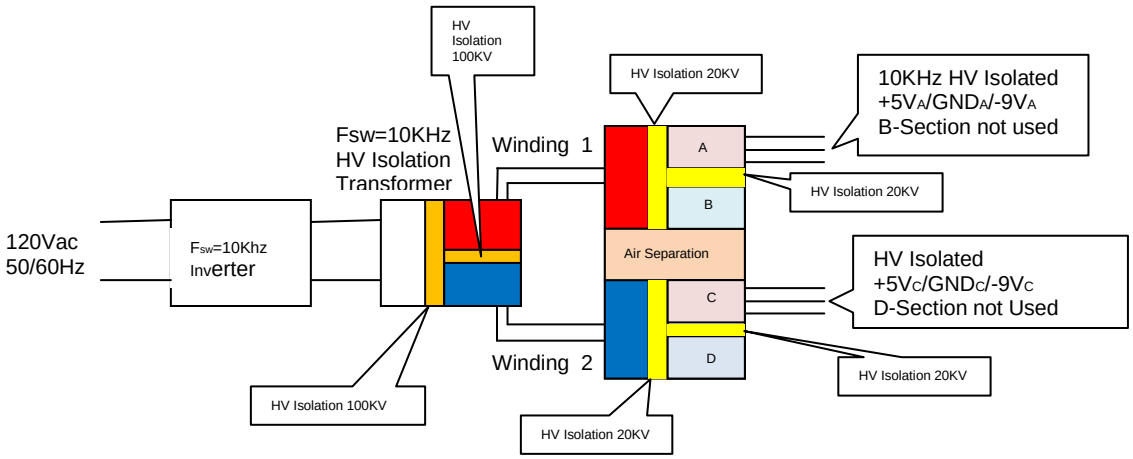


Figure 6-24: High Voltage Isolated Power Supply

The isolated power supply is one of the most important parts of the Ultrafast Power Processor. It maintains the high isolation for supply voltages necessary for multi-level gate driving circuits required to control half/full-bridge modules. Keeping the stray coupling capacitances/inductances between gate driver/modules/instrumentation is especially important to minimize transient effects, such as, current/voltage spikes and spurious resonant noises. Another importance of the isolated power supply is for compliance to hypot and BIL requirements (15KV class systems would require 35KV hypot and 95KV BIL). The SPCO isolation uses dual isolation transformers operating at high frequency to acquire this high level of isolation, small size and light weight needed in a multilevel configuration.

The gate driver circuit also maintains this high isolation established by the HV isolated power supply by optically linking to the signal source or controller. The gate drive requirements were increased to 5A for this application due to the irradiation (the irradiation of these SGTO's causes a deviation from the non-irradiated data sheet specifications that these devices received to trade off conduction losses for better switching losses with the anticipation that these modules could be used for hard as well as resonant switched configurations). There is a need to characterize the gate driver/SGTO with associated power supplies at low duty cycle and high duty cycle at high load

The SGTO modules with matched ultrafast switching anti-parallel diodes demonstrate the ability to hard/resonant switch with low switching and conduction losses. Silicon Power sees the need for a high speed switching S-diode to complement the SGTO voltage, current and switching performance. Silicon Power's efforts over the years have been in the pulse applications and the characterization to that extent. The push for ever higher power at higher switching frequencies allows the SGTO to be very competitive in that playing field. The cost of power real estate, the ability to drive the reactive component sizes down and maintain to high efficiency are favorable attributes for the SGTO-based modules.

The SGTO technologies have been intentionally designed and optimized, to allow tailoring for participation in various pulse and switching applications, where high efficiency switching are mandated. The characterization of these devices for continuous switching applications, such as,

inverters under PWM control, emphasizes the need for additional characterization of the SGTO-based modules and some level of life testing at elevated temperature.

Silicon Power has cooperative efforts with CREE to extend the SGTO technology into the SiC. 10KV to 25KV devices (SiC-GTO and SiC-Diodes) are evolving and at the proto-type stages to meet the ever increasing demands for higher voltage and power. Silicon Power also has cooperative efforts with SemiSouth for the development of high power/speed SiC-J-FET devices. Silicon Power also has present efforts for the integrated/hybrid optical control of these newly evolving devices and the standard Si-SGTO. This will reduce circuit complexity, ease control requirements and allow for a much needed compact easily thermal managed package with high galvanic isolation due to completely optically isolated levels.

Now that the HV isolation and switching functionality of the SGTO-based ¼ bridge module has been independently validated in hard/resonant single/double-pulse/continuous switching, the next logical steps would be to establish a device data sheet with the key device parameters, using lessons learned. Then take these devices and place into a robust half/full-bridge module with optimized galvanic and optically isolated gate drivers and then generate a module data sheet inclusive of the key parameters for the module. Validate performance of this HV/HF module (single module capable of resonant and hard switching) in reference to the data sheet. The next step would be to implement in a single phase 15KV @ 25/50/100KVA or higher if viable.

7 CHARACTERIZATION OF SGTO MODULES AT ENERTRONICS FACILITY

Auxiliary Power Supply and Gate Driver

For high-voltage device characterization, the auxiliary power supply needs to have not only high-voltage isolation, but also high common mode rejection to avoid di/dt and dv/dt induced noise. The gate signal needs to be isolated by optical fiber. In this project, the auxiliary power supply and gate driver are provided by SPCO as a matched set for SGTO driving. Figure 7-1 shows the block diagram of the SPCO power supply. It consists of a square-wave generator, a toroidal transformer for high-voltage isolation, a step-down transformer for to obtain the desire gate drive voltage. The square-wave generator takes the electrical outlet 120-V, 60-Hz ac voltage and produces a 10-kHz, 170-V peak high-frequency power, which feeds into the primary side of the toroidal transformer to serve as the high-frequency AC link source for the down-stream low voltage power conversions.

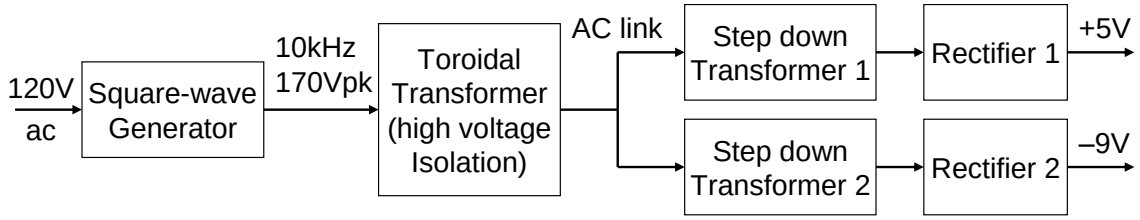


Figure 7-1. Block diagram of the auxiliary power supply.

Figure 7-2 shows experimental setup for the auxiliary power supply test. The output of the power supply is connected to a resistive load bank. The input and output of the toroidal transformer are monitored with the oscilloscope using isolated probes. Figure 7-3 shows the waveforms at each transformer input and output. The high-voltage one with 105.8V rms is the output of the square wave generator or the input of the main toroidal transformer. The two overlapped waveforms are the output of the main toroidal transformer and the output of the small toroidal transformer with 10.65V rms.

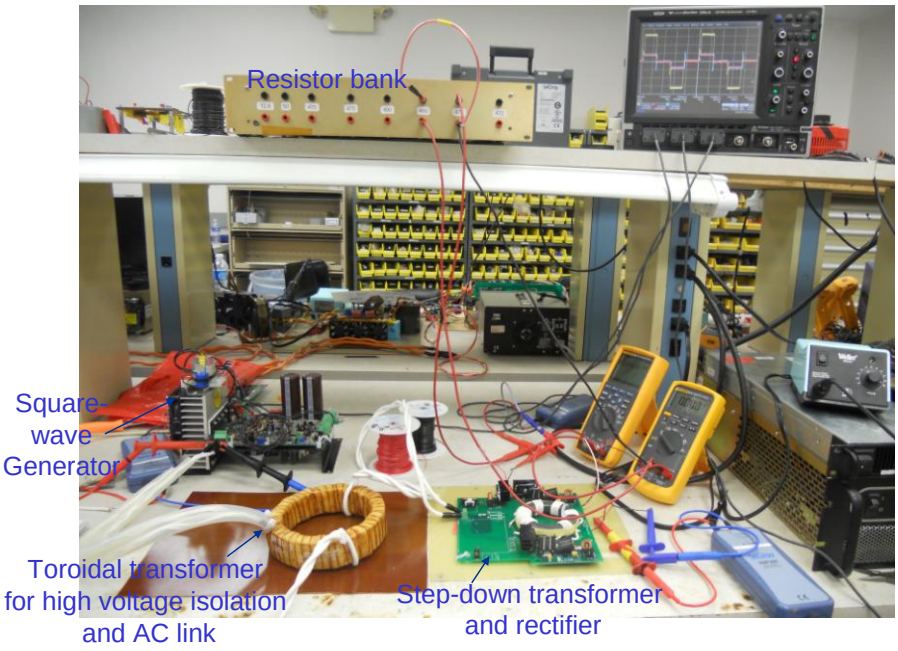


Figure 7-2. Experimental setup for the high-voltage insulated auxiliary power supply.

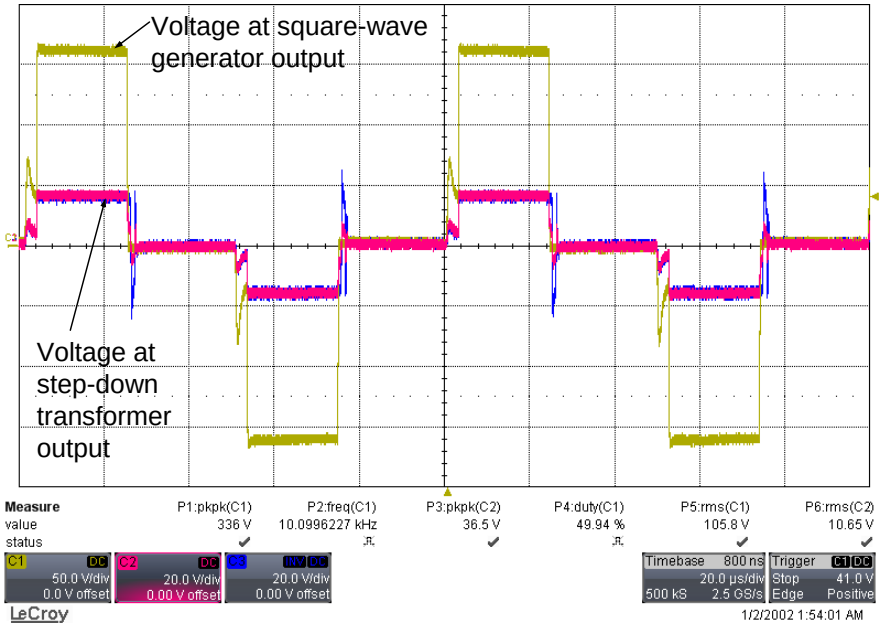


Figure 7-3. Experimental voltage waveforms at different stages.

The gate driver circuit needs +5 and –9 V power supplies. Its gating signal input is from optical fiber receiver, model HFBR 2522. Figure 7-4 shows the photograph of the two-channel gate driver board that fits the module footprint.

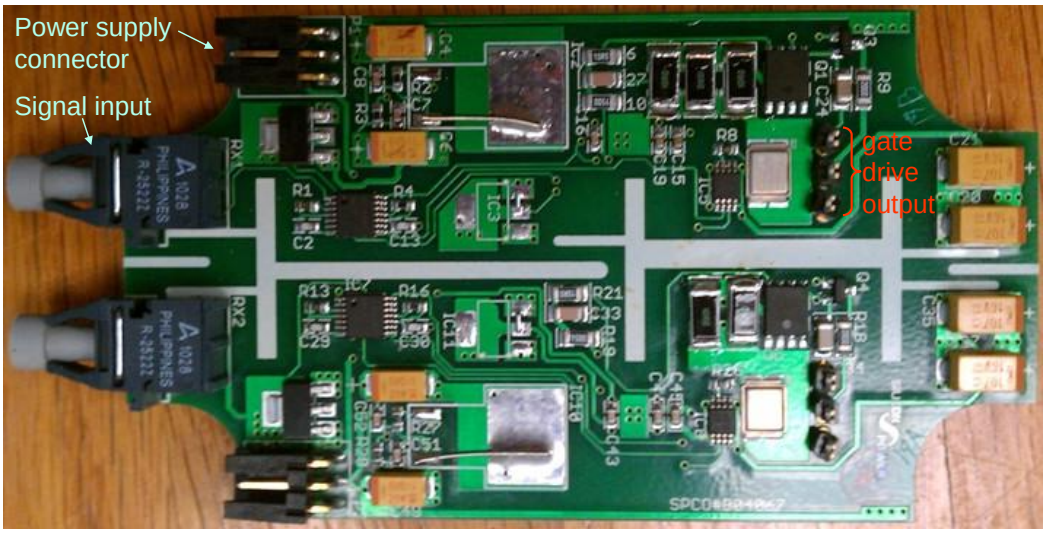


Figure 7-4. Gate driver board that fits the module footprint.

Two-Pulse Tester

Figure 7-5 shows the schematic circuit diagram of a device tester. The main power circuit consists of an SGTO device and an SiC diode, which serves as the freewheeling diode. An inductor L controls the current build-up rate. The gating pulse signal is produced by a pulse generator, which in this case is a digital signal processor (DSP). The output of DSP feeds into a fiber optic interface board and send the light to the gate driver board through a fiber optic cable. The power source is a simple voltage multiplier, which is capable of providing up to 10 kV for high-voltage device testing.

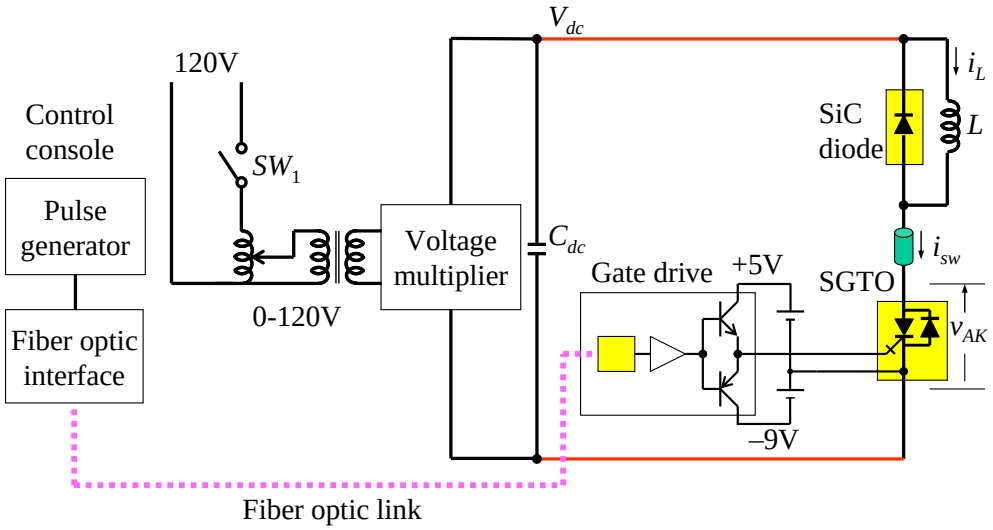


Figure 7-5. Complete test setup of a high-voltage device tester.

The signal needed for device switching characteristic testing is a repetitive two-pulse waveform. To avoid heating up the device, the repetition period T_0 is typically more than 1 s. The first pulse

period T_1 is to build up the inductor current. Time period T_2 is for inductor to freewheel the current, so the device will hard turn on at time period T_3.

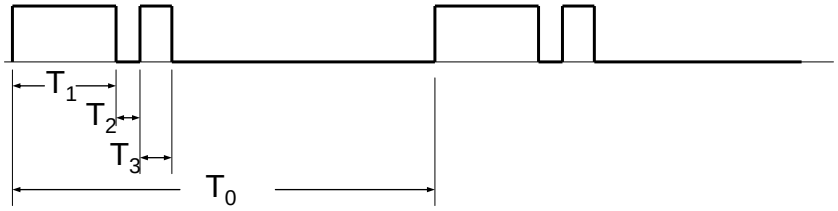


Figure 7-6. Repetitive two-pulse testing waveform.

Figure 7-7 shows possible voltage and current waveforms during each time period. Basic operation is described as follows.

- T_1 period: First pulse is to establish a desire current level I_{test}. The required T_1 time depends on V_{dc} and inductance L, typically ~100µs.
- T_2 period: Turn off the device for a short time to allow diode freewheeling. T_2 depends on how fast can device be turned off, typically <5µs.
- T_3 period: Turn on device again to turn off diode so the reverse recovery characteristic can be observed. T_3 depends on how the device switching speed, typically <5µs.

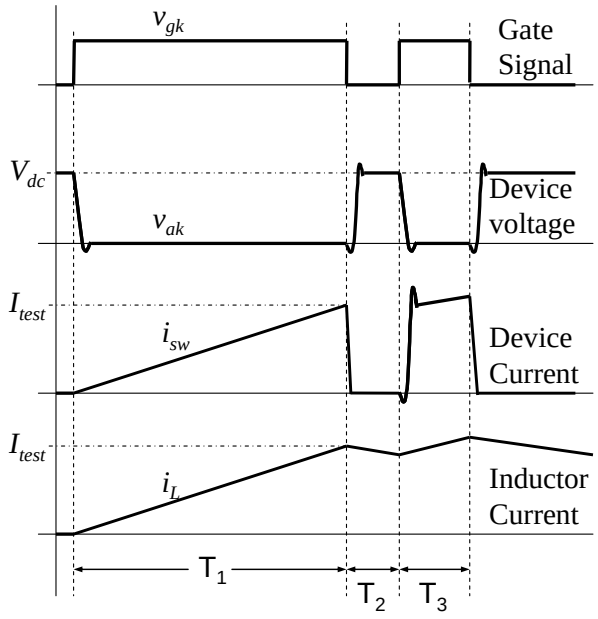


Figure 7-7. Typical voltage and current waveforms under two-pulse test condiction.

The measurement loop unavoidably contains a lot of parasitic inductance between each connecting terminals. Typically, the entire loop inductance includes equivalent series inductance (ESL) of dc bus capacitor, bus bar, current sensor all the wirebond and terminal leads of the devices. The loop inductance varies among different devices and packages. It tends to cause a voltage spike during turn-off. Higher voltage devices tend to have larger parasitic inductances due to voltage insulation requirement. Faster switching devices (higher di/dt and dv/dt) need to have lower parasitic inductances to avoid sever overshoot. The power circuit layout needs to have minimum parasitic loop inductance

Figure 7-8 shows all the parasitic inductances in the main power circuit loop. The total loop inductance L_{loop} that affects the measurement is the sum of all the parasitic inductances in the loop, i.e.,

$L_{loop} = L_{Cdc} + L_{bus} + L_{ad} + L_{kd} + L_{as} + L_{ks}$

where

L_{Cdc}: DC bulk capacitor ESL

L_{bus}: DC bus parasitic inductance

L_a: Diode anode wirebond and lead

L_k: Diode cathode wirebond and lead

L_c: IGBT collector wirebond and lead

L_e: IGBT emitter wirebond and lead

L_{cs}: Current sensor and connections

Normally the connection between the power source V_{dc} and the device tester has a long lead inductance L_{Vdc}, which will interact with the dc bus capacitor C_{dc} and create a low-frequency ripple. Thus, C_{dc} needs to be large enough to avoid the bus voltage swing.

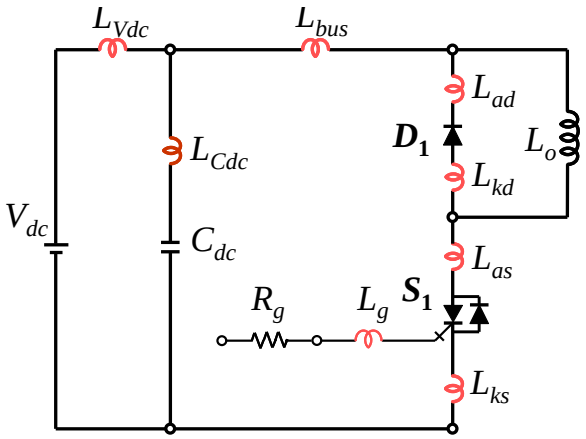


Figure 7-8. Parasitic inductances of the main power circuit in a typical device tester.

With a large C_{dc}, the connection between C_{dc} and the power device tends to have an excessive inductance. Therefore, we added a local bypass capacitor physically right across the power device section. Figure 7-9(a) shows the power circuit with actual components, and Figure 7-9(b) shows the photograph of the added bypass capacitors, which consists of three 5-kV, 10-nF high-frequency polypropylene capacitors in parallel. These added bypass capacitors can significantly cut down L_{bus}. Since SiC diode is only rated 1200V, we connected 5 in series to ensure voltage

withstand capability. To ensure voltage balance, each SiC diode is paralleled with 3-MΩ resistance, which consists of three 1-MΩ resistors in series.

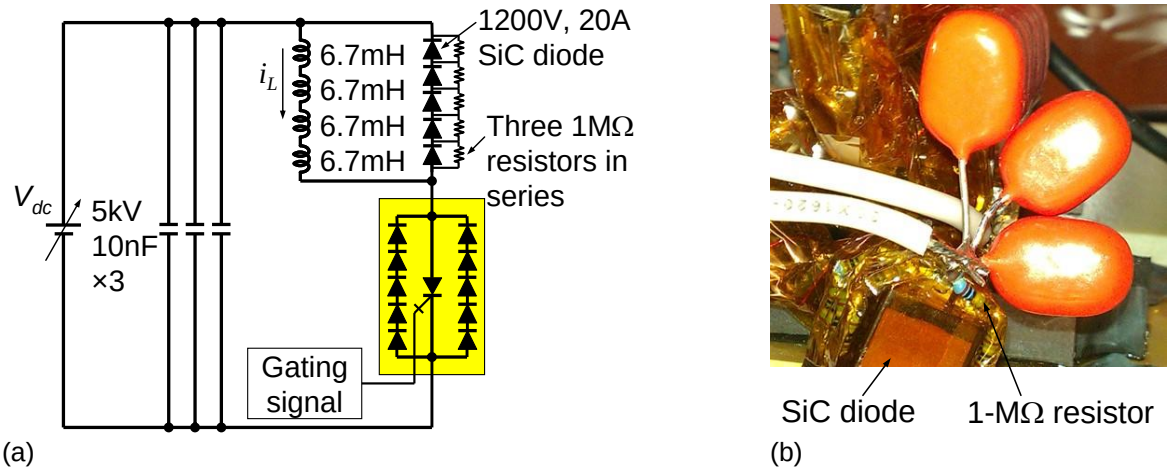


Figure 7-9. Power circuit of the SGTO tester: (a) actual power circuit components and (b) photograph showing diode and high frequency bypass capacitors.

Conduction Voltage Drop Test

The conduction voltage drop was tested with a bench power supply which provided a constant current source. Through some repetitive tests, we found that that device voltage drop v_{AK} was a function of the gate current, as shown in Figure 7-10. Since SGTO is a latch-on thyristor device, this phenomenon is quite unexpected. We assume the gate does not draw much current after turn-on. In this case, the voltage drop seems to be much higher than what we found in the data sheet, which states V_{AK} = 1.8 V at I_A = 50 A under I_G = 500 mA condition.

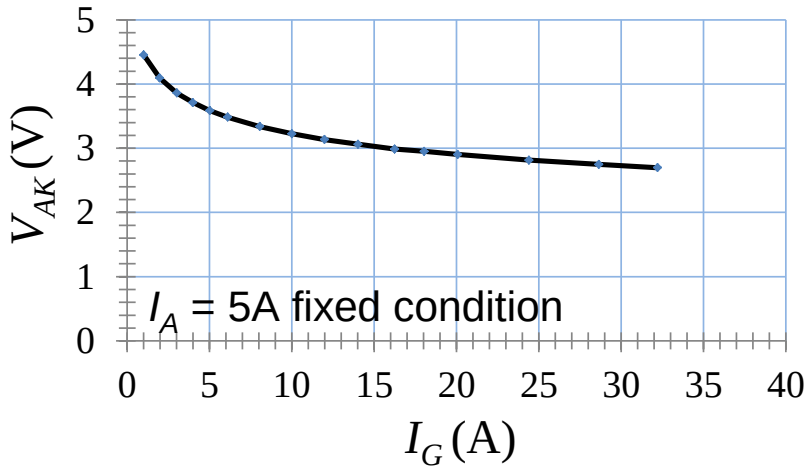


Figure 7-10. Voltage drop as a function of the gate current under I_A = 5 A condition.

Figure 7-11 shows the measurement results with two different test methods. The first one is to fixed the gate current at I_G = 5.86A and I_G = 0 after powered on. The device is then swept with a constant current source from 5 A to 40 A. The second measurement method is to use single-

pulse test and then measure the voltage drop with oscilloscope. The reason to perform the second method is to ensure that the device temperature does not increase during the test.

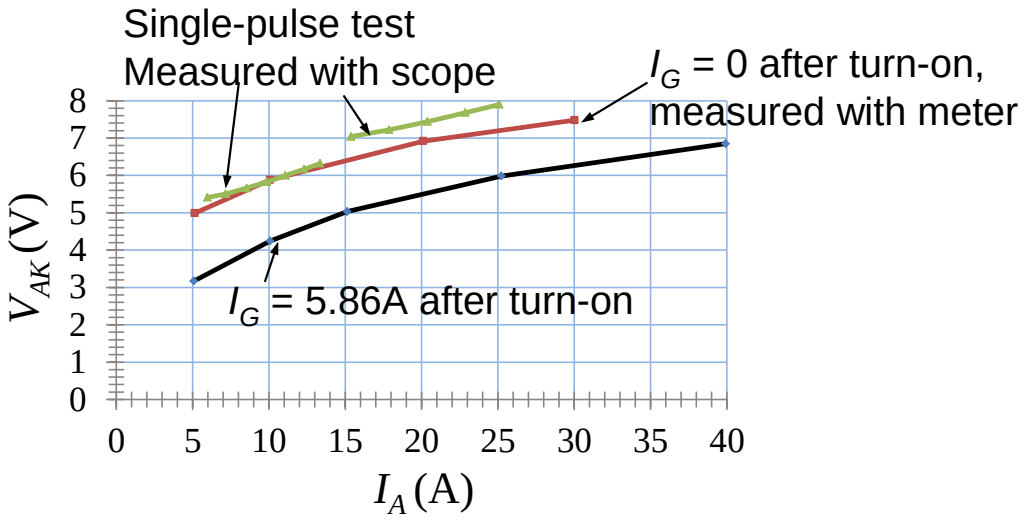


Figure 7-11. Voltage drop as a function of anode current under two different test conditions.

The single-pulse test results agree with the steady-state test under $I_G = 0$ condition from 5 to 13 A range, but their results are slightly higher under higher current conditions, possibly due to measurement error. Nevertheless, both single-pulse test and steady-state test results are much higher than the datasheet value.

In order to further verify the datasheet, we took three additional samples and tested them again. Figure 7-12 shows the measured V_{AK} as a function of I_A for the three samples. The test was stopped at 25A because the heat sink temperature got too hot beyond that, but the results agree with the datasheet better.

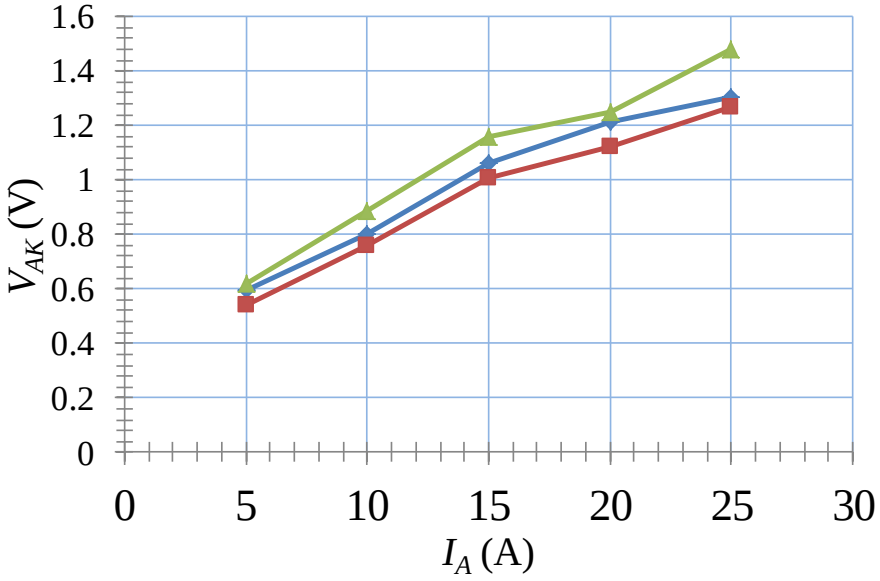


Figure 7-12. Measured voltage drop as a function of current for three test samples.

Figure 7-13 shows the average voltage drop of the three test samples and its trend line extending to 50 A. The voltage drop at 50 A is about 2.3 V, which is higher than the value specified in the datasheet, but is considered low enough for a device with blocking voltage of 5 kV. In other words, the conduction loss at 50 A is less than 0.05%.

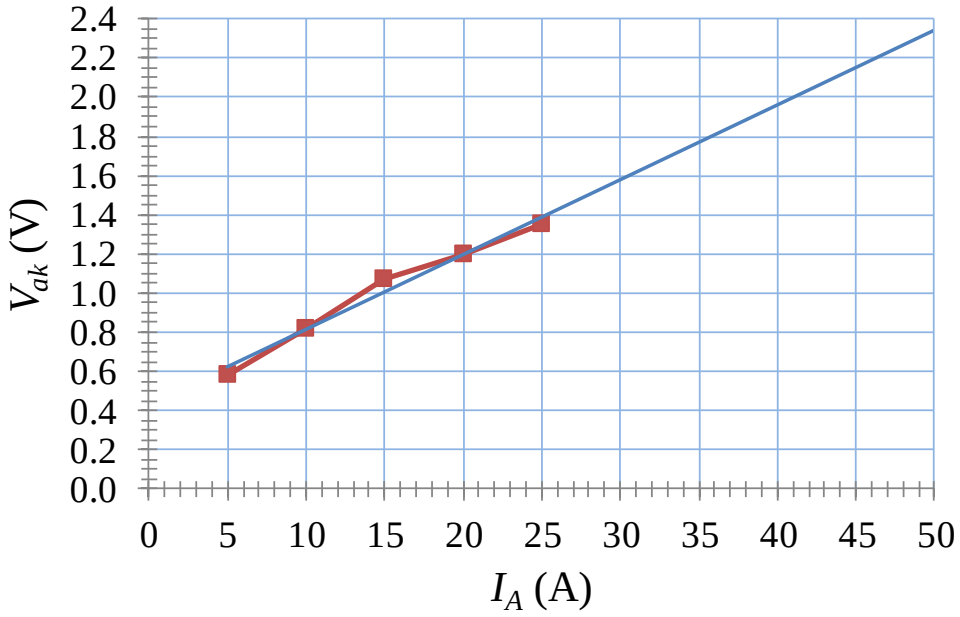


Figure 7-13. Average voltage drop of the three samples and its trend line.

Figures 7-14 through Figure 7-16 show the measured voltage drop for two of the three test samples as a function of the gate current under 5 A, 10 A, and 20 A conditions. The voltage drops of the two samples are very closed except a noticeable variation under 10-A condition. The results are slightly higher than those obtained with the fixed gate current test results. Overall, increasing the gate current tends to decrease the voltage slightly, but not as significant as the one shown in Figure 7-10. Most likely the sample tested in Figure 7-10 has defect in either the chip or the package.

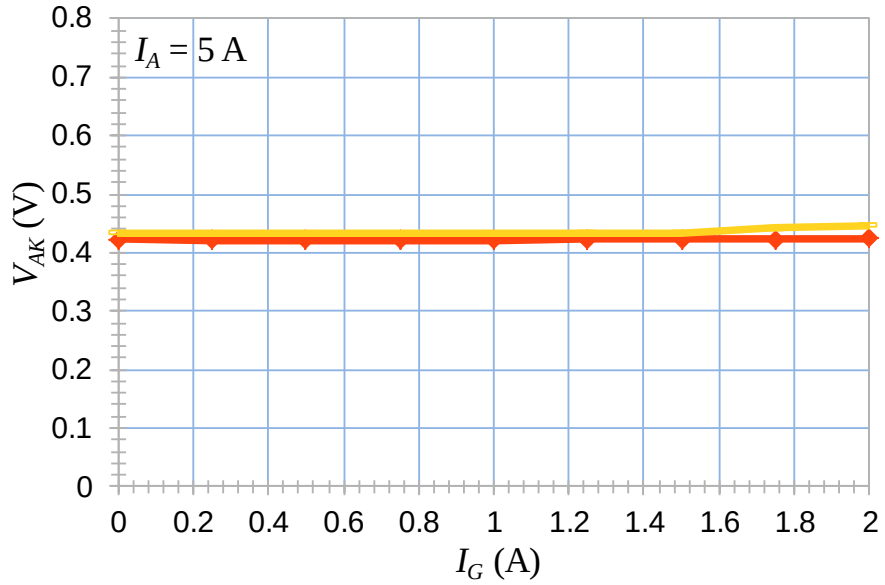


Figure 7-14. Measured voltage drop as a function of the gate current for two test samples under 5-A anode current condition.

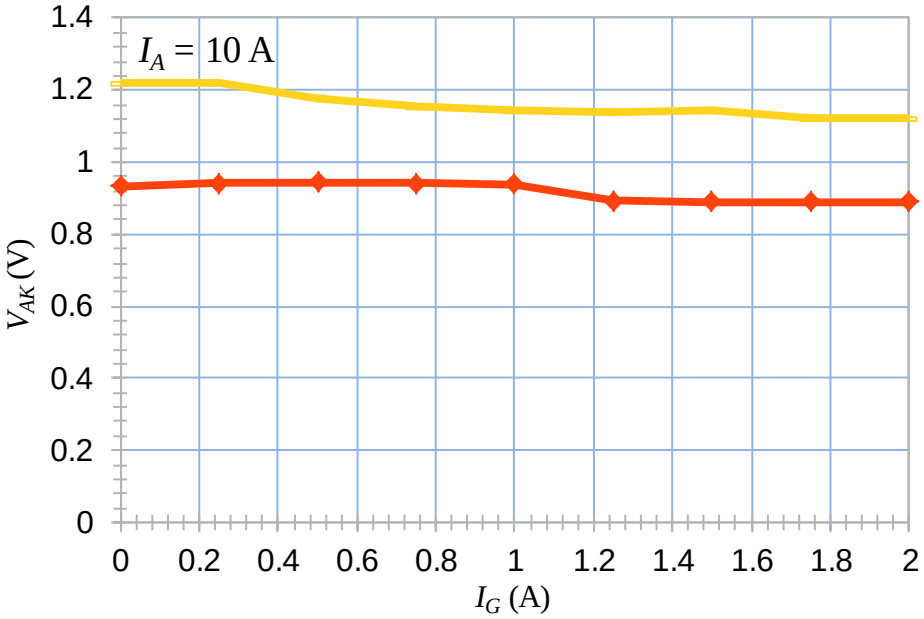


Figure 7-15. Measured voltage drop as a function of the gate current for two test samples under 10-A anode current condition.

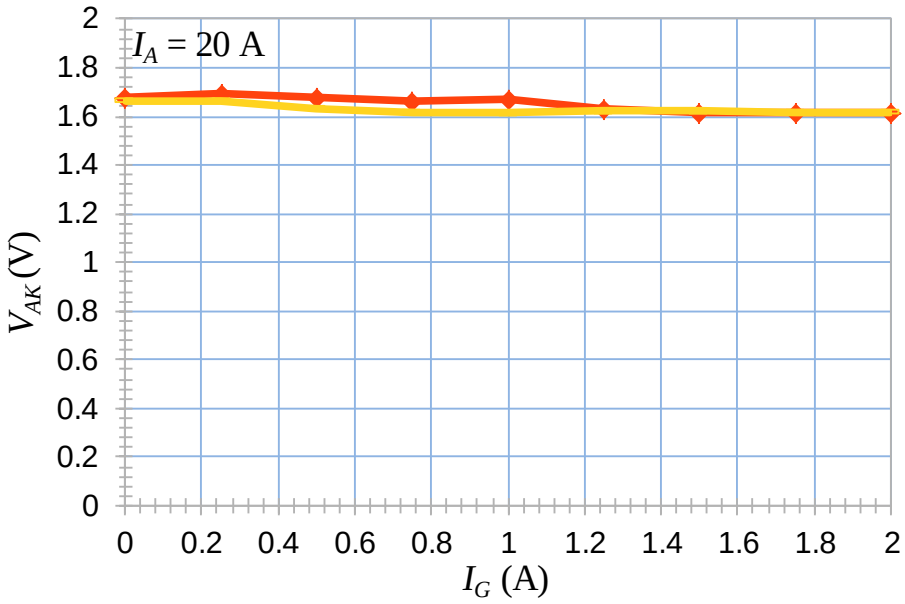


Figure 7-16. Measured voltage drop as a function of the gate current for two test samples under 20-A anode current condition.

In summary, the conduction voltage drop measurement results indicate that SGTO has excellent conduction characteristics despite inconsistency among some prototype devices. For a 5-kV blocking voltage level, the voltage drop is less than 2.5 V under 50-A condition. If the device is adopted in a converter operating under soft-switching condition, then the converter can achieve ultrahigh efficiency.

Switching Test

Setup and Current Measurement Calibration

The device voltage measurement is done with a non-isolated probe that has a bandwidth of 400 Mhz. However, the device current measurement is quite difficult to match such a bandwidth and is likely to create significant measurement error. Table 7-1 compares three commercially available current monitoring devices. The T&M current viewing resistor (CVR) has the highest bandwidth and lowest rise time, but it tends to introduce too much parasitic inductance and distort the waveforms. The Rogowski coil is ideal with sufficient bandwidth and reasonable rise time. It can be inserted into the device pins and will not create any additional parasitic inductance. The Pearson current transformer (CT) shows reasonable bandwidth and rise, but its height prevents it from inserted into the loop without creating significant inductance. Therefore, the Rogowski coil was first selected for the current measurement.

Table 7-1. Comparison of current monitoring devices

	Bandwidth (MHz)	Rise time (ns)	Current Range
T&M CVR (SDN-414-10)	2000	0.18	5-A dc
Rogowski Coil (CWT 3B)	50	1.5	200-A ac rms
Pearson CT (411)	20	20	50-A ac rms

Figure 7-17 shows the photograph of the device switching test setup with the use of Rogowski coil. The inductor current is measured with the scope current probe to serve as the calibration purpose. The dynamic response of inductor current measurement is not crucial, but its steady-state accuracy needs to be good, so the output of Rogowski coil can be calibrated. The photograph also indicates key components in the test including inductor, DC bus capacitor C_{dc}, pulse generator, and voltage multiplier capacitor bank.

At a relatively low voltage (800 V), the device was tested to check the gate driver functionality am waveform consistency and measurement delay. Figure 7-18 shows the measured device voltage, current, gate drive output, and inductor current. It can be seen that the gate drive output voltage v_{GK} drops to about 1 V during turn-on, but it maintains at –9V during turn-off. The measured device anode current i_A is slightly mismatched with the inductor current i_L during dynamic rising periods.

Notice a strange phenomenon happens on the device voltage v_{AK}, which has a small bump after device is turned on. Because this is a relatively low voltage input, the current rise rate di/dt is also low. Most likely, the device is trying to turn back off with insufficient holding current.

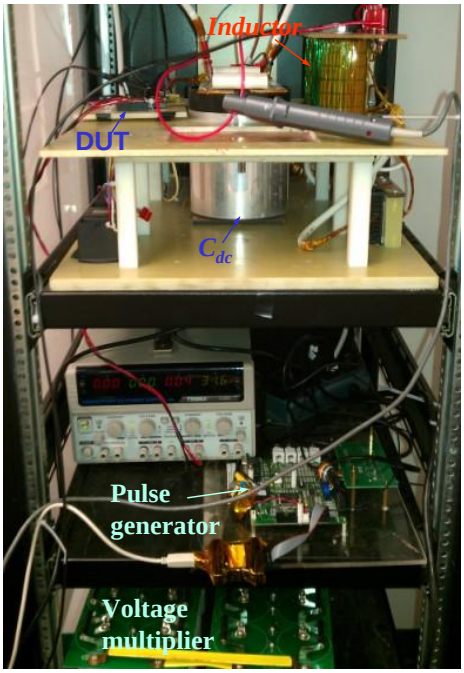


Figure 7-17. Photograph showing switching test setup.

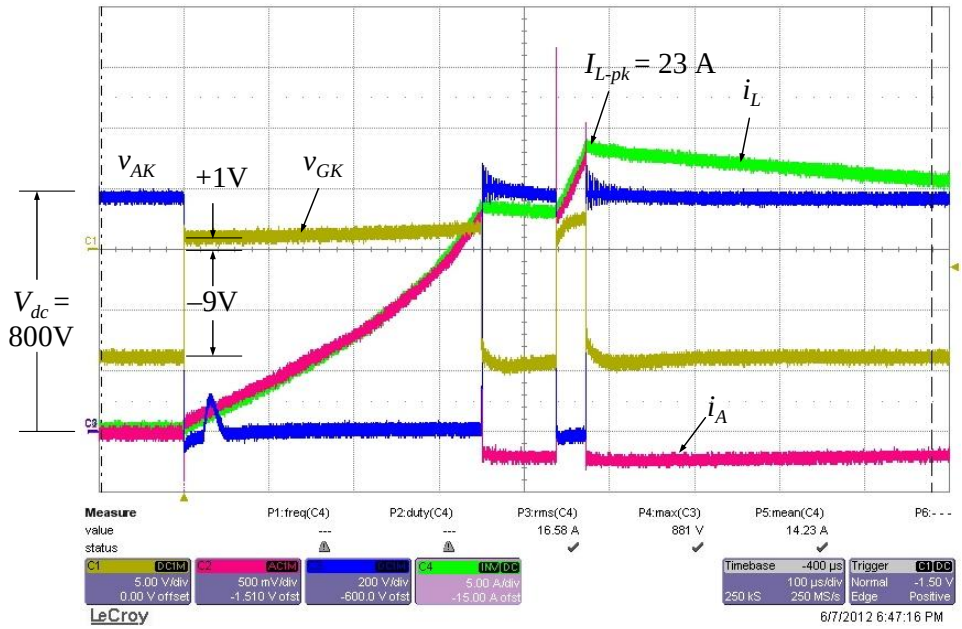


Figure 7-18. Initial test with Rogowski coil at 800-V DC bus voltage condition.

Figure 7-19 shows detailed current bump during device turn-on process. The energy of this bump is nontrivial. With a peak voltage around 60 V and non-zero current, the calculated energy is about 2.2 mJ.

The second pulse during time period T_3, shown in Figure 7-20, does not have such a current bump because the device current is high enough to avoid going under holding current range. Notice that the gate voltage v_{GK} increases as the device current i_A increases. At this current condition, the gate voltage is slightly higher than 2 V during device conduction.

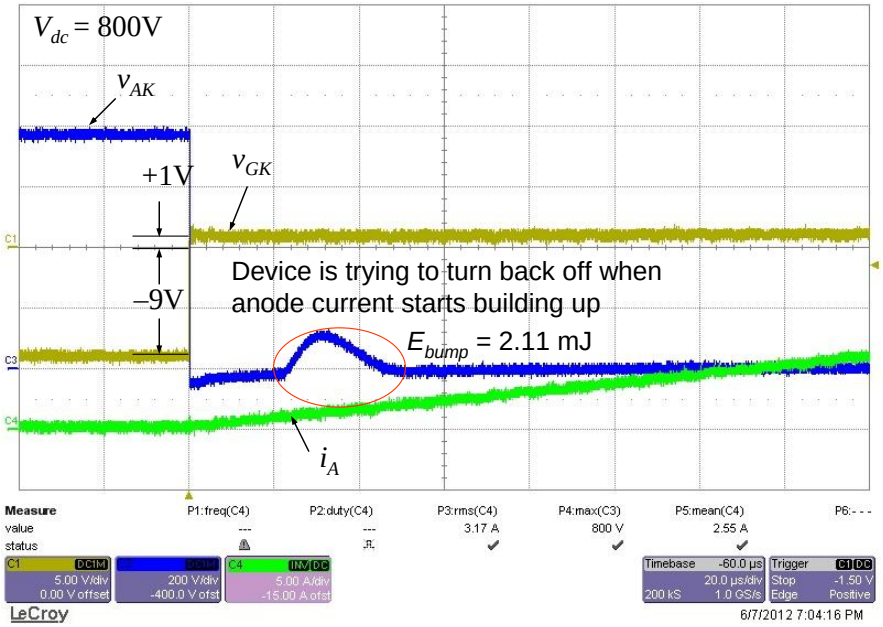


Figure 7-19. Voltage bump during initial current build up.

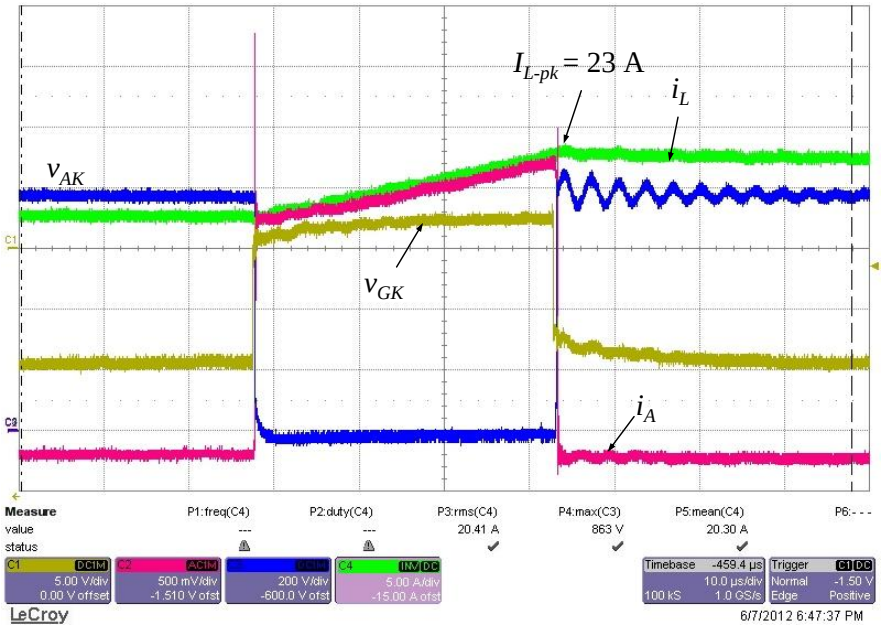


Figure 7-20. Switching waveforms during T_3 period with Rogowski coil at 800-V DC bus voltage condition.

The recorded data was processed with Excel spreadsheet for switching energy calculation. Figure 7-21 shows detailed turn-on voltage, current, and energy waveforms. The turn-on energy, E_{on} = 1.52 mJ, is obtained from the integration of the voltage v_{AK} and current i_A product. A noticeable current spike is observed. This appears to be the reverse recovery current of the diode, and the phenomenon poses a question about the validity of the measurement because the diode is majority carrier SiC Schottky diode. Our guess is the current is caused by the high-voltage field.

Figure 7-22 shows the detailed turn-off voltage, current, and energy waveforms. The turn-off energy, E_{off} is measured at 2.4 mJ, which is also skeptical because the current falling waveform is very unusual and is not corresponding to the voltage rise, we suspect again the high-voltage field or high dv/dt is causing the measurement problem with the Rogowsky coil.

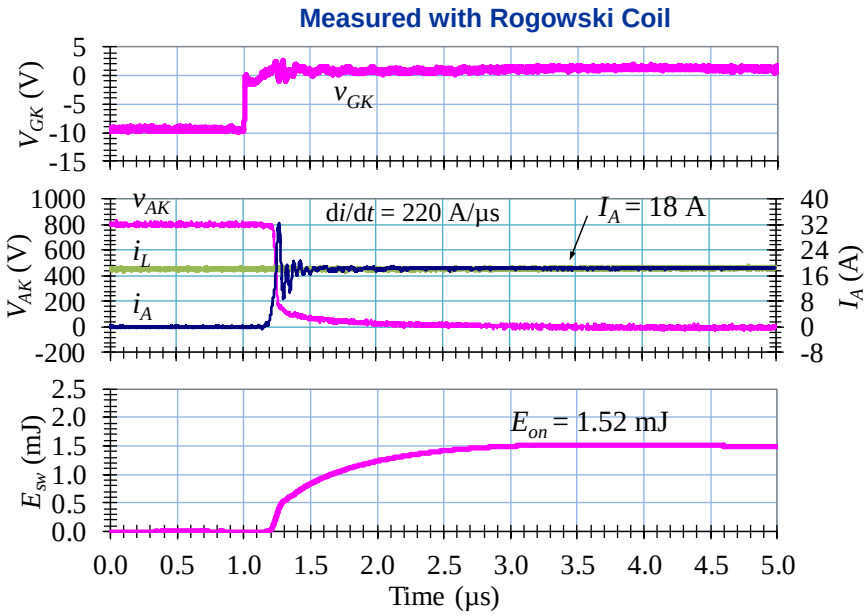


Figure 7-21. Detailed turn-on waveforms during T_3 period with Rogowski coil at 800-V DC bus voltage condition.

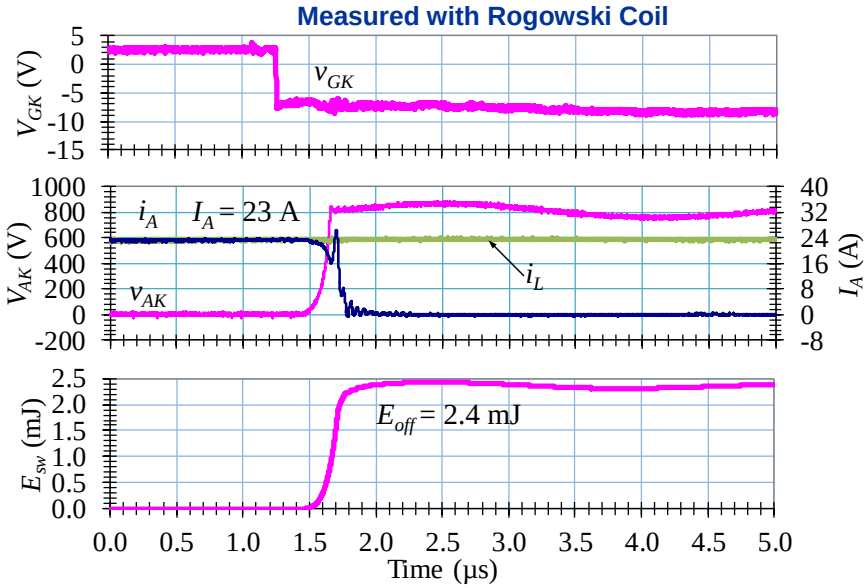


Figure 7-22. Detailed turn-off waveforms during T_3 period with Rogowski coil at 800-V DC bus voltage condition.

With some repetitive testing using the Rogowski coil, we concluded that its measurement results were unreliable. The following list briefly summarizes Rogowski coil measurement approach.

- Reasonably clean waveform with minimized loop inductance.
- Significant delay is observed and thus the results are non-trustable
- Waveform is highly distorted by the high voltage field; high dv/dt causes the coil to produce some spiky currents, especially at turn-on.
- Measurement delay can be adjusted in spreadsheet, but the waveform distortion or current spike cannot be compensated.
- Overall, Rogawsky coil is an inappropriate measurement tool in the high-voltage environment

Measurement with Pearson Current Transformer

The Pearson current transformer (CT) is too balky to be used without inserting significant leakage inductance. In order to use this high bandwidth CT, we inserted a small ferrite core to the device pin to create a 10:1 current ratio for the subsequent Pearson CT measurement. This avoids creating additional inductance while maintain sufficient bandwidth. Figure 7-23 shows measured voltage and current waveforms under 1200-V DC bus voltage, 10-A condition using Pearson CT for current measurement.

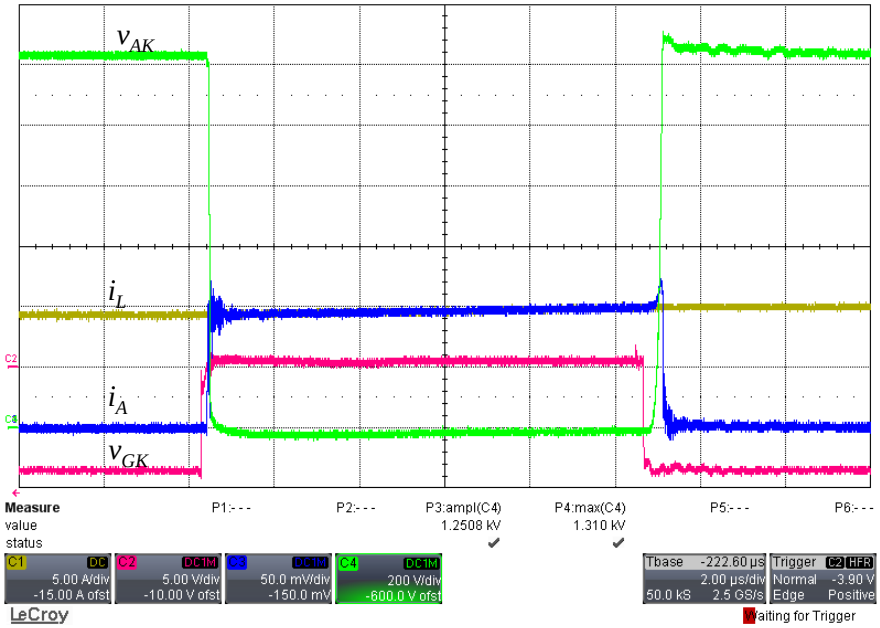


Figure 7.23. Switching test waveforms at 1200-V DC bus voltage condition using Pearson CT for current measurement.

Figure 7-24 shows the same measured voltage and current waveforms with energy calculation results obtained from spreadsheet calculation. Notice that both turn-on energy E_{on} (0.6 mJ) and turn-off energy E_{off} (1.7 mJ) are significantly lower than those measured with the use of Rogowski coil even with a significantly higher voltage condition. Most importantly, the current spike during turn-on no longer appears. This result is more explainable and provides better confidence. Therefore, we decide to move ahead with Pearson CT approach for the 2-kV testing.

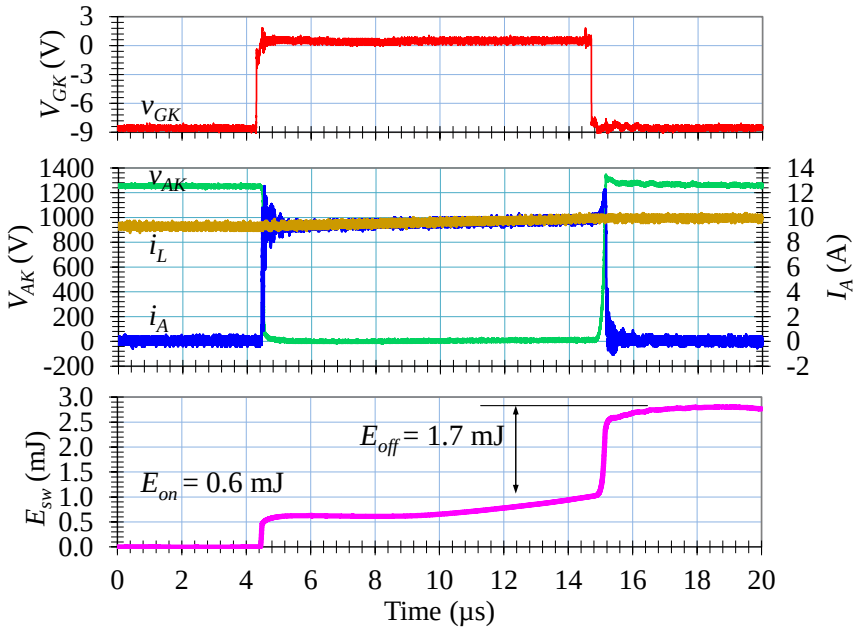


Figure 7-24. Switching waveforms during T_3 period with Pearson CT under 1200-V DC bus voltage condition.

Figure 7-25 shows switching waveforms during T_3 period with Pearson CT under 2000-V DC bus voltage condition. Again, there is not a significant turn-on current spike, and the current measurement under this high-voltage condition is more trustable than that of Rogowski coil measurement result. Figure 7-26 shows the same measured voltage and current waveforms with energy calculation results obtained from spreadsheet calculation. Here the turn-on energy E_{on} (0.72 mJ) is not a big increase over the previous 1200-V case, but the turn-off energy E_{off} (4.3 mJ) is a significant increase from the 1200-V case. The main reason is a current spike occurred during voltage rise edge.

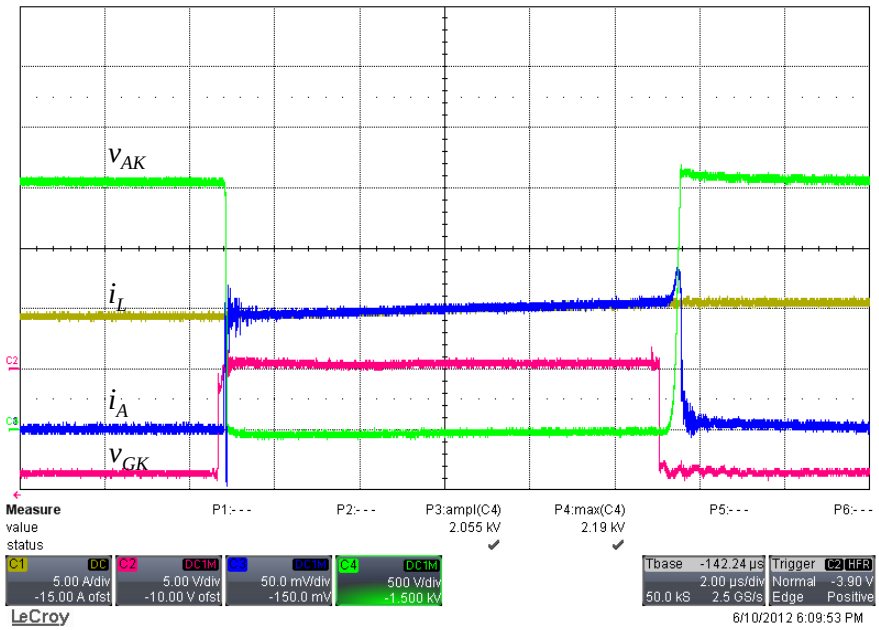


Figure 7-25. Switching waveforms during T_3 period with Pearson CT at 2000-V DC bus voltage condition.

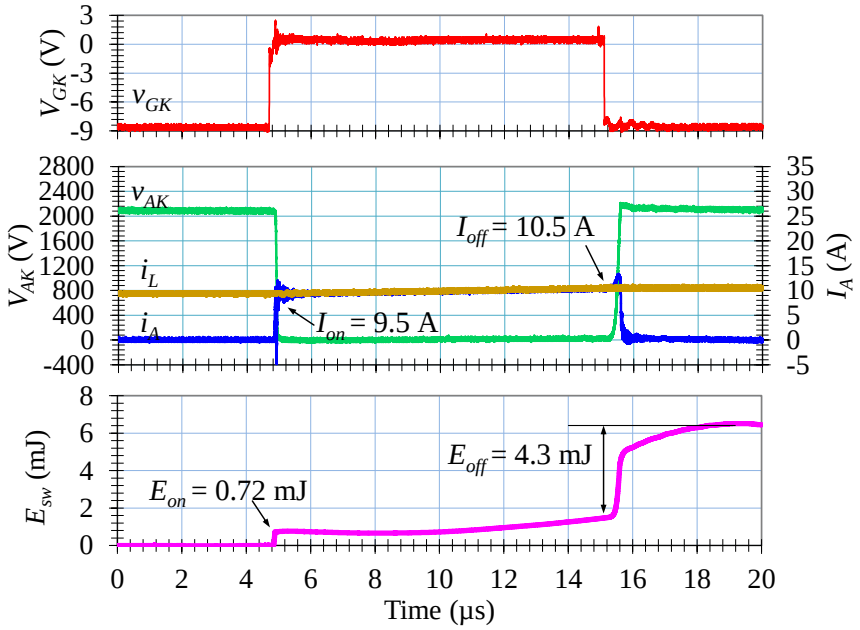


Figure 7-26. Switching waveforms and calculated energy at 2000-V, 10-A condition.

Figure 7-27 and Figure 7-28 show the exploded view of turn-on and turn-off voltage and current waveforms and the calculated switching energies. During turn-on, there is a current dip that corresponds to the device voltage falling from full voltage to zero. Similarly, during turn-off, there is a current swing that corresponds to the device voltage rising from zero to full voltage. This is most likely caused by the parasitic capacitance between A and K junctions. By aligning the timing, the results seem explainable, and are apparently not the measurement error. The turn-on current dip or undershoot is the main reason that the turn-on energy remains low, and the

turn-off current swing or spike is the main reason that turn-off energy increases substantially as compared to the lower voltage test results.

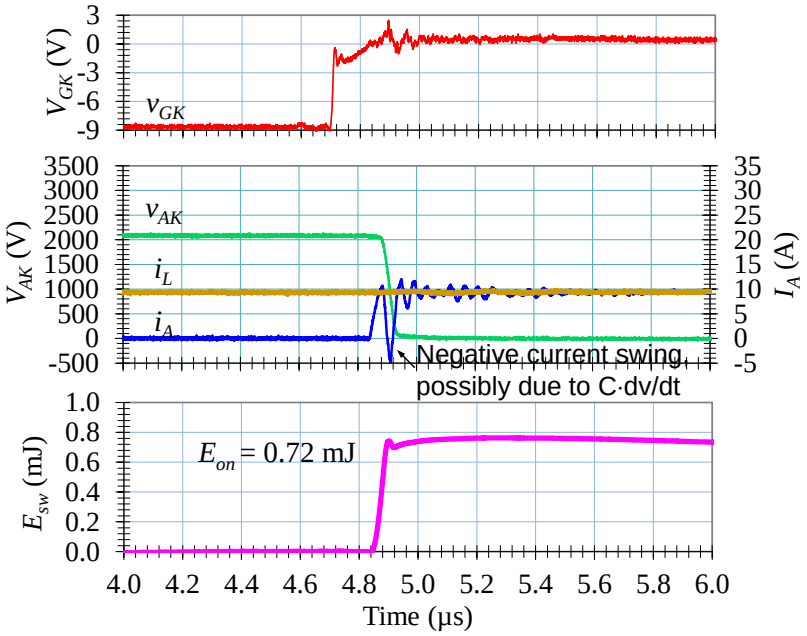


Figure 7-27. Detailed turn-on waveforms and calculated energy at 2000-V, 10-A condition.

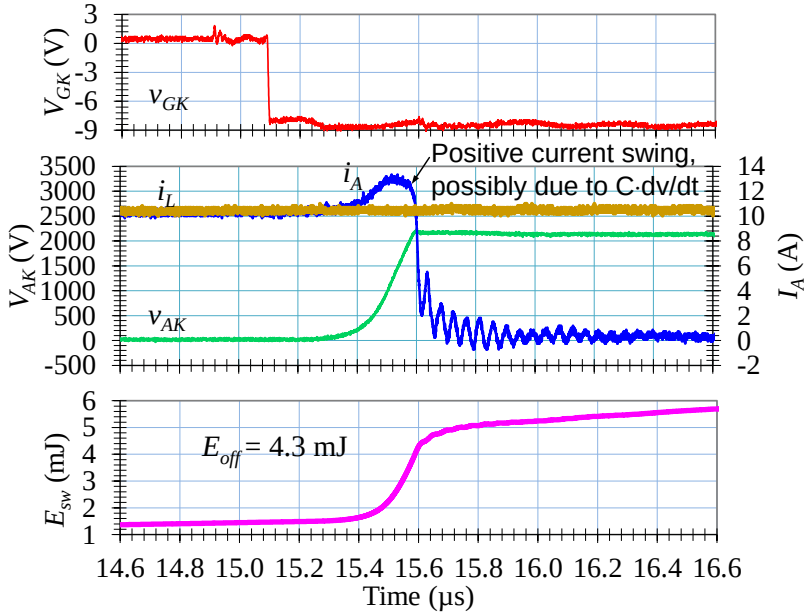


Figure 7-28. Detailed turn-off waveforms and calculated energy at 2000-V, 10-A condition.

Figure 7-29 shows the switching voltage and current waveforms under 2000-V, 25-A condition. The current was measured with the Pearson CT again. There is a noticeable high-frequency switching noise during turn-on, which again, is most likely caused by the fast rate of device voltage change (dv/dt). Similarly, a noticeable device current spike occurs during turn-off

voltage rise edge. Figure 7-30 shows the same measured voltage and current waveforms with energy calculation results obtained from spreadsheet calculation.

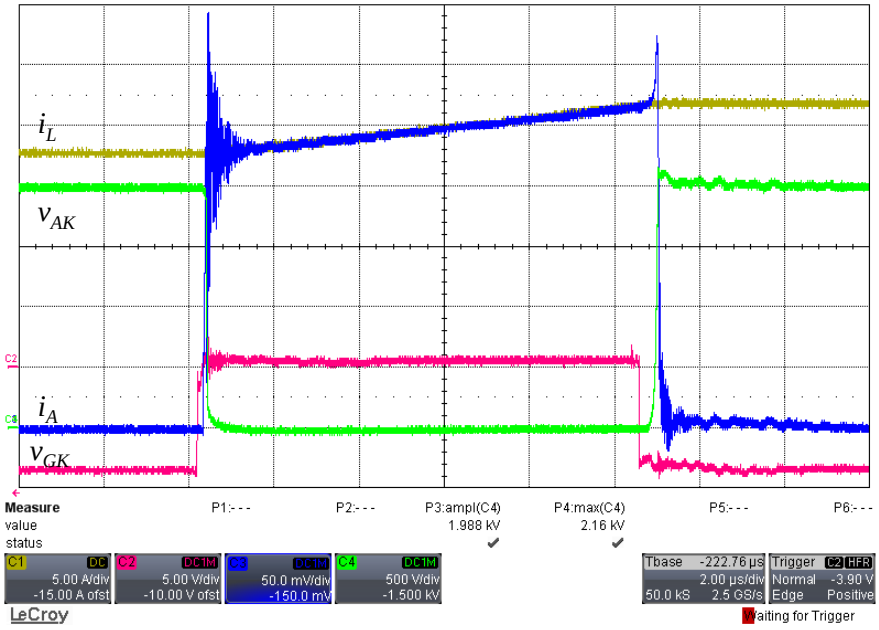


Figure 7-29. Switching voltage and current waveforms under 2000-V, 25-A condition.

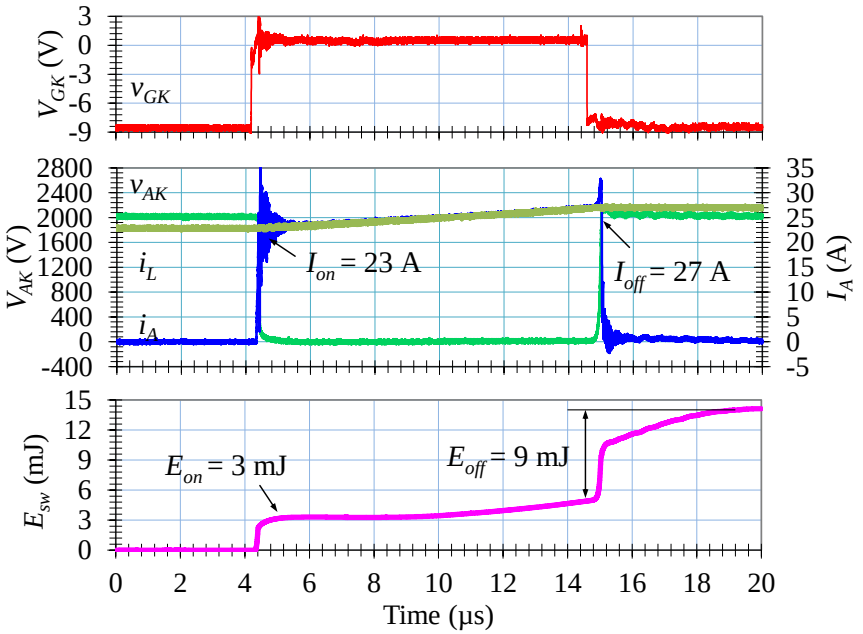


Figure 7-30. Switching waveforms and calculated energy at 2000-V, 25-A condition.

Figure 7-31 and Figure 7-32 show the exploded view of turn-on and turn-off voltage and current waveforms and the calculated switching energies under 2000-V DC bus voltage, 25-A nominal current test condition. With a higher current (23 A) condition, the turn-on current dip that corresponds to the device voltage falling edge does not go below zero. This explains why the turn-on energy (3 mJ) is significantly increased from 10-A measurement condition. The turn-off

current swing that corresponds to the device voltage rising edge remains noticeable, and the turn-of energy (9 mJ) also represents a significant increase from 10-A measurement result.

In order to verify the output capacitance induced current, we measure the device capacitances for 5 samples and find their average capacitances between A, K, and G terminals. Table 7-2 lists the measurement results.

Table 7.2. Measured capacitances at zero device voltage condition.

Capacitance (nF)	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Average
C_{AK} @ v_{AK} = 0	49.9	71.4	60.4	54.7	59.1	59.1
C_{KA} @ v_{AK} = 0	44.7	74.8	61.2	45.7	51.9	55.7
C_{KG} @ v_{AK} = 0	75.8	75.1	76.5	75.6	77.6	76.1

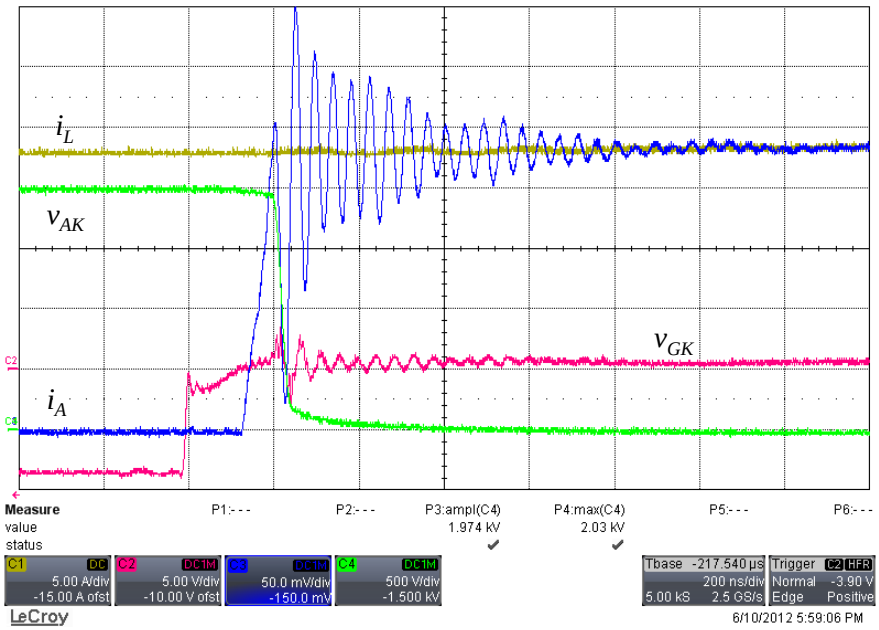


Figure 7-31. Detailed turn-on waveforms at 2000-V, 23-A condition.

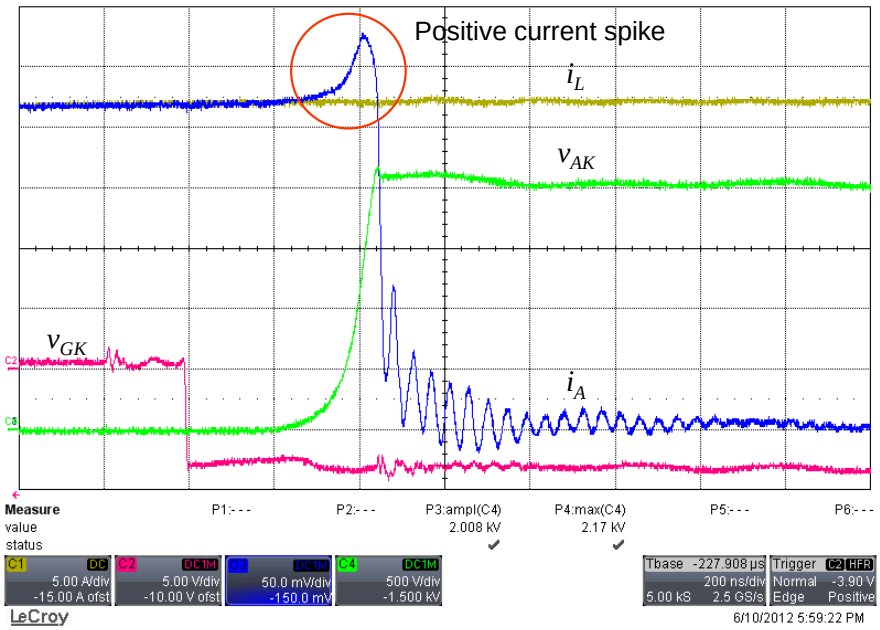


Figure 7-32. Detailed turn-off waveforms at 2000-V, 27-A condition.

The average output capacitance under zero device voltage is 59.1 nF. This capacitance will be drastically reduced when there is a voltage across A and K. Assuming the equivalent output capacitance under switching condition is 1% of the capacitance under zero voltage condition, the capacitance induced current during turn-on and turn-off can be calculated as follow.

During turn-on, dv/dt = –37.5 V/ns, $i_{C\text{-}on}$ = –22.2 A

During turn-off, dv/dt = 15 V/ns, $i_{C\text{-}off}$ = 8.9 A

The waveforms shown in Figures 5.15 and 5.16 indicate that $i_{C\text{-}on}$ = –22.5 A, and $i_{C\text{-}off}$ = 9 A. These measurement results agree with the theoretical calculation very well.

8 COMPARISON WITH HV-IGBT TEST RESULTS

Conduction Voltage Drop Comparison

The EPRI high-voltage IGBT (HV-IGBT) module was developed by Powerex for intelligent universal transformer (IUT) applications. The internal schematic circuit diagram and photograph of the HV-IGBT module are shown in Figures 8-1(a) and 8-1(b). The module was designed for diode-clamp type multilevel converters. It consists of four IGBT devices. Each IGBT is rated 4500 V, 60 A. All the matched diodes are also rated with the same voltage and current. The phase-leg represents 9000-V blocking capability, or 2.4 times the peak DC bus voltage. The intention of designing such a module is to avoid connection wire induced parasitic inductance. However, the insulation requirement of the medium voltages level prevents it from compact and low inductance.

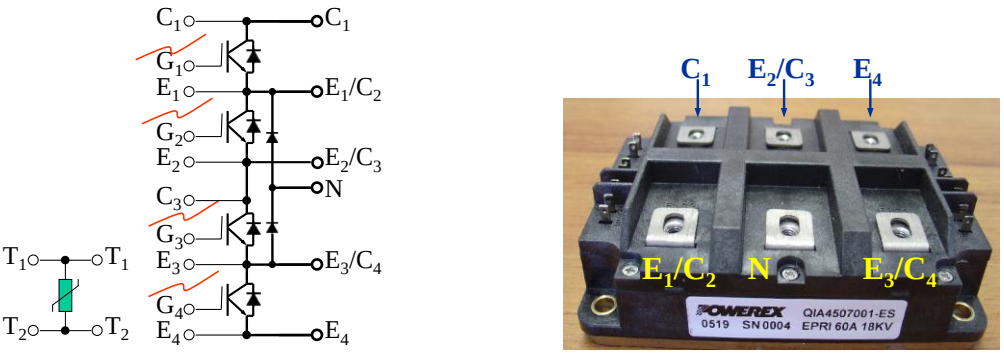


Figure 8-1. HV-IGBT: (a) Internal schematic circuit diagram and (b) photograph of a prototype module.

Figure 8-2 shows the conduction voltage drop of a prototype HV-IGBT module. There are some variations between different switches, but the overall HV-IGBT voltage drop is significantly lower than the measurement results obtained from the SGTO. For an input average device current at 10.5 A rms, the HV-IGBT voltage drop is less than 2.4 V, or 0.1%. The SGTO with similar voltage blocking capability has a voltage drop of 6 V, or 0.25%.

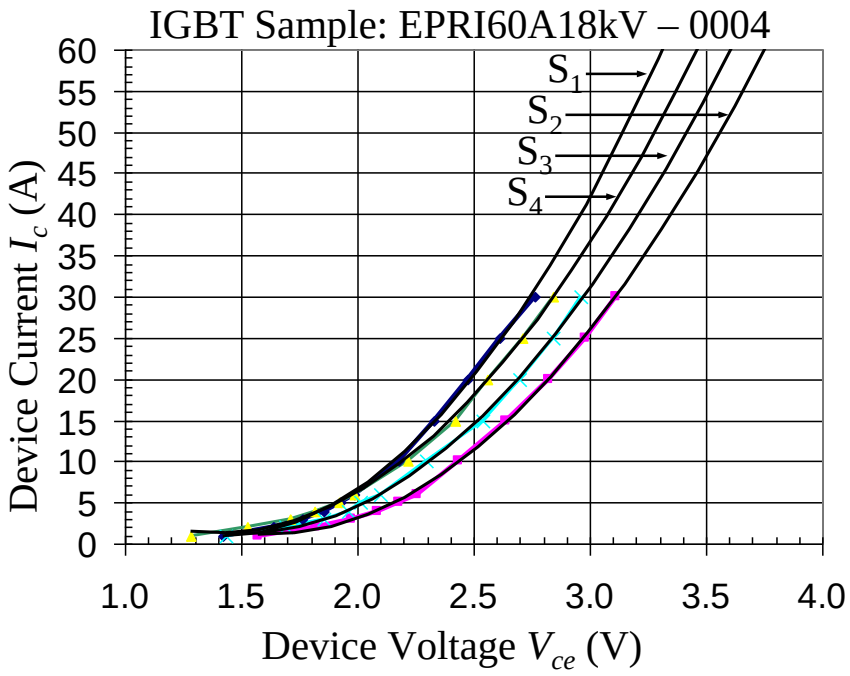


Figure 8-2. Conduction voltage drop of the EPRI HV-IGBT module.

Switching Loss Comparison

Note that the high-voltage silicon diodes used in the HV-IGBT module are relatively slow as compared to the SiC diodes used in the SGTO testing. The reverse recovery current and therefore the loss can be very significant. Figure 8-3 shows the two-pulse test results of the HV-IGBT under 2000V, 11A condition.

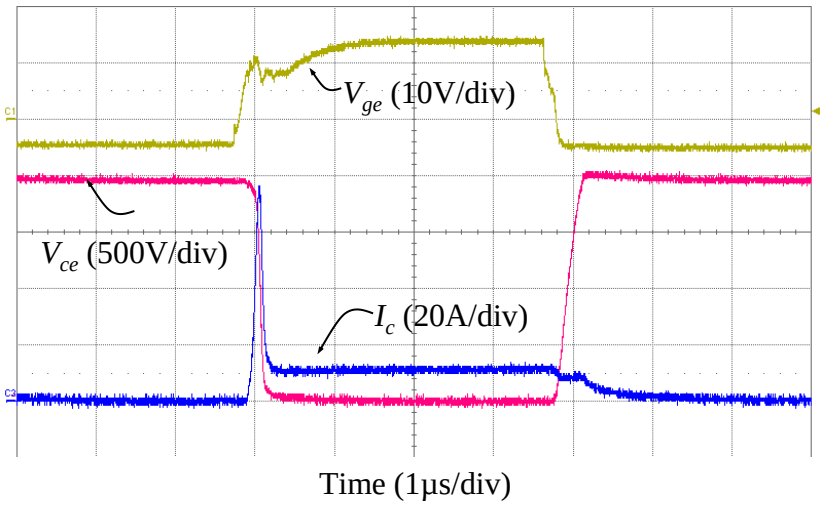


Figure 8-3. Measured voltage and current waveforms during T_3 period.

Figure 8-4 shows detailed HV-IGBT turn-on device voltage and current waveforms under 2000-V, 11-A condition. The turn-on energy E_{on} is 11.2 mJ, which is significantly larger than the E_{on}

measured with SGTO and SiC diode combination (0.72 mJ). There are three major reasons that cause such a big difference.

1. Much faster switching speed. The turn-on current rise time is 40 ns with SGTO, but it is 150 ns with HV-IGBT.
2. Diode reverse recovery. The SGTO turns on by turning off SiC Schottky diode, while HV-IGBT turns on by turning off silicon diode.
3. Current notch created by the Cdv/dt. The SGTO junction capacitance interacting with the ultrafast dv/dt rate that creates a current notch that undershoot to negative and thus reducing the turn-on energy.

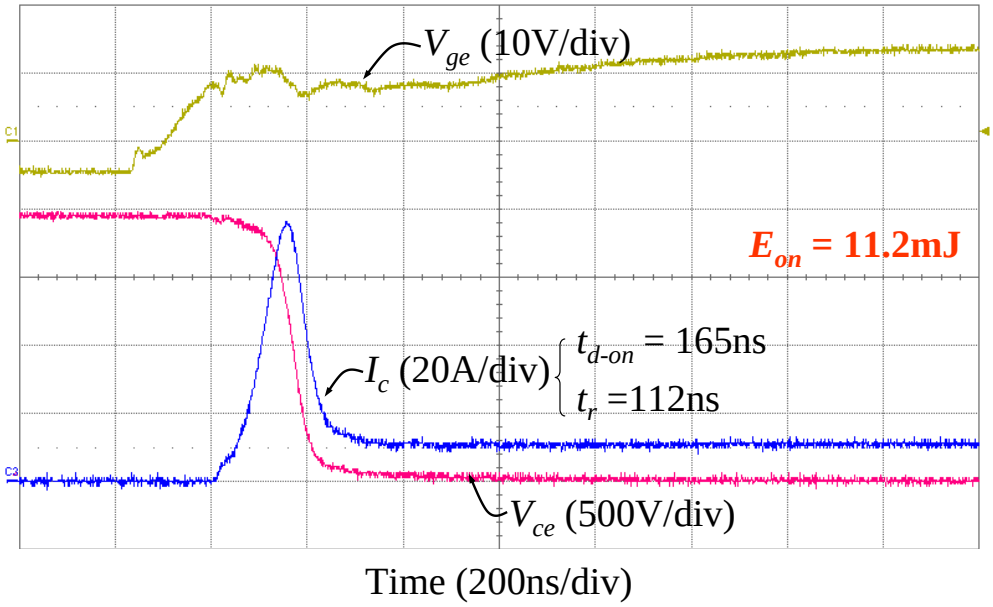


Figure 8-4. Detailed HV-IGBT turn-on device voltage and current waveforms under 2000-V, 11-A condition.

Figure 8-5 shows detailed HV-IGBT turn-off device voltage and current waveforms under 2000-V, 11-A condition. The turn-off energy E_{off} is 10.6 mJ, which is also higher than the E_{off} measured with SGTO (4.3 mJ). The main reason can be attributed to the first turn-off current fall. This difference can be attributed to a much faster turn-off with SGTO and a tail current that increases turn-off loss significantly. Note that the turn-off dv/dt with HV-IGBT is 8.1 V/ns, but with SGTO is 13.3 V/ns under this current condition.

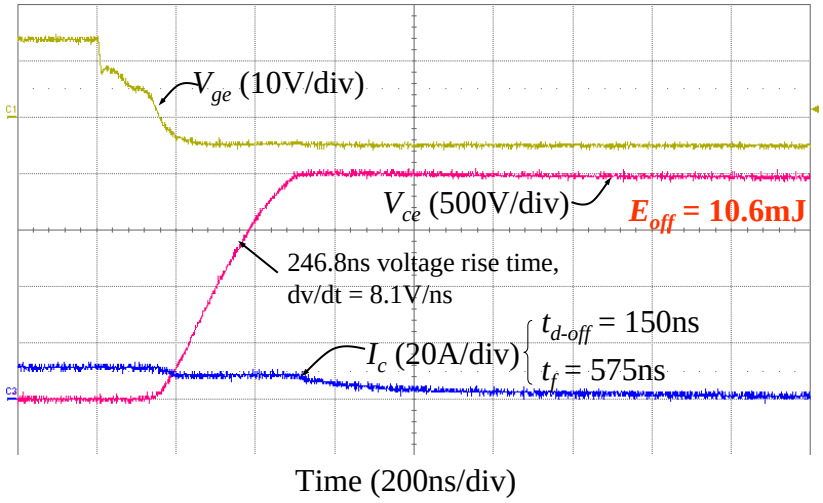


Figure 8-5. Detailed HV-IGBT turn-off device voltage and current waveforms under 2000-V, 11A condition.

Figure 8-6 shows detailed HV-IGBT turn-on device voltage and current waveforms under 2000-V, 20-A condition. The turn-on energy E_{on} is 17.3 mJ, which is significantly larger than the E_{on} measured with SGTO and SiC diode combination (3 mJ) under 23-A condition, but the ratio is significantly lowered because the Cdv/dt current does not reach negative in the SGTO case.

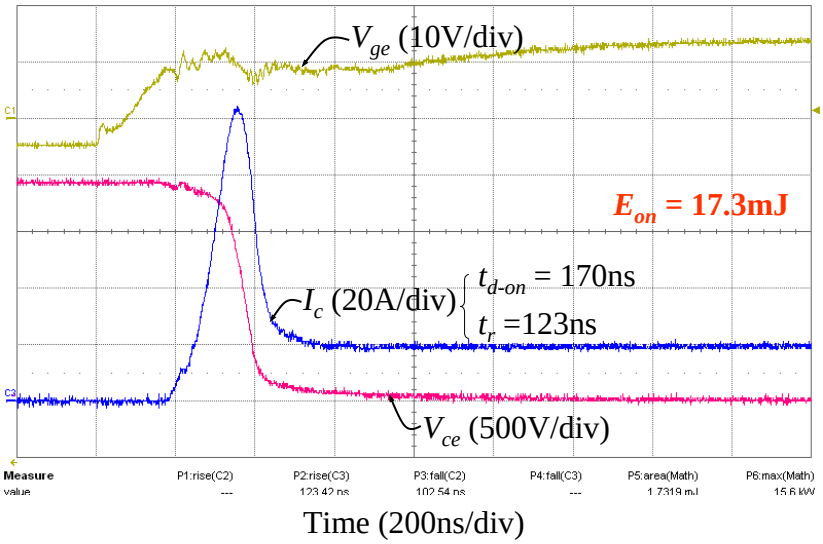


Figure 8-6. Detailed HV-IGBT turn-on device voltage and current waveforms under 2000-V, 20-A condition.

Figure 8-7 shows detailed HV-IGBT turn-off device voltage and current waveforms under 2000-V, 20-A condition. The turn-off energy E_{off} is 15.0 mJ, which is also higher than the E_{off} measured with SGTO (9 mJ) under 27-A condition. The main reason again can be attributed to the first turn-off current fall. This difference can be attributed to a much faster turn-off with SGTO and a tail current that increases turn-off loss significantly. Note that the turn-off dv/dt with HV-IGBT is 13.4 V/ns, but with SGTO is 15 V/ns under this current condition.

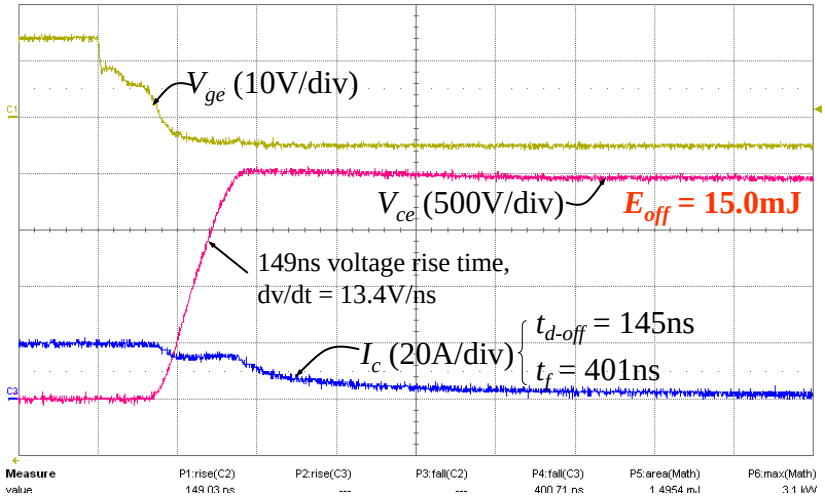


Figure 8-7. Detailed HV-IGBT turn-off device voltage and current waveforms under 2000-V, 20-A condition.

Figure 8-8 shows detailed HV-IGBT turn-on device voltage and current waveforms under 2000-V, 29-A condition. The turn-on energy E_{on} is 26.4 mJ. With the reverse recovery of silicon diode, the HV-IGBT turn-on loss is non-trivial, and the turn-on current spike is unacceptably high.

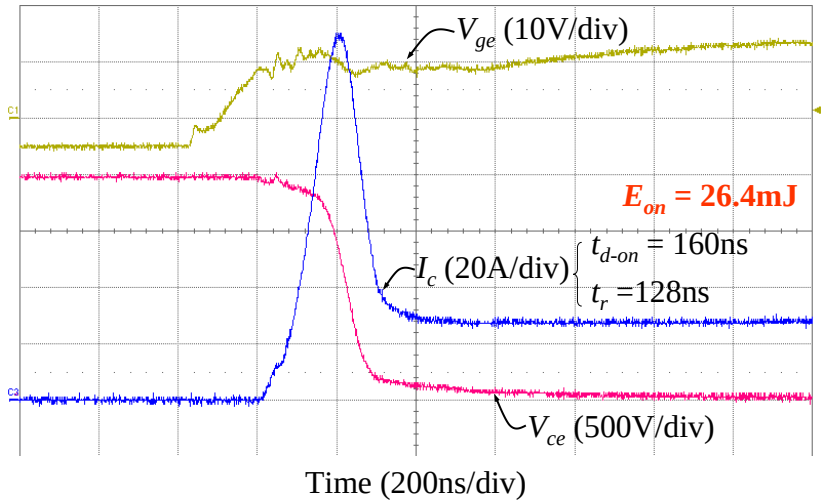


Figure 8-8. Detailed HV-IGBT turn-on device voltage and current waveforms under 2000-V, 29A condition.

Figure 8-9 shows detailed HV-IGBT turn-off device voltage and current waveforms under 2000-V, 29-A condition. The turn-off energy E_{off} is 22.0 mJ. The turn-off dv/dt with is 18.9 V/ns in this case.

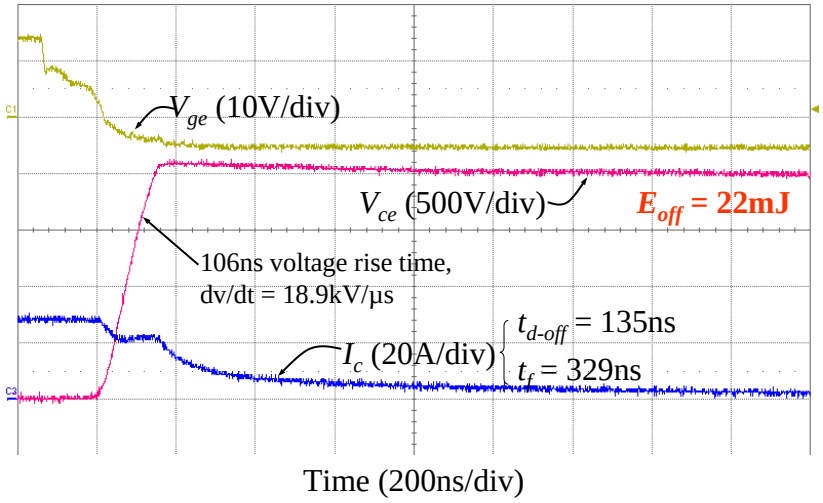


Figure 8-9. Detailed HV-IGBT turn-off device voltage and current waveforms under 2000-V, 29A condition.

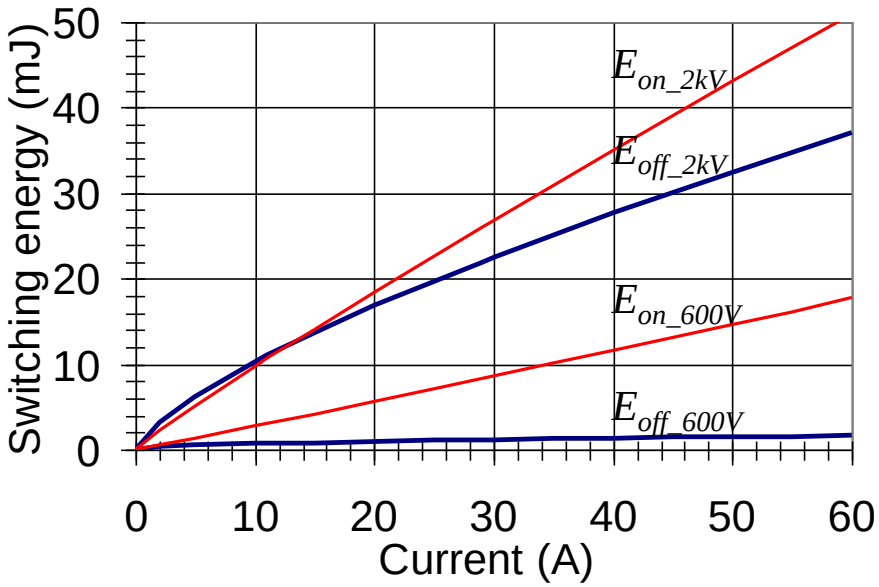


Figure 8-10. HV-IGBT switching energy as a function of device current under 2000-V and 600-V conditions.

9 CONCLUSIONS

In this project, the prototype super gate-turn-off thyristor (SGTO) has been tested fully under continuously conducting and double-pulse hard-switching conditions for conduction and switching characteristics evaluation. Due to unavailability of the matched high-voltage ultrafast reverse recovery diode, the SGTO chip is anti-paralleled with series stacked commercially available 1.2-kV silicon diodes. These diodes are in To-247 package and are series connected through their external pins, which tend to create a large leakage inductance loop.

The conduction voltage drop measurement results indicate that SGTO has excellent conduction characteristics despite inconsistency among some prototype devices. Tests were conducted with two conditions: (1) fixed gate voltage and varying anode current condition, and (2) fixed anode current and varying gate voltage condition. The conduction voltage drop is relatively a constant under different gate voltage condition. In terms of voltage drop as a function of the load current, there is a fixed voltage drop about 0.5V under zero current condition, and then the voltage drop is linearly increased with the current. For a 5-kV voltage blocking device that may operate under 2.5-kV condition, the projected voltage drop is less than 2.5 V under 50-A condition, or 0.1%. If the device is adopted in a converter operating under soft-switching condition, then the converter can achieve an ultrahigh efficiency, typically above 99%.

The two-pulse switching test results indicate that SGTO switching speed is very fast. The switching loss is relatively low as compared to that of the insulated-gate-bipolar-transistors (IGBTs). A special phenomenon needs to be noted is such a fast switching speed for the high-voltage switching tends to create an unexpected $C \cdot dv/dt$ current, which reduces the turn-on loss because the dv/dt is negative and increases the turn-off loss because the dv/dt is positive. As a result, the turn-on loss at low current is quite low, and the turn-off loss at low current is relatively high. The phenomenon was verified with junction capacitance measurement along with the dv/dt calculation. Under 2-kV test condition, the turn-on and turn-off losses at 25-A is about 3 and 9 mJ, respectively. As compared to a 4.5-kV, 60-A rated IGBT, which has turn-on and turn-off losses about 25 and 20 mJ under similar test condition, the SGTO shows significant switching loss reduction. The switching loss depends on the switching frequency, but under hard-switching condition, the SGTO is favored to the IGBT device.

One major concern is during low current turn-on condition, there is a voltage bump that can translate to significant power loss and associated heat. The reason for such a current bump is not known from this study. It is necessary that the device manufacturer perform though test and provide the answer so the user can properly apply SGTO in pulse-width-modulated (PWM) converter and inverter applications,

The second major concern is the matched diode. Without matched ultrafast or Schottky diode, the module was packaged with discrete low-voltage ultrafast reverse recovery diodes, which create significant leakage loop inductance and potential voltage share imbalance between individual diodes. It is necessary that a matched ultrafast high-voltage diode can be packaged in the same module to cut down parasitic loop inductance, to reduce diode voltage drop, and to avoid voltage share imbalance among individual diodes.

Future work is to compare the test results with those obtained either from manufacturer or another third party. Once the module parasitic and diode issues are resolved, using the STGO to build an active-front-end converter and soft-switched DC-DC for IUT can be considered.