

NUCLEAR PHYSICS IN A PEGASUS PAYLOAD Experiment on the International Space Station

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ISS and Shuttle imagery Courtesy of NASA

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Outline

- MISSE Overview
 - Background
 - Objectives
 - Environment
- SEUXSE (pronounced *Suzy*) on MISSE
 - Architecture
 - Electrical Interface
 - Mechanical and Thermal
 - Experiment Details
 - Status
 - CONOPS and Data Flow
- Launch and Deployment of MISSE 7



MISSE Overview

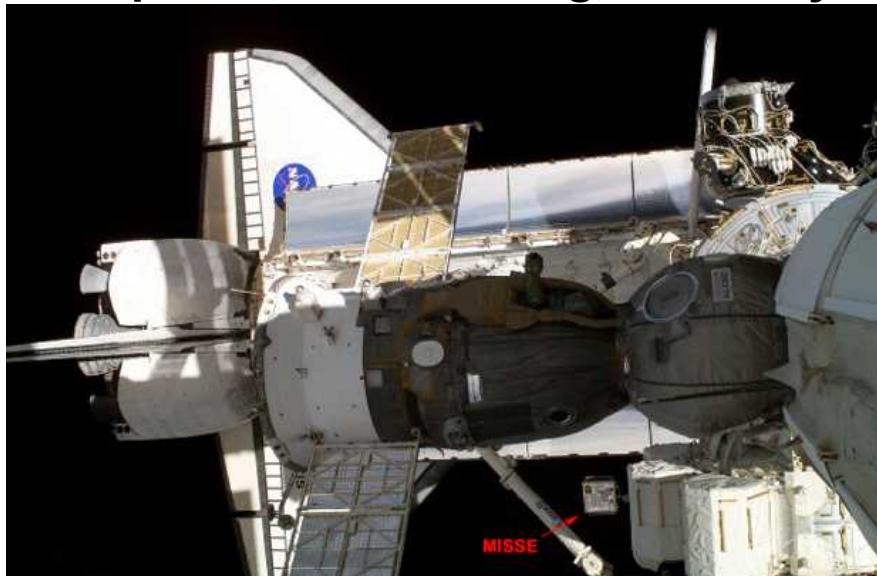
- The purpose of the Materials International Space Station Experiment (MISSE) is to characterize the performance of new and prospective spacecraft materials and technologies when subjected to the combined effects of the space environment.
- The MISSE program has a rich history and benefits from six previous on-orbit payloads with substantial legacy hardware and design.
- MISSE 7 (launched Nov. 2009) is the first science payload for the Express Logistics Carrier (ELC) program and carries passive and actively powered experiments.
- One of two MISSE 7 Passive Experiment Containers (PECs) will be replaced by a MISSE 8 PEC (launch July 2010).





MISSE Background

- Experiments up to 2 years on the ISS
- Launched and returned by Shuttle.
- Initially passive experiments only – combined UV, AO, radiation.
- Active experiments connect to ISS for power, commanding, telemetry.



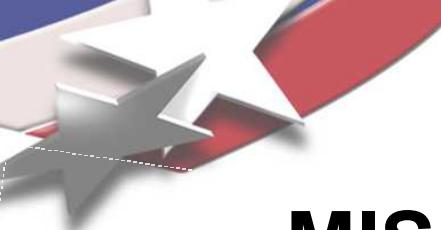
- MISSE 1 & 2 (AFRL/ML)
 - Passive material exposures
 - Launched 2001, returned 2005
- MISSE 3 & 4 (AFRL/ML)
 - Passive material exposures
 - Launched 2006, returned 2007
- MISSE 5 (NRL)
 - Self-powered with on-board, two-way comm
 - Active solar cell and passive material experiments
 - Launched Aug 2005, returned Sept 2006
- MISSE 6 (AFOSR)
 - Passive and active expts –data loggers
 - Launched March 2008, returned Sept 2009
- MISSE 7 (NRL)
 - Passive and Active experiments (NRL-0602)
 - Launched Nov 2009
- MISSE 8 (NRL)
 - Passive and Active experiments (NRL-0602)
 - Launch scheduled for July 2010



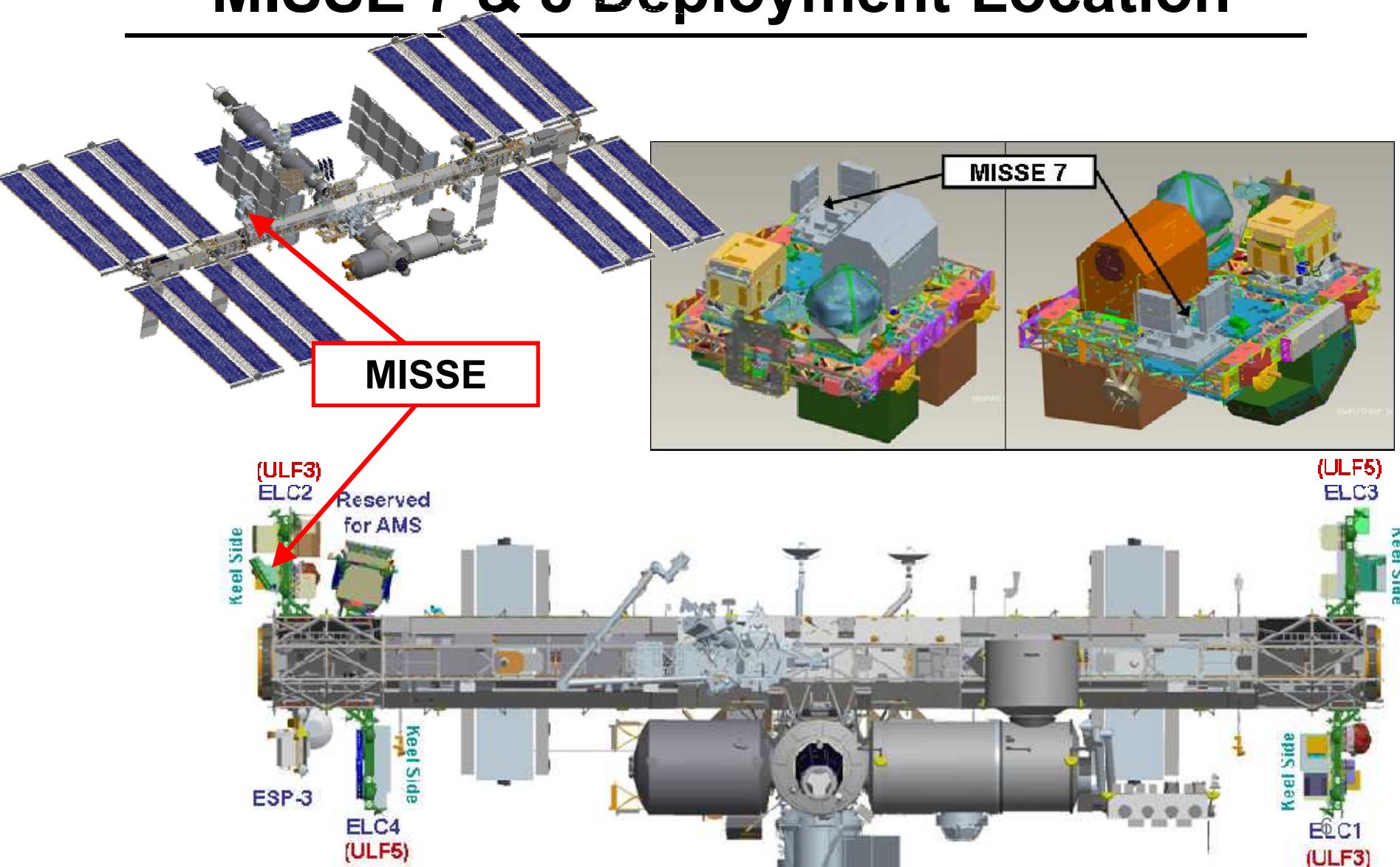
Sandia Contributions to MISSE

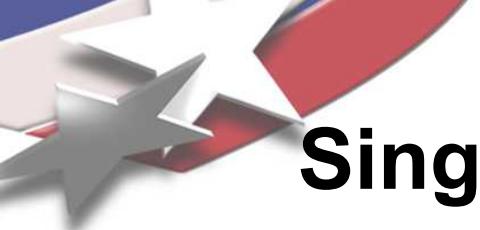
- MISSE 6
 - Piezoelectric polymer materials experiment
- MISSE 7
 - Single Events Upset Xilinx-Sandia Experiment (SEUXSE I)
 - Sandia Passive ISS Research Experiments (SPIRE)
- MISSE 8
 - Single Events Upset Xilinx-Sandia Experiment (SEUXSE II)

SEUXSE I & II are architecturally similar with differences highlighted in blue/red colors.



MISSE 7 & 8 Deployment Location



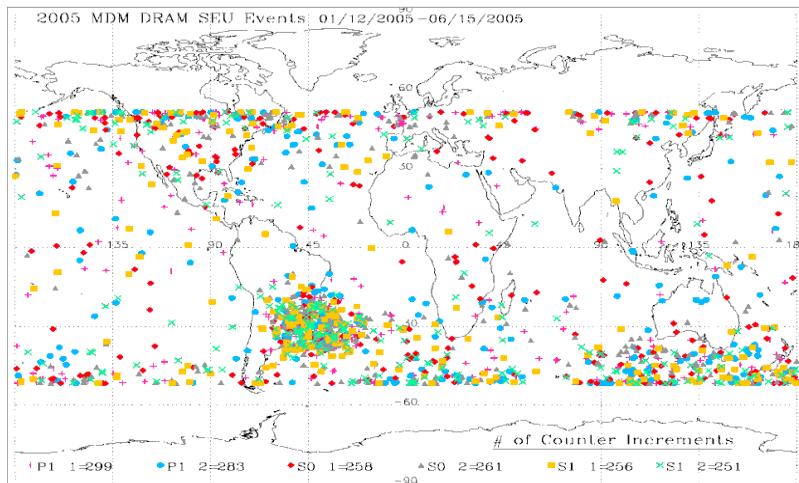


Single Event Upset Xilinx Sandia Experiment (SEUXSE) Objectives

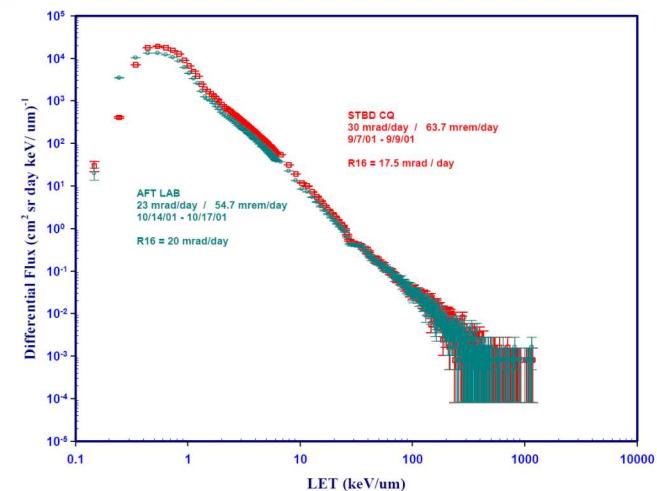
- **Single Event Upset (SEU) Detection and Characterization Using High Density Xilinx Field Programmable Gate Arrays (FPGA)**
- **Record Time and Bit Value of Each SEU Detected**
 - Continuous scrubbing of Xilinx configuration bits
 - Continuous exercising and monitoring of most functional logic elements within each Xilinx Virtex FPGA
- **Early design, delivery and deployment of technologies relevant to the DOE/NNSA's Joint Architecture Standard (JAS)**
 - Xilinx Virtex-4 and Virtex-5 FPGAs
 - Point-of-Load (POL) power converters
 - Intellectual Property (IP)
 - Demonstrate in LEO space environment
- **Develop Relationships with NRL, NASA, Xilinx, BYU and Many Other Academic and Industry Partners**

ISS Radiation Environment I

- ISS environment is suitable for a Single Event Effects experiment
 - High inclination (51.5°) exposes ISS to higher fluence of trapped electrons and protons and solar and galactic cosmic rays than would be the case in a lower inclination orbit with the same altitude range, largely as a result of the overall shape and magnitude of the geomagnetic field.
 - ISS passes through the South Atlantic Anomaly (SAA).



Aggregate MDM DRAM SEU Map
(155 days)



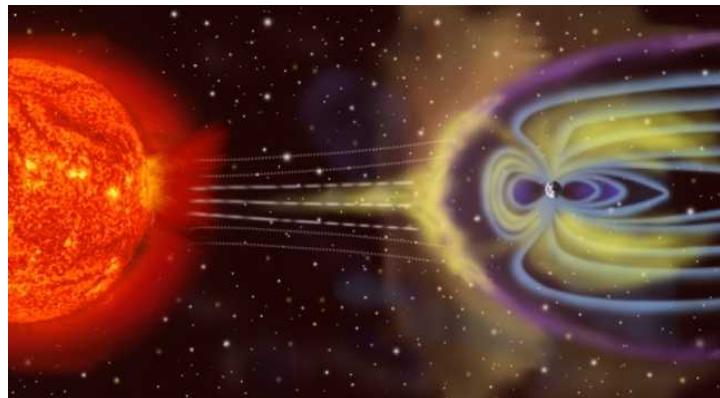
ISS Extra-Vehicular Charged Particle Spectrometer (EV-CPDS)
Real-time LET measurements

Detected SEUs will be correlated to ISS radiation and environmental monitored data.



ISS Radiation Environment II

- **ISS Orbit:** 336 km x 347 km, 51.6 deg. inclination
- **Passive experiments TID (no shielding):** ~30 krad/yr total dose at the surface.
- **FPGA experiment TID (100 mil Al shield):** ~30 rad/yr total dose.
- **Predicted error rates:**
 - Galactic cosmic rays to cause ~2 FPGA config bit errors/day and ~0.3 BRAM bit errors/day.
 - From LANL Cibola Flight Expt. SEU data (Virtex 1 FPGA's, similar orbit) ~4 errors/day.
 - About ½ of errors will be multiple bit upsets.
 - South Atlantic Anomaly will cause about 0.2 errors/day.
 - We predict about 7 flares/year with 4 errors/day and 1 flare/year with 20 errors/day.
 - ***Total errors/year expected to be about 1000.***





SEUXSE Design

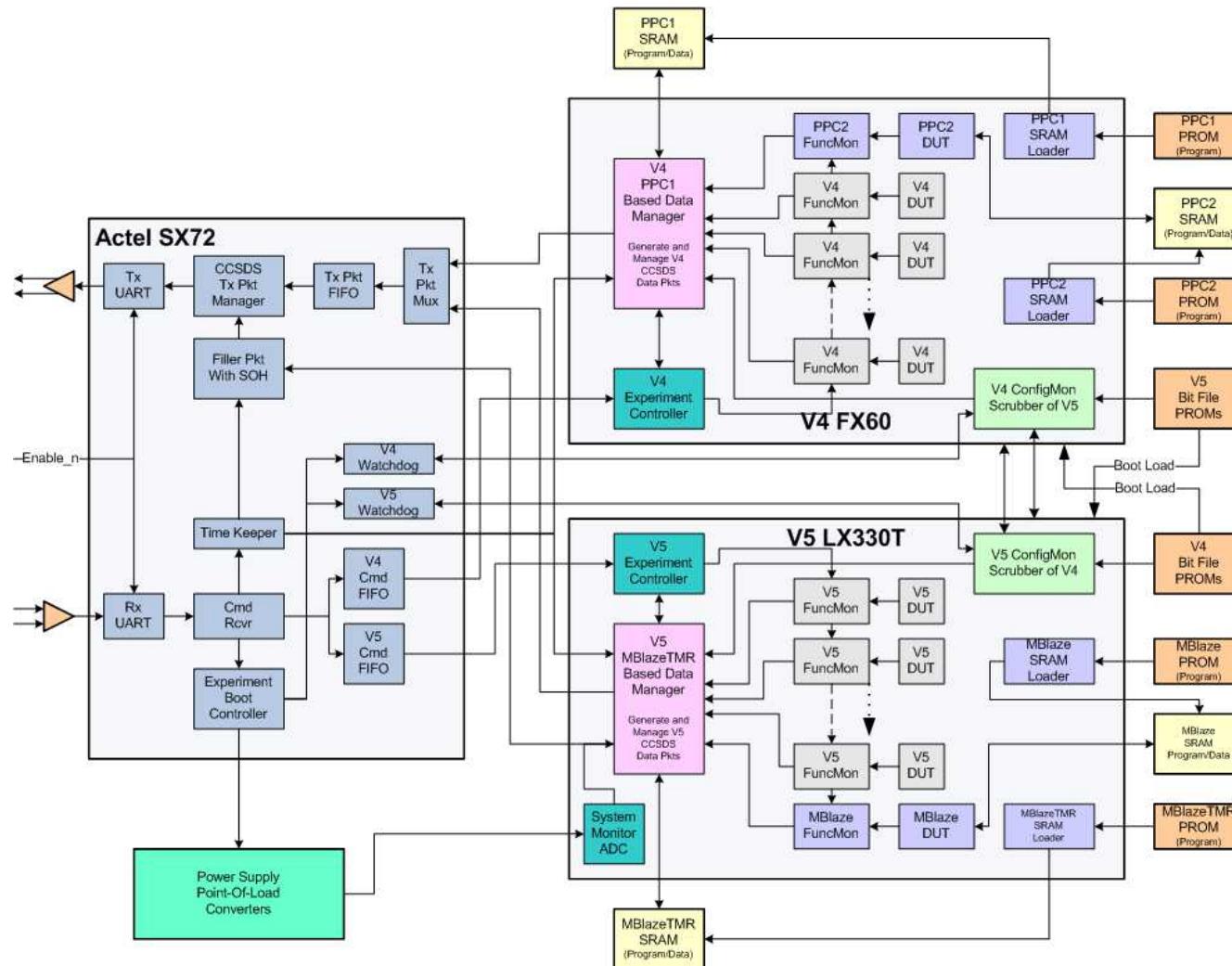
- **Xilinx Virtex 4 XQR4VFX60 FF1152 pin BGA**
 - 50,560 Flip-Flops, 21 Mbit configuration memory
- **Xilinx Virtex 5**
 - **SEUXSE I:** Commercial LX330T FF1738 pin BGA
 - 207,360 Flip-Flops, 83 Mbit configuration memory
 - **SEUXSE II:** SIRF FX1 CF1752 pin BGA
 - 81,920 Flip-Flops, 50 Mbit configuration memory
- **Four Embedded Processors Active**
 - 2 silicon based PowerPCs, 2 soft core FPGA fabric based processors
 - 512K bytes of SRAM for each processor with EDAC
- **OTP PROMs (XQR17V16) store FPGA configuration and Processor software**
- **Radiation Hardened Point-Of-Load (RHPOL) Power Converters**
 - Sandia custom ASIC
 - First flight use of these devices
 - Two triple output controllers provide six rails
 - (3.3, 2.5, 1.2 (2), 1.0 (2))



Design Details

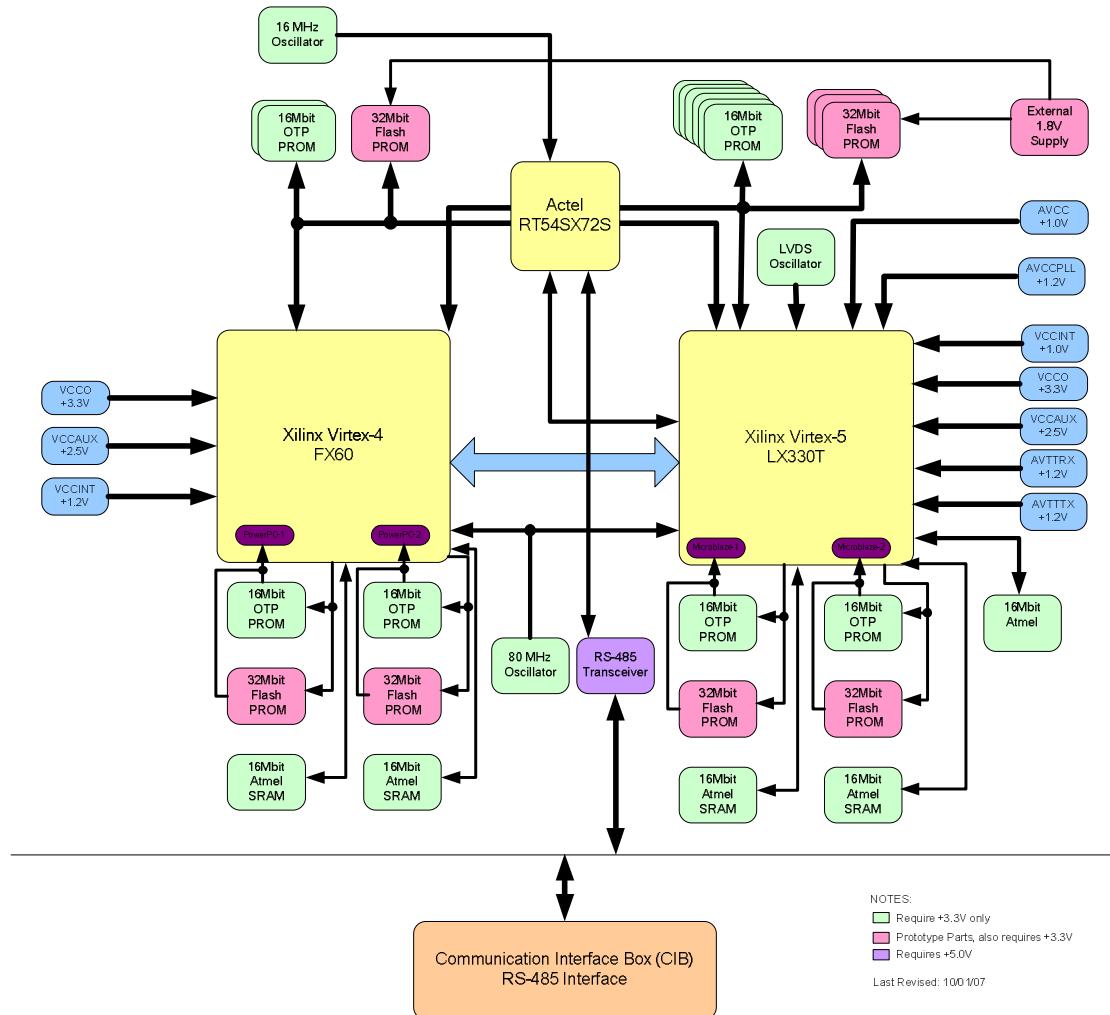
- **Configuration PROMs:** Boot each device, then are accessed by the other Virtex to provide cross scrubbing of each Xilinx FPGA.
- **V4 embedded PPCs:** One provides software control, self monitor for upsets, and data handling functions; The other runs self monitoring upset codes.
- **V5 MicroBlazes:** One provides software control, self monitor for upsets, and data handling functions; The other soft-core (MicroBlaze/LEON) runs self monitoring upset codes.
- **To detect and report SEU events:** Each Virtex contains several hardware logic element Device-Under-Test (DUT) units with associated Functional Monitors (FuncMon).
- **DUT and Functional Monitor logic elements include:** Block RAM, embedded FIFO logic, DCM, DSP48, etc.
- **Actel provides:** Non-volatile hardware interface to ISS command and data channels; Watchdog monitors of each Xilinx FPGA to recover from SEFI modes.
- **V5 System monitor:** used to monitor state of health and radiation monitor sensor

SEUXSE Internal Functional Block Diagram



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SEUXSE Printed Circuit Board Block Diagram



Unclassified Unlimited Release



SEUXSE Electrical Interface

- **Standard D shell 25 pin connector**
 - Power (11 wires for power, return, chassis and signal ground):
 - Designated converter provided for SEUXSE: +28V to +5V
 - Maximum power budget of 30W (5V @ 6A)
 - Command and Data (6 wires):
 - SEUXSE interfaces with the Communications Interface Box (CIB)
 - Command and Data links are differential RS485 at 9600 baud
 - Bandwidth requirements:
 - Science and State-Of-Health (SOH) Data: 400K bytes per day, average
 - Early orbit testing: 2M bytes per day (maximum)
 - Minimum bandwidth is estimated at 51K bytes per day
 - Most days, there will be no serial commands required
 - Maximum of 2-10 serial configuration commands per month
 - All Data products are CCSDS formatted packets
 - Internal variable length CCSDS data packets embedded in CIB packet
 - Unused/spares (8 wires)
- **Integration and test connector**
 - For internal use only
 - Has an Aluminum cover plate in the flight configuration



SEUXSE Mechanical and Thermal

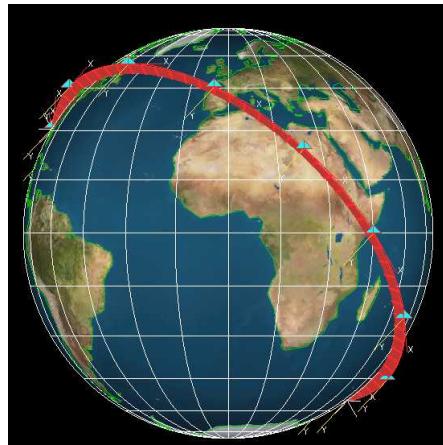
- **Volume is 7 Inches Wide By 14 Inches Long By 1.8 Inches High**
 - Single 18 layer Printed Circuit Board contains all electronics
 - Enclosure mounted with screws through bottom of PEC deck plate
- **Aluminum Enclosure**
 - Alodine surface coating
 - Silver Teflon tape on alodine surfaces
- **SEUXSE I has a Carbon-Fiber Composite Lid (Top Face)**
 - 80-mil thick composite top lid mounted in an aluminum frame
 - Low outgassing epoxy with ~ 8 layers of pre-preg
 - Nickel plating for EMI shielding
 - AZ-400 white paint for passive thermal control
- **SEUXSE II has an Aluminum Lid (better thermal control)**
- **Mass is 5 Pounds**
- **Enclosure has Rounded Edges and Corners for Astronaut Safety**
- **Kick Load analysis was required**
- **Thermal Requirements**
 - Operating Range is 0 to +60C at the baseplate mounting surface (0 to +95C for internal components)
 - Non-Operating Range is -40C to +125C



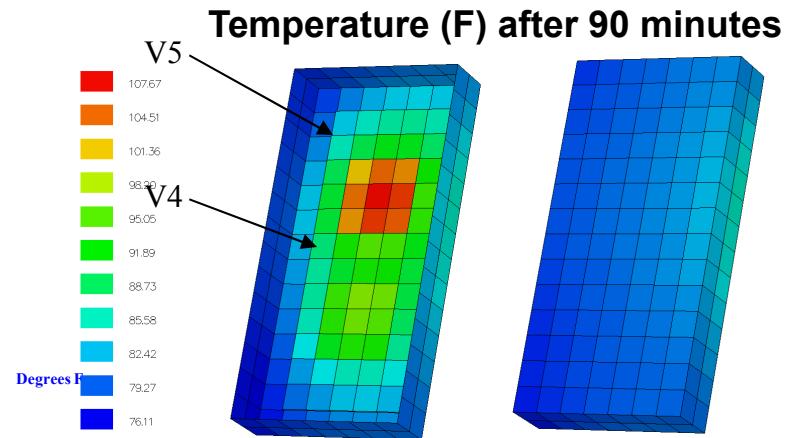
SEUXSE Thermal Model

Assumptions:

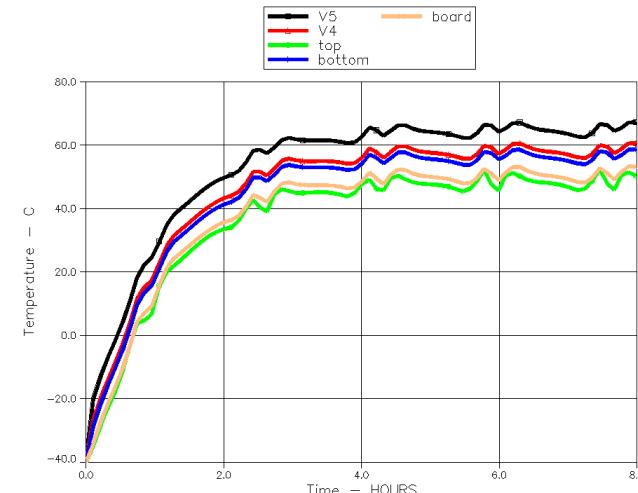
- Housing: 6061-T6, 0.1 inch thick
- Board, nominal, 0.08 inch thick
- V5 – 19 Watts, V4-10 Watts
- Orbit, 90 minute period
- EOL, SSM outer surface
- Heat conducted from board to bottom surface



Orbit – Sun View at time=0



Temperature Profile over 8 hours, $T_0=-40$ C





SEUXSE I FPGA Experiments

Virtex 4 FX60

- V5 configuration scrubber
- BRAM scrubber
- Two PPCs
- Digital Signal Processors (DSP48)
- Digital Clock Managers (DCM)
 - Monitor clock for changes

Virtex 5 LX330T

- V4 configuration scrubber
- BRAM scrubber
- Two Microblazes
- Digital Signal Processors (DSP48E)
- Digital Clock Managers (DCM)
 - Monitor clock for changes



SEUXSE II FPGA Experiments

Virtex 4 FX60

- V5 configuration scrubber
- Two PPCs
- Partial Reconfiguration
 - Load different functional blocks into reconfigurable area while the rest of the device continues to operate
- Block RAM monitoring for SEU upsets
- Digital Clock Managers (DCM) and PLL
- Spacewire
 - Packets between the two FPGAs are monitored for errors
- Digital Signal Processing (DSP)
 - Various algorithms to monitor DSP blocks for upsets
 - Four additional experiments from BYU
- Commercial compression/decompression IP engine

Virtex 5 FX1 (SIRF)

- V4 configuration scrubber
- Two soft-core processors
 - MicroBlazes
 - LEON3 SPARC (Gaisler)
- Block RAM monitoring for SEU upsets
- Digital Clock Managers (DCM) and PLL
- Spacewire
 - Packets between the two FPGAs are monitored for errors
- Digital Signal Processing (DSP)
 - Various algorithms to monitor DSP blocks for upsets
- Four additional experiments from Mike Wirthlin's group (BYU)
- Commercial compression/decompression IP engine



SEUXSE FPGA Utilization

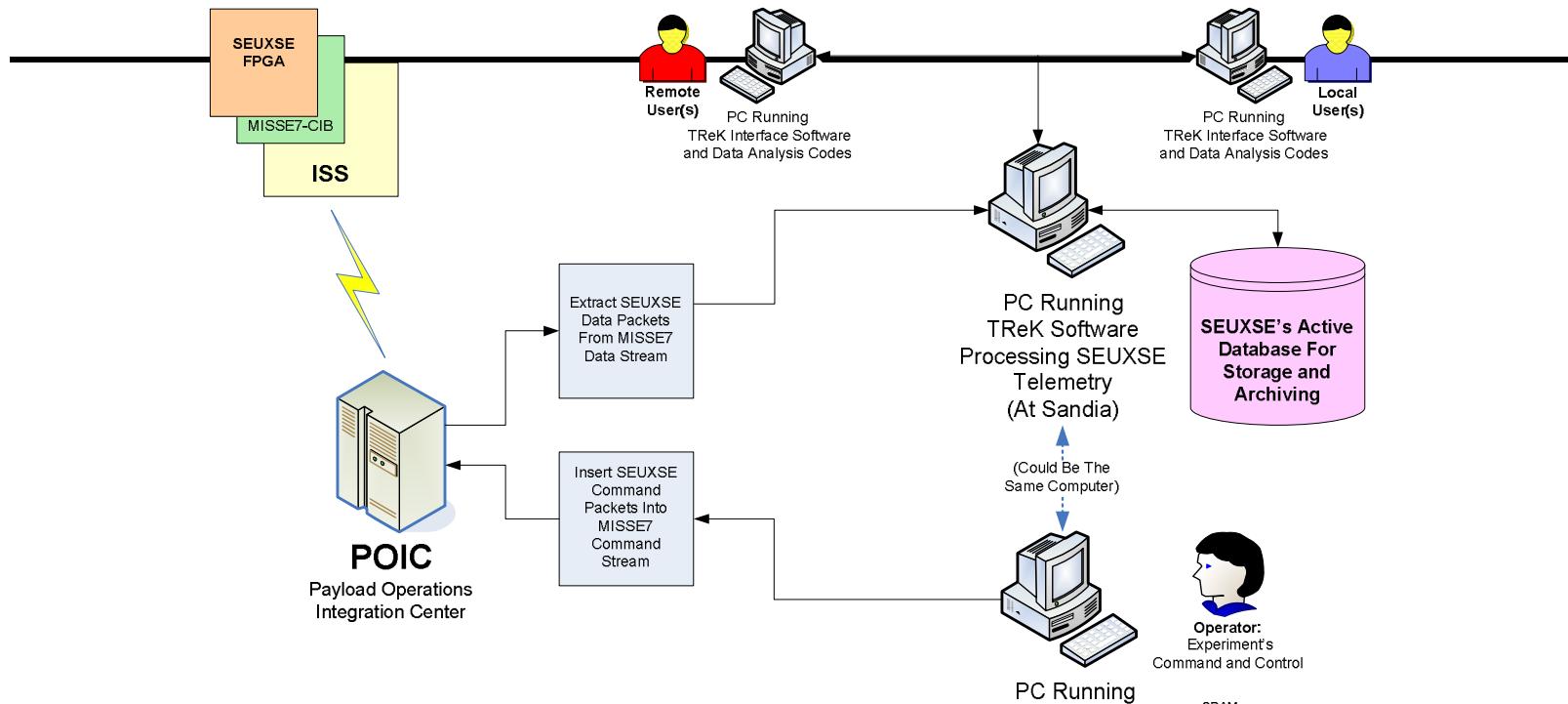
SEUXSE I

- 9 Watts (1.8A @ 5V)
- V4 utilization
- V5 utilization
- Actel utilization

SEUXSE II

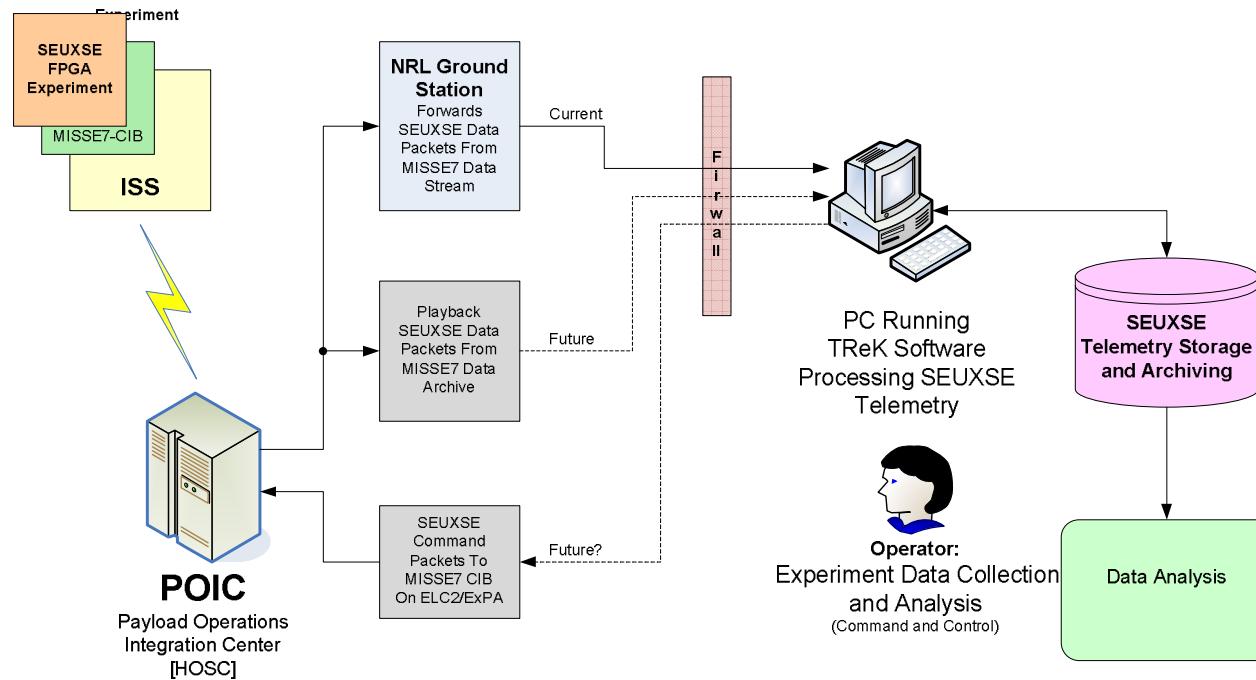
- Power
- V4 utilization
- V5 utilization
- Actel utilization

Concept Of Operations



- **Sandia Operator sends commands to SEUXSE**
- **Experiment's CCSDS data packets flow through TReK to Sandia**
 - All data stored and archived in TReK (Microsoft Access) database
- **Internal and External Users access TReK database to retrieve data for analysis**
- **Requires NASA - Sandia network connectivity and security approvals**

SEUXSE Operations and Data Flow



- **Experiment's CCSDS data packets flow through TReK to Sandia**
 - All data stored and archived for data analysis
- **Now: NRL forwards data stream until Sandia completes setup to get data stream directly from NASA POIC/HOSC**
- **Future possibility: Sandia Operator sends commands to SEUXSE**
 - NASA and Sandia network connectivity and security setup required



SEUXSE Status

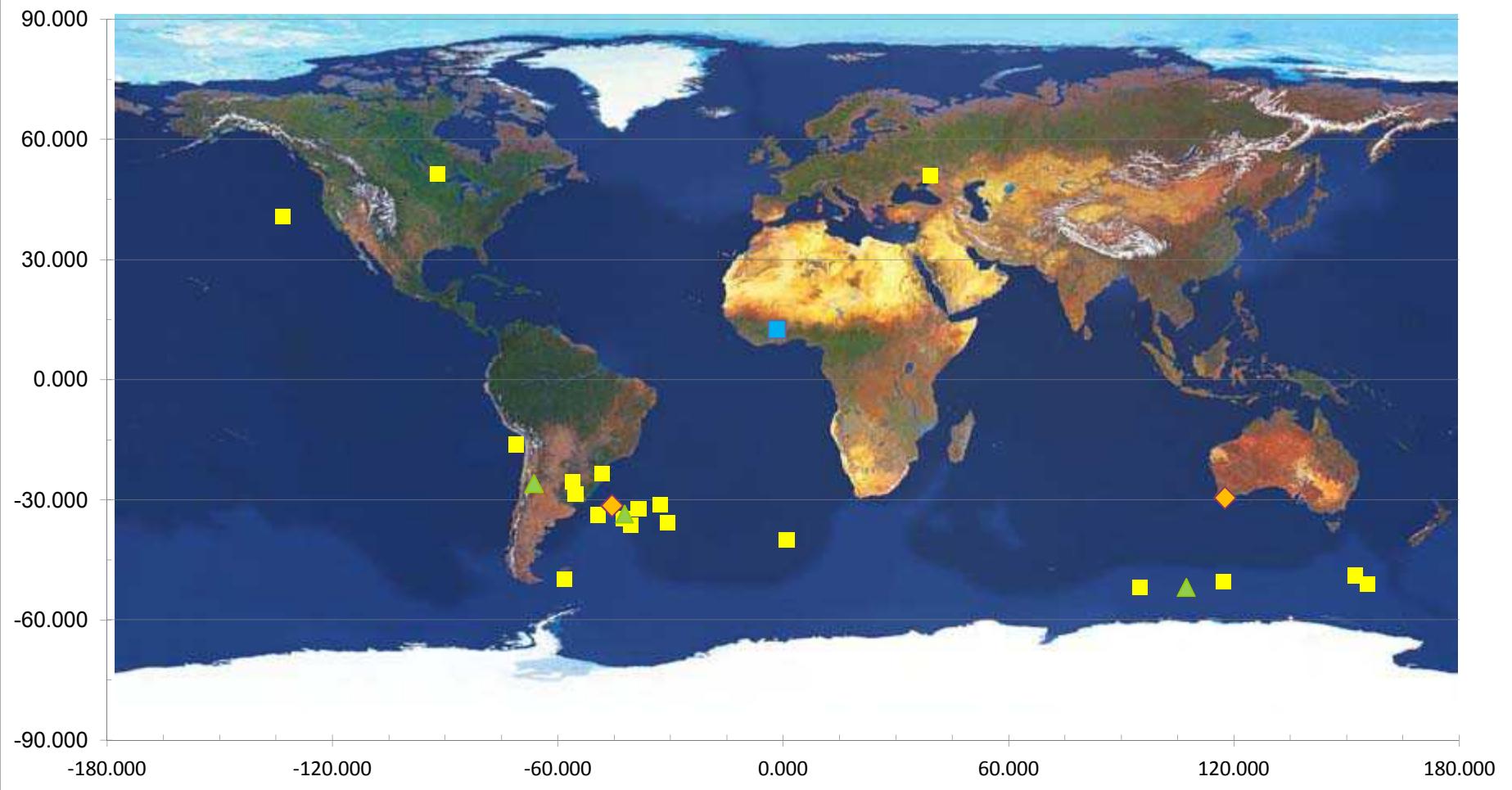
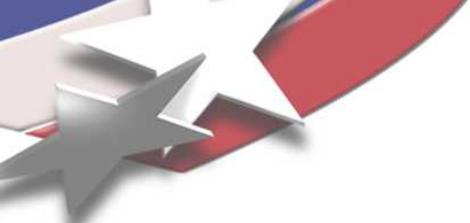
SEUXSE I

- Launched on STS-129 (11/16/09)
- ELC2 and MISSE 7-ExPA Deployed (11/21/09)
- MISSE7 PEC-A (SEUXSE) and PEC-B Deployed (11/23/09)
- SEUXSE has operated continuously for 39.8 days since deployment.
V4 has detected 3 BRAM errors.
V4 has seen 3 scrubber errors.
V5 has detected 5 BRAM errors.
V5 has seen 26 scrubber errors.

SEUXSE II

- Delivery to NRL on Feb 2, 2010
- I&T summary at NRL [here](#)
- To Launch July, 2010, when SEUXSE I is returned.

SEUs on MISSE 7's SEUXSE (Dec 09)

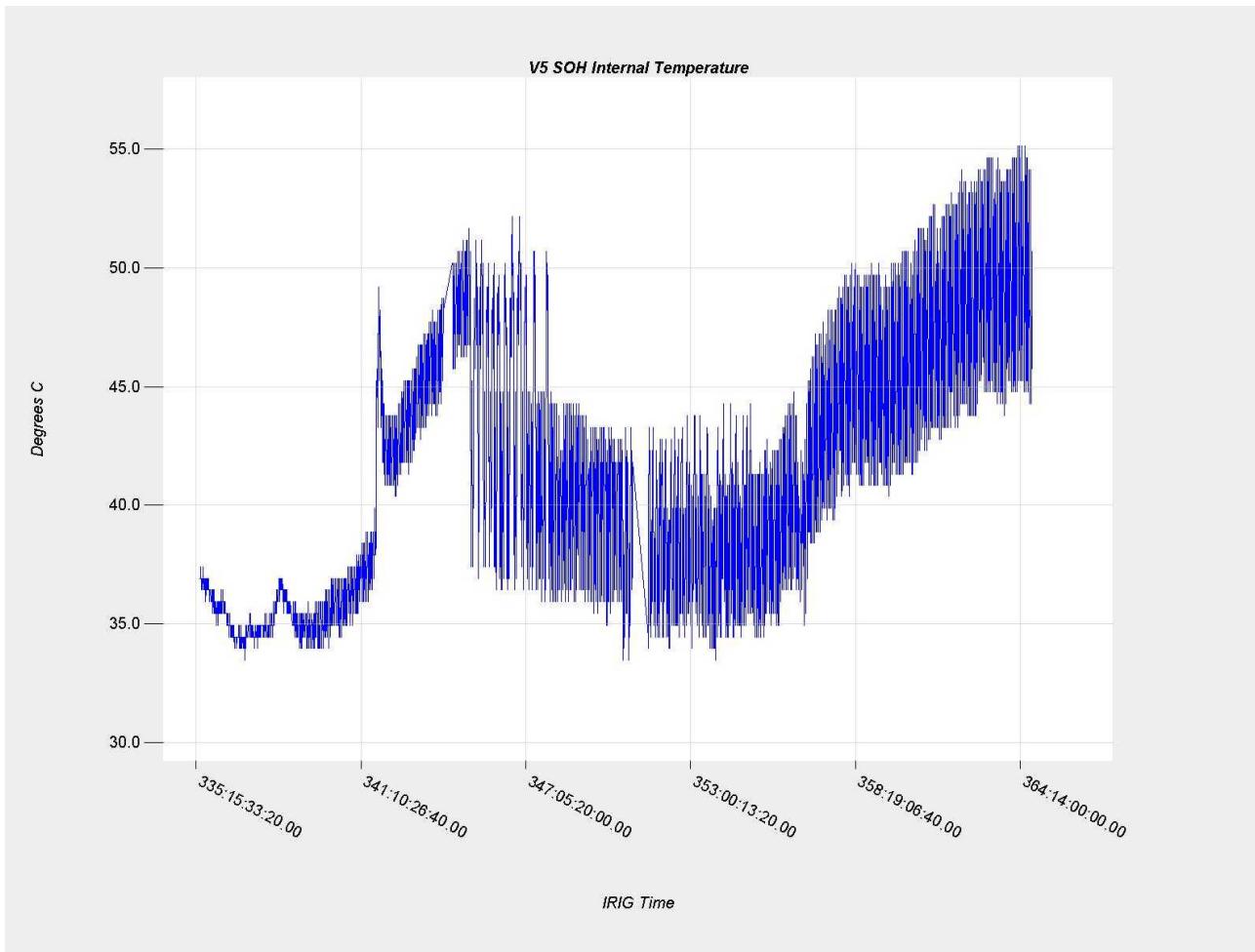


ISS location at SEU events.

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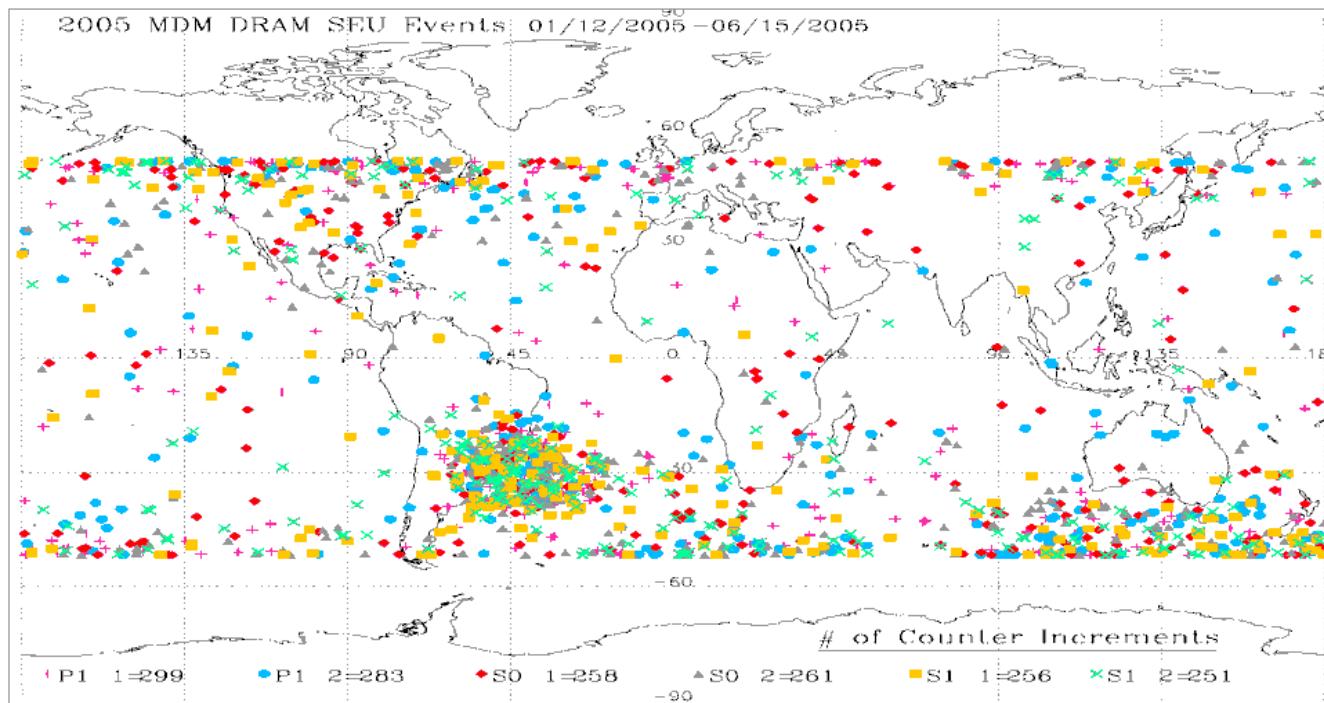


SEUXSE I V5 Internal Temperature



Unclassified Unlimited Release

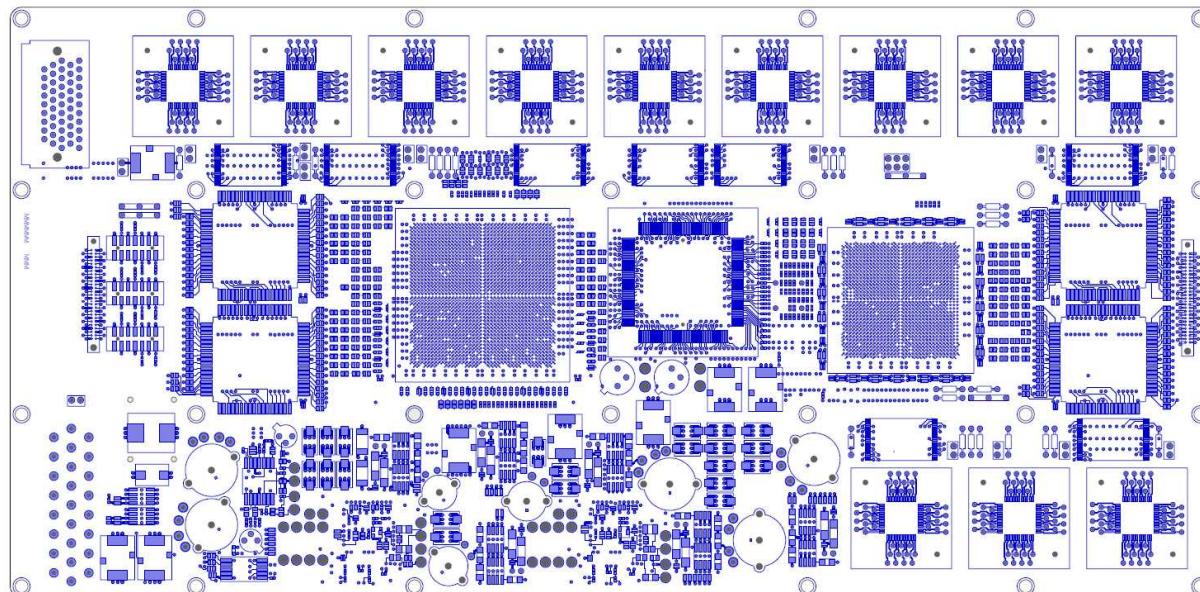
SEUXSE I On-Orbit SEU Data I



ISS location at SEU events.



SEUXSE Printed Circuit Board



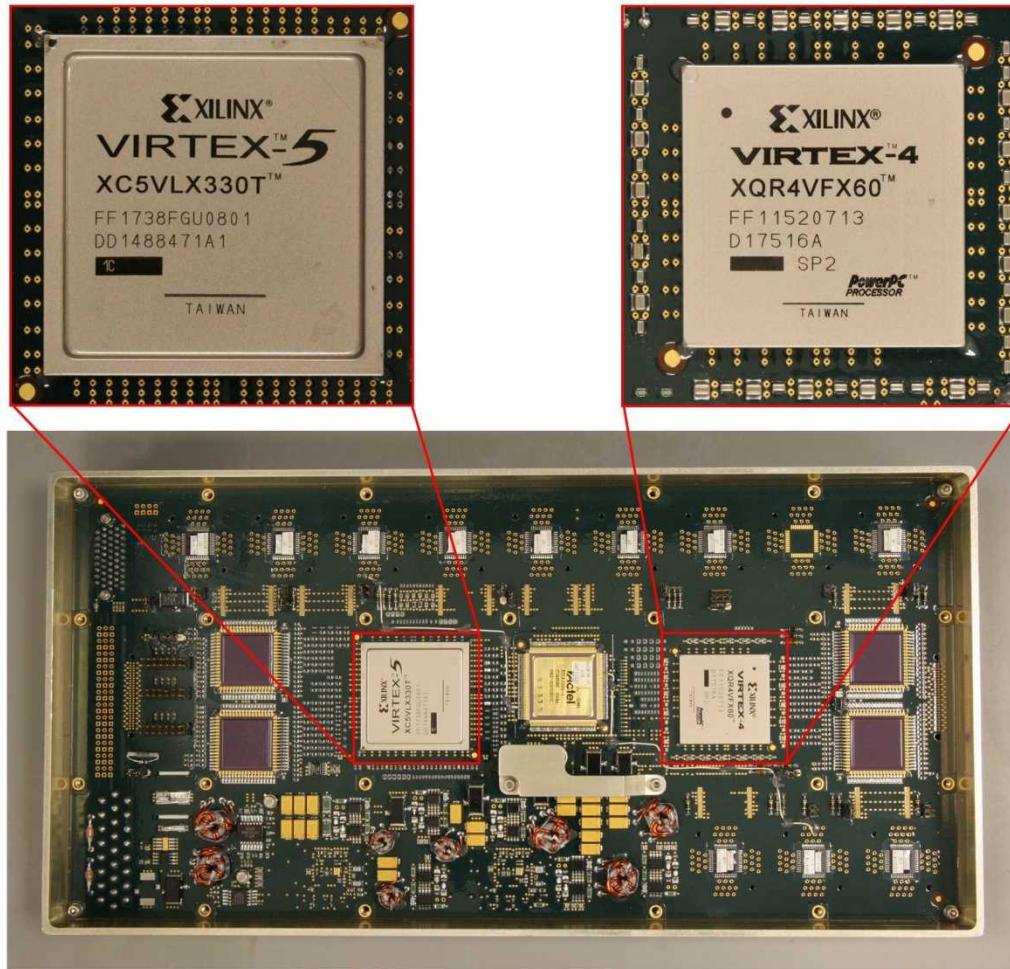
Top Side View

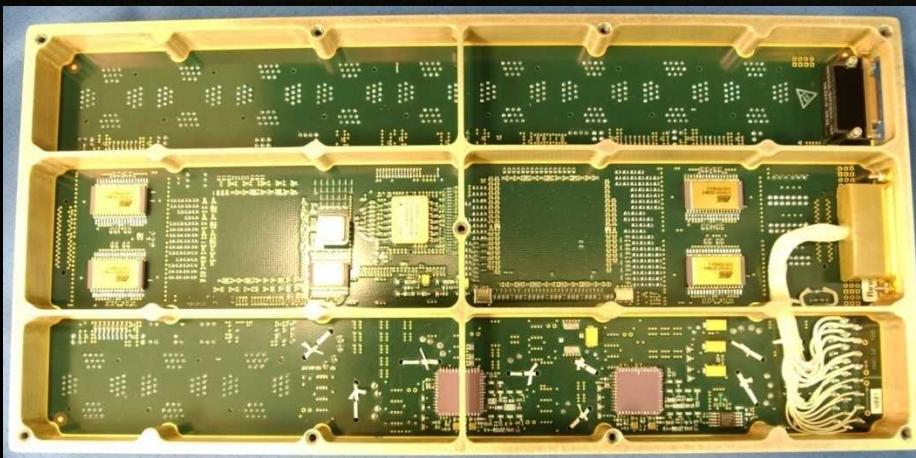
Bottom Side View





SEUXSE I Hardware



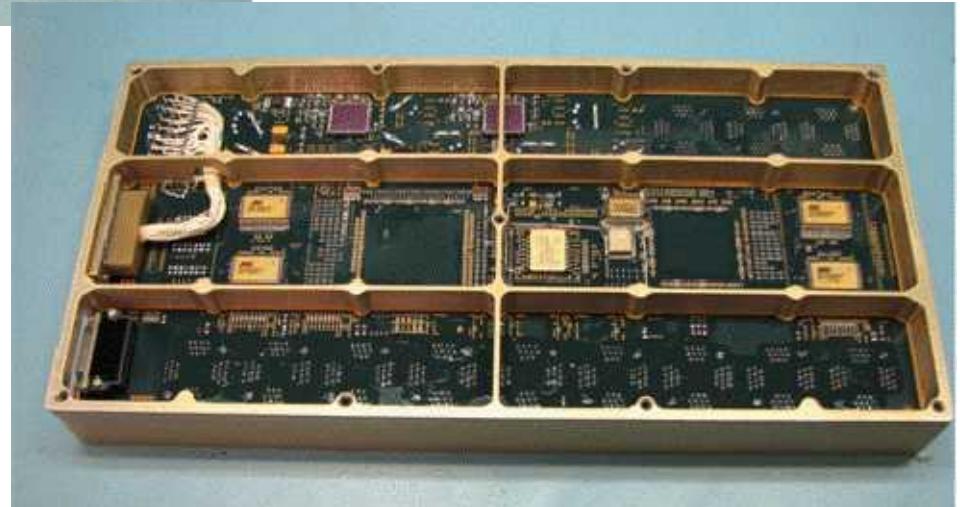




SEUXSE I Flight Unit



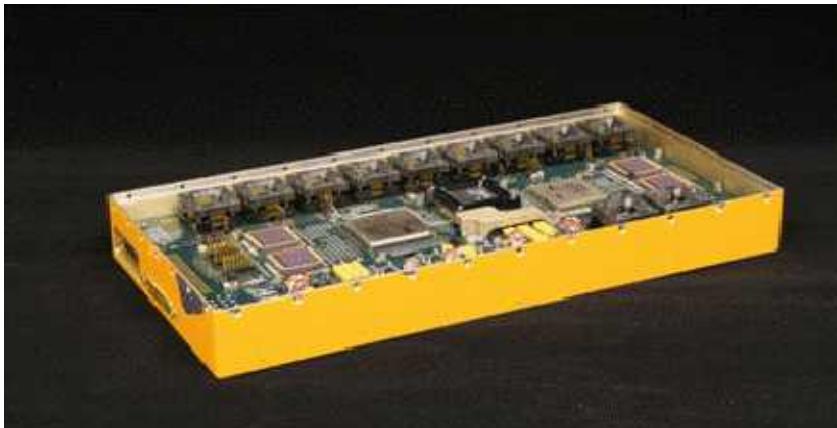
Top



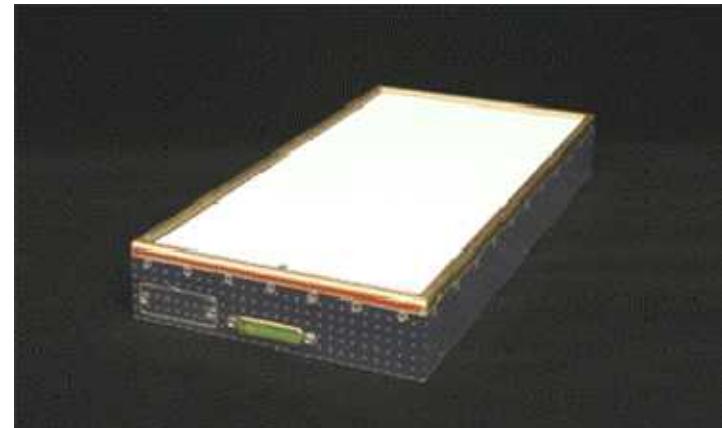
Bottom



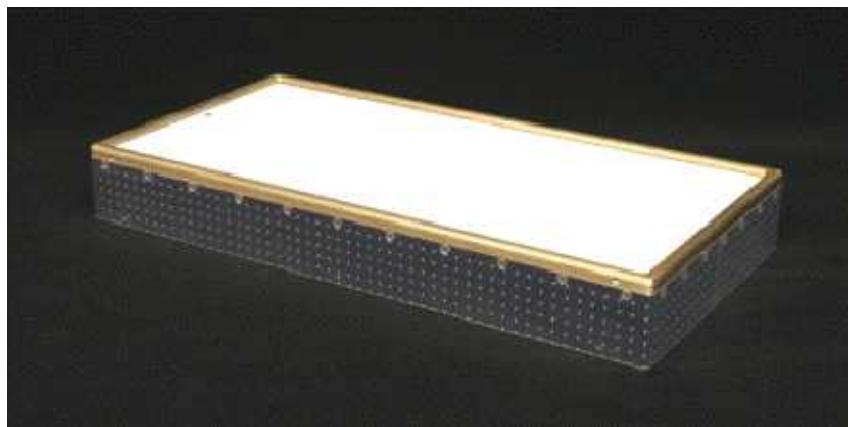
SEUXSE I Flight Unit



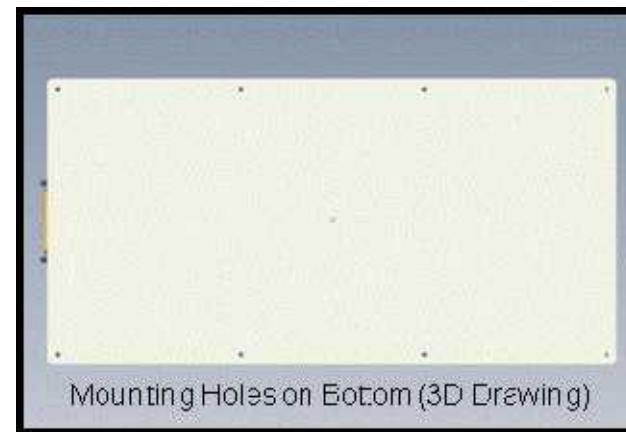
Cover Removed, w/Protective Tape



CIB Interface Connector View

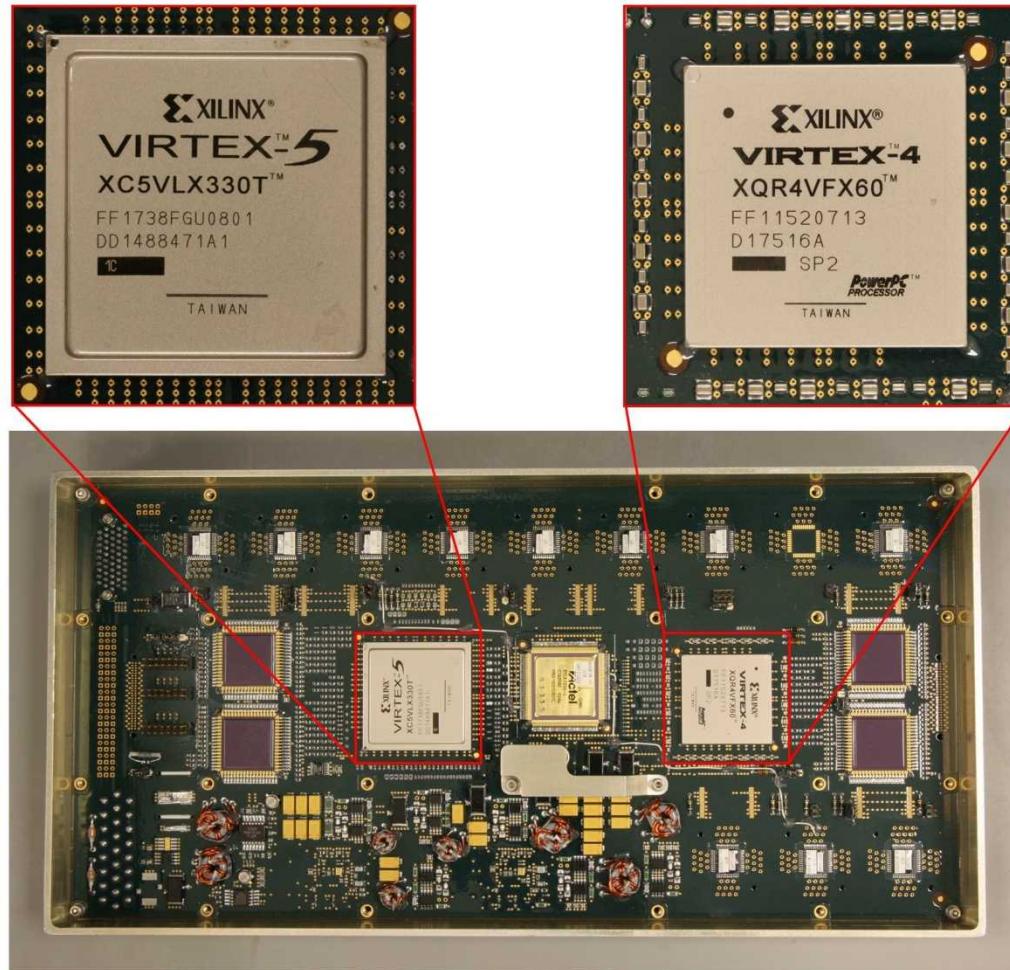


Backside View, with Composite Lid



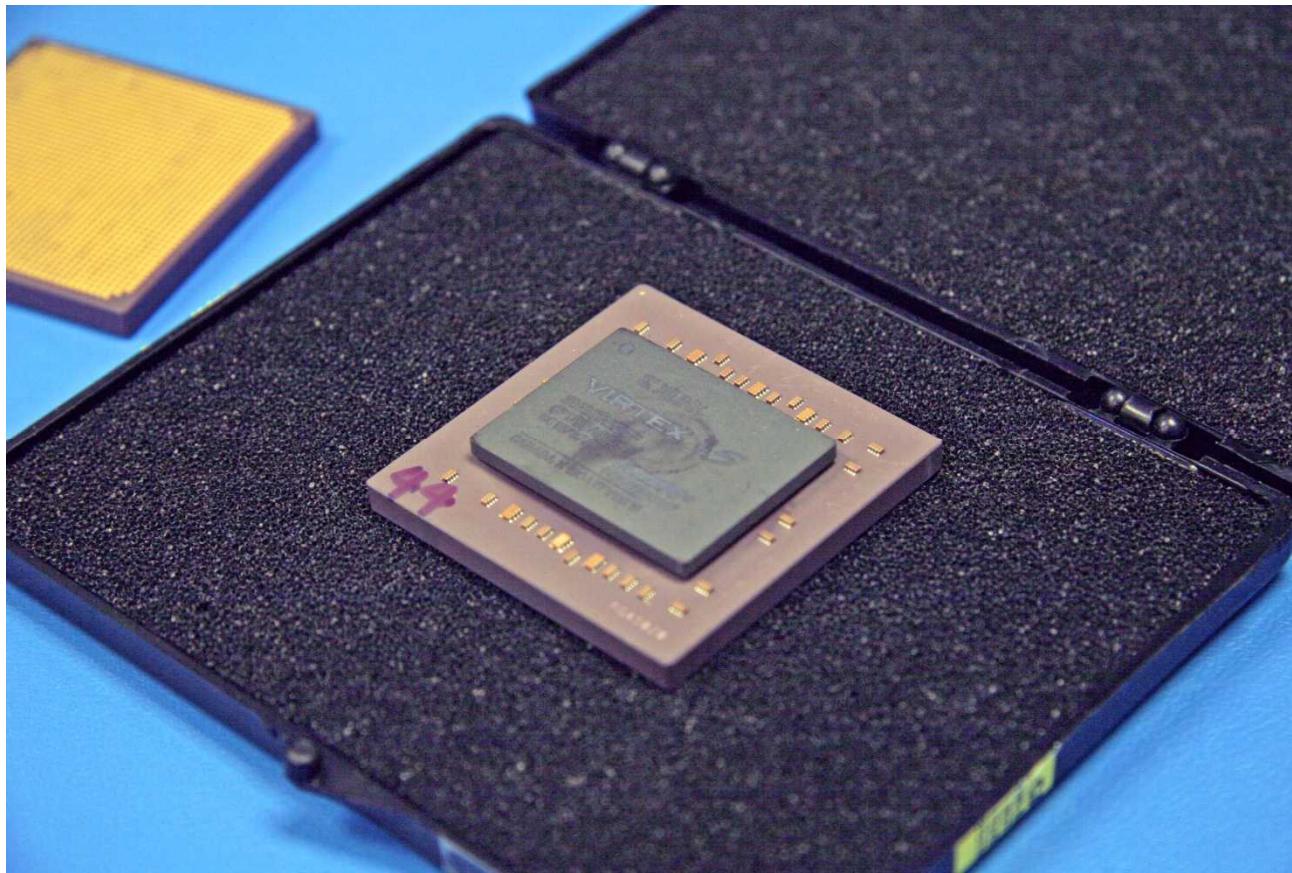


SEUXSE II Hardware I





Virtex 5 (SIRF) on **SEUXSE II**





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- Launch and Deployment of MISSE 7



- STS-129 Launched on November 16, 2009
- ELC2 and MISSE 7-ExPA Deployed Nov 21, 2009
- MISSE 7 PEC-A (SEUXSE) and PEC-B Deployed Nov 23, 2009

ISS and Shuttle imagery Courtesy of NASA

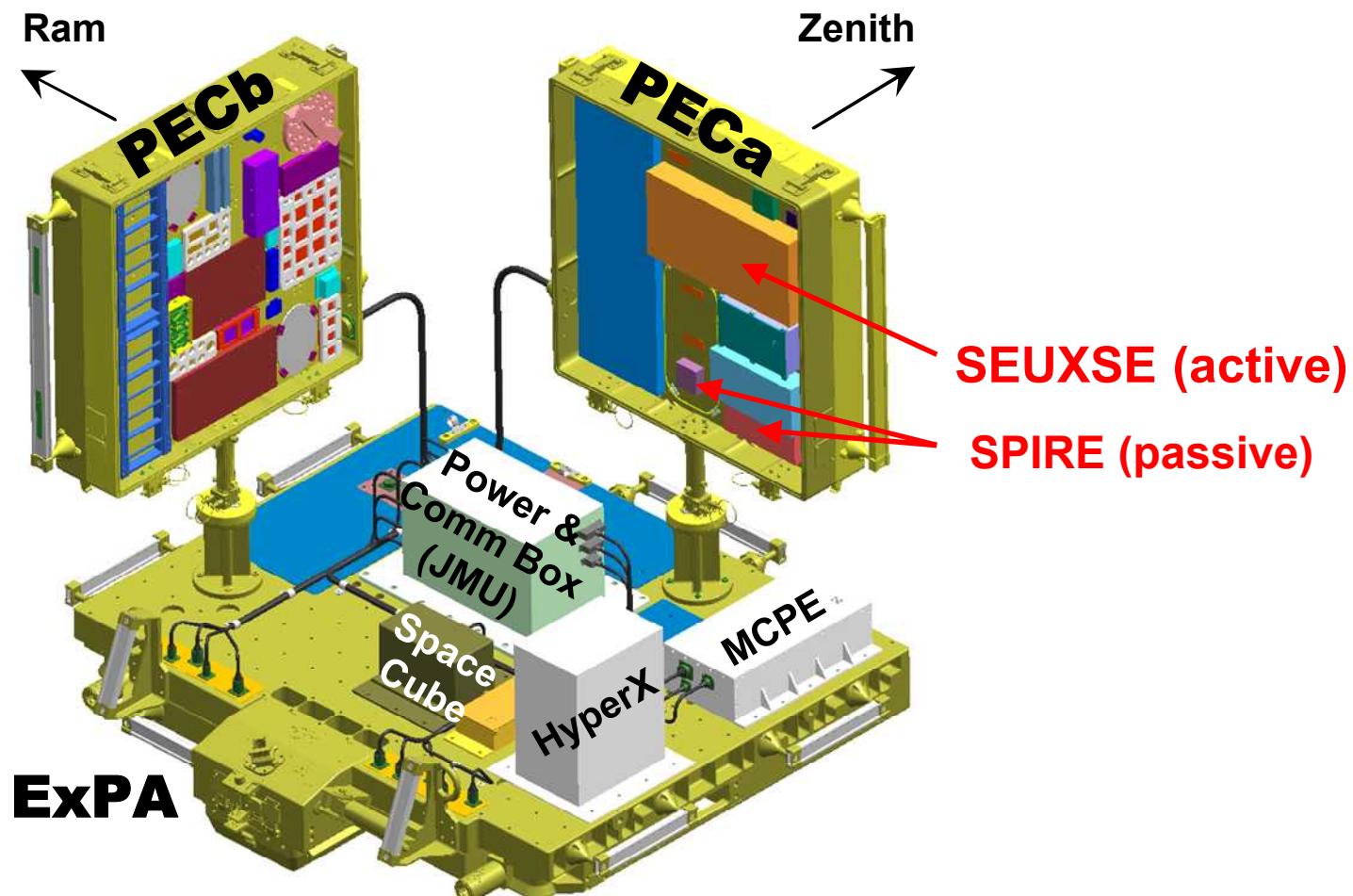


Acronym List

- **ISS: International Space Station**
- **KSC: Kennedy Space Center**
- **ELC: Express Logistics Carrier**
- **MISSE 7: Materials on International Space Station, number 7**
- **ExPA: Express Payload Adapter**
- **PEC: Passive Experiment Carrier**
 - Two PECs on MISSE 7: PEC-A and PEC-B
- **SEUXSE: Single Event Upset Xilinx-Sandia Experiment**
- **SPIRE: Sandia Passive ISS Research Experiment**
- **EVA: Extra-Vehicular Activity (space walk)**



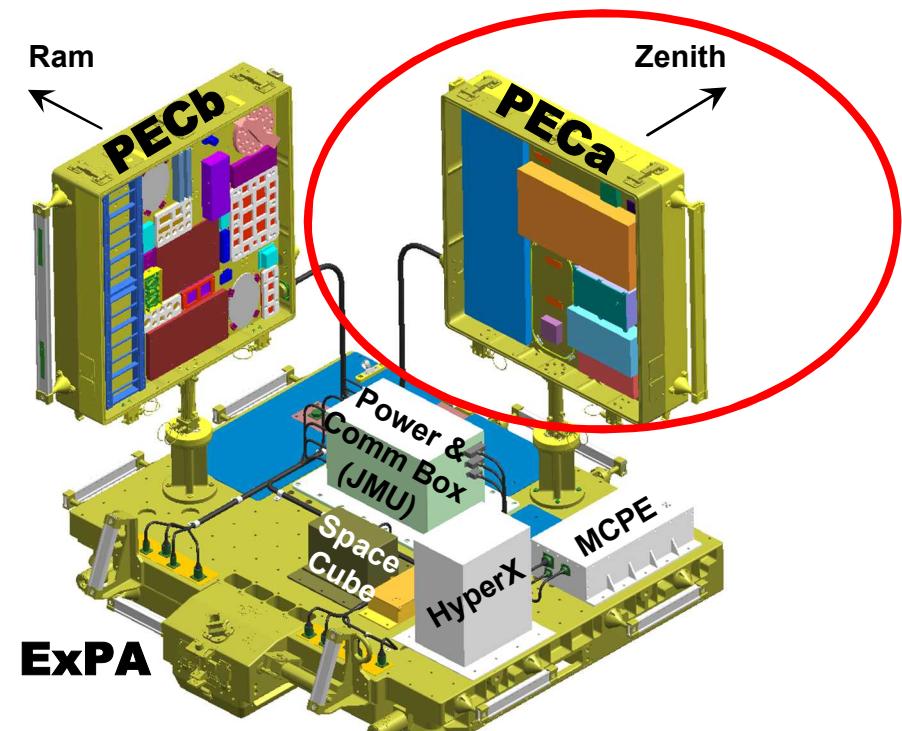
MISSE 7 3D Pictorial View





MISSE 8 Deployment

- MISSE 8 will Re-use MISSE 7 Infrastructure
 - Single Passive Experiment Container (PEC)
 - ISS Power
 - ISS Telemetry
 - 4 channels available/3 used
- MISSE 8 will be only a single PEC to replace PECA
- Schematic diagram of MISSE 7. MISSE 8 will be an exchange of one of the two MISSE 7 PECs using the same physical, data, and power interfaces





MISSE 7 On the Ground at NRL and KSC





STS-129 Space Shuttle Launch





STS-129 Launch



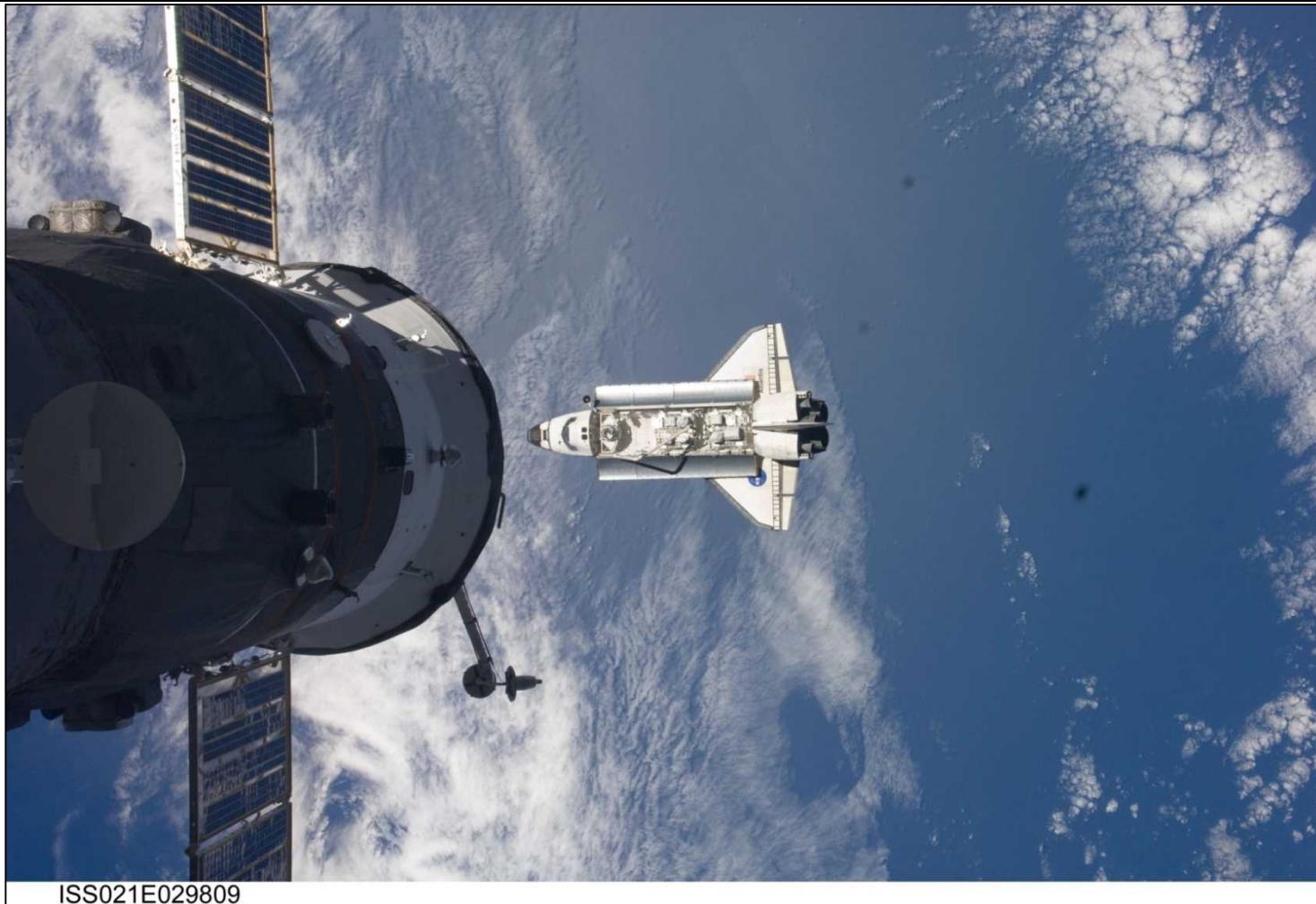


STS-129 Launch





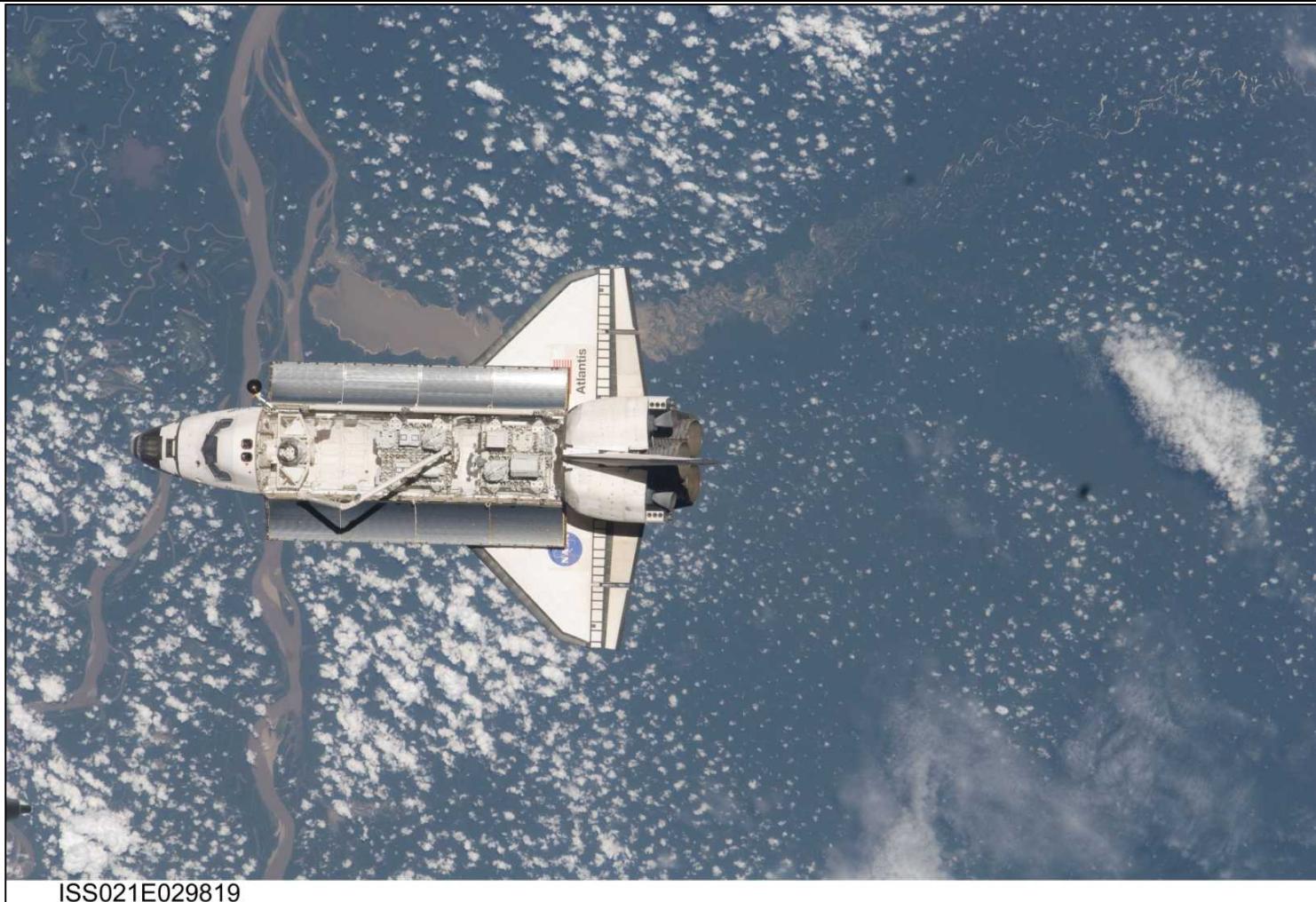
Shuttle Approach to ISS



ISS021E029809



Shuttle with ELC1 and ELC2(rear)



ISS021E029819



ISS Docking Port



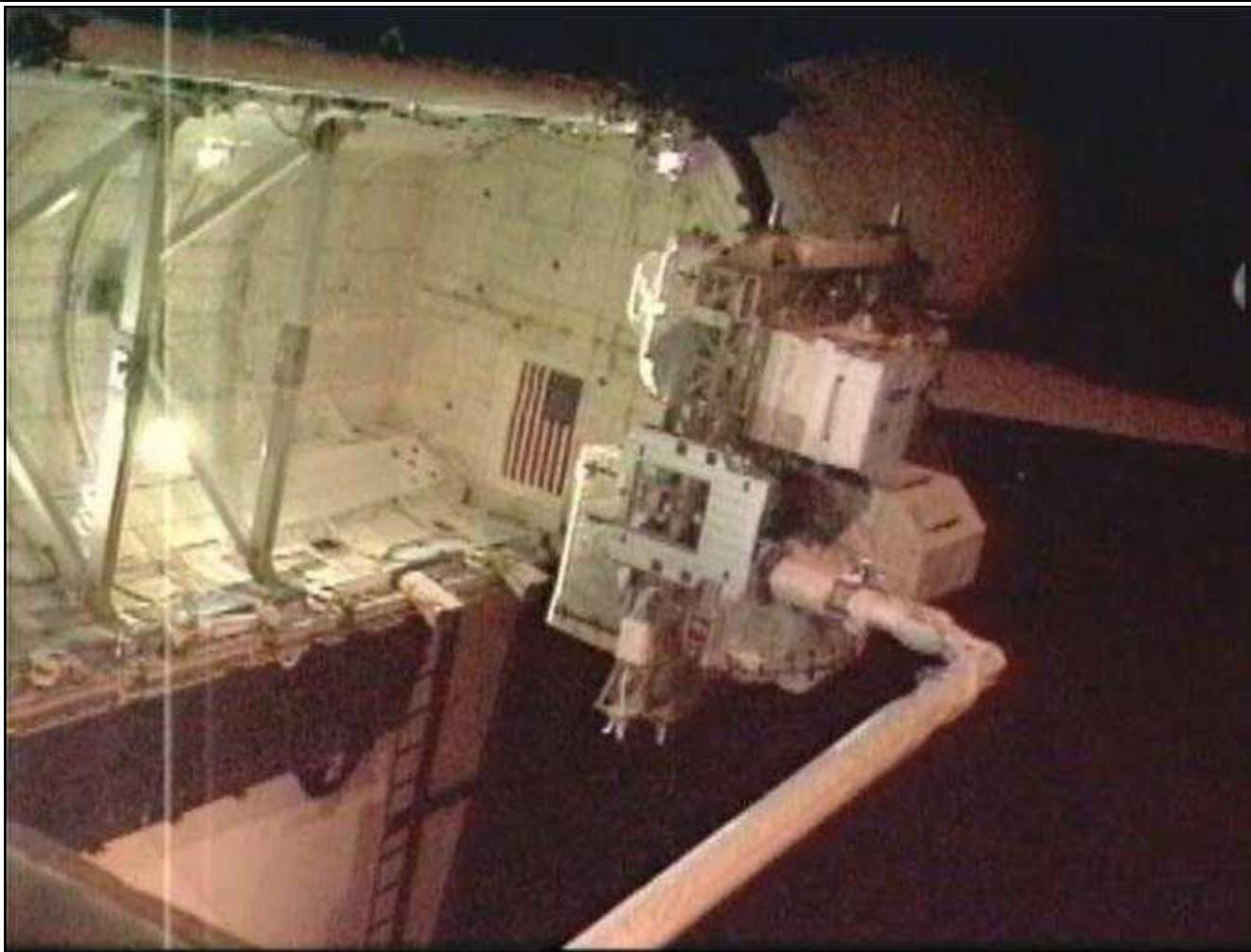


ELC2 w/MISSE7-ExPA in Cargo Bay



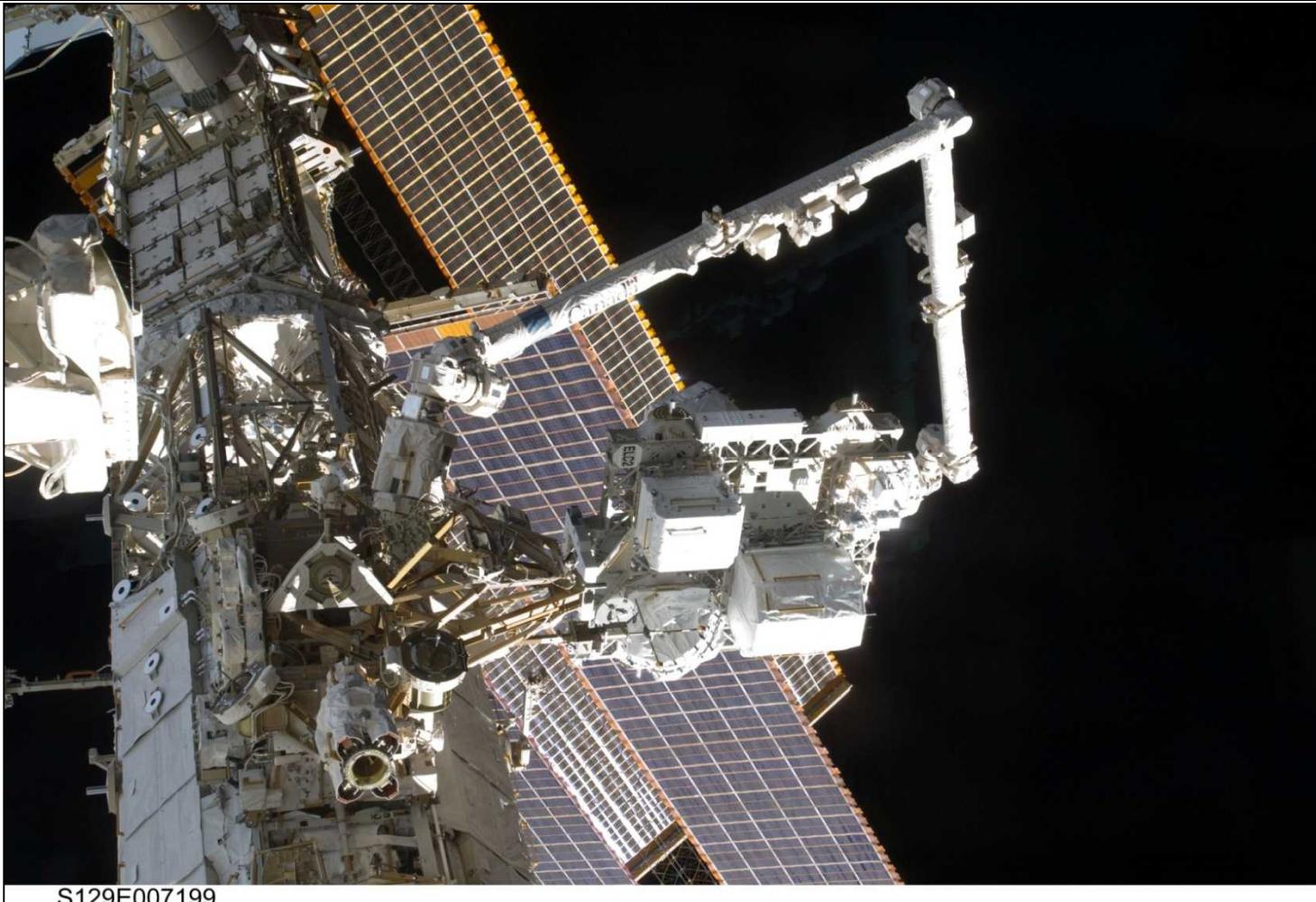


ELC2 Extracted From Cargo Bay (NASA TV)



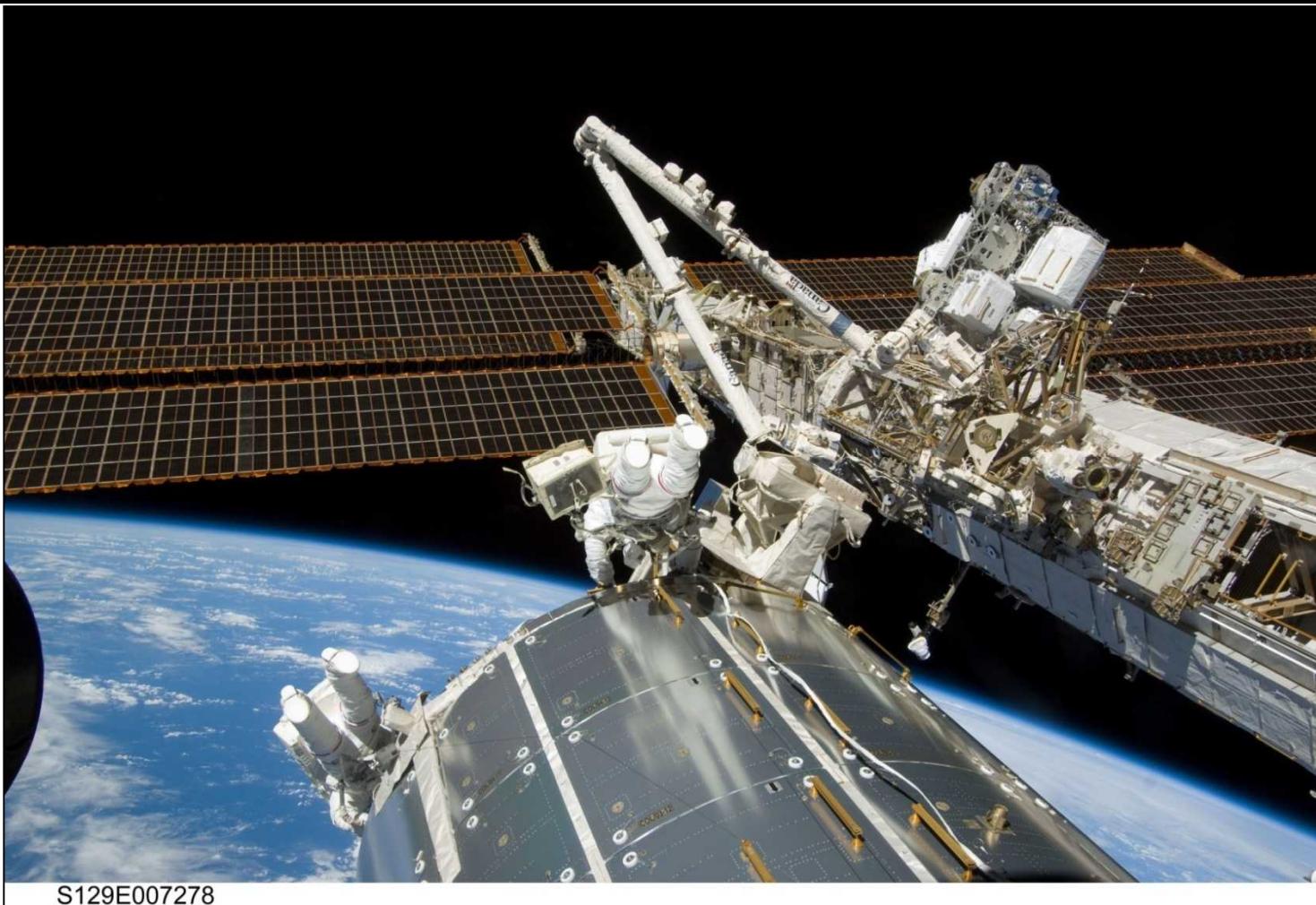


Station Arm Deploys ELC2

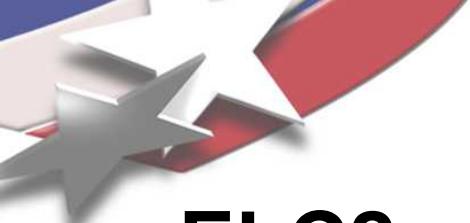




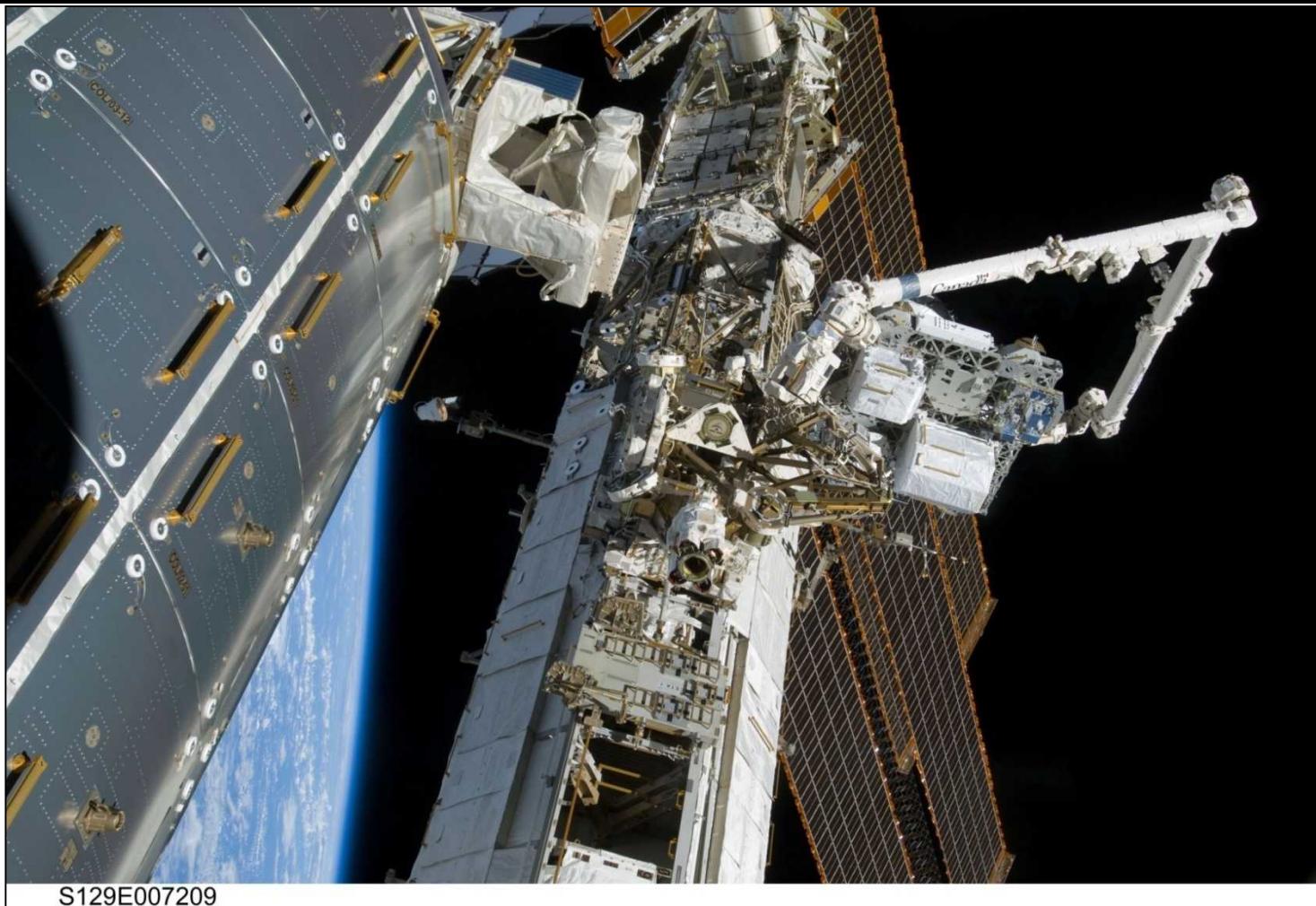
EVA-1 To Attach ELC2 to ISS



S129E007278



ELC2 w/MISSE 7-ExPA Mounted to ISS

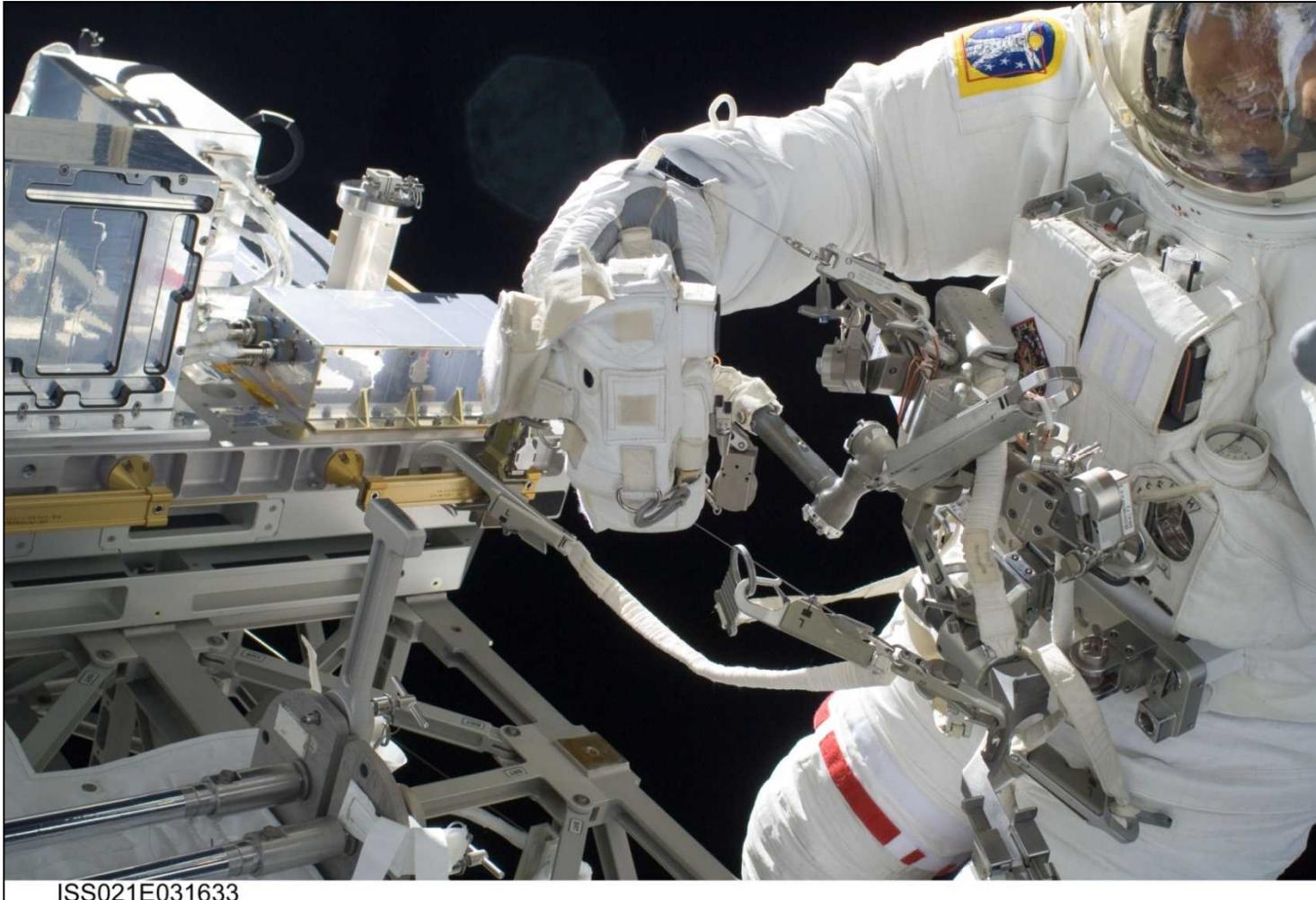


S129E007209



Astronaut with MISSE 7 ExPA

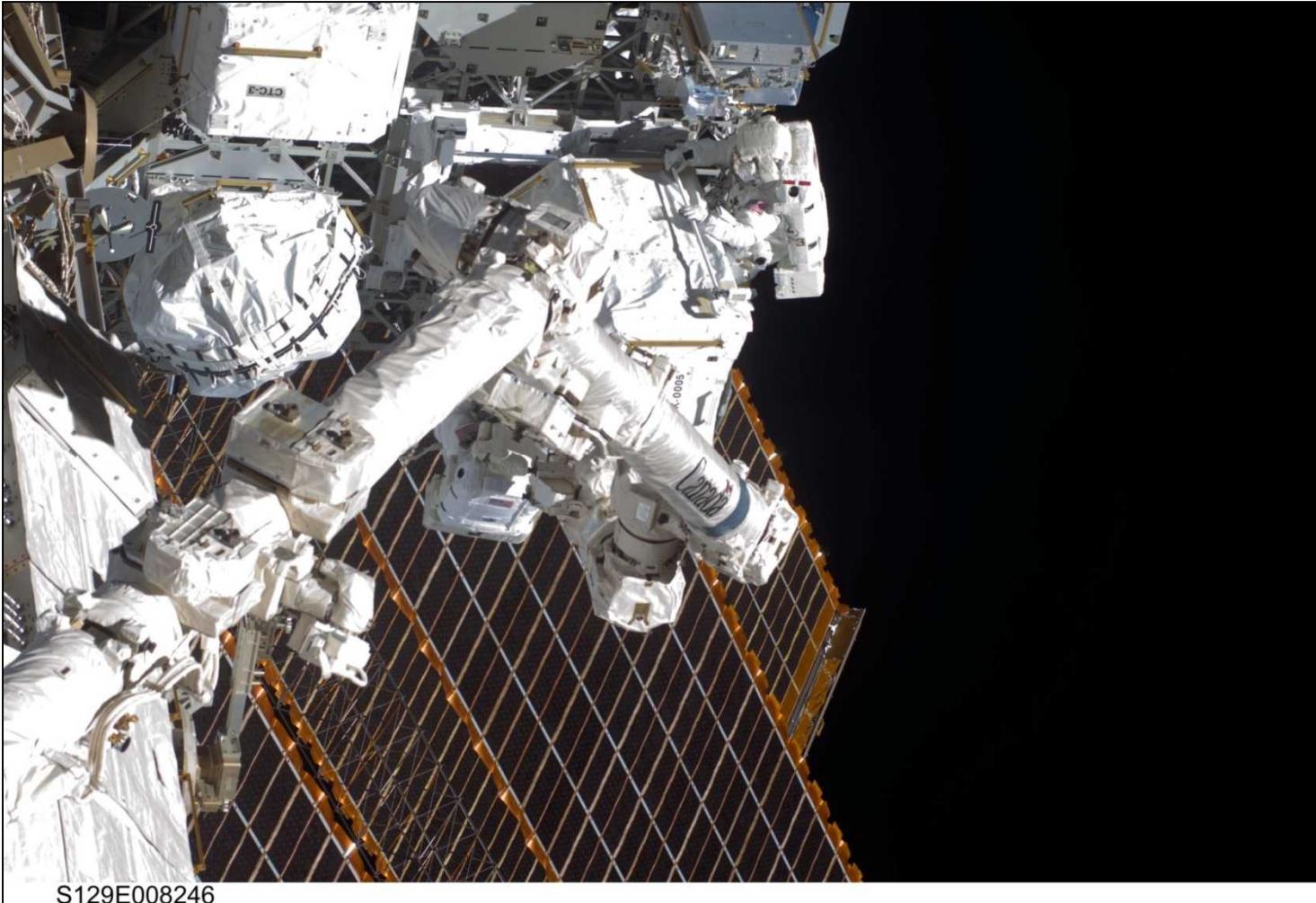
(One of the PEC attachment sockets is shown)



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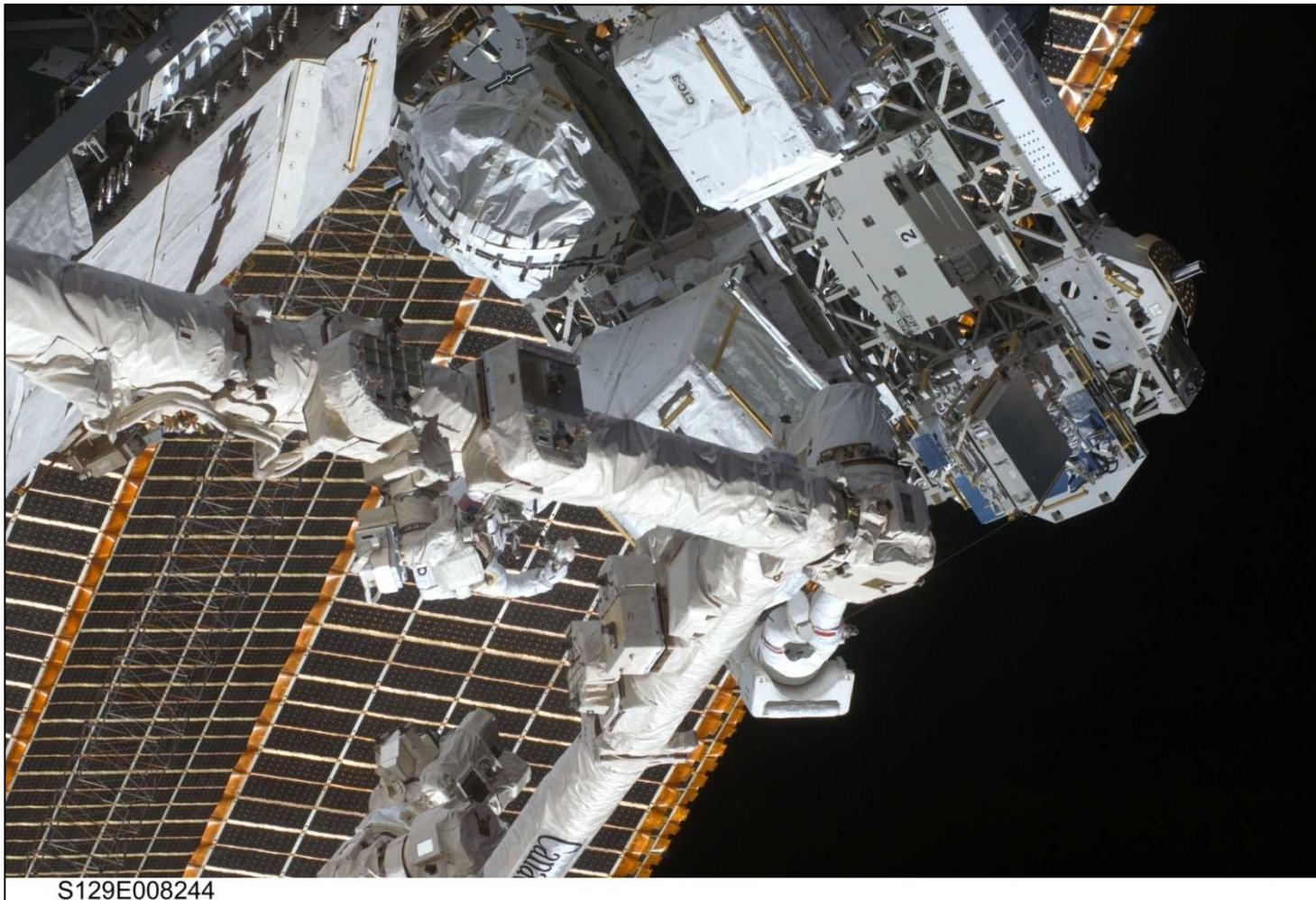


EVA-2 to Deploy MISSE 7 PECs (Removing Gas Tank From ELC2)



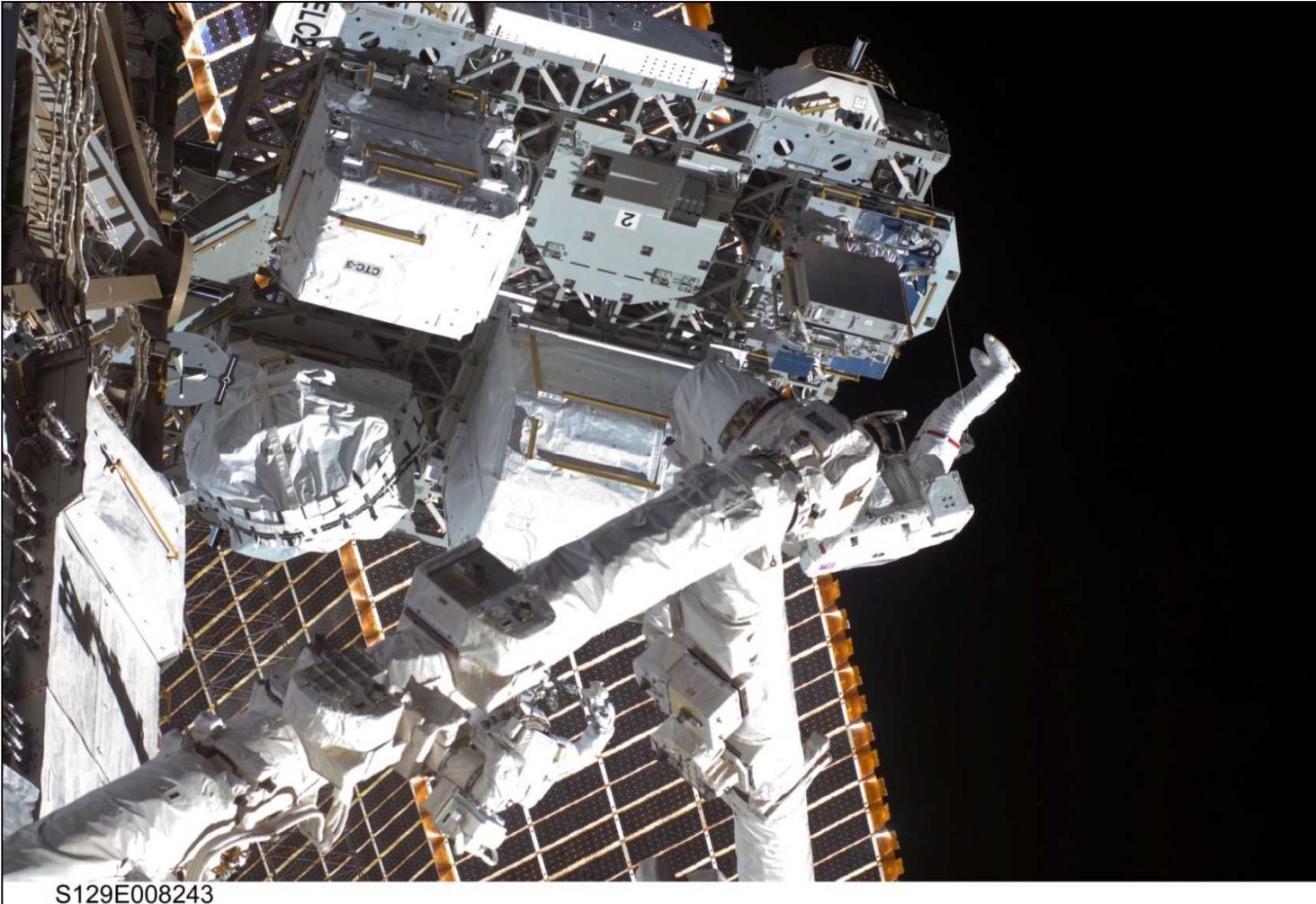


Stowed PEC A/B Attached to ExPA



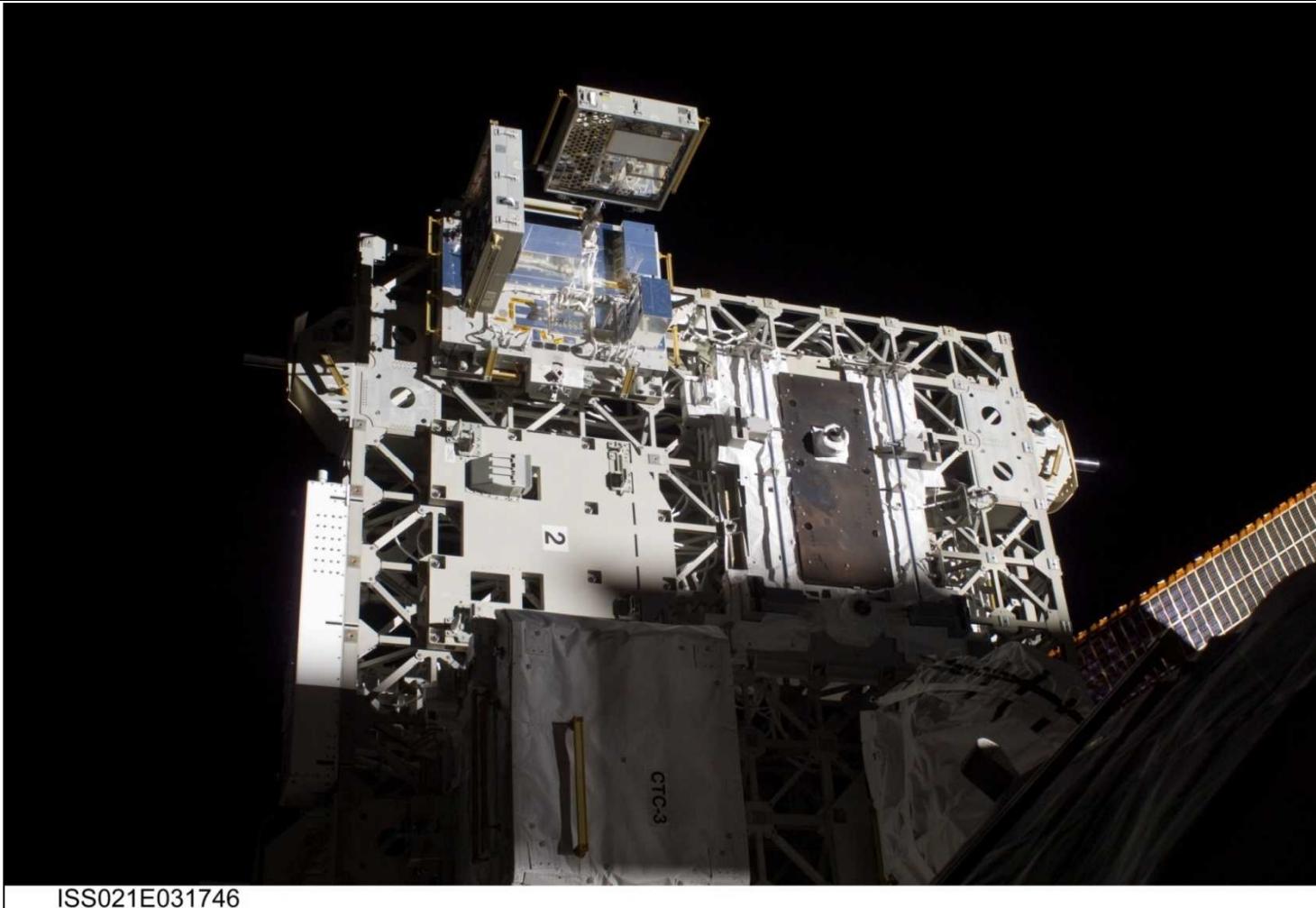


Stowed PEC A/B Before Deployment





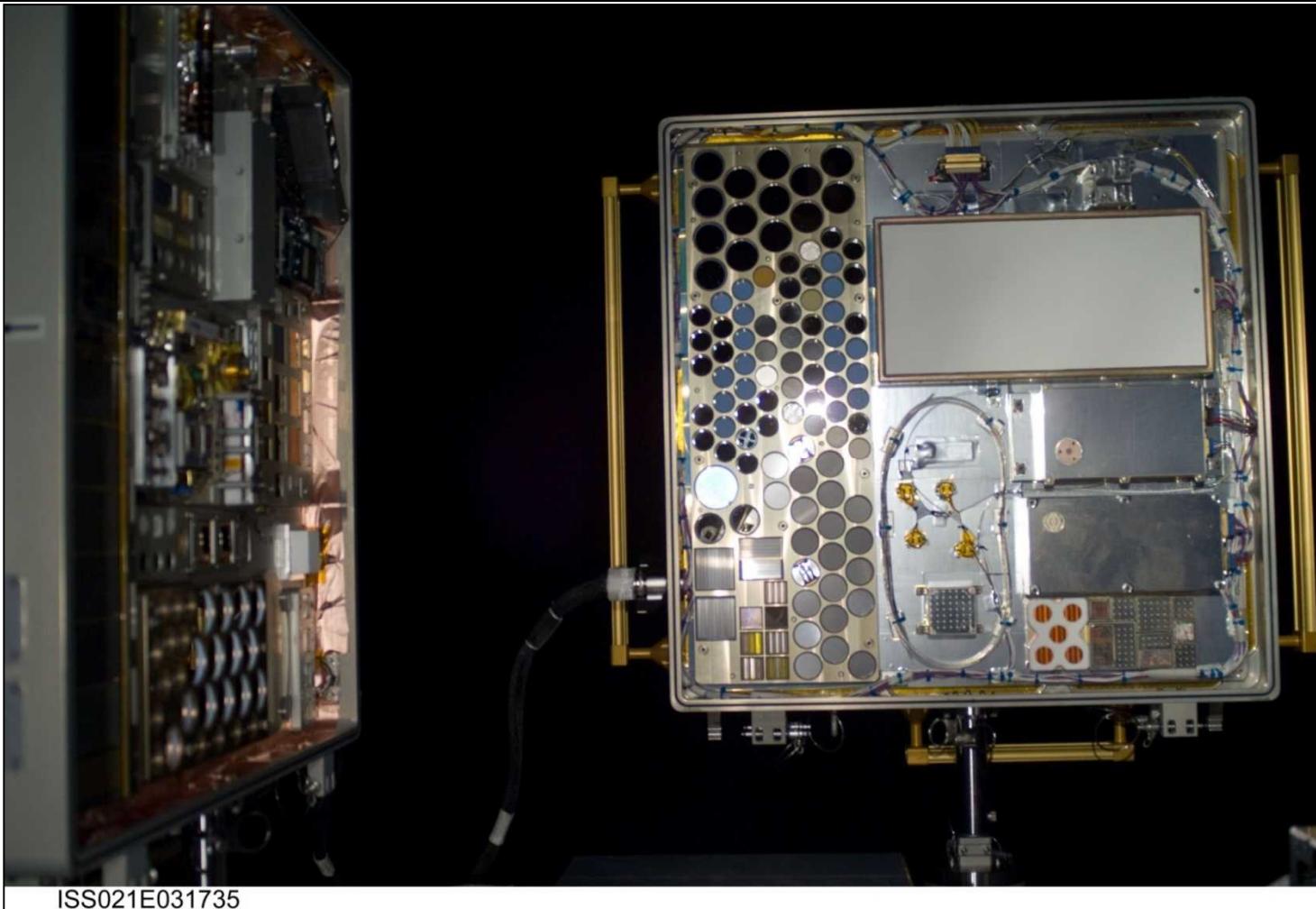
PEC A & B Deployment Completes MISSE 7



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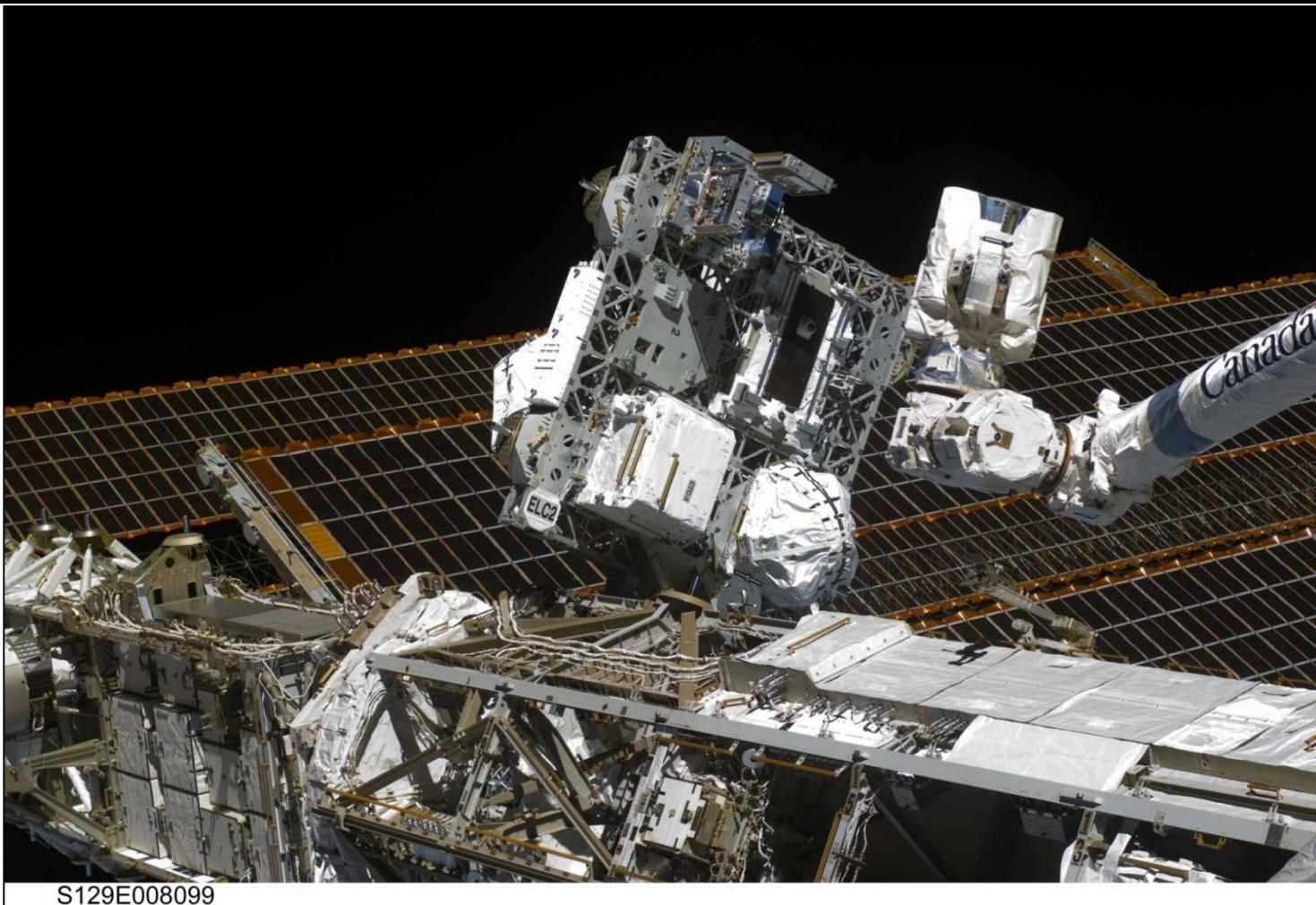
Closeup of PEC-A Nadir and SEUXSE/SPIRE



ISS021E031735



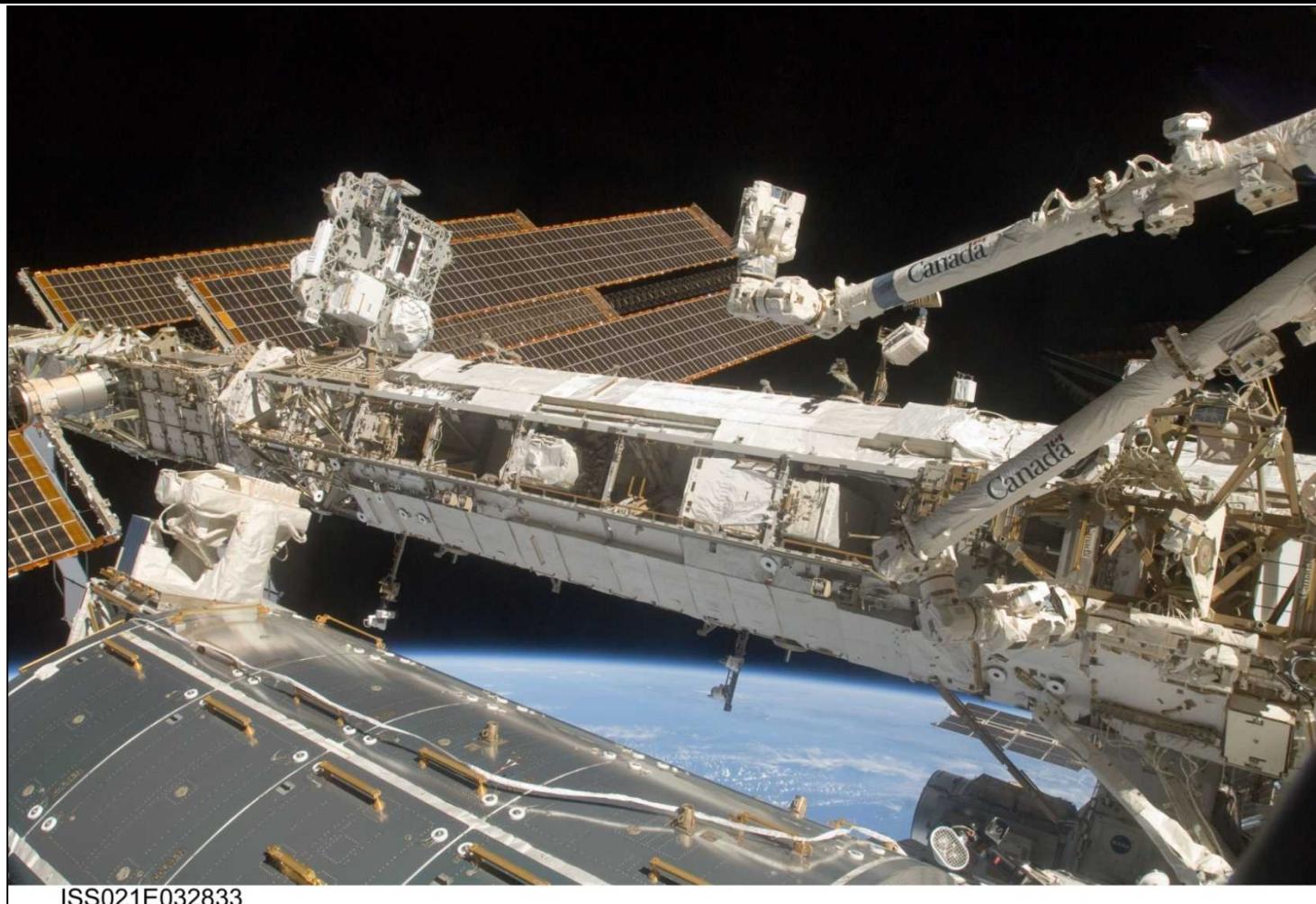
ELC2 with MISSE 7 on ISS



S129E008099



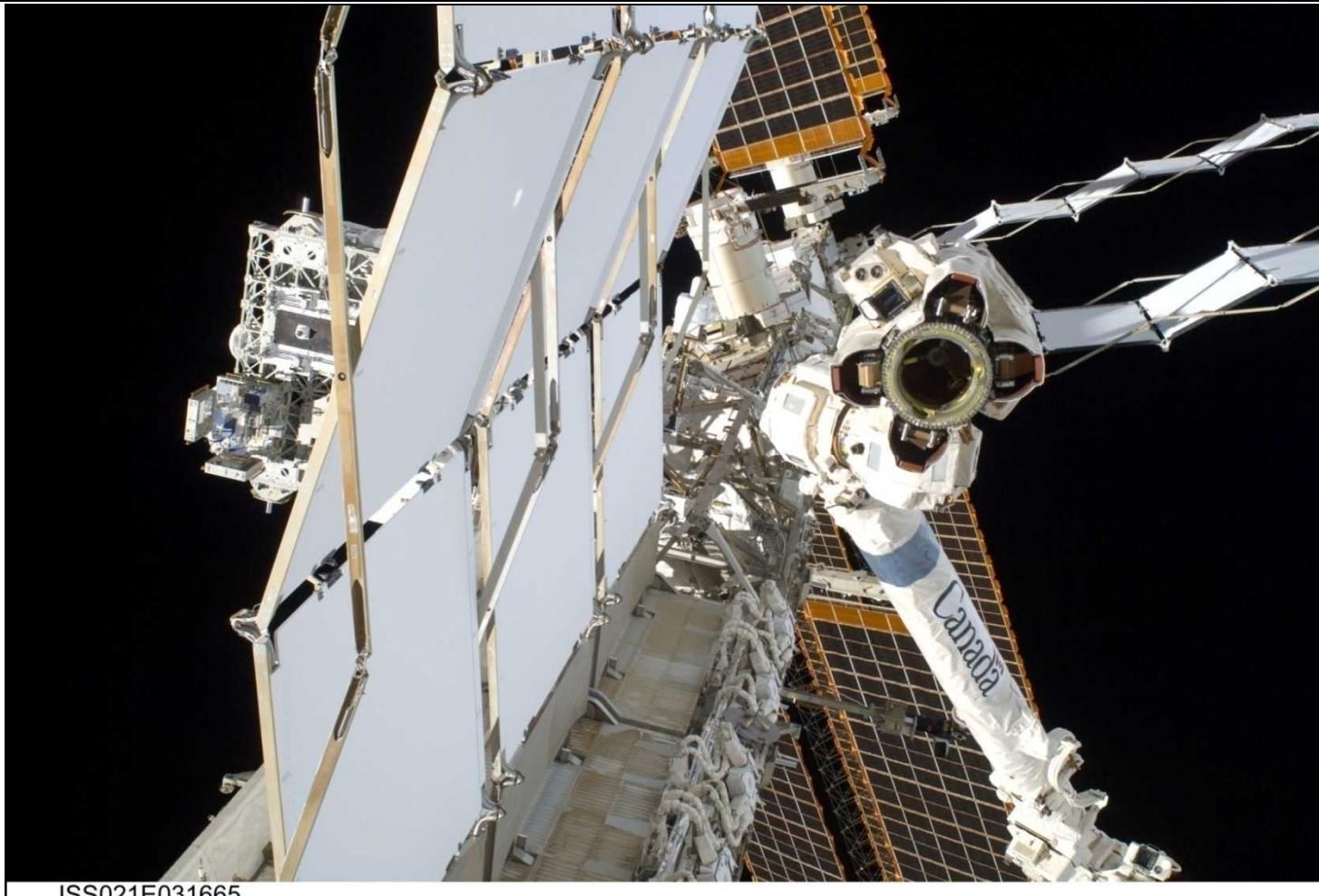
ELC2 Position On ISS SEUXSE on PEC-A Nadir Face



ISS021E032833



ELC2 with MISSE 7 on ISS



ISS021E031665



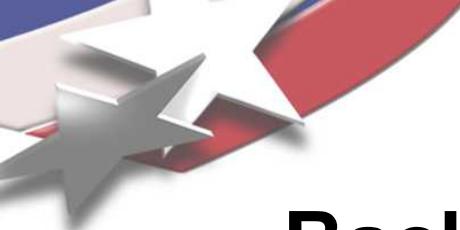
ELC2 with MISSE 7 on ISS



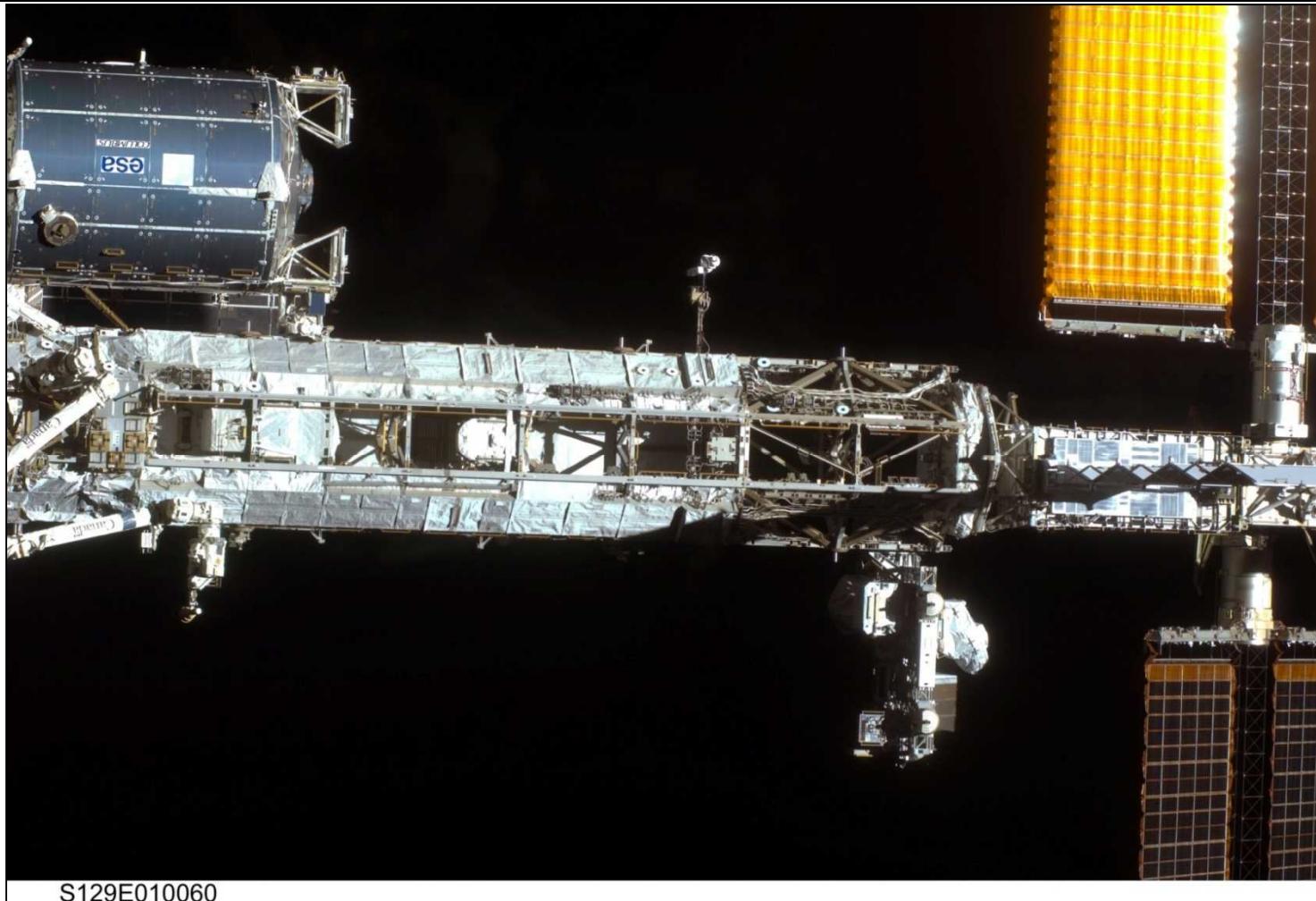


Backside of PEC-A Visible on ISS



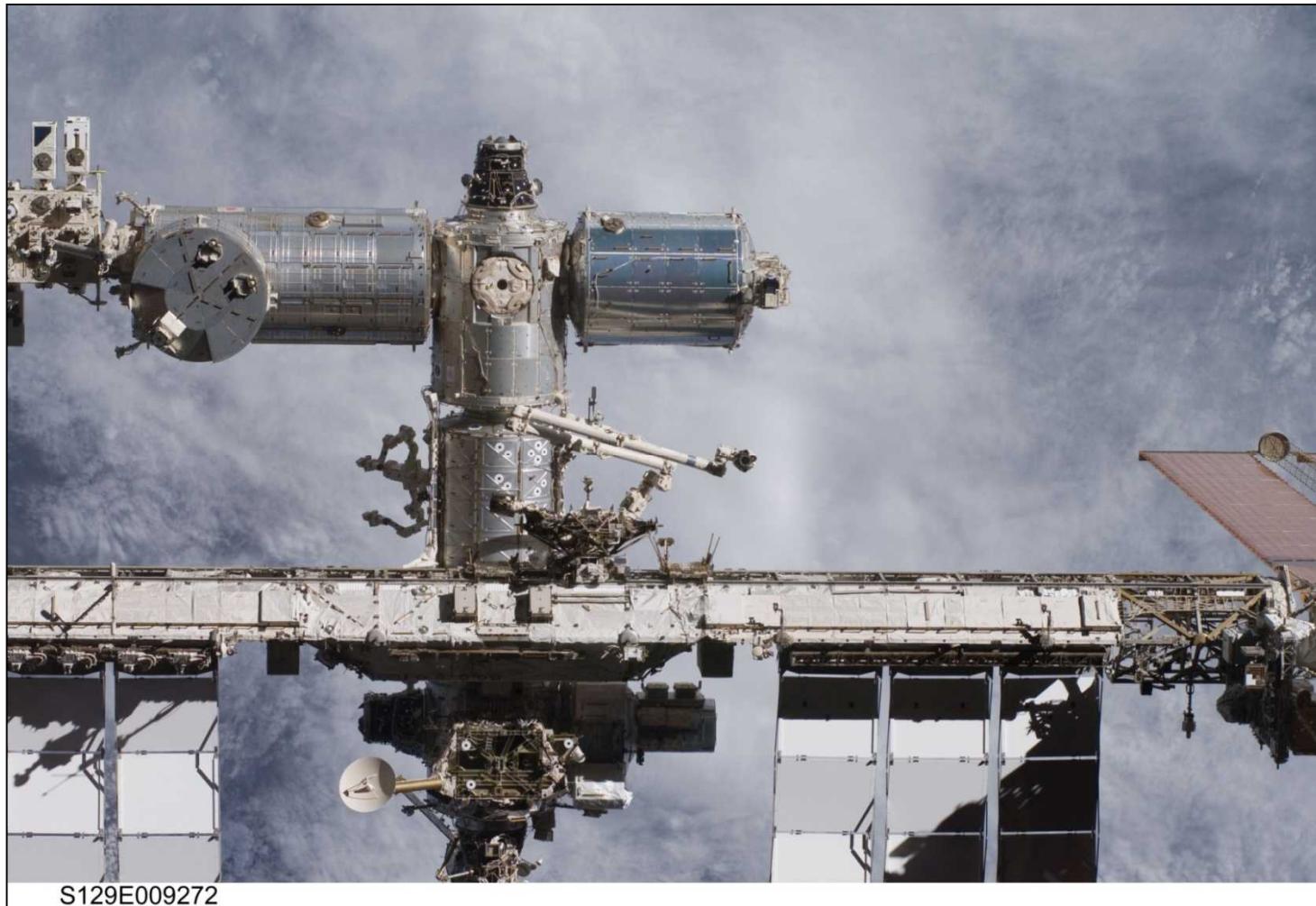


Backside of PEC-B Visible on ISS



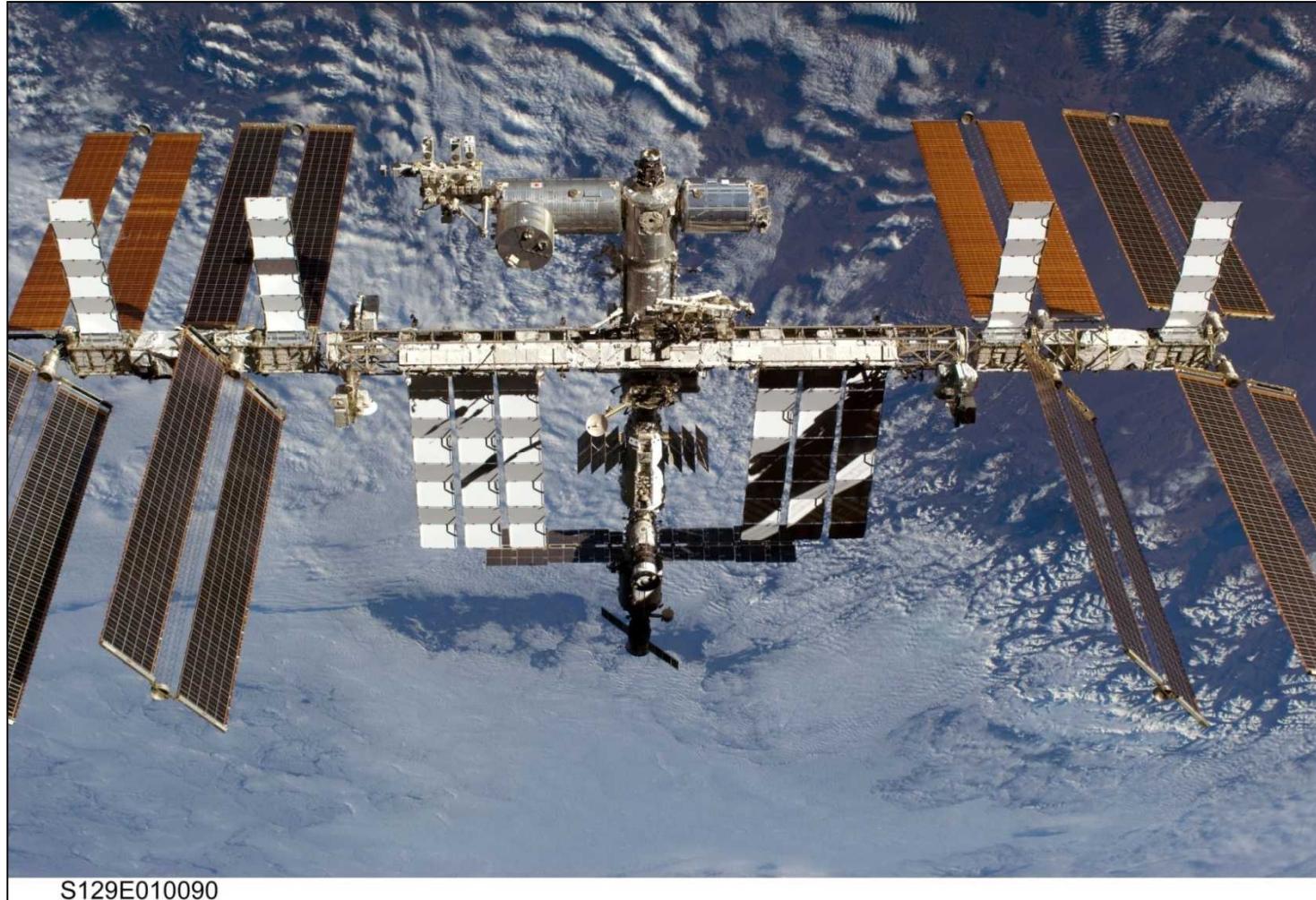


Backside of PEC-A Visible on ISS



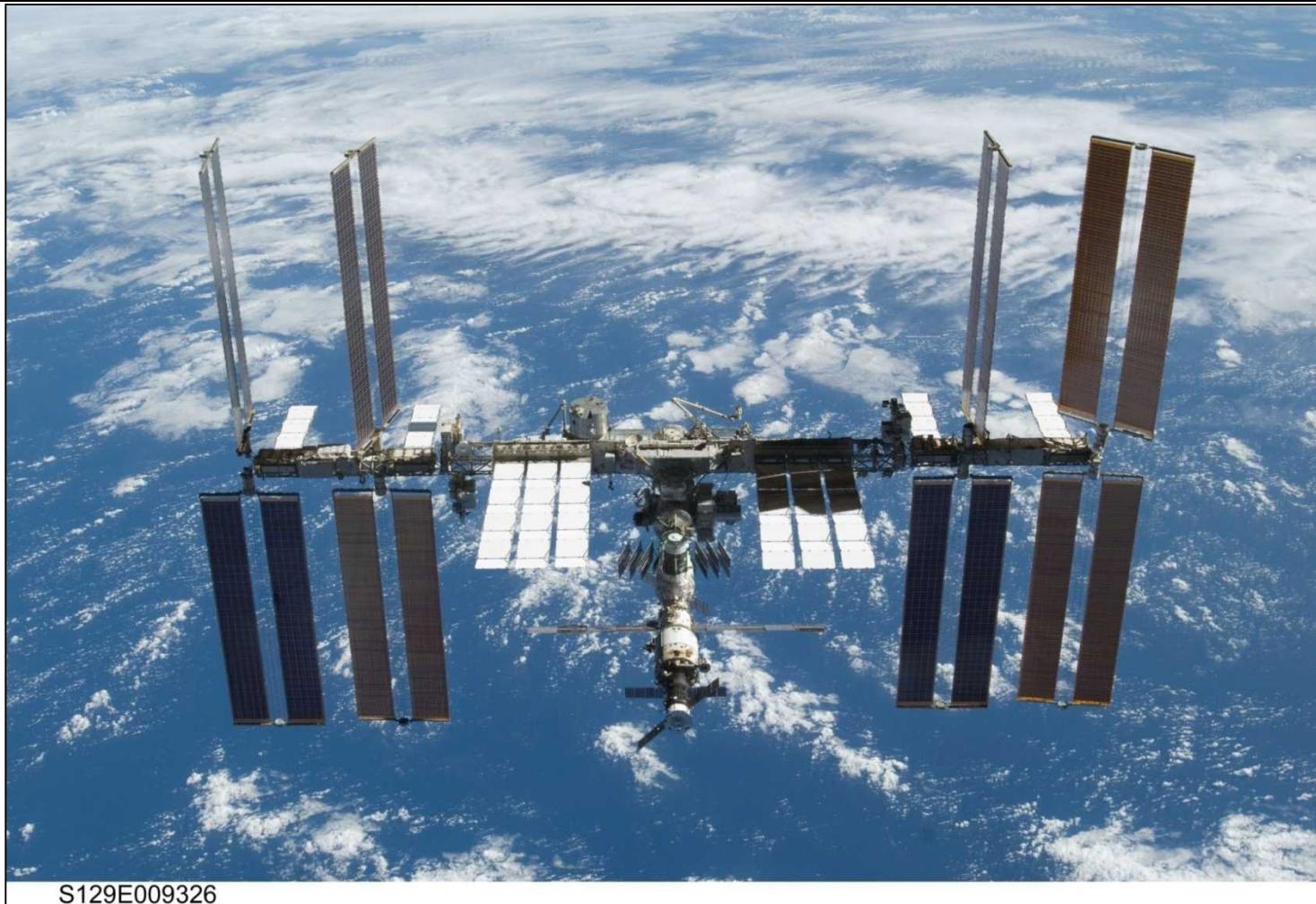


Shuttle Departs ISS





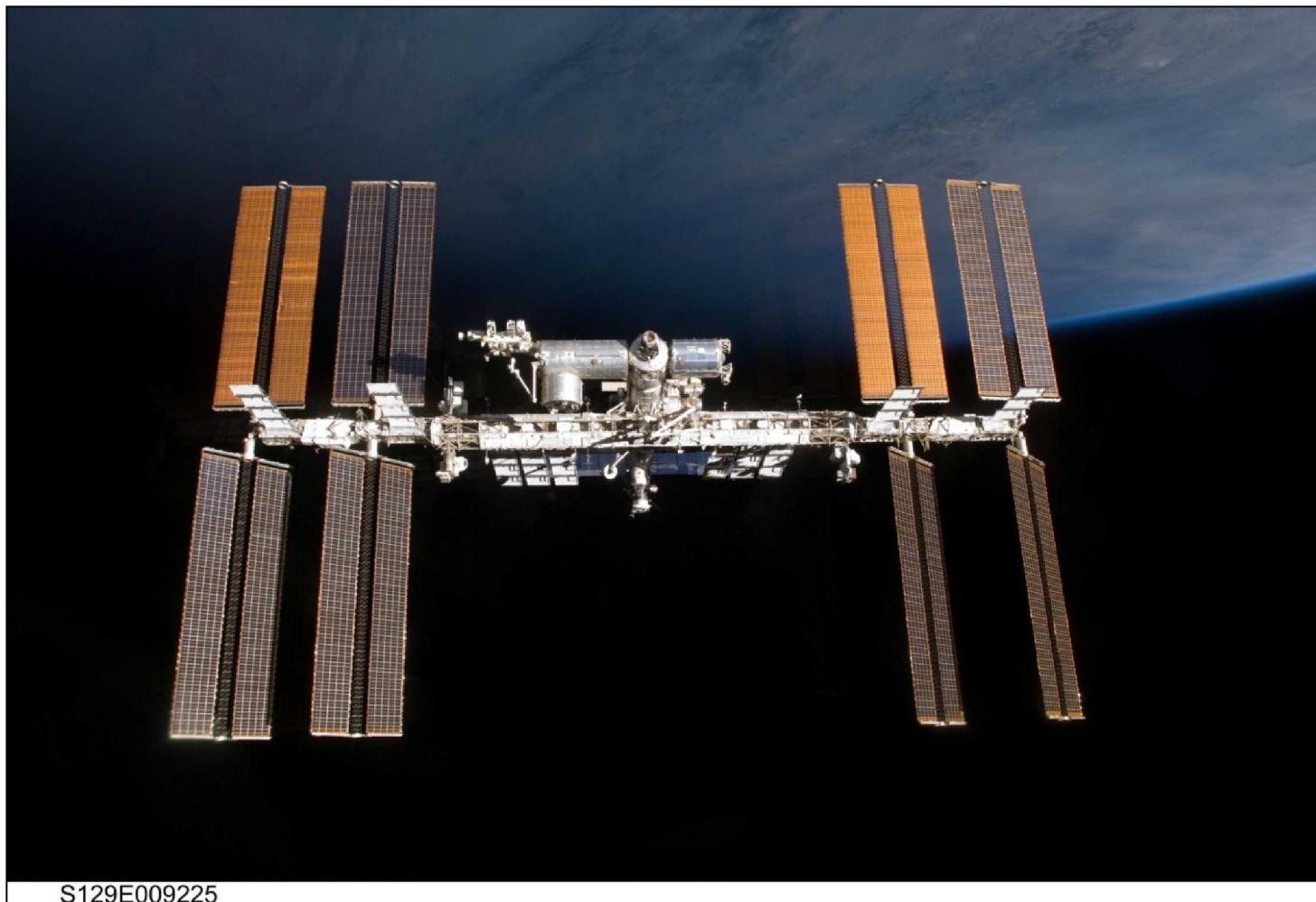
Shuttle Fly Around of ISS



S129E009326



ISS With MISSE 7, SEUXSE, and SPIRE





STS-129 Shuttle Atlantis Touch Down





STS-129 Space Shuttle Landing





Thanks to All Collaborators



Electrical and Computer
Engineering



Unclassified Unlimited Release





Backup

Unclassified Unlimited Release



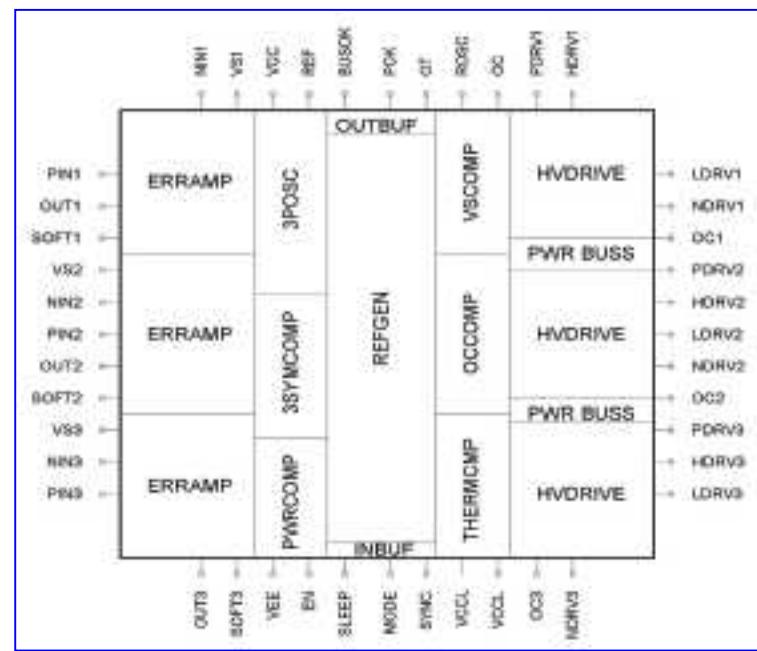


MISSE-7 Power System

- Rad-hard point-of-load (RHPOL) power converters to generate the required low voltages
 - 6 POL Converters: +3.3V, +2.5V, 2 at +1.2V, 2 at +1.0V
 - 90% efficiency
- RHPOL controller IC developed as part of internal Sandia research efforts
 - 3 outputs per controller
 - Total-dose tolerant to >1Mrad(SiO₂)
 - Immune to single-event latchup, burnout, and gate rupture
 - No POL output single-event transients to >80MeV-cm²/mg
- COTS power FETs tested
 - Total-dose tolerant to >30krad(SiO₂)
 - Immune to single-event burnout and gate rupture

POL Controller Development

- 3-Output
 - Multi-rail digital parts (e.g. FPGAs)
- Synchronous Buck topology
 - **High efficiency > 90%**
- High frequency > 300kHz per phase
 - **Reduced size**
- High gain-bandwidth > 3MHz
 - **Improved transient response**
- Phase interleaving
 - **Reduced size and stresses**
- Flexible for varying applications
 - **V_{IN} from 4.5 – 13.2 volts**
 - **V_{OUT} from 0.6 – 5 volts**
- Fully protected
 - **Over-current**
 - **Under/Over-voltage**
 - **Over-temperature**



Basic Controller Architecture

- Radiation-Hardened
 - Total-dose > 100krad(SiO₂)
 - SEL, SEGR, SEB immune to LET > 80 MeV-cm²/mg