

Silicon nanoelectronics for solid-state quantum computing

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Acknowledgements

The technical teams

Silicon quantum dot: E. Nordberg, L. Tracy, G. Ten Eyck, D. Tibbets, K. Childs, J. Wendt, J. Stevens, B. Silva

Donor and donor-dot: E. Bielejec, N. Bishop

Device modeling: R. Muller, R. Young, W. Witzel, E. Nielsen, R. Rahman

Numerous joint research efforts with external community:

Australian Centre for Quantum computing Technology (L. Hollenberg, A. Morello, D. Jamieson, M. Simmons, A. Dzurak)

U. Wisconsin (M. Eriksson, D. Savage, M. Friesen, R. Joynt)

Princeton University (S. Lyon)

U. Maryland (M. Peckerar, S. Das Sarma)

Lawrence Berkeley National Labs (T. Schenkel)

University of New Mexico (A. Landahl)

University of Oklahoma (H. Stalford)

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Outline

MOS quantum dots for quantum computing

Fabrication

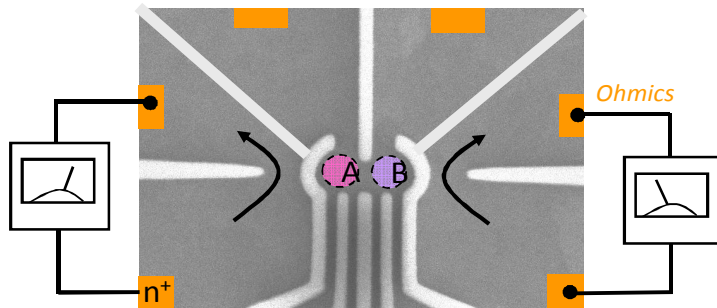
Electrostatically gated quantum dots and electrometry

Donor devices

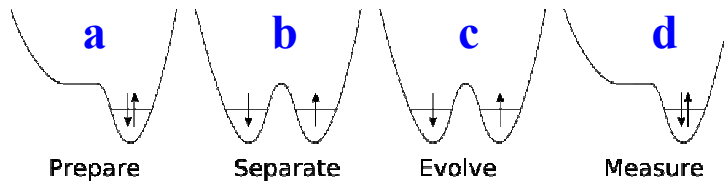
Next steps: yield and single electrons

Quantum computing with singlet/triplet states

Double quantum dot structure

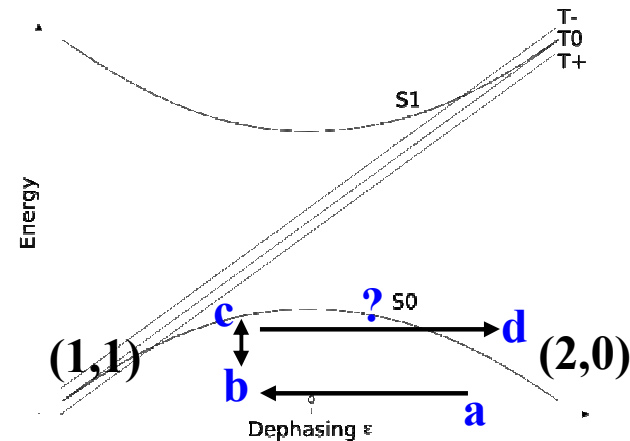


Electron sequence



Petta et al., Science 2005

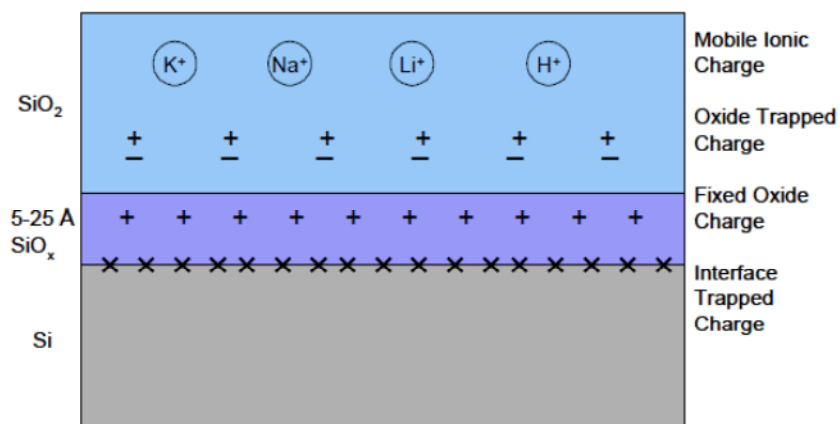
Energy levels



- Quantum states are singlet and triplet of two-electron double quantum dot.
- Electrons can be isolated from the reservoirs and spin state is detected using electrometry.
- DC and pulsed voltages are used to control the qubit.

Challenges to MOS system

Identified critical risk:



Defect density required?

Disorder at amorphous Si/SiO₂ interface

- Single e- dot formation:
 - defects create unwanted fluctuations in potential landscape
- Electrical drift and noise
 - local fluctuations in trap occupation
- Spin coherence:
 - paramagnetic defects

- Minimize damage created to interface during processing
- Move electrons away from interface (donors)
- Improve the defects at the interface (SiGe)

Slide 5

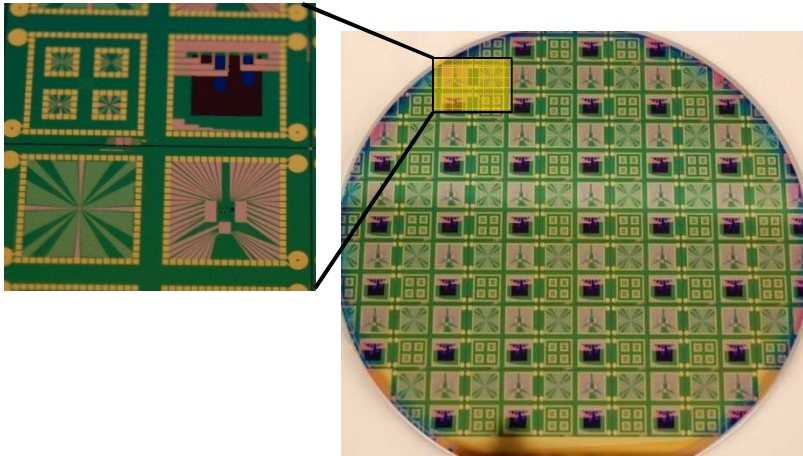
MPL1

Mention Lyon's T1, T2 measurements in MOS systems as another motivation for SiGe and donor approaches. Better interface and further from interface respectively

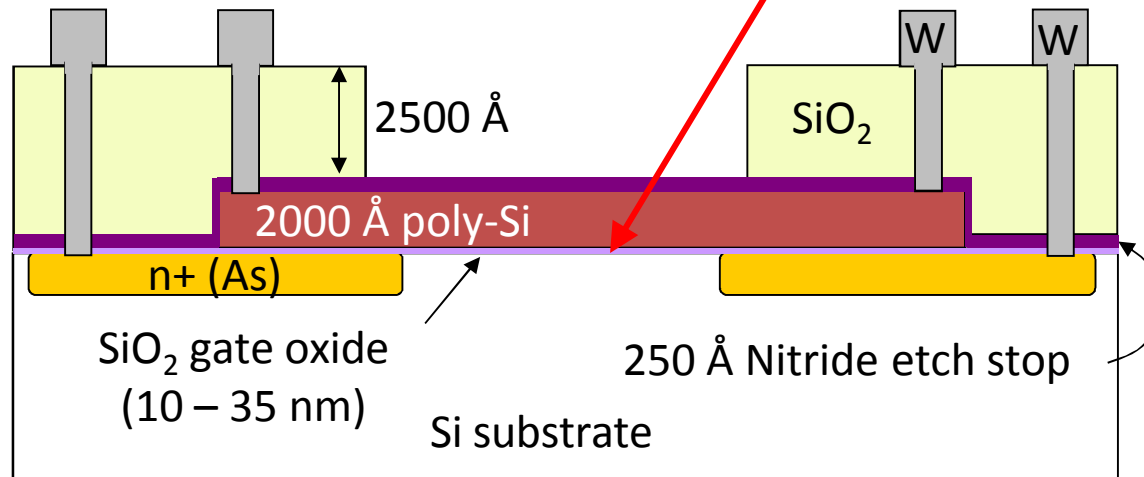
Michael Lilly, 2/3/2010

Si MOS stack

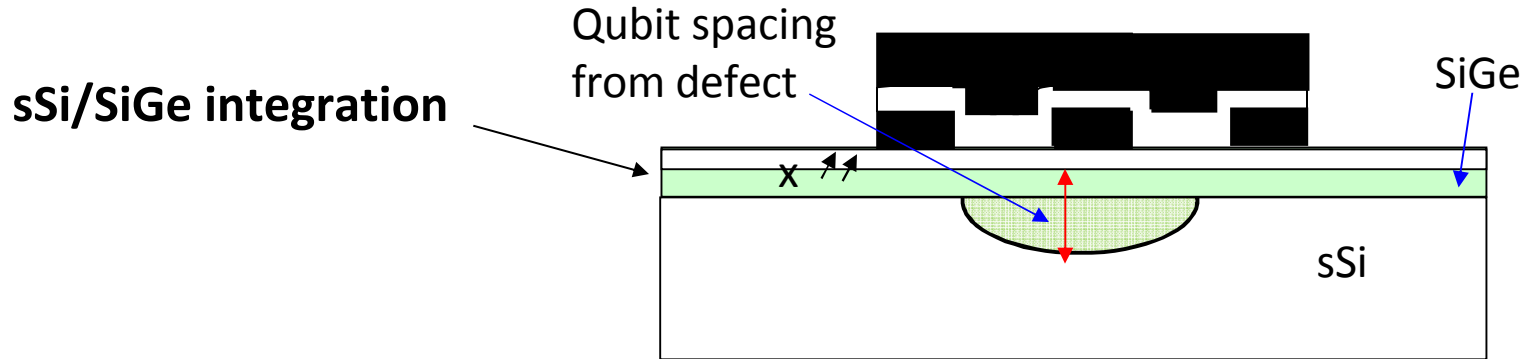
1. Front end: MDL (K. Eng, K. Childs)



2D electron gas formed at
Si/SiO₂ interface



SiGe integration



SiGe/sSi approach:

- Si DQD platform provides starting point to SiGe or donor integration
- Use strained Si on Insulator (SOI) as starting substrate
- SiGe growth to form enhancement mode SiGe/sSOI structures

Initial work is a collaboration with D. Savage, U. Wisconsin

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MOS quantum dots for quantum computing

Fabrication

Electrostatically gated quantum dots and electrometry

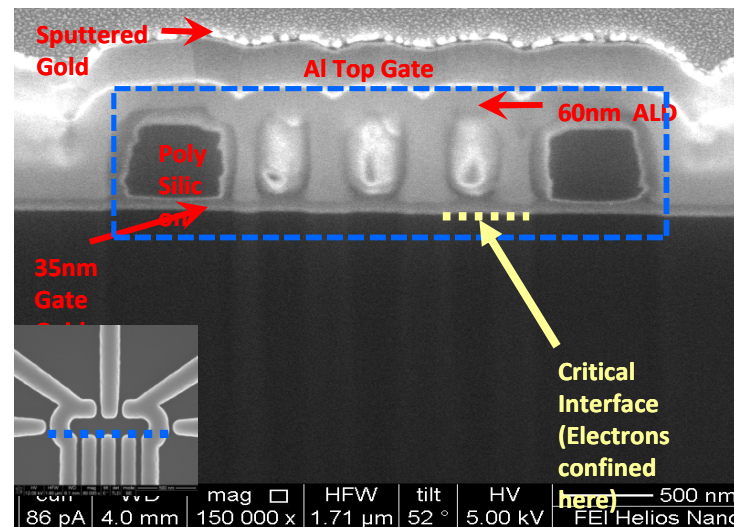
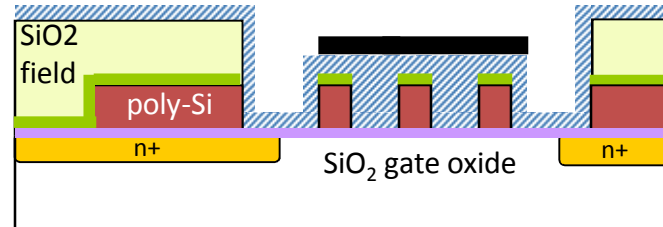
Donor devices

Next steps: yield and single electrons

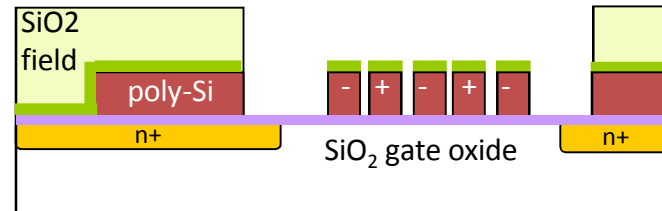
Design of electrostatic gated nanostructures

Double top gate *full process flow*

- MDL processing
- E-beam lithography
- Poly-Si etch
- Strip metal
- Poly-Si reoxidation
- Deposit ALD Al_2O_3
- Etch via holes
- Deposit top gate
- Forming gas anneal

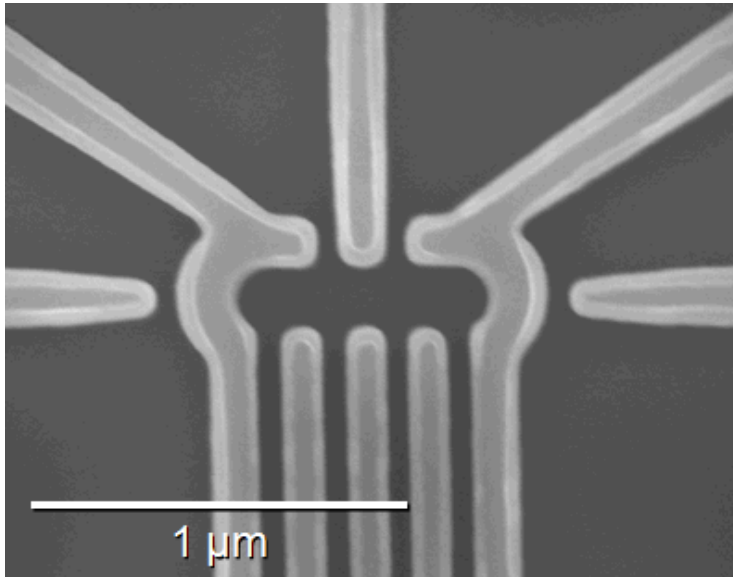


Single polysilicon layer *minimal processing*

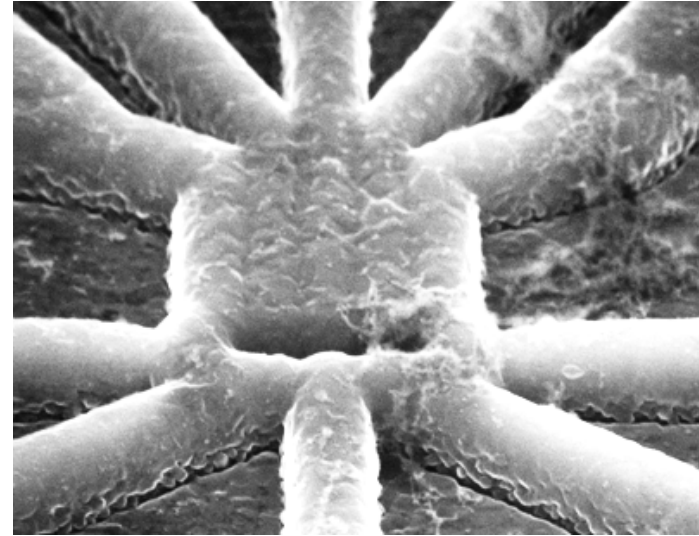


Back-end fabrication: results

DQD poly gate etch



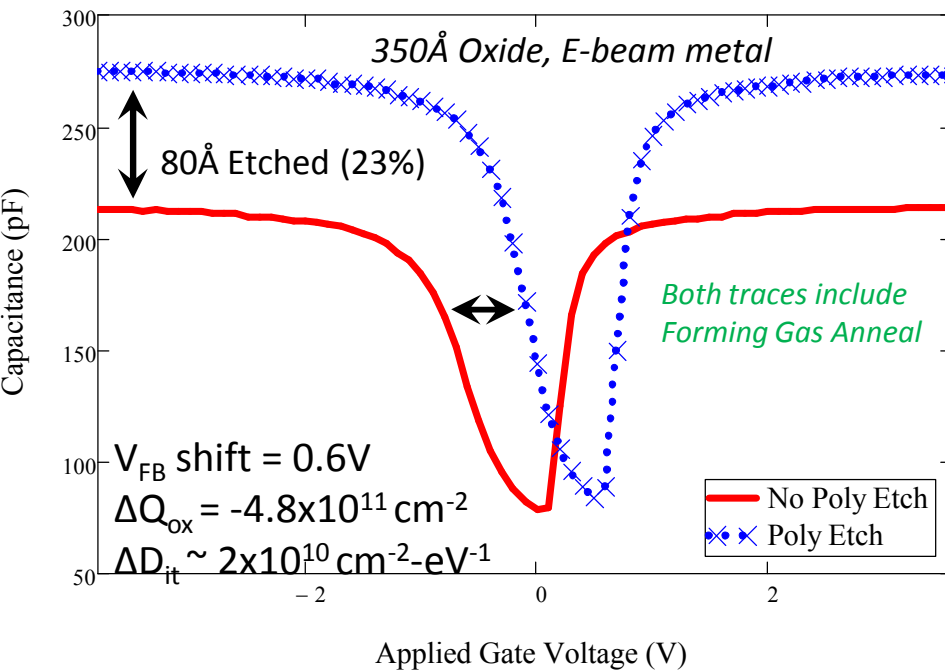
After ALD and Al metal



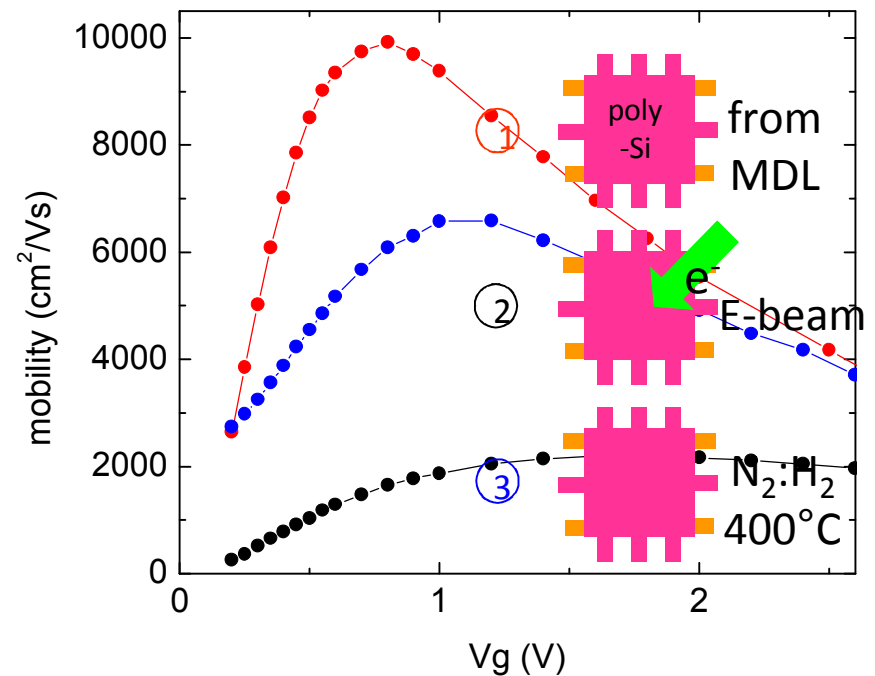
- Quantum point contacts and quantum dots with good transport characteristics have been fabricated
- Yield is a key issue
- Many variations in the queue in parallel

Impact of nanoelectronics fabrication

C-V characterization of oxide



Mobility characterization of charge scattering



Max. mobility: $\sim 15,000 \text{ (cm}^2\text{V}^{-1}\text{s}^{-1}) \Rightarrow \sim 200$

Start $D_{it} : \sim 10^{10} \text{ eV}^{-1}\text{cm}^{-2} \Rightarrow 10^{12}$

Start $Q_{ox} : \sim 10^{11} \text{ cm}^{-2} \Rightarrow 10^{12}$

Slide 11

MPL4

will also need CV table if CV is introduced at this point

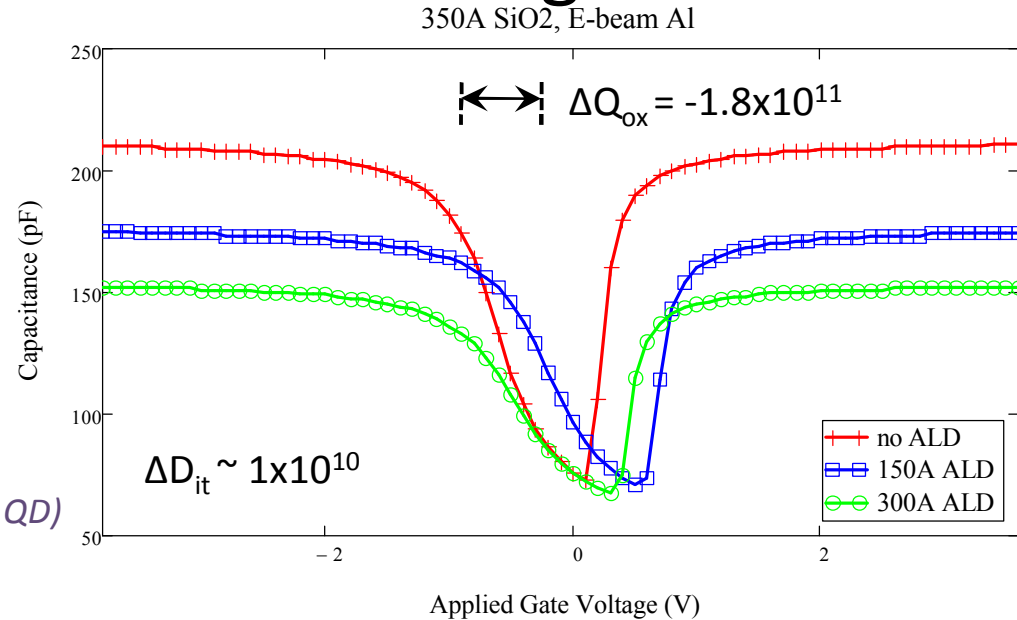
Michael Lilly, 2/3/2010

ALD Process Damage

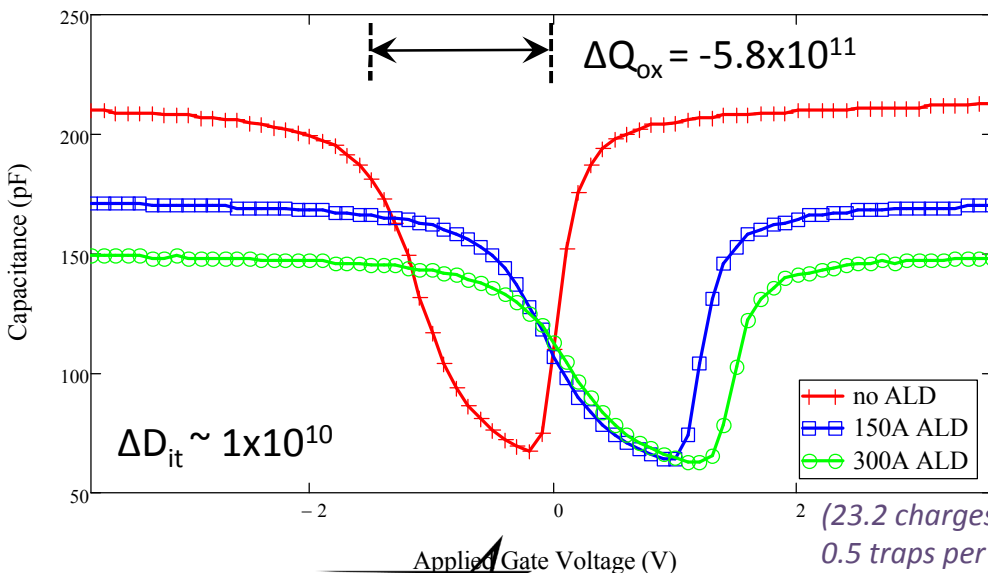
Understanding the charge in ALD is complicated by coupled process effects

All CV traces include
Forming Gas Anneal

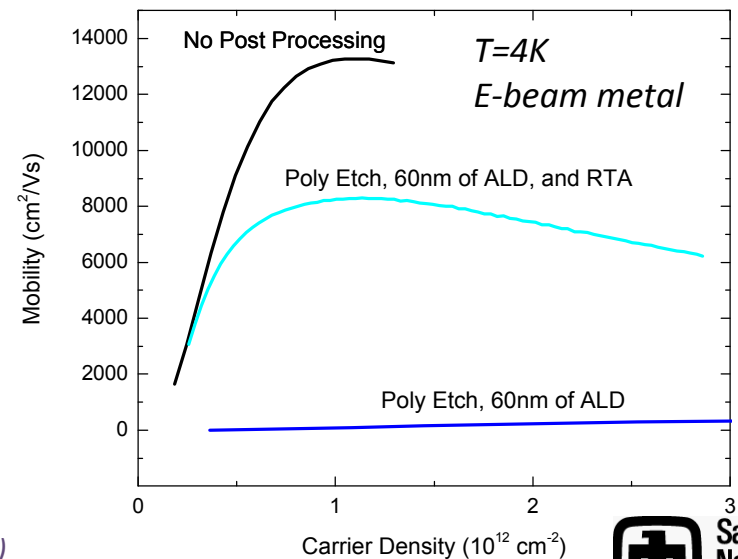
(7.2 charges,
0.5 traps per QD)



350Å SiO₂, Thermal Al



(23.2 charges,
0.5 traps per QD)



Disorder characterization for process steps

DQD process

Condition	T_{SiO_2} [nm]	$T_{Al_2O_3}$ [nm]	μ_{peak} [cm ² V ⁻¹ s ⁻¹]	Start μ_{peak} [cm ² V ⁻¹ s ⁻¹]	n_{peak} [cm ⁻²]	$\mu(n=5 \times 10^{11}$ cm ⁻²) [cm ² V ⁻¹ s ⁻¹]	Density Method	Oxidation Condition
Phase I only	35	0	8,000 – 16,000 (wafer dependant)	8,000 – 16,000	$\sim 10^{12}$	5,500- 10,000	C _{ox} - nominal	Various
Phase I / e-beam litho (EBL)	10	0	2,000	10,000	3.5×10^{11} 2	650	C _{ox} - nominal	10nm Ox. w/ DCE*
Phase I / e-beam litho (EBL) / forming gas	10	0	6,600	10,000	2.4×10^{11} 2	3,500	C _{ox} - nominal	10nm Ox. w/ DCE
Phase I / poly etch / Al	35	0	150	13,800	$> 4 \times 10^{12}$	30	C _{ox} - nominal	35nm Ox. w/ DCE
Phase I / poly etch / Al / forming gas	35	0	5,250	13,800	1.8×10^{11} 2	750	Hall	35nm Ox. w/ DCE
Phase I / poly etch / ALD / Al	35	60	300	13,800	$> 4 \times 10^{12}$	50	C _{ox} - nominal	35nm Ox. w/ DCE
Phase I / poly etch / ALD / Al / forming gas	35	60	8,300	13,800	1×10^{12}	6,800	Hall	35nm Ox. w/ DCE
Phase I / ebeam Al	35	0	4,950	14,250	2×10^{12}	2,500	C _{ox} - nominal	35nm Ox. w/ DCE
Phase I / ebeam Al / forming gas	35	0	8,700	14,250	1.2×10^{11} 2	5,700	C _{ox} - nominal	35nm Ox. w/ DCE
Phase I / thermal Al	35	0	8000	8000	X	X	X	X

- MDL processing
- E-beam lithography
- Poly-Si etch
- Strip metal
- Poly-Si reoxidation
- Deposit ALD Al₂O₃
- Etch via holes
- Deposit top gate and contact pads
- Forming gas anneal

- Nanostructure fabrication has strong impact on mobility
- Forming gas is important for cleaning up interface

Outline

MOS quantum dots for quantum computing

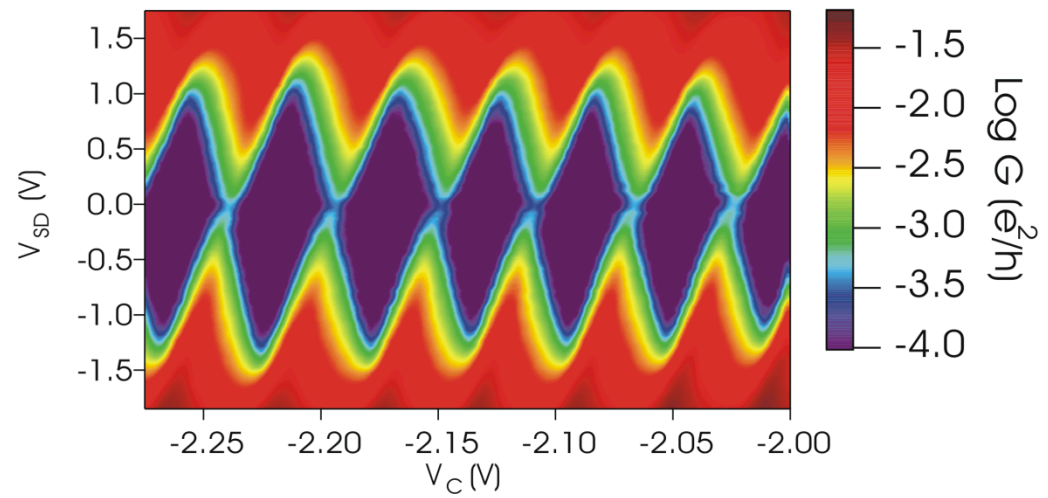
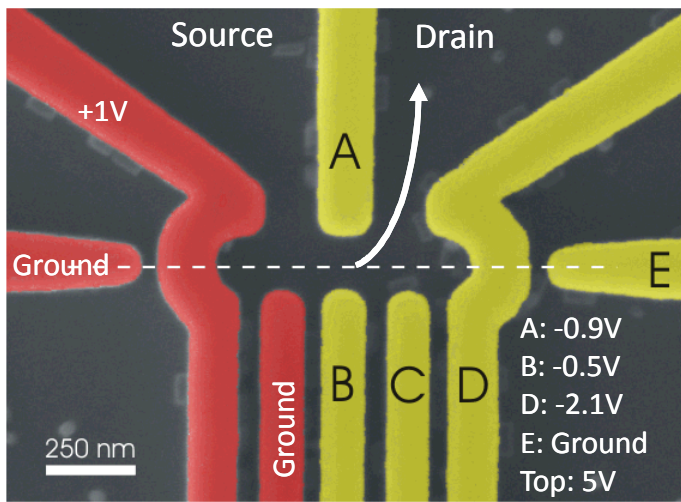
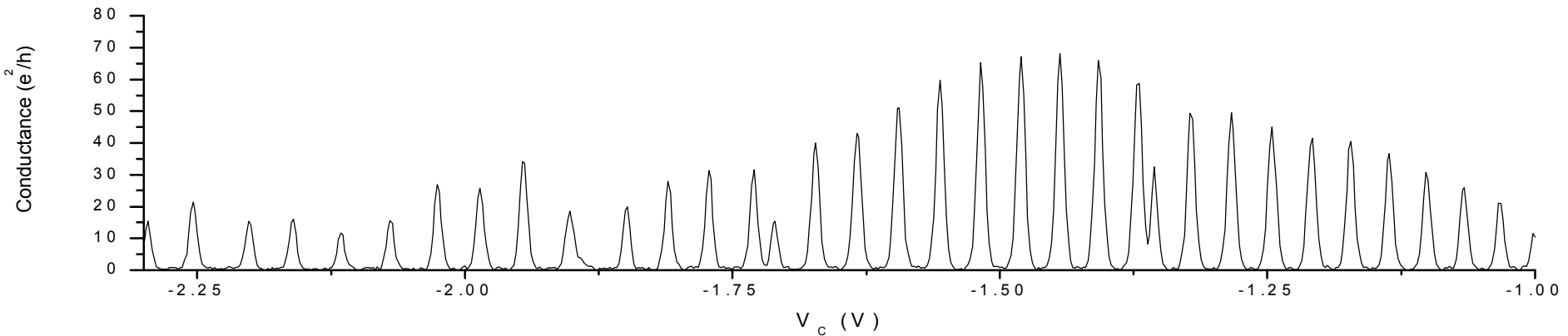
Fabrication

Electrostatically gated quantum dots and electrometry

Donor devices

Next steps: yield and single electrons

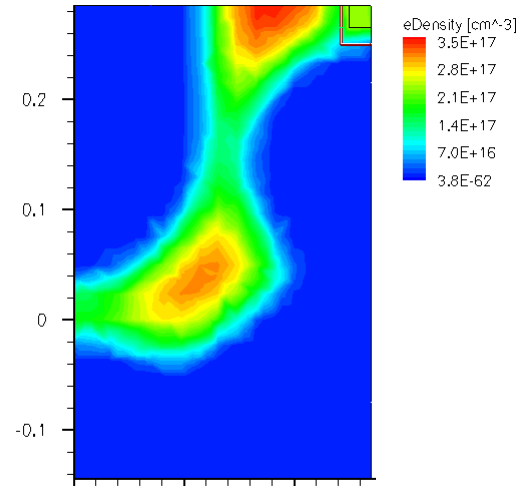
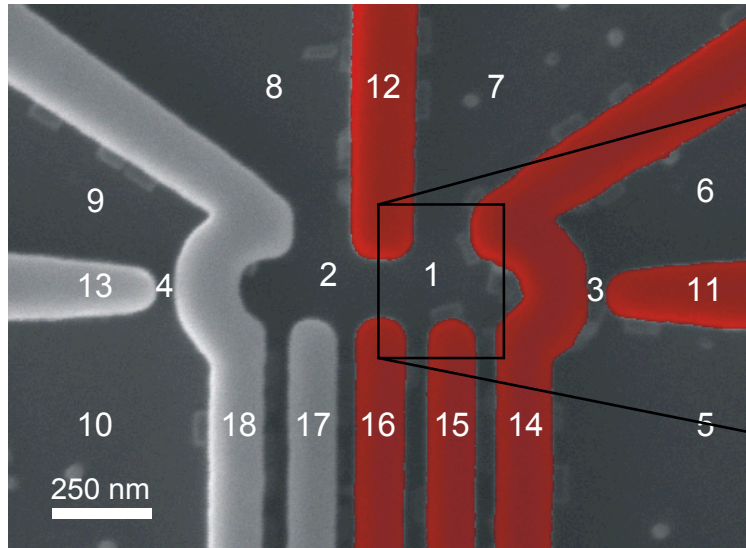
Result of reduced defects



Nordberg et al., PRB (2009)

0.4% drift in oscillation period per day

Modeling quantum dot structures

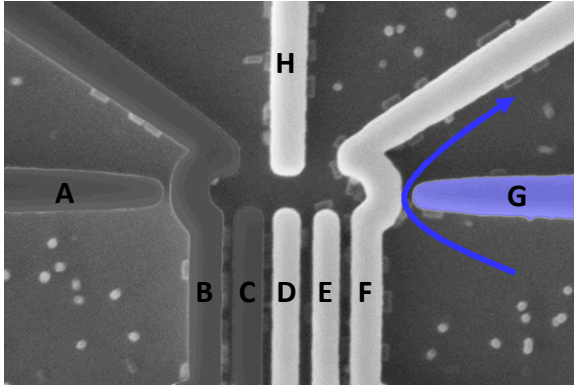


Capacitive Matrix:

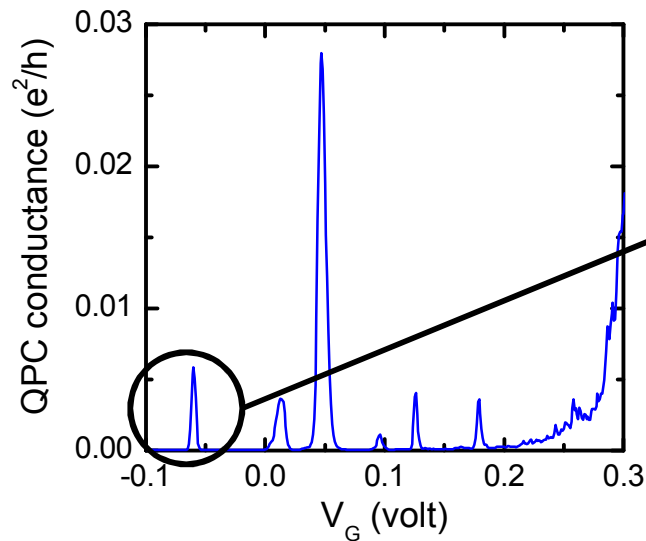
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	73.498	11.488	0.092	0.028	2.805	1.558	14.712	2.698	0.800	1.601	0.295	6.217	0.150	7.186	3.373	3.242	1.050	1.386	14.818
2	11.488	73.421	0.028	0.092	1.608	0.801	2.700	14.475	1.567	2.816	0.150	6.210	0.297	1.391	1.053	3.260	3.379	7.199	14.882
3	0.092	0.028	7.869	0.001	1.649	1.434	0.288	0.077	0.039	0.080	1.305	0.024	0.007	2.014	0.079	0.051	0.028	0.045	0.629
4	0.028	0.092	0.001	7.922	0.080	0.039	0.077	0.288	1.433	1.856	0.007	0.024	1.322	0.045	0.028	0.051	0.079	2.028	0.643
5	2.805	1.608	1.649	0.080	475.201	34.803	10.974	4.918	3.298	7.943	40.337	1.142	0.647	45.041	8.523	5.480	2.935	4.032	298.983
6	1.558	0.801	1.434	0.039	34.803	319.262	22.655	3.507	1.809	3.296	37.377	0.929	0.322	56.828	1.479	1.312	0.869	1.757	148.423
7	14.712	2.700	0.288	0.077	10.974	22.655	290.716	19.226	3.506	4.916	1.951	32.096	0.565	49.103	1.662	1.676	1.195	3.449	120.043
8	2.698	14.475	0.077	0.288	4.918	3.507	19.226	290.588	22.630	10.977	0.565	32.150	1.953	3.457	1.198	1.678	1.661	49.169	119.964
9	0.800	1.567	0.039	1.433	3.298	1.809	3.506	22.630	319.124	34.873	0.322	0.929	37.419	1.758	0.870	1.314	1.478	56.724	148.285
10	1.601	2.816	0.080	1.696	7.943	3.296	4.916	10.977	34.873	475.438	0.646	1.142	40.398	4.030	2.932	5.476	8.506	45.123	299.031
11	0.295	0.150	1.305	0.007	40.337	37.377	1.951	0.565	0.322	0.646	569.446	0.142	0.059	9.174	0.359	0.296	0.186	0.334	475.955
12	6.217	6.210	0.024	0.024	1.142	0.929	32.096	32.150	0.929	1.142	0.142	503.061	0.142	1.470	0.355	0.546	0.354	1.457	417.668
13	0.150	0.297	0.007	1.322	0.647	0.322	0.565	1.953	37.419	40.398	0.059	0.142	569.012	0.335	0.187	0.297	0.360	9.155	475.446
14	7.186	1.391	2.014	0.045	45.041	56.828	49.103	3.457	1.758	4.030	9.174	1.470	0.335	1350.500	110.369	4.914	1.980	2.398	1049.083
15	3.373	1.053	0.079	0.028	8.523	1.479	1.662	1.198	0.870	2.932	0.359	0.355	0.187	110.369	365.775	94.507	2.782	1.976	134.150
16	3.242	3.260	0.051	0.051	5.480	1.312	1.676	1.678	1.314	5.476	0.296	0.546	0.297	4.914	94.507	381.870	94.478	4.905	158.447
17	1.050	3.379	0.028	0.079	2.935	0.869	1.195	1.661	1.479	8.506	0.186	0.354	0.360	1.980	2.782	94.478	365.298	110.398	133.618
18	1.386	7.199	0.045	2.028	4.032	1.757	3.449	49.169	56.724	45.123	0.334	1.457	9.155	2.398	1.976	4.905	110.398	1351.939	1050.347
19	14.818	14.882	0.629	0.643	298.983	148.423	120.043	119.964	148.285	299.031	475.955	417.668	475.446	1049.083	134.150	158.447	133.618	1050.347	5060.414

Gate	Model	Measured
B-Q	40.2aF	48.1aF
C-Q	16.4aF	14.7aF
D-Q	16.9aF	11.2aF
E-Q	16.4aF	14.1aF
F-Q	40.2aF	48.1aF
H-Q	16.7aF	20.8aF

Disorder dots in the point contacts

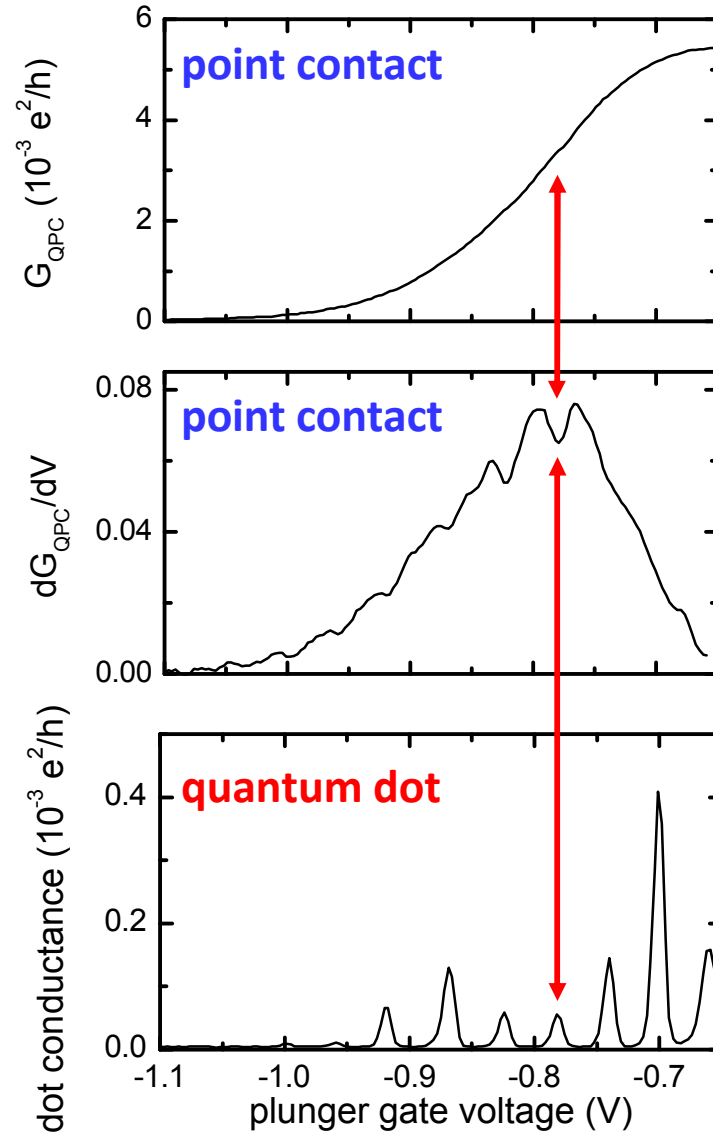
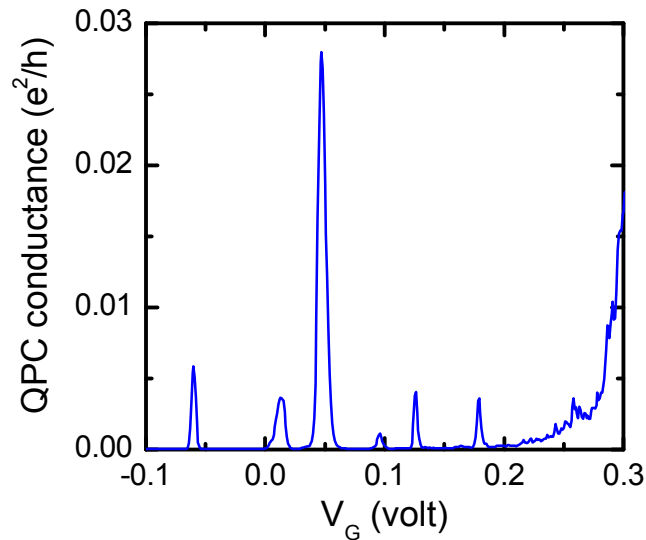
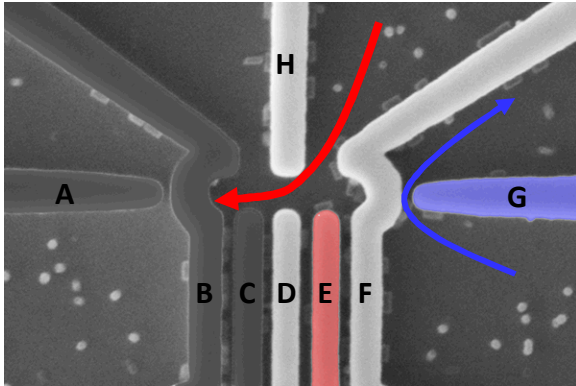


Quantum point contact conductance

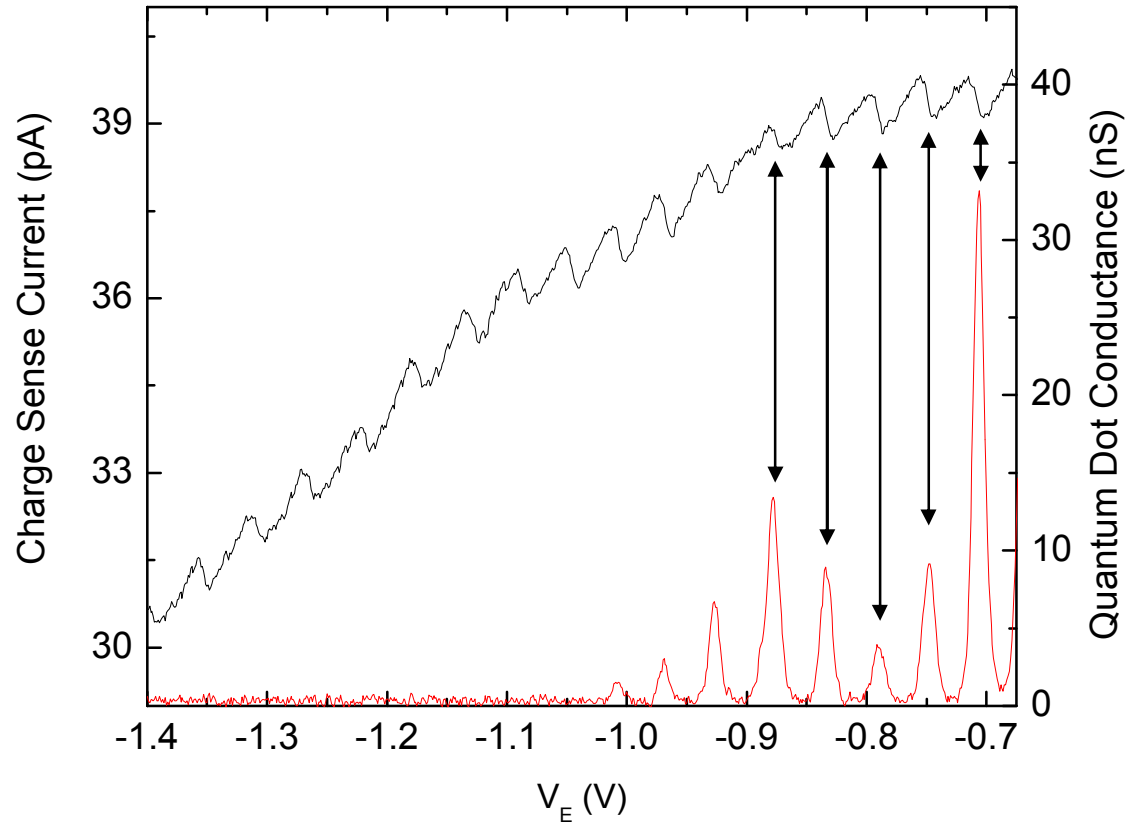
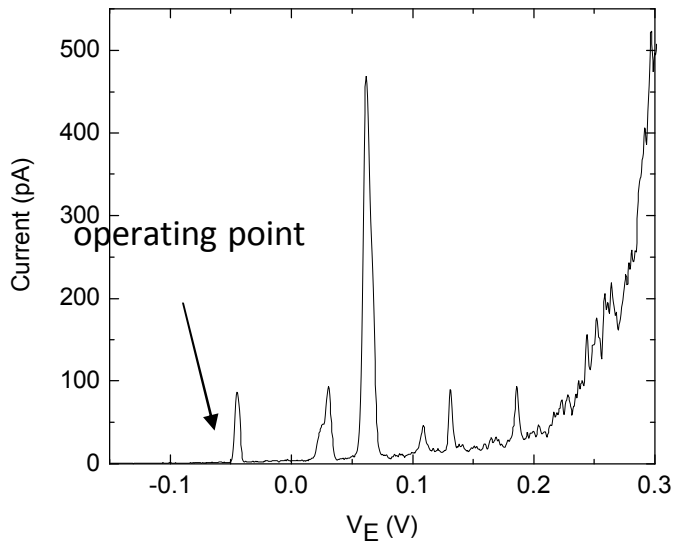
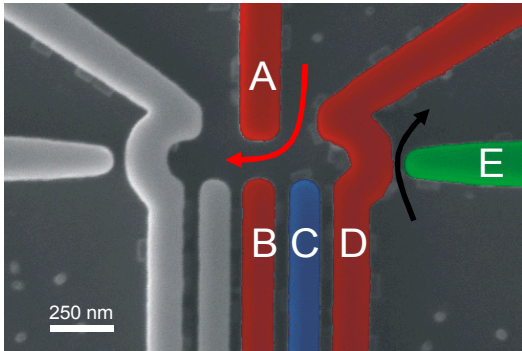


This peak is a disorder dot in the barrier, and is the most stable of the peaks shown here.

Charge sensing a dot with a point contact



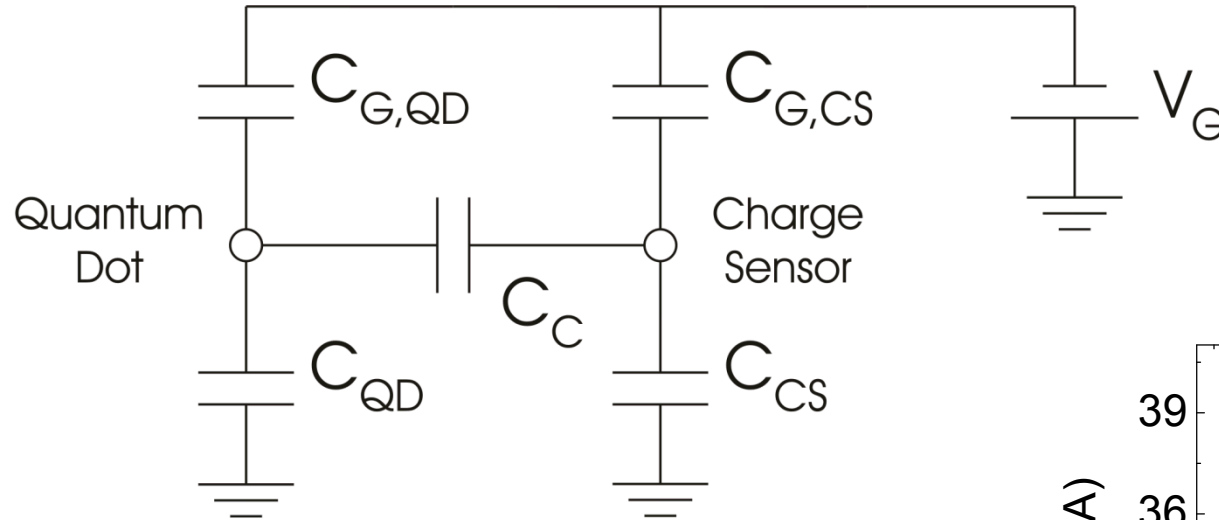
Charge sensing with compensation



As V_C ramps from -0.7 V to -1.4 V, V_E is smoothly ramped from -50.57 mV to -42.46 mV.

Nordberg et al., APL 95, 202102

Capacitance model for electrometer sensitivity



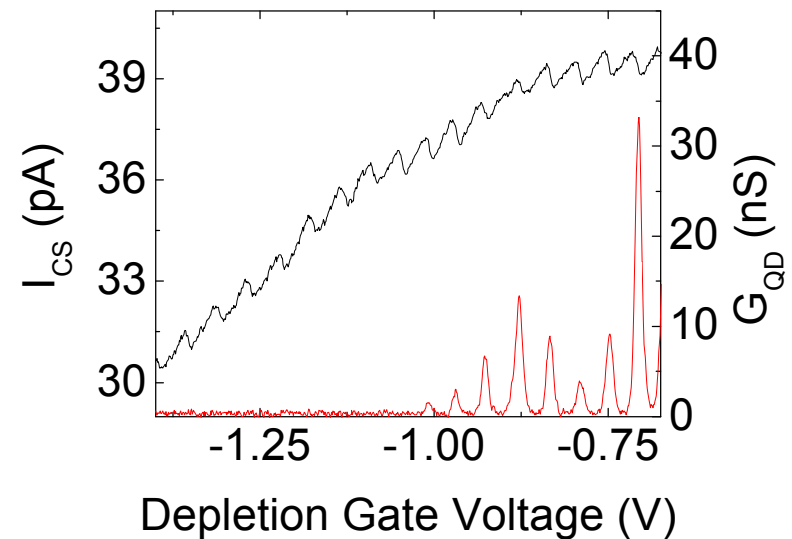
Experiment:

$$C_C = 0.09 \pm 0.01 \text{ aF}$$

Capacitive Model:

$$C_C = 0.092 \text{ aF}$$

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2											0.150	6.210	0.297	1.391	1.053	3.260	3.379	7.199	14.882
3											1.305	0.024	0.007	2.014	0.079	0.051	0.028	0.045	0.629
4											0.007	0.024	1.322	0.045	0.028	0.051	0.079	2.028	0.643
5											40.337	1.142	0.647	45.041	8.523	5.480	2.935	4.032	298.983
6											37.377	0.929	0.322	58.828	1.479	1.312	0.869	1.757	146.423
7											1.951	32.096	0.585	49.103	1.862	1.676	1.195	3.449	120.043
8											0.585	32.150	1.953	3.457	1.198	1.678	1.651	49.189	119.984
9											0.322	0.929	37.419	1.758	0.870	1.314	1.479	56.724	148.285
10											0.646	1.142	40.398	4.030	2.932	5.476	8.506	45.123	299.031
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16											0.296	0.546	0.297	4.914	94.507	381.870	94.478	4.905	158.447
17											0.186	0.354	0.360	1.980	2.782	94.478	365.298	110.398	133.618
18											1.386	7.199	0.045	2.028	4.032	7.157	3.449	49.169	56.724
19											14.818	14.882	0.629	0.643	298.983	148.423	120.043	119.984	148.285



- Using measured gate capacitances, the charge sense signal magnitude, and dI/dV_G , C_C can be found experimentally
- Confidence exists that we can predict the magnitude of a charge sense signal in similar geometries with a capacitive simulation

Outline

MOS quantum dots for quantum computing

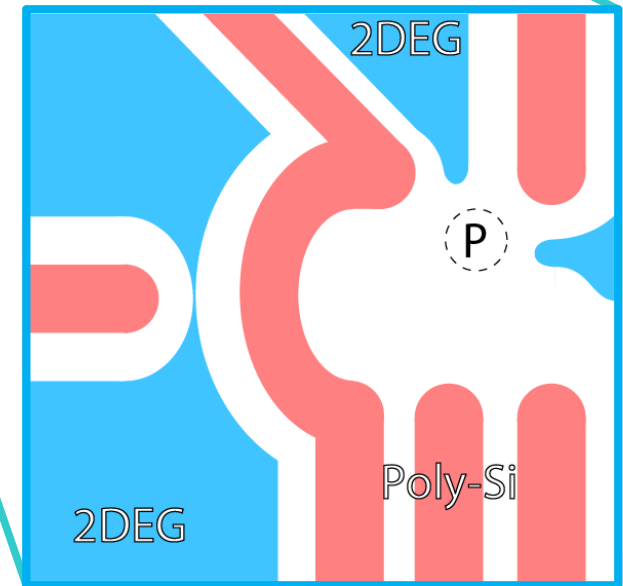
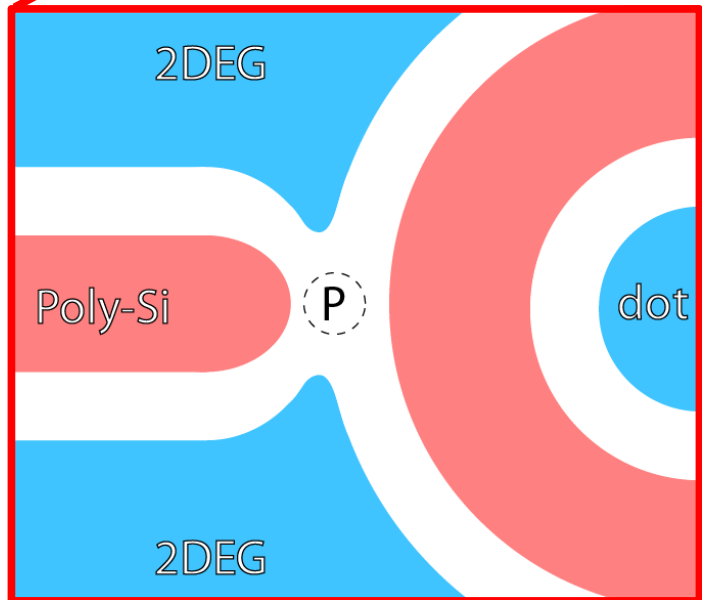
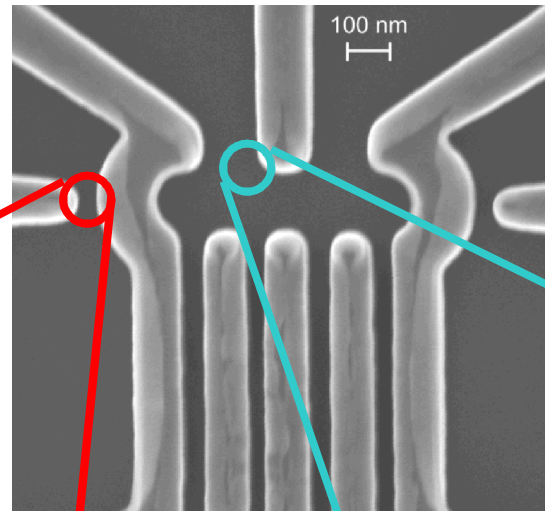
Fabrication

Electrostatically gated quantum dots and electrometry

Donor devices

Next steps: yield and single electrons

Donor – DQD devices



Changes to standard DQD process

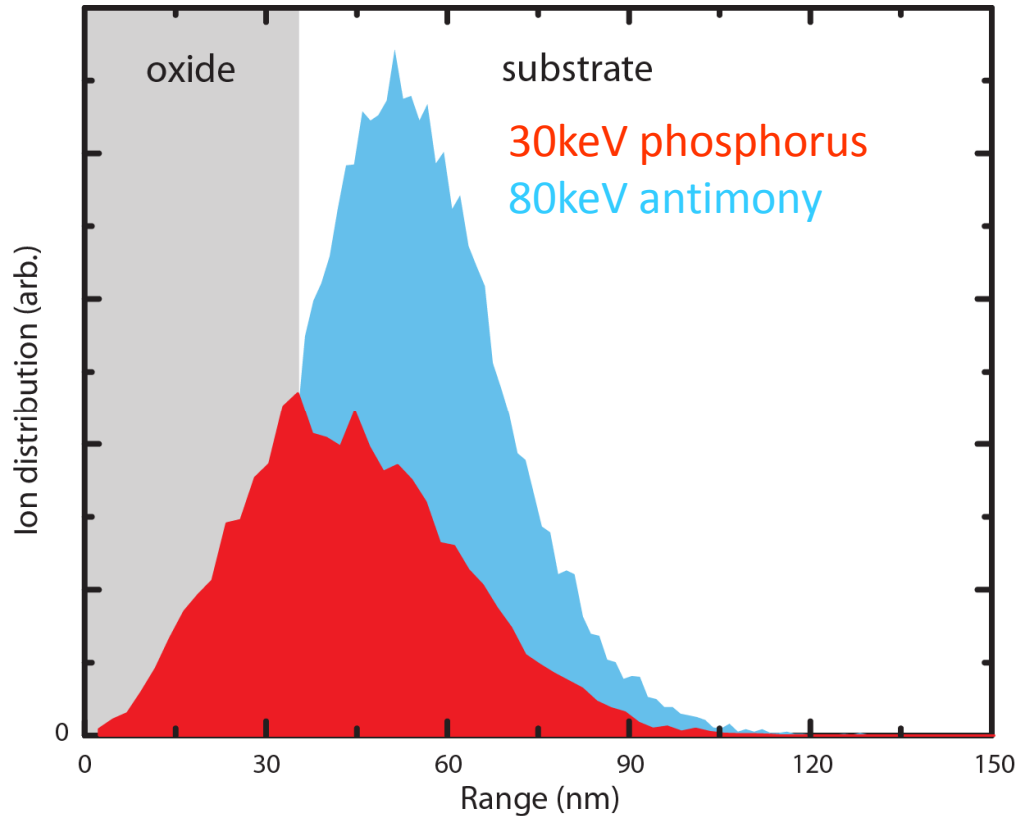
DQD process

- MDL processing
- E-beam lithography
- Poly-Si etch
- Strip metal
- Poly-Si reoxidation
- Deposit ALD Al_2O_3
- Etch via holes
- Deposit top gate and contact pads

Donor-DQD process

- MDL processing
- E-beam lithography
- Poly-Si etch
- EBL for implant window
- Donor implantation
- Strip metal
- Poly-Si reoxidation?
- Implant activation anneal
- Deposit ALD Al_2O_3
- Etch via holes
- Deposit top gate and contact pads

Implanted donor distribution



Donor-DQD process

- MDL processing
- E-beam lithography
- Poly-Si etch
- EBL for implant window
- Donor implantation
- Strip metal
- Poly-Si reoxidation?
- Implant activation anneal
- Deposit ALD Al_2O_3
- Etch via holes
- Deposit top gate and contact pads

Phosphorus:

- Less implant damage
- Activates at low temp (800°C)
- High diffusivity
- High straggle

Antimony:

- More implant damage
- Activates at higher temp ($900+^\circ\text{C}$)
- Low diffusivity
- Low straggle

Implant activation anneal

Diffusion lengths for 900 °C anneals.

	30 seconds	24 minutes
Phosphorus	30 nm	200 nm
Antimony	0.8 nm	6 nm

Donor-DQD process

- MDL processing
- E-beam lithography
- Poly-Si etch
- EBL for implant window
- Donor implantation
- Strip metal
- Poly-Si reoxidation?
- Implant activation anneal
- Deposit ALD Al₂O₃
- Etch via holes
- Deposit top gate and contact pads

Poly-Si reoxidation is 24 minutes at 900 °C.

Implant activation anneal is 30 seconds at 900 °C.

Outline

MOS quantum dots for quantum computing

Fabrication

Electrostatically gated quantum dots and electrometry

Donor devices

Next steps: yield and single electrons

Outlook for single electron

Sample 131 can be operated with lower electron number.

Capacitance to top gate provides dot size

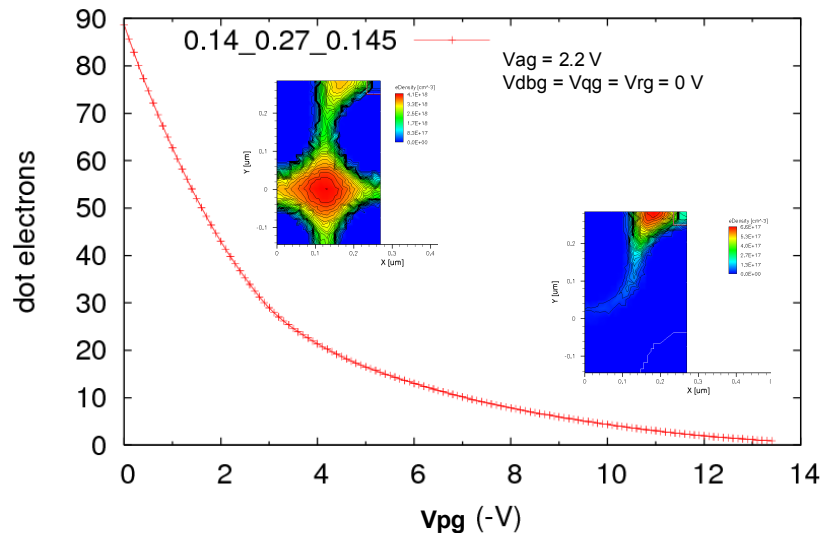
$$C = 14.7 \text{ aF}$$

$$d = 187 \text{ nm (assuming circular dot)}$$

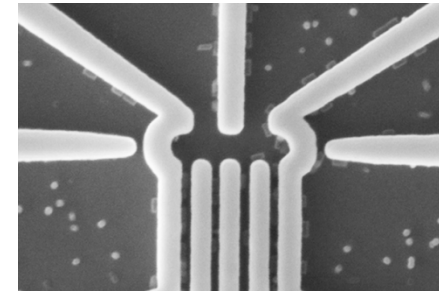
$$N \sim 400 \text{ electrons (assuming 2DEG density)}$$

TCAD modeling of 131

GateOxThk=35nm, Al₂O₃Thk=60nm, PolyThk=200nm

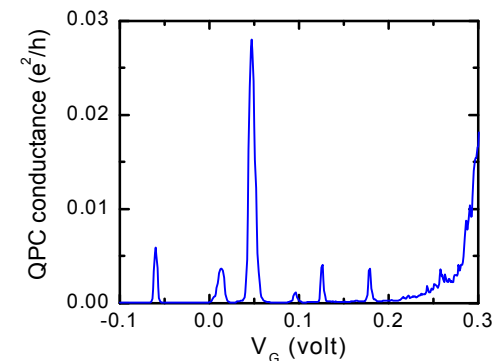


Gate voltage and risk

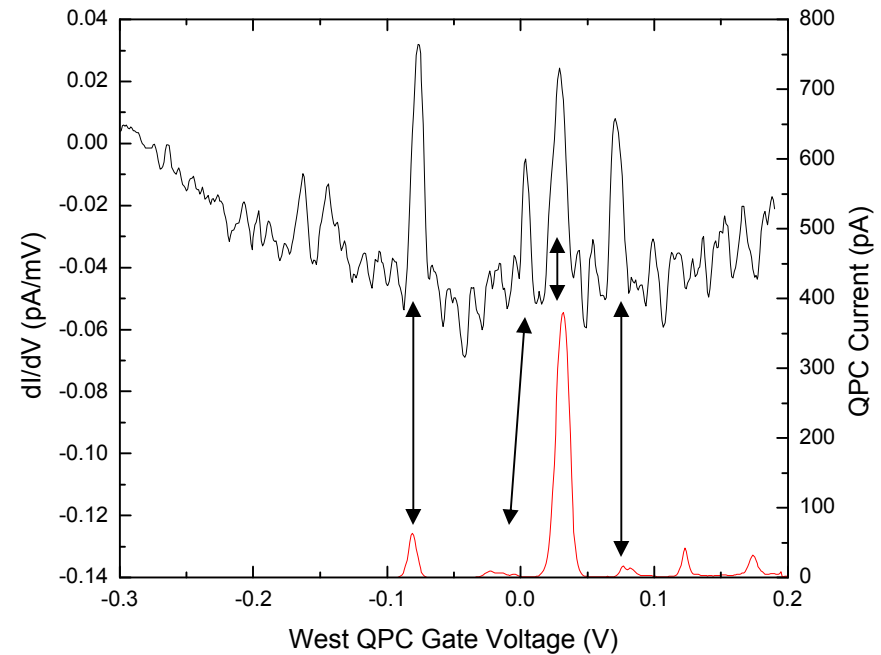
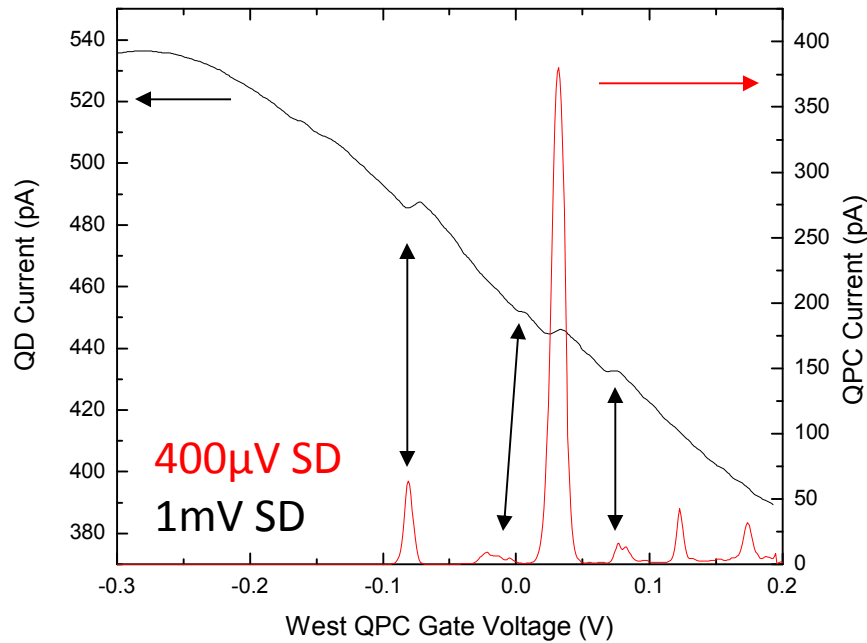


Fewer electrons requires larger voltage on depletion gates.

Disorder dots for low electron number?

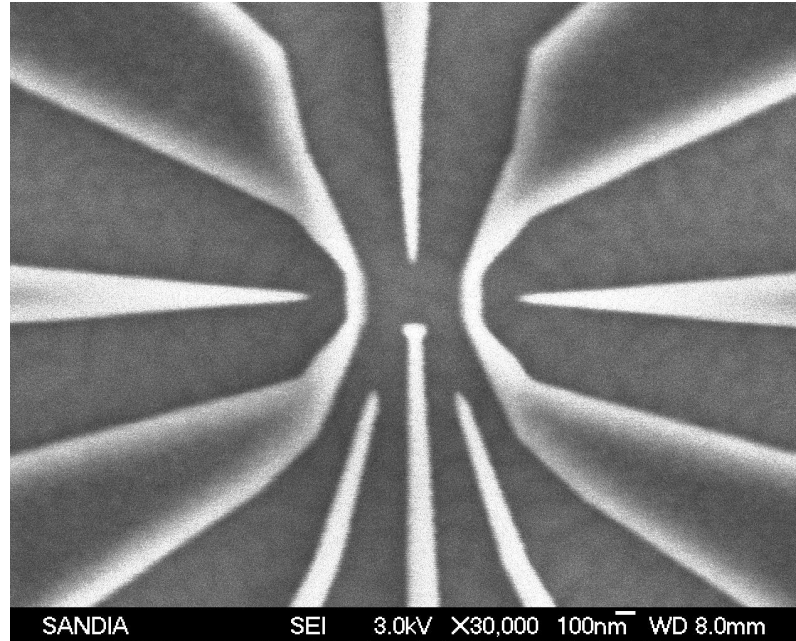


Reverse charge sensing



Capacitive coupling between the external QPC gate and the main QD is so small, that gate compensation on the QD is *almost* unnecessary
 Noisy, no parallel field & broad CB line widths => warm fridge and alter wiring

DQD designs for either single or double gates

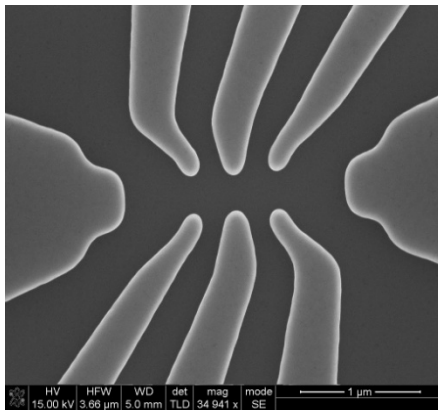


- Recent designs minimize size
- Can be operated in single poly (minimal process) for diagnostics
- Consistent with donor implant

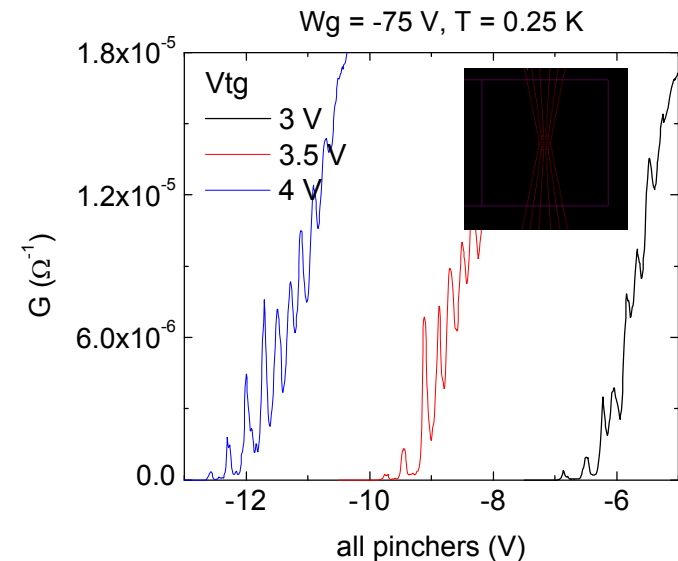
Silicon fab quantum dots

- One path to improve yield is to minimize back-end processing
- Large (180 nm features) quantum dots from MDL appear to have very repeatable gates and show Coulomb blockade.
- EBL is approved for the MDL silicon fab.

0.18 μm front-end lithography



Coulomb blockade in MDL dot

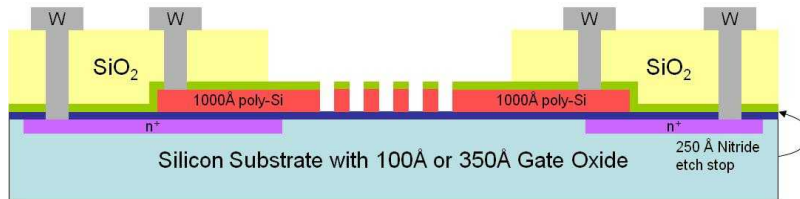


additional supporting slides

Back-end fabrication details: depletion gates



Device window opens to the SiN_x etch stop.

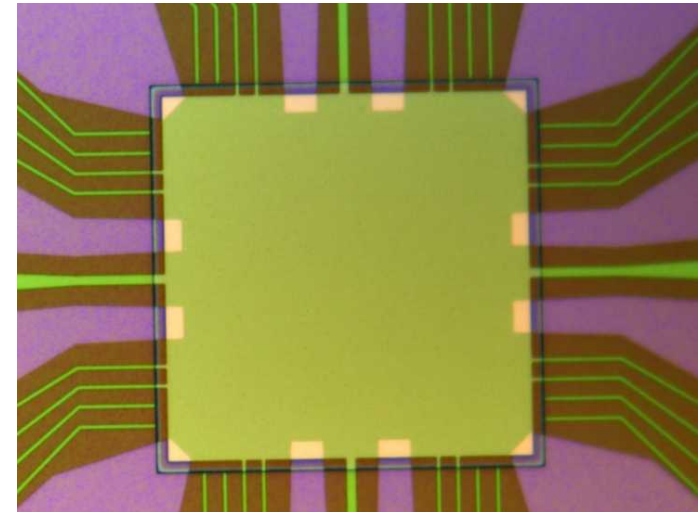


300nm negative EBL resist patterned to form one of the Qubit structures

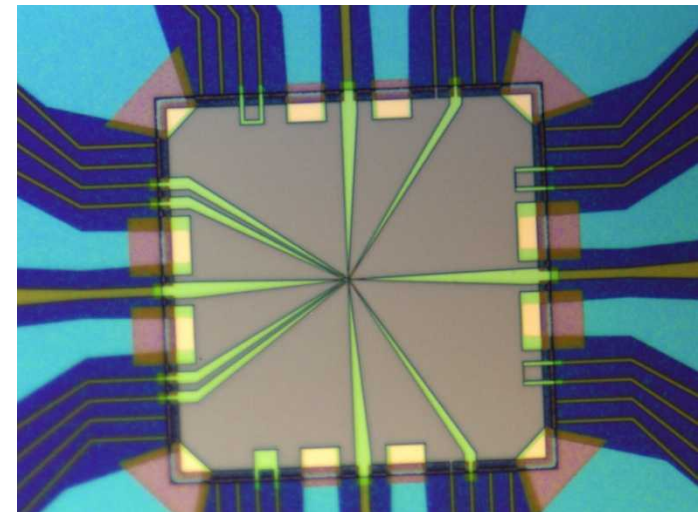
CHF_3 used to etch SiN_x down to poly-Si

HBr used to etch poly-Si down to gate oxide

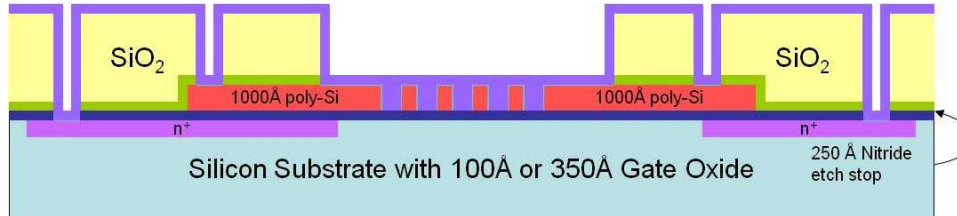
Acetone spray used to clear residual EBL resist



← 100 µm →



Back-end fabrication details: anneals, ALD and top gate

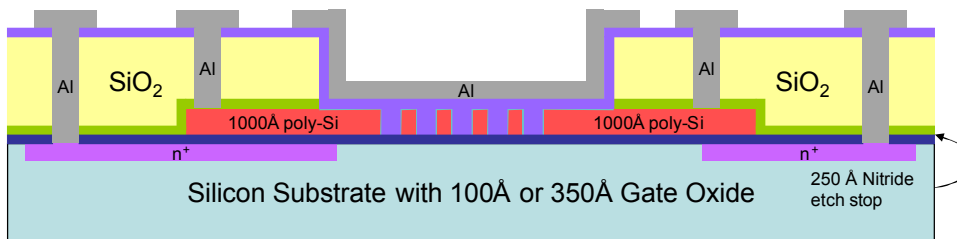


H₂O₂ removes W down to poly-Si pads and n⁺ contacts

H₃PO₄ removes Si₃N₄ in device region

900°C 24min re-oxidation in dry O₂

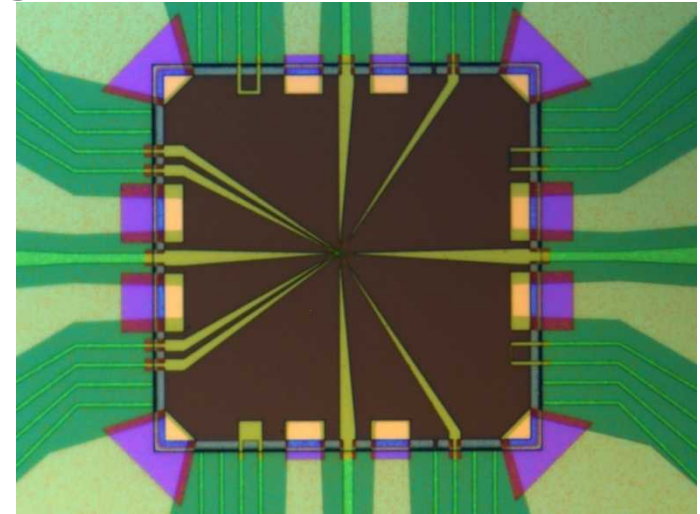
600Å Al₂O₃ deposited via ALD over entire surface (200°C process)



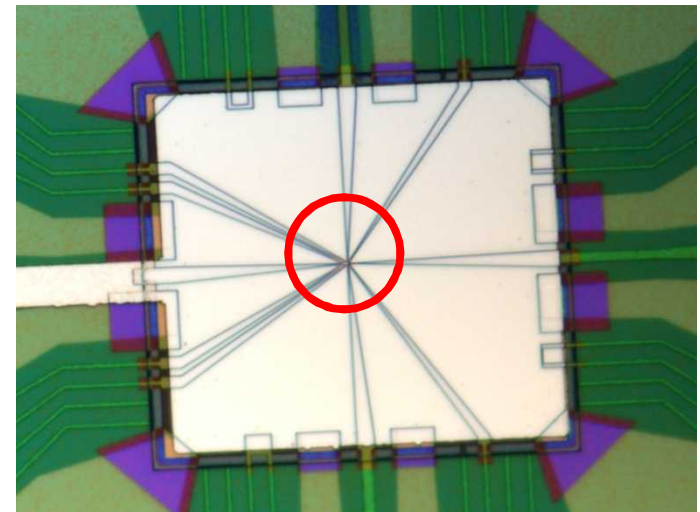
1000Å Aluminum blanket metallization patterned with etch-back in field to form Top Gate

Al₂O₃ patterned for BOE etch of ALD above poly-Si and n⁺ bond pads

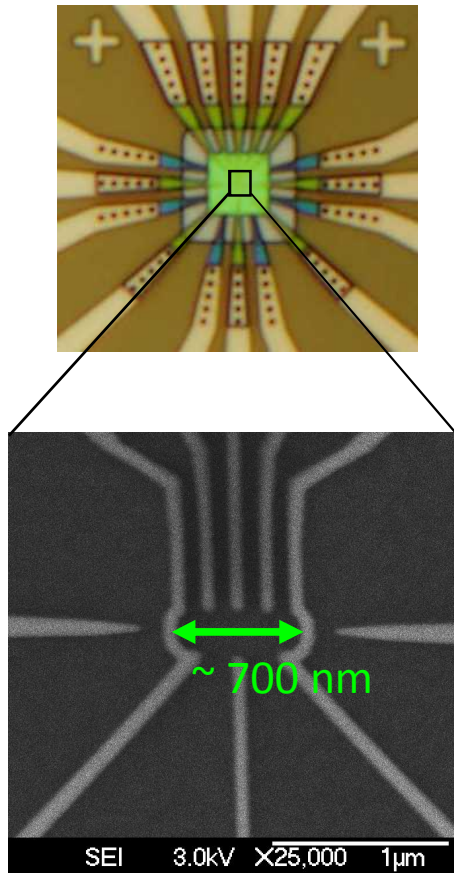
1000Å Aluminum deposited to form bond pads for vias



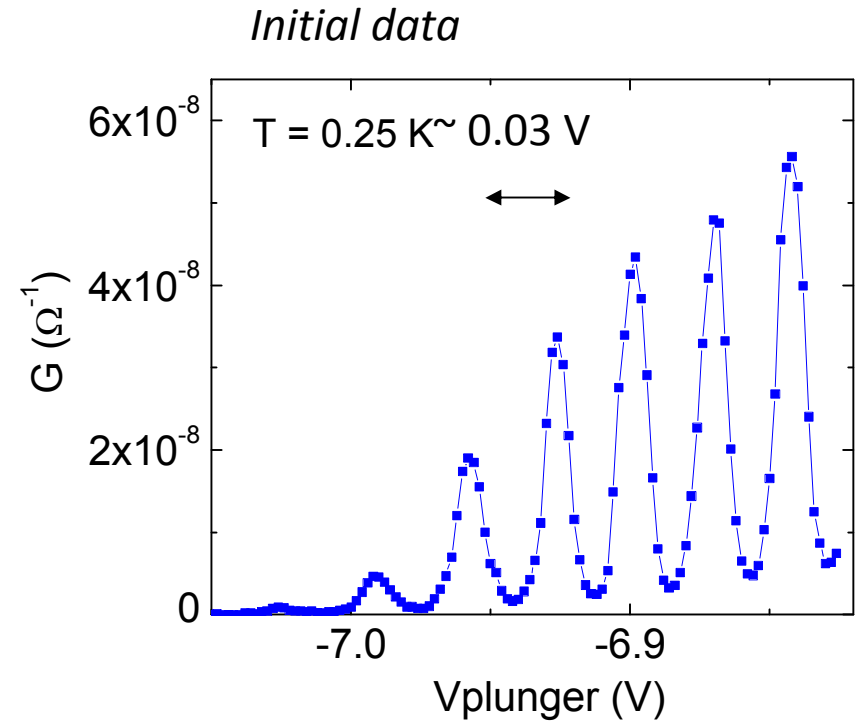
← 100 μm →



RF compatible nanoelectronics

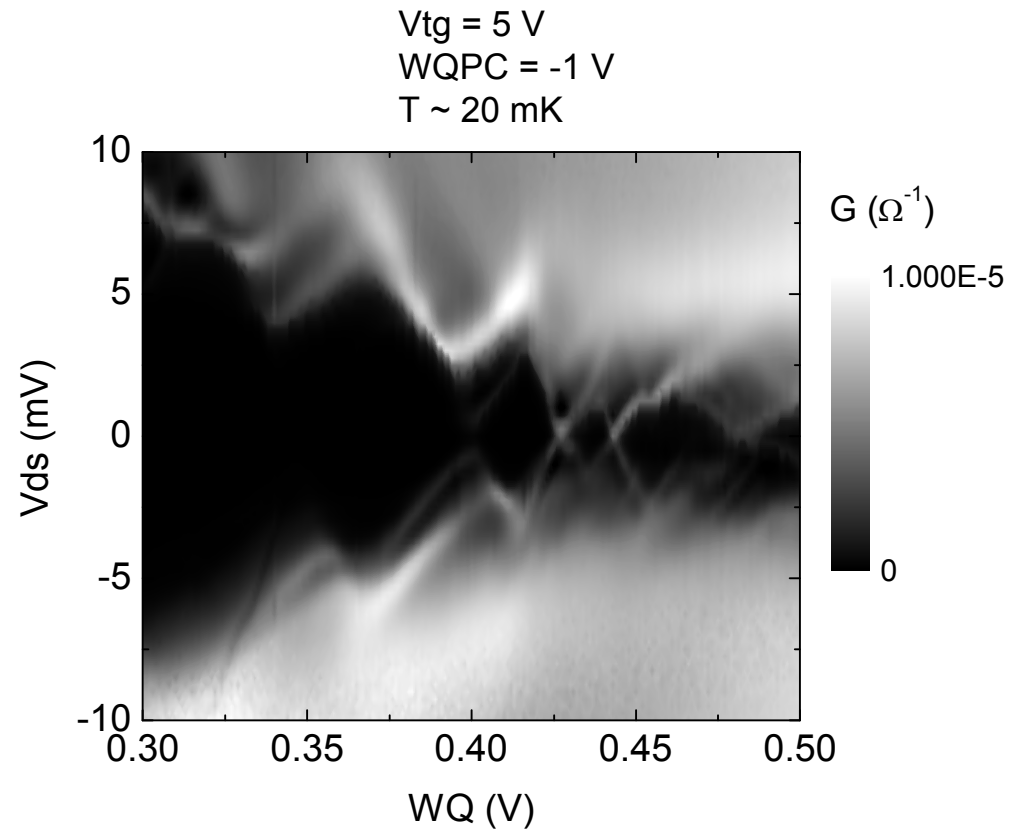
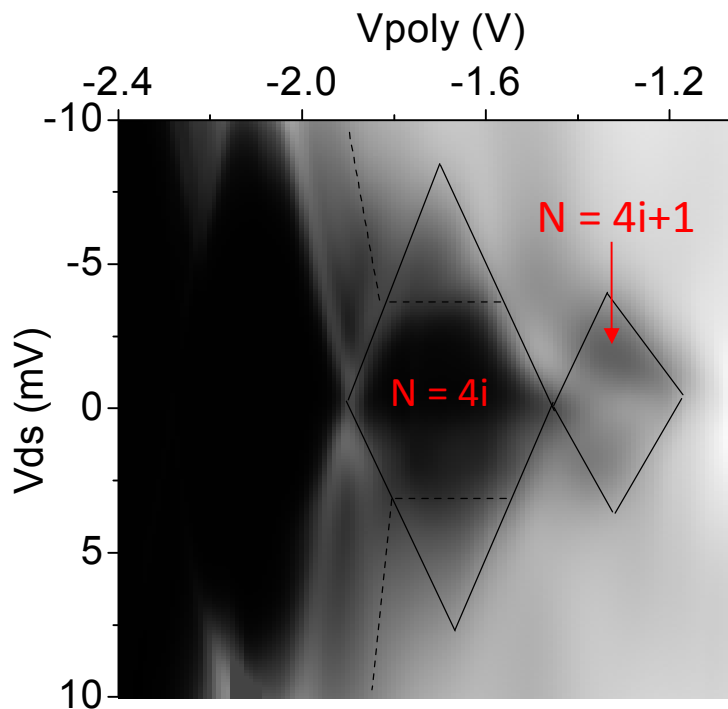


Greg Ten Eyck,
Joel Wendt,
Denise Tibbetts,
Beverly Silva



Minimizing the stray capacitance in an rf-device requires much smaller sizes. We have developed a front-end structure specifically for rf experiments.

Disorder dots diamonds



Electron temperature in quantum dots

