SAND2010-5523C

Sandia-Xilinx Virtex FPGA SEU Experiment on the International Space Station

Principal Investigators: Gayle Thayer, Jeff Kalb

Lead Electrical Engineer: David Bullington

Team Members: Ethan Blansett, Dennis Clingan, Jim Daniels, Jonathon Donaldson, Tracie Durbin, David Heine, David Lee, MyThi To, Brandon Witcher, and Chris Wojahn

SEE Symposium

April 12-14, 2010

Sponsored by the National Nuclear Security Administration
Office of Non-Proliferation Research and Development, NA-22

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

ISS and Shuttle imagery Courtesy of NASA

NNSA National Nuclear Security Administration

UNCLASSIFIED
Unlimited Release (SAND 2010-xxxx)

Sandia National Laboratories

Outline

- **MISSE Overview**
  - Background
  - Objectives
  - Environment
- **SEUXSE on MISSE**
  - Architecture
  - Electrical Interface
  - Mechanical and Thermal
  - Experiment Details
  - CONOPS and Data Flow
  - Status
- **Launch and Deployment of MISSE 7**

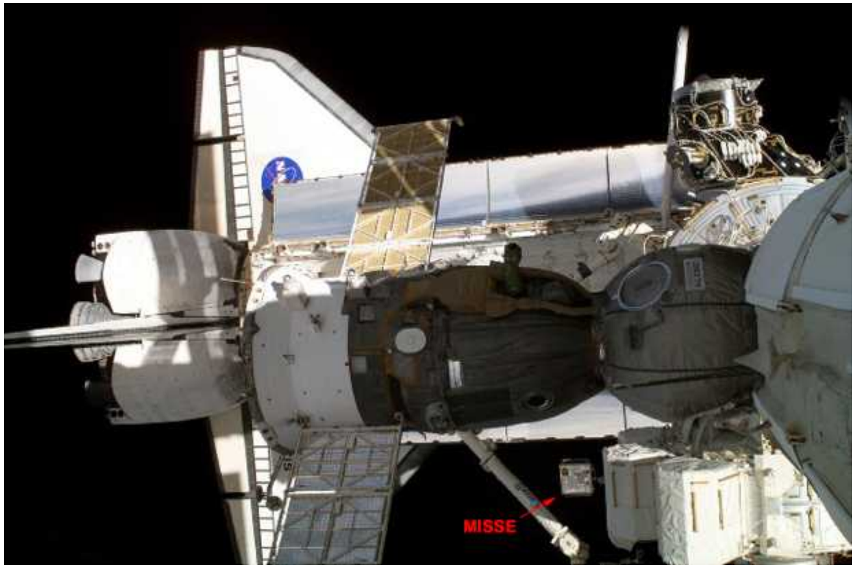
MISSE Overview

- The purpose of the Materials on the International Space Station Experiment (MISSE) is to characterize the performance of new and prospective spacecraft materials and technologies when subjected to the combined effects of the space environment.

- The MISSE program has a rich history and benefits from six previous on-orbit payloads with substantial legacy hardware and design.

MISSE Background

- Experiments up to 2 years on the International Space Station (ISS).
- Launched and returned by Shuttle.
- Initially passive experiments only – combined UV, AO, radiation.
- Active experiments connect to ISS for power, commanding, telemetry.



- MISSE 1 & 2 (AFRL/ML)
  - Passive material exposures
  - Launched 2001, returned 2005
- MISSE 3 & 4 (AFRL/ML)
  - Passive material exposures
  - Launched 2006, returned 2007
- MISSE 5 (NRL)
  - Self-powered with on-board, two-way comm
  - Active solar cell and passive material experiments
  - Launched Aug 2005, returned Sept 2006
- MISSE 6 (AFOSR)
  - Passive and active expts – data loggers
  - Launched March 2008, returned Sept 2009
- MISSE 7 (NRL)
  - Passive and Active experiments (NRL-0602)
  - Launched Nov 2009
- MISSE 8 (NRL)
  - Passive and Active experiments (NRL-0602)
  - Launch scheduled for July 2010

Sandia National Laboratories

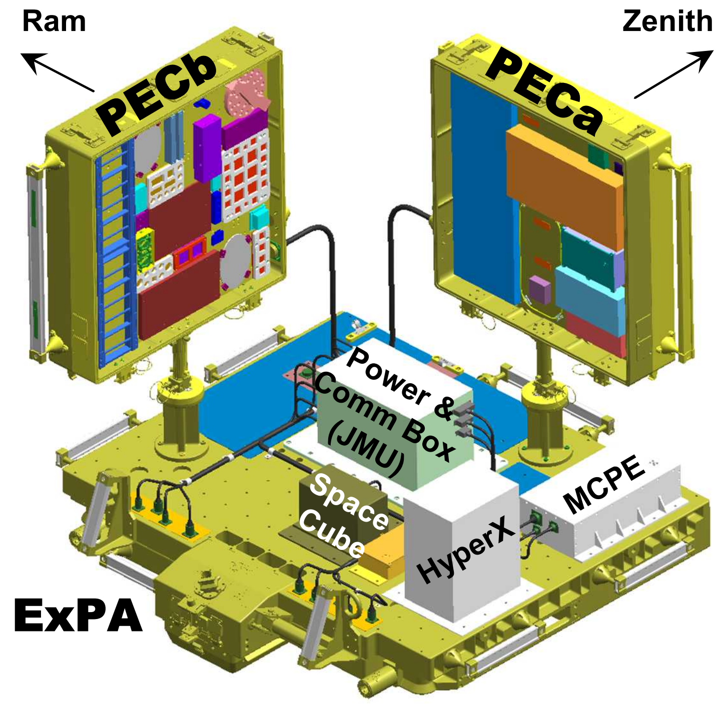
Sandia Contributions to MISSE

- **MISSE 6**
  - Piezoelectric polymer materials experiment
- **MISSE 7**
  - Single Events Upset Xilinx-Sandia Experiment (SEUXSE I)
  - Sandia Passive ISS Research Experiments (SPIRE)
- **MISSE 8**
  - Single Events Upset Xilinx-Sandia Experiment (SEUXSE II)

SEUXSE I & II are architecturally similar with differences highlighted in blue/red colors.

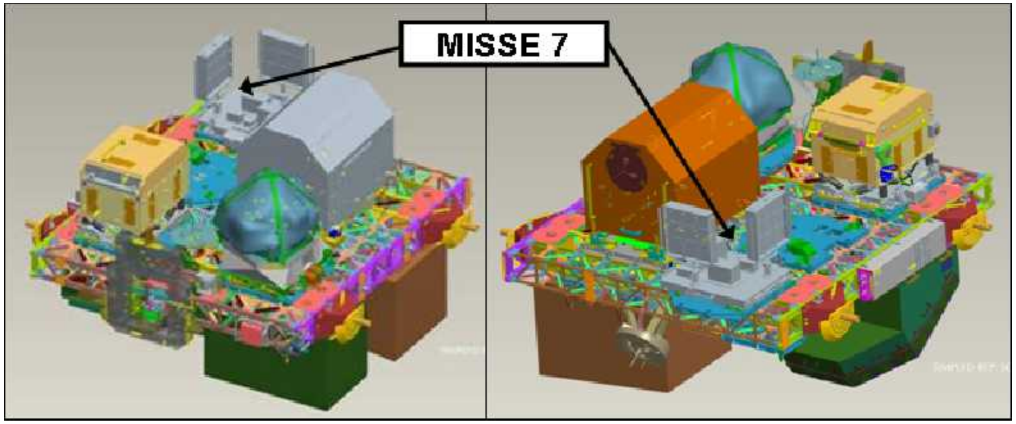
Passive Experiment Container (PEC) and Express Payload Adapter (ExPA)

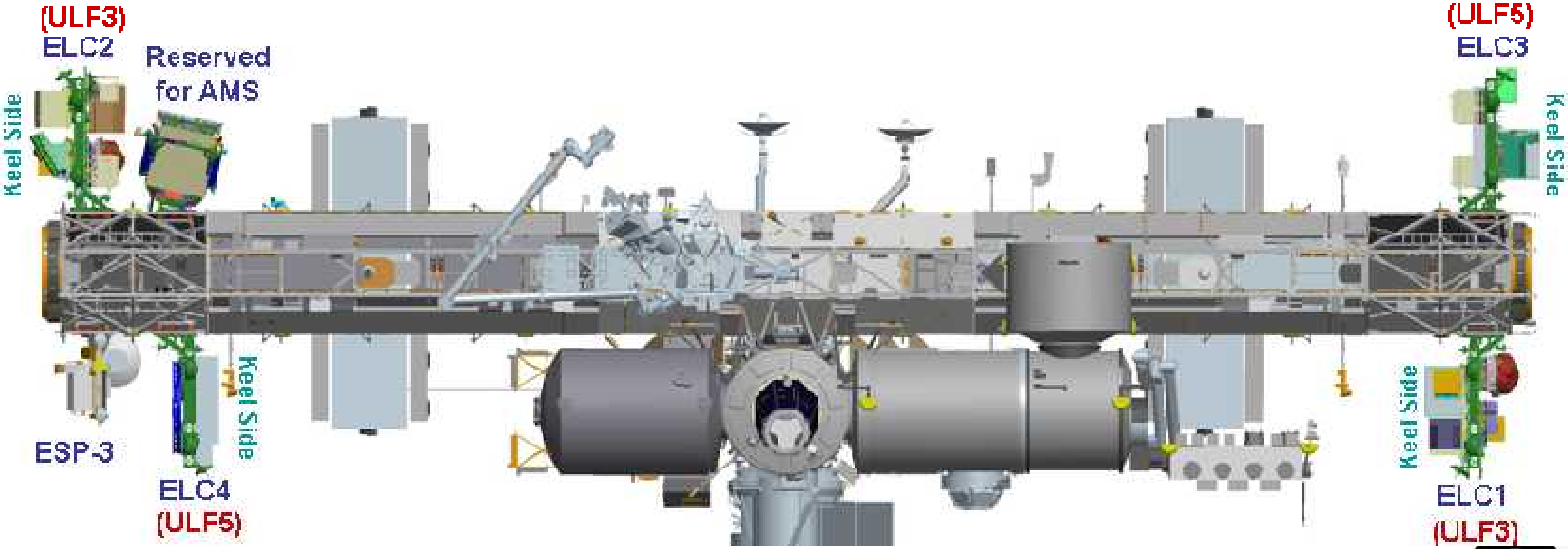
- **MISSE-7 (launched in November 2009) is the first science payload for the Express Logistics Carrier (ELC, not pictured here) program and carries passive and actively powered experiments.**
- **The Express Payload Adapter (ExPA) mounts to the ELC and provides communication and power between experiments and the ISS.**
- **One of two MISSE 7 Passive Experiment Containers (PECs) will be replaced by a MISSE 8 PEC (launch July 2010).**



Express Payload Adapter (ExPA) and Express Logistics Carrier (ELC)

- **These images depict the ExPA mounted to the ELC (right) and the ELC mounted to the ISS (below).**





SEUXSE Objectives

- **Early design, delivery and deployment of technologies relevant to the DOE/NNSA's Joint Architecture Standard (JAS)**
  - Xilinx Virtex-4 and Virtex-5 FPGAs
  - Point-of-Load (POL) power converters
  - Intellectual Property (IP)
  - Demonstrate in LEO space environment
- **Single Event Upset (SEU) detection and characterization using high-density Xilinx Field Programmable Gate Arrays (FPGA)**
- **Record time and bit value of each SEU detected**
  - Continuous scrubbing of Xilinx configuration bits
  - Continuous exercising and monitoring of most functional logic elements within each Xilinx Virtex FPGA
- **Develop relationships with NRL, NASA, Xilinx, BYU and many other academic and industry partners**

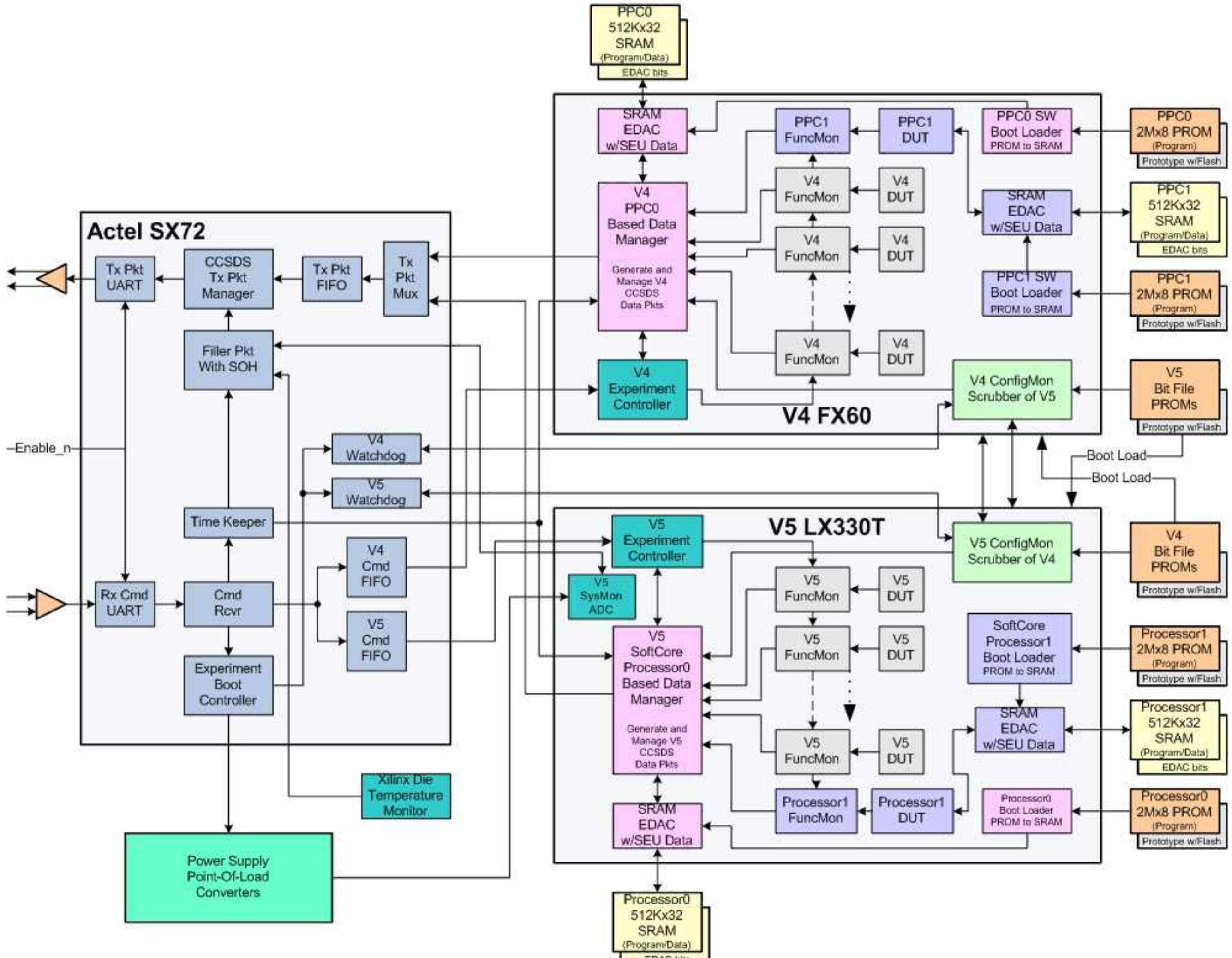
SEUXSE Design

- **Xilinx Virtex 4 XQR4VFX60 FF1152 pin BGA**
  - 50,560 Flip-Flops, 21 Mbit configuration memory
- **Xilinx Virtex 5**
  - SEUXSE I: Commercial LX330T FF1738 pin BGA
    - 207,360 Flip-Flops, 83 Mbit configuration memory
  - SEUXSE II: SIRF FX1 CF1752 pin BGA
    - 81,920 Flip-Flops, 50 Mbit configuration memory
- **Four Embedded Processors Active**
  - 2 silicon based PowerPCs, 2 soft core FPGA fabric based processors
  - 2 Mbytes of SRAM for each processor with EDAC
- **OTP PROMs (XQR17V16) store FPGA configuration and Processor software**
- **Radiation Hardened Point-Of-Load (RHPOL) Power Converters**
  - Sandia custom ASIC
  - First flight use of these devices
  - Two triple output controllers provide six rails
    - (3.3, 2.5, 1.2 (2), 1.0 (2))

Design Details

- **Configuration PROMs:** Boot each device, then are accessed by the other Virtex to provide cross scrubbing of each Xilinx FPGA.
- **V4 embedded PPCs:** One provides software control, self monitor for upsets, and data handling functions; The other runs self monitoring upset codes.
- **V5 Soft-cores:** One MicroBlaze provides software control, self monitor for upsets, and data handling functions; The other soft-core (MicroBlaze/LEON) runs self monitoring upset codes.
- **Detect and report SEU events:** Each Virtex contains several hardware logic element Device-Under-Test (DUT) units with associated Functional Monitors (FuncMon).
- **DUT and Functional Monitor logic elements include:** Block RAM, DCM, DSP48, etc.
- **Actel provides:** Non-volatile hardware interface to ISS command and data channels; Watchdog monitors of each Xilinx FPGA to recover from SEFI modes.
- **V5 System monitor (SEUXSE I):** used to monitor state of health and radiation monitor sensor

SEUXSE Internal Functional Block Diagram



SEUXSE I FPGA Experiments

Virtex 4 FX60

- V5 configuration scrubber
  - Full chip CRC based scrub
  - Compares readback to golden CRC
  - Runs continually
- BRAM error 0→1 (128 BRAM, 2.3 Mb)
- PPC0
  - Experiment controller
  - DSP algorithm running in background
  - External SRAM EDAC experiment
  - Icache and Dcache enabled
- PPC1
  - DSP algorithm running continuously
  - Icache and Dcache enabled
- Digital Signal Processors (DSP48)
  - Dan McMurtrey's XRTC test – static/dynamic
- Digital Clock Managers (DCM)
  - Ray Byrne's XRTC test
  - Lock and clock frequency (golden count)

Virtex 5 LX330T

- V4 configuration scrubber
  - Full chip CRC based scrub
  - Compares readback to golden CRC
  - Runs continually
- BRAM error 0→1 (200 BRAM, 3.6 Mb)
- MicroBlaze0
  - Experiment controller
  - DSP algorithm running in background
  - External SRAM EDAC experiment
  - Cache disabled
- MicroBlaze1
  - DSP algorithm running continuously
  - Cache enabled
- Digital Signal Processors (DSP48E)
  - Dan McMurtrey's XRTC test – static/dynamic
- Digital Clock Managers (DCM)
  - Ray Byrne's XRTC test
  - Lock and clock frequency (golden count)

SEUXSE II FPGA Experiments

Virtex 4 FX60

- V5 configuration scrubber
  - Full chip CRC based scrub (SEUXSE I)
  - Runs once per second (BYU tests)
- BRAM error 0→1 (128 BRAM, 2.3 Mb)
- Two PPCs
  - Experiment controller
  - DSP algorithm running in background
  - External SRAM EDAC experiment
  - Mark Learn's XRTC cache mitigation test
- Dynamic Partial Reconfiguration
- Digital Clock Managers (DCM)
- SpaceWire "target" endpoint
- Digital Signal Processors (DSP48)
  - "Project" algorithms
- Compression/decompression IP engine
- BYU experiments
  - BRAM experiment
  - Smart detector
  - Picoblaze reliability

Virtex 5 FX1 (SIRF)

- V4 configuration scrubber
  - Frame CRC based scrub
  - Runs once per second (BYU tests)
  - Partial Reconfiguration
- BRAM error 0→1 (256 BRAM, 4.6 Mb)
- Two soft-core processors
  - MicroBlaze – Exp controller, SRAM EDAC
  - LEON3 SPARC (Gaisler) - SpW
- Digital Clock Managers (DCM)
- SpaceWire "initiator" endpoint
- Digital Signal Processors (DSP48E)
  - "Project" algorithms
- Compression/decompression IP engine
- BYU experiments
  - BRAM experiment
  - Smart detector
  - Picoblaze reliability
  - BPSK experiment
  - BRAM ECC

SEUXSE FPGA Utilization

SEUXSE I

- 9 Watts (1.8A @ 5V)
- V4 utilization (FX60)
  - 8K (16%) FF
  - 12K (23%) LUT
  - 219 (94%) BRAM
  - 16 (12%) DSP48
  - 253 (43%) IOB
  - 2 DCM
  - 7 BUFG
- V5 utilization (LX330T)
  - 12K (5%) FF
  - 14K (6%) LUT
  - 243 (75%) BRAM
  - 22 (11%) DSP48E
  - 253 (26%) IOB
  - 2 DCM
  - 8 BUFG
- Actel utilization: 72% of SX72A

SEUXSE II

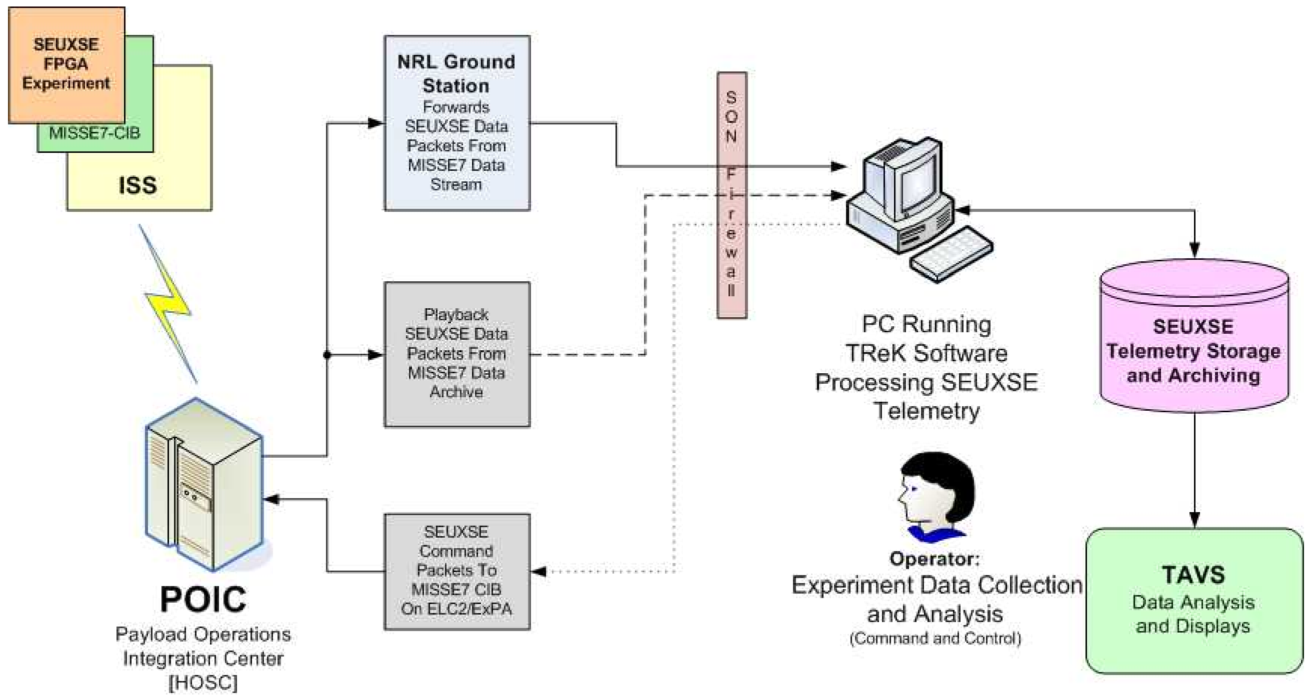
- 11 Watts (2.2A @ 5V)
- V4 utilization (FX60)
  - 21K (38%) FF
  - 30K (58%) LUT
  - 227 (97%) BRAM
  - 102 (79%) DSP48
  - 266 (46%) IOB
  - 2 DCM
  - 11 BUFG
- V5 utilization (FX130T equivalent)
  - 29K (35%) FF
  - 44K (53%) LUT
  - 262 (87%) BRAM
  - 253 (79%) DSP48E
  - 268 (31%) IOB
  - 3 DCM
  - 19 BUFG
- Actel utilization: 72% of SX72A

SEUXSE Electrical Interface

- **ISS connector**
  - Power:
    - Designated converter provided for SEUXSE: +28V to +5V
    - Maximum power budget of 30W (5V @ 6A)
  - Command and Data:
    - SEUXSE interfaces with the Communications Interface Box (CIB)
    - Command and Data links are differential RS485 at 9600 baud
    - Bandwidth requirements:
      - Receive 1.5 Mbytes per day, State-Of-Health (SOH) and event data
      - Most data is SOH as event rates are low
      - SEUXSE I commands only required to recover from a WDT event
      - SEUXSE II will require 2-10 serial configuration commands per month to cycle FPGA Partial Reconfiguration experiments.
    - All Data products are CCSDS formatted packets
      - Internal variable length CCSDS data packets embedded in CIB packet

- **Integration and test connector**
  - For internal use only
  - Has an Aluminum cover plate in the flight configuration

SEUXSE Operations and Data Flow



- **Experiment's CCSDS data packets flow through TReK to Sandia**
  - All data stored and archived for data analysis
- **Sandia obtains data stream directly from NASA POIC/HOSC**
- **Data processed and analyzed at Sandia with TAVS**
- **Future possibility: Sandia Operator sends commands to SEUXSE**

SEUXSE Status

SEUXSE I

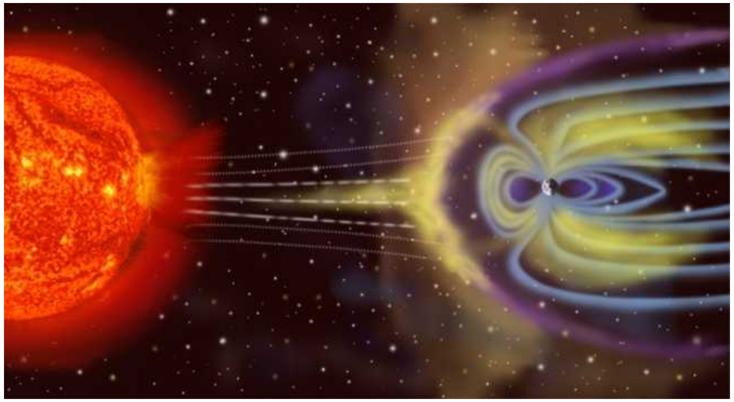
- Launched on STS-129 (11/16/09)
- ELC2 and MISSE 7-ExPA Deployed (11/21/09)
- MISSE7 PEC-A (SEUXSE) and PEC-B Deployed (11/23/09)
- SEUXSE mission started (11/25/09)
  - No processor watchdog time outs
  - V4 has detected 10 BRAM errors
  - V4 has had 13 configuration errors scrubbed by V5 CFGMON.
  - V5 has detected 15 BRAM errors
  - V5 has had 69 configuration errors scrubbed by V4 CFGMON.

SEUXSE II

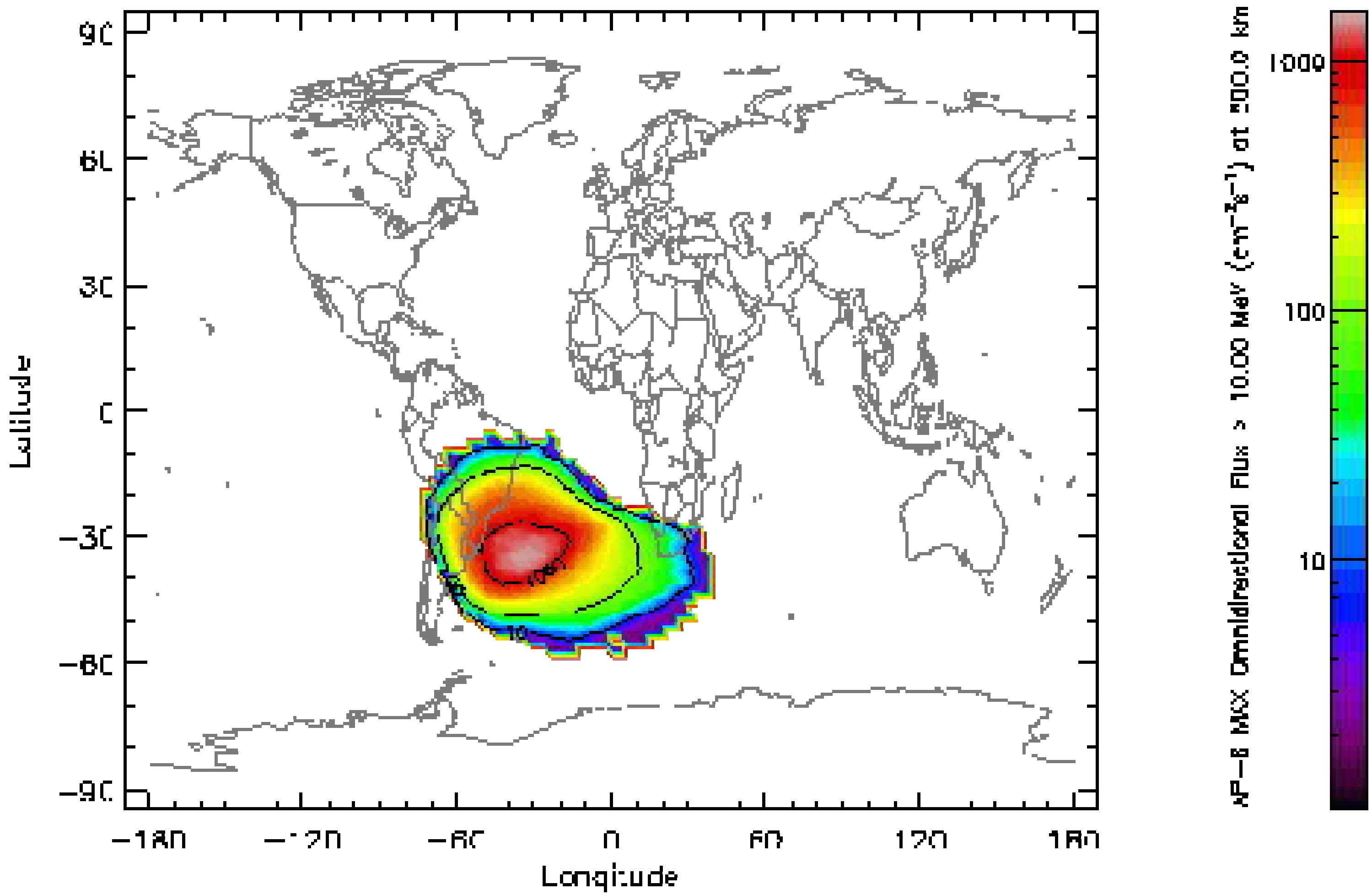
- Delivery to NRL on Feb 1, 2010
- NRL deliver to NASA KSC in April 2010
- Launch in July 2010, when SEUXSE I is returned.

ISS Radiation Environment

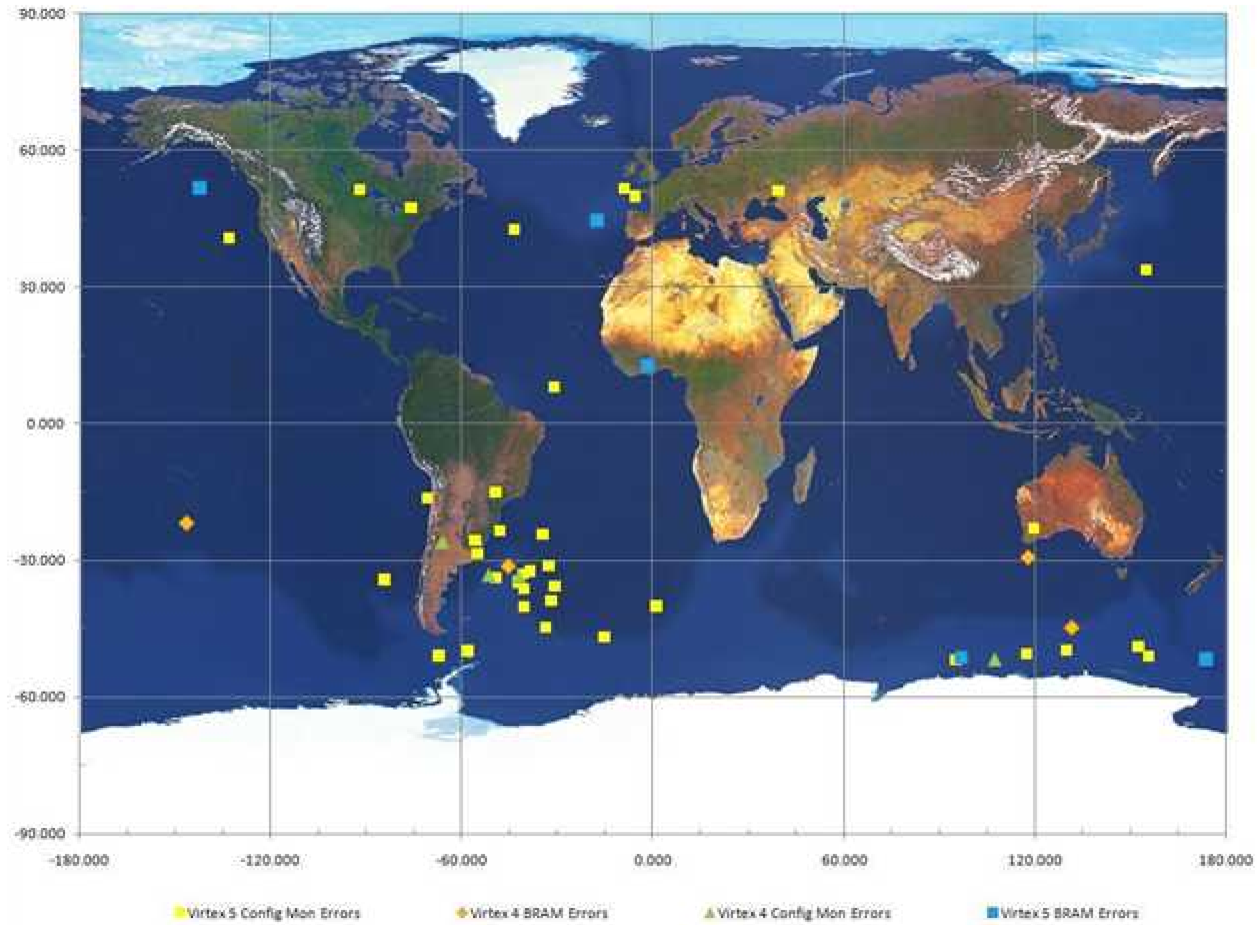
- **ISS Orbit:** 336 km x 347 km, 51.6 deg. inclination
- **Passive experiments TID (no shielding):** ~30 krad/yr total dose at the surface.
- **FPGA experiment TID (100 mil Al shield):** ~30 rad/yr total dose.
- **SEUXSE I predicted error rates: ~325 errors/year (~1 error/day)**
  - **Rad-tolerant Virtex-4 and commercial Virtex-5**
  - **Estimates based on trapped protons**
  - **PECa shielded somewhat by PECb and ISS**
  - **~300 FPGA configuration errors/year**
  - **~25 BRAM errors/year.**
- **Detected SEUs will be correlated to ISS radiation and environmental monitors.**



Boundaries of the South Atlantic Anomaly

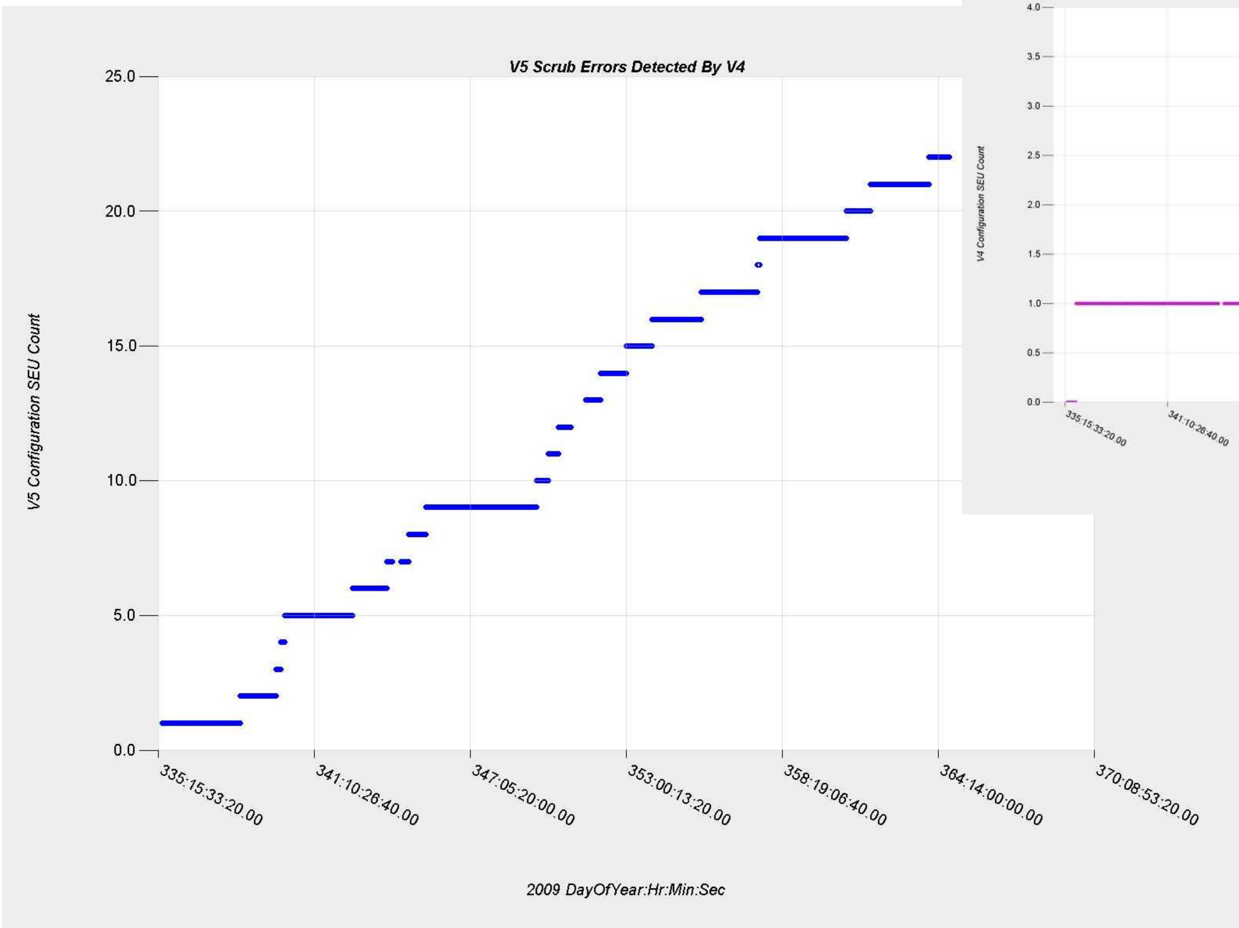


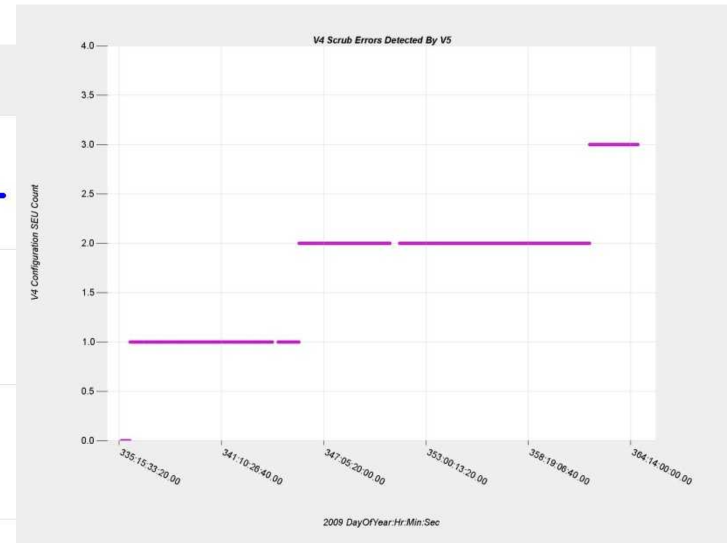
SEUs reported by SEUXSE on MISSE-7



ISS location at SEU events as of February 9, 2010

Virtex-5 and Virtex-4 Configuration Errors





Data for December 2009

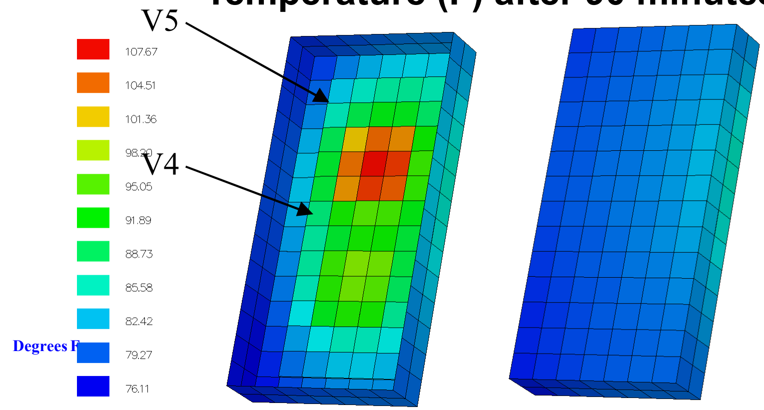
SEUXSE Mechanical and Thermal

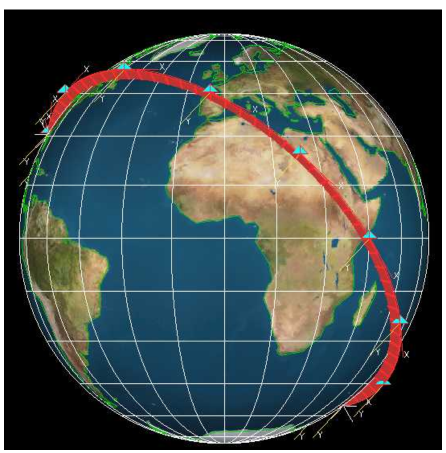
- **Volume is 7 Inches Wide By 14 Inches Long By 1.8 Inches High**
  - Single 18 layer Printed Circuit Board contains all electronics
  - Enclosure mounted with screws through bottom of PEC deck plate
- **Aluminum Enclosure**
  - Alodine surface coating
  - Silver Teflon tape on alodine surfaces (thermal)
- **SEUXSE I has a Carbon-Fiber Composite Lid (Top Face)**
  - 80-mil thick composite top lid mounted in an aluminum frame
    - Low outgassing epoxy with ~8 layers of pre-preg
    - Nickel plating for EMI shielding
    - AZ-400 white paint for passive thermal control (also a materials experiment)
- **SEUXSE II has an Aluminum Lid (better thermal control)**
- **Mass is 5.0/5.2 Pounds**
- **Enclosure has Rounded Edges and Corners for Astronaut Safety**
- **Kick Load analysis was required**
- **Thermal Requirements**
  - Operating Range is 0 to +60C at the baseplate mounting surface (0 to +95C for internal components)
  - Non-Operating Range is -40C to +125C

SEUXSE Thermal Model

Assumptions:
- Housing: 6061-T6, 0.1 inch thick
- Board, nominal, 0.08 inch thick
- V5 – 19 Watts, V4-10 Watts
- Orbit, 90 minute period
- Heat conducted from board to bottom surface

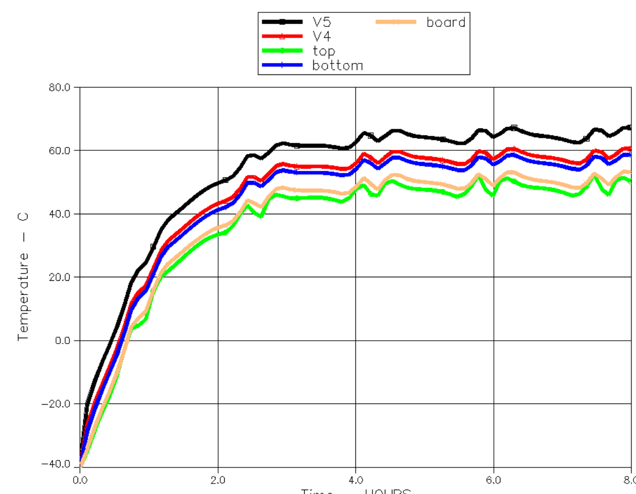
Temperature (F) after 90 minutes



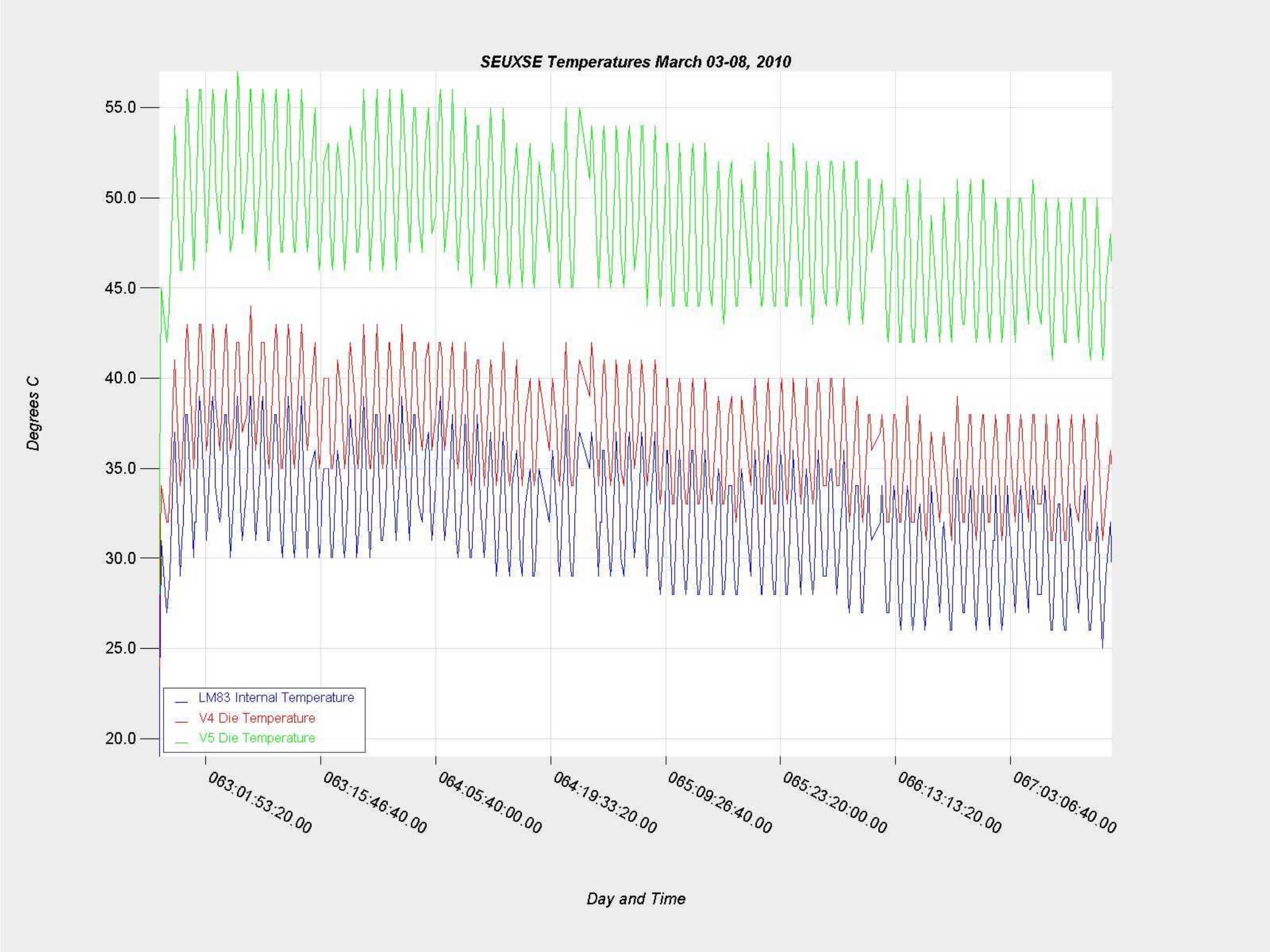


Orbit – Sun View at time=0

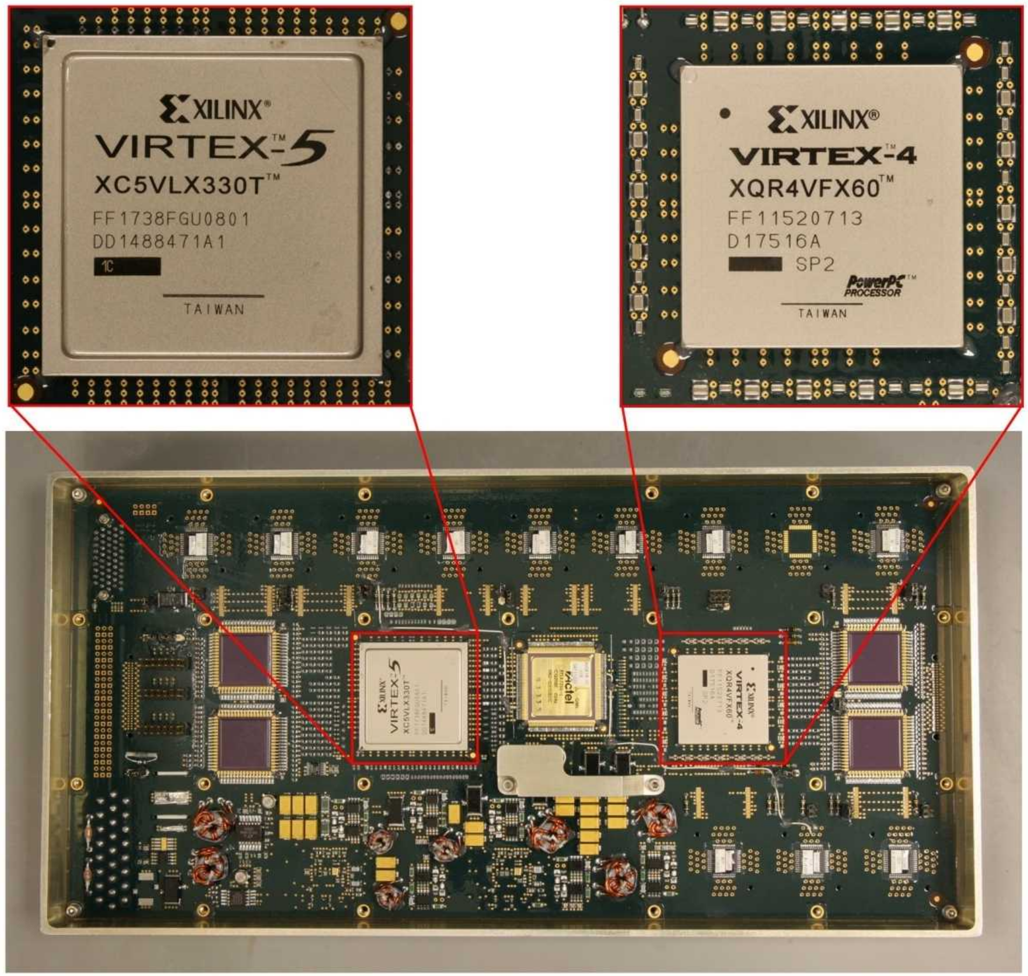
Temperature Profile over 8 hours, T_0=-40 C



SEUXSE I Temperature (3/3-3/8/10)

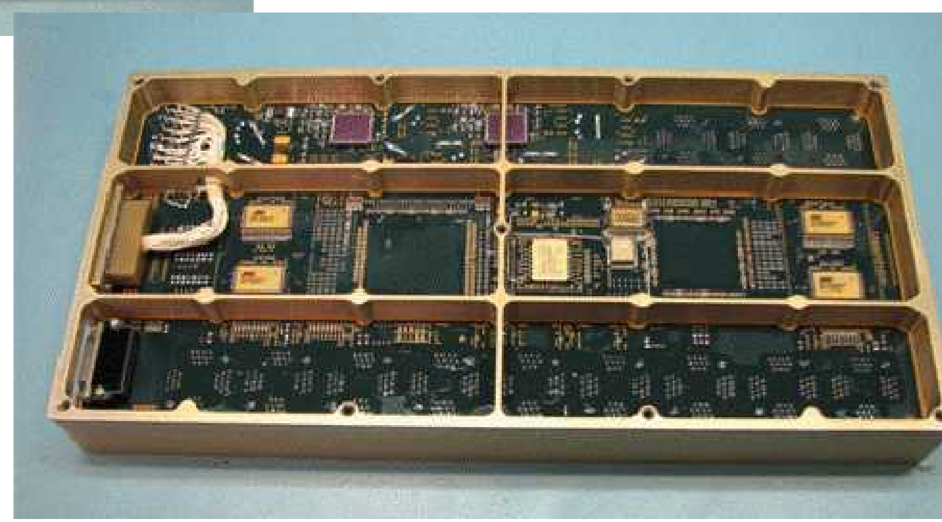


SEUXSE I Hardware



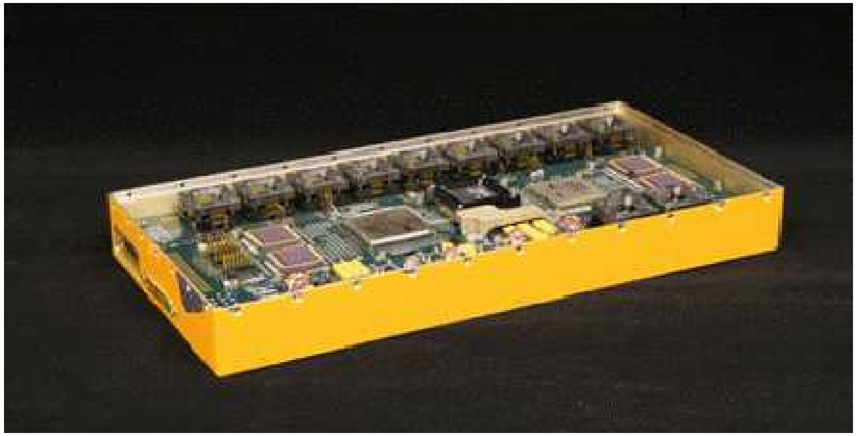
SEUXSE I Flight Unit

Top

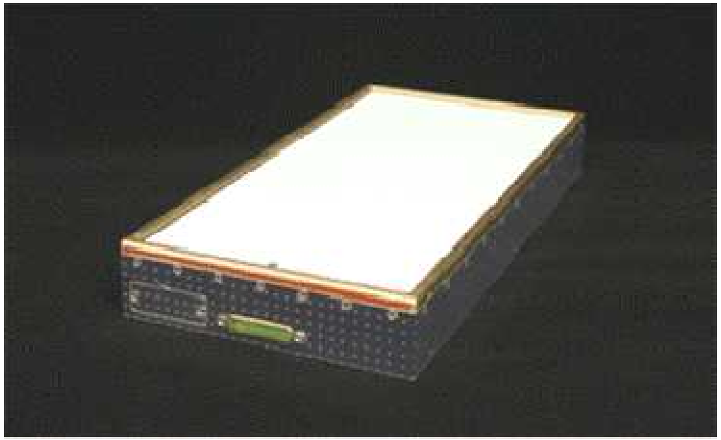


Bottom

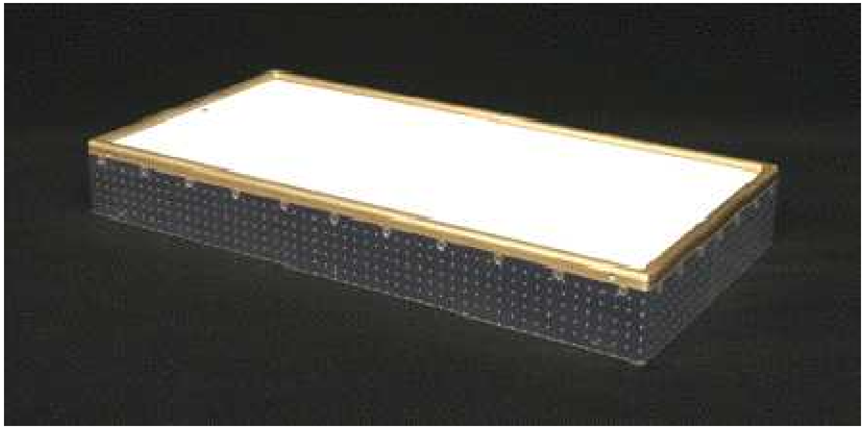
SEUXSE I Flight Unit



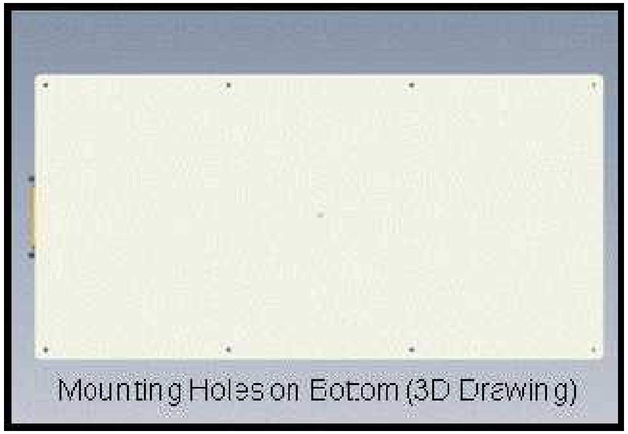
Cover Removed, w/Protective Tape



CIB Interface Connector View

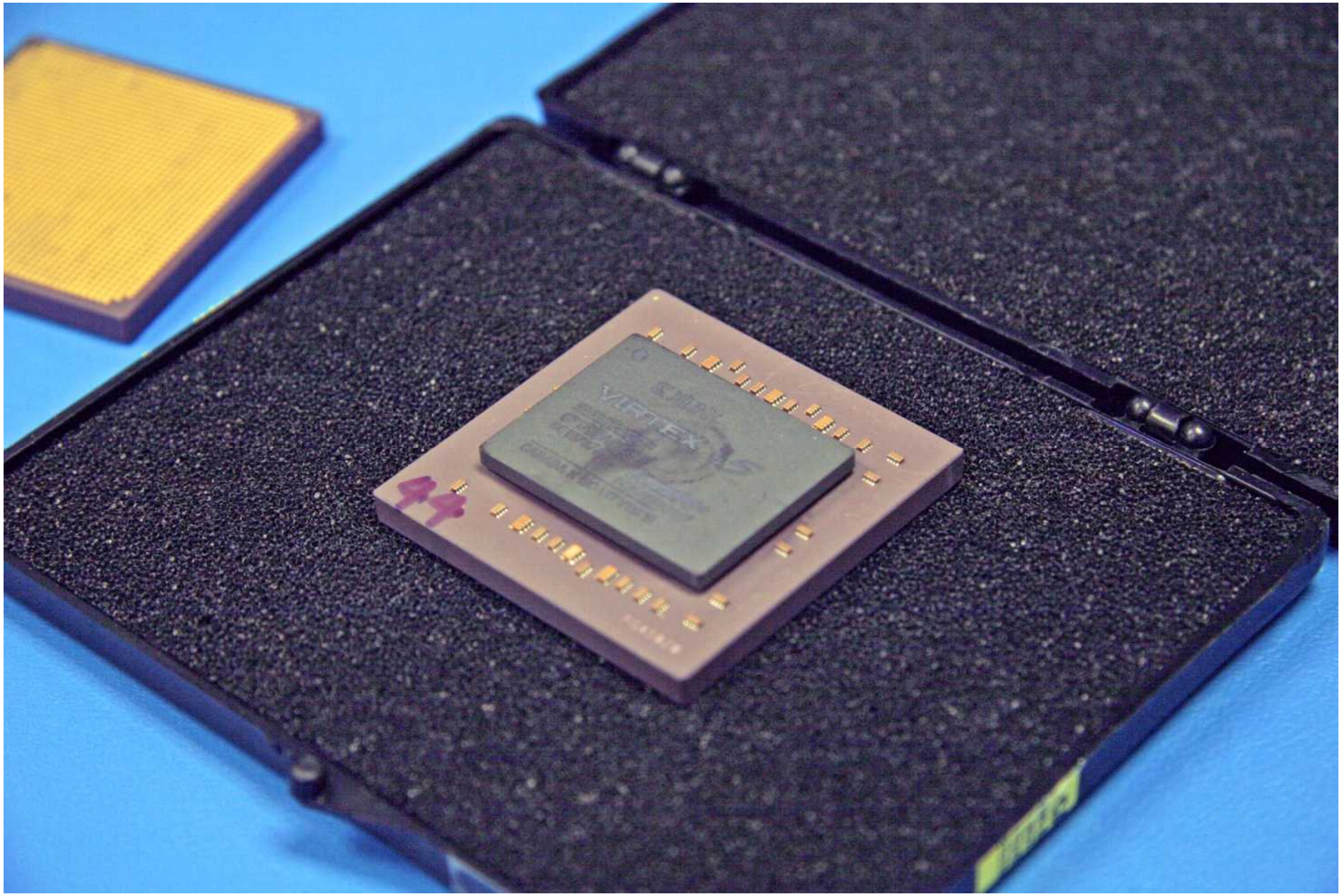


Backside View, with Composite Lid



Sandia National Laboratories

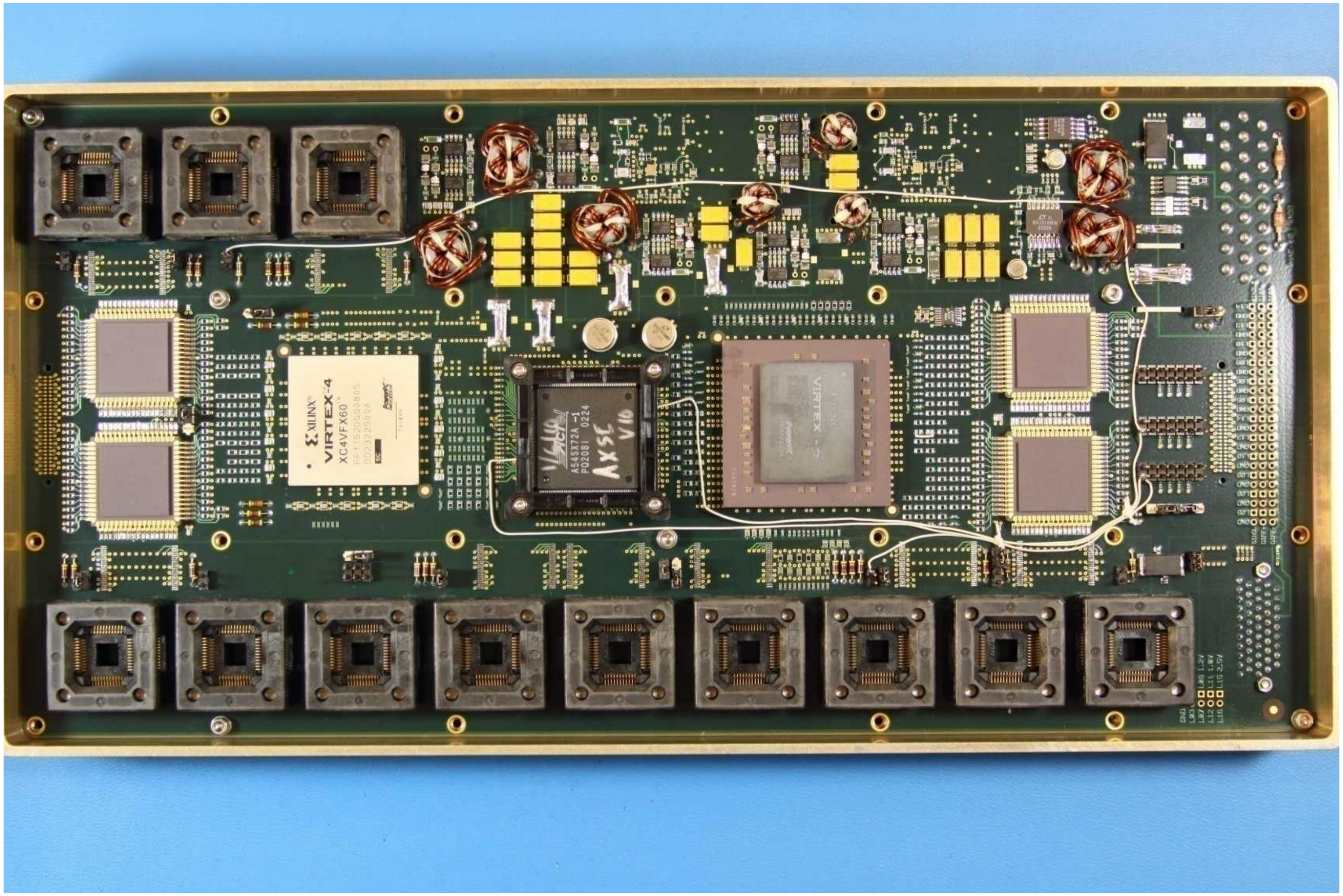
SIRF FX1 (SEUXSE II)



UNCLASSIFIED
Unlimited Release (SAND 2010-xxxx)

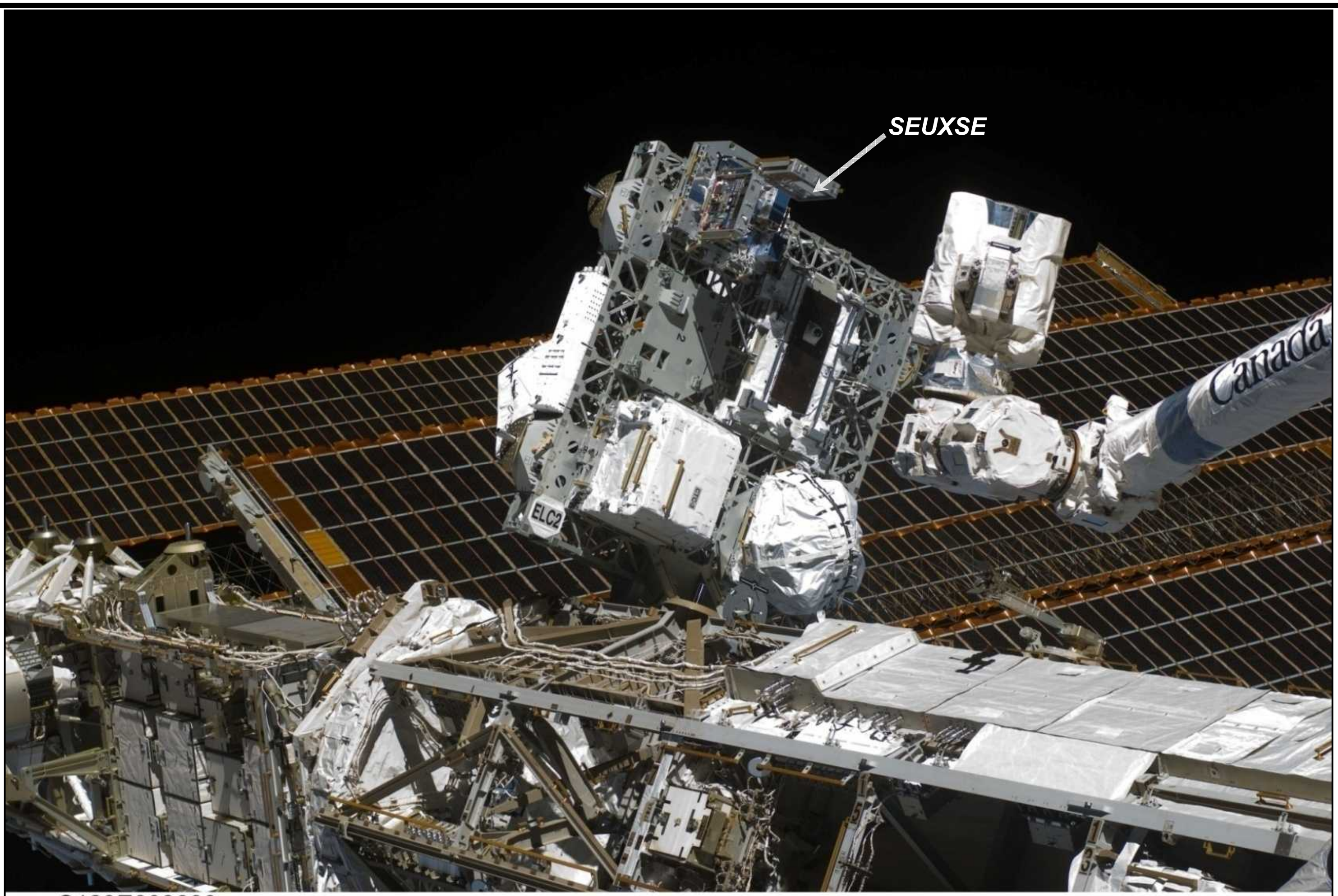
Sandia National Laboratories

SEUXSE II Hardware



Sandia National Laboratories

ELC2 with MISSE 7 on ISS



S129E008099

Thanks to All Collaborators

XILINX

Brigham Young University BYU Electrical and Computer Engineering

Los Alamos National Laboratory

The University of New Mexico

COSMIAC

JPL Jet Propulsion Laboratory California Institute of Technology

Launch and Deployment of MISSE 7

ISS and Shuttle imagery Courtesy of NASA

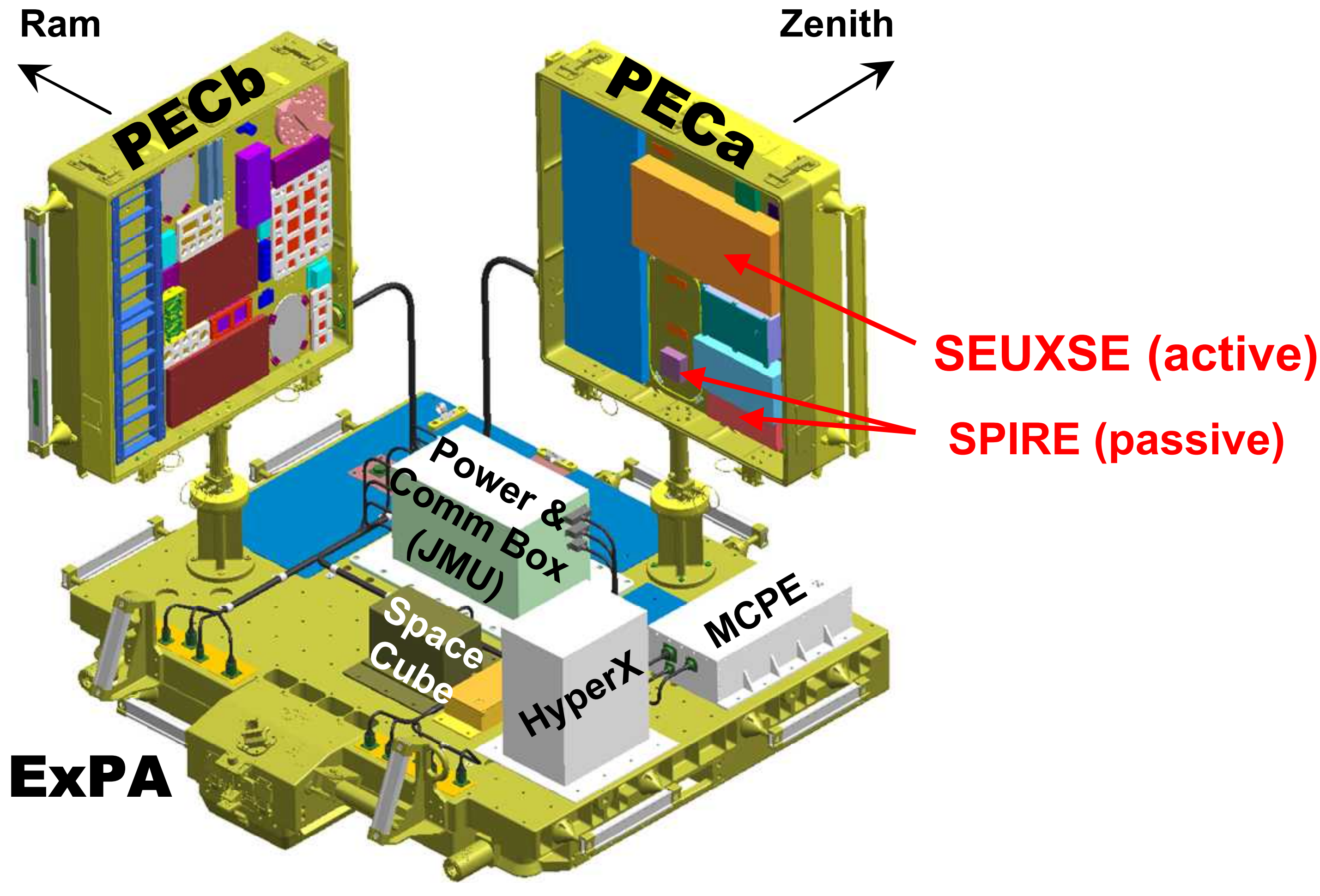
Unless otherwise noted

- **STS-129 Launched on November 16, 2009**
- **ELC2 and MISSE 7-ExPA Deployed Nov 21, 2009**
- **MISSE 7 PEC-A (SEUXSE) and PEC-B Deployed Nov 23, 2009**

Acronym List

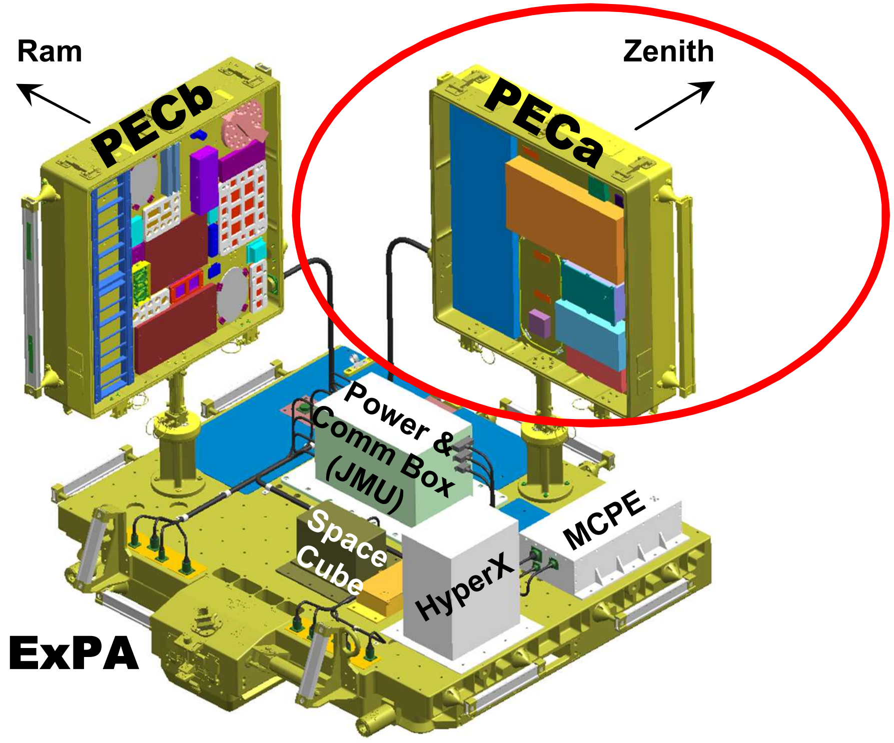
- ISS: International Space Station
- KSC: Kennedy Space Center
- ELC: Express Logistics Carrier
- MISSE 7: Materials on International Space Station, number 7
- ExPA: Express Payload Adapter
- PEC: Passive Experiment Carrier
  - Two PECs on MISSE 7: PEC-A and PEC-B
- SEUXSE: Single Event Upset Xilinx-Sandia Experiment
- SPIRE: Sandia Passive ISS Research Experiment
- EVA: Extra-Vehicular Activity (space walk)

MISSE 7 3D Pictorial View

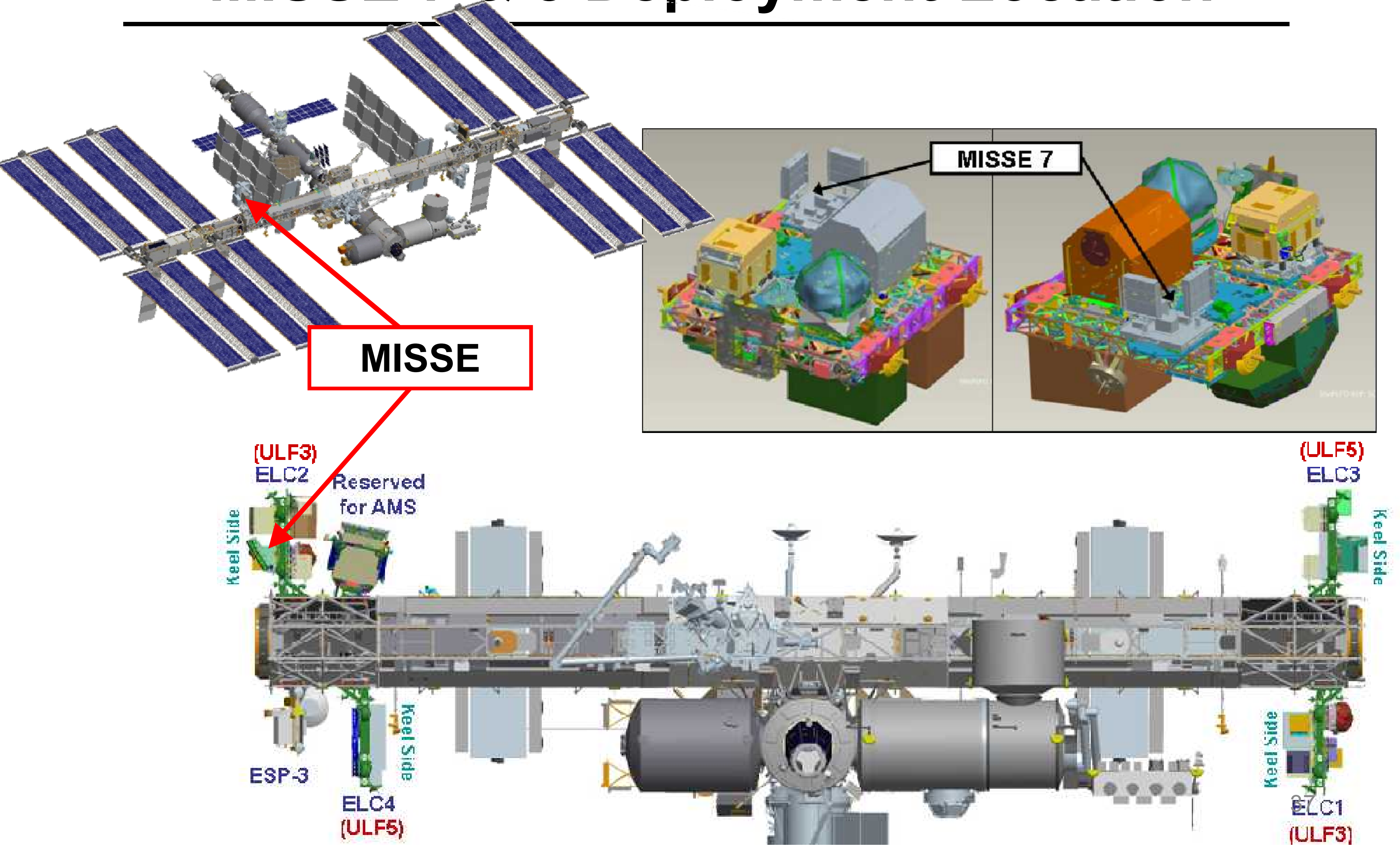


MISSE 8 Deployment

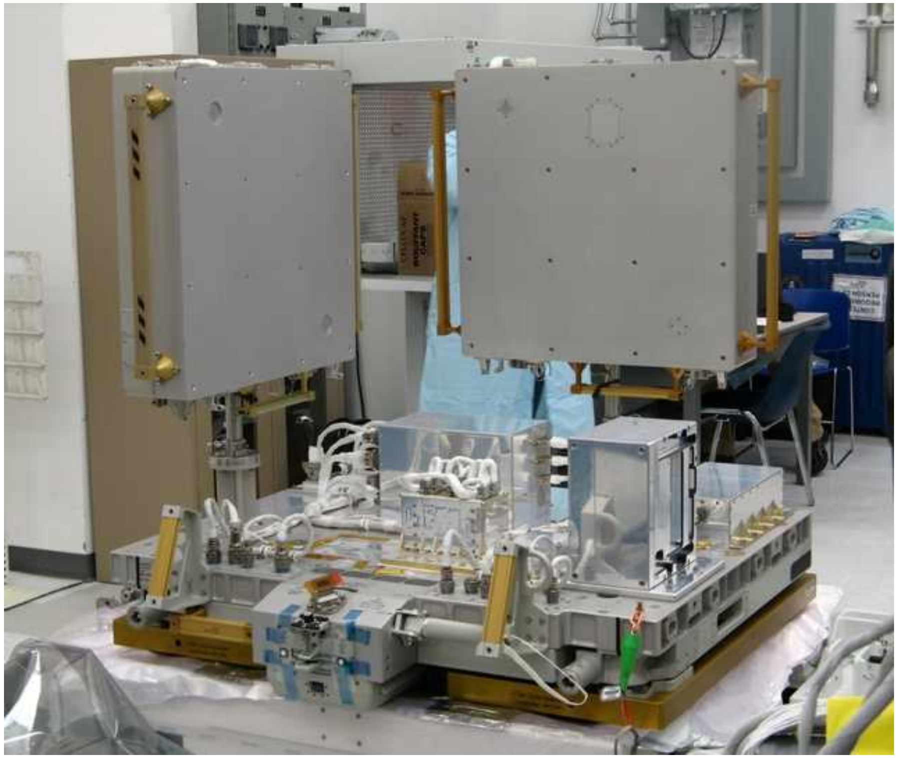
- **MISSE 8 will Re-use MISSE 7 Infrastructure**
  - *Single Passive Experiment Container (PEC)*
  - ISS Power
  - ISS Telemetry
- **MISSE 8 will be only a single PEC to replace PECa**
- **MISSE 8 will be an exchange of one of the two MISSE 7 PECs using the same physical, data, and power interfaces**



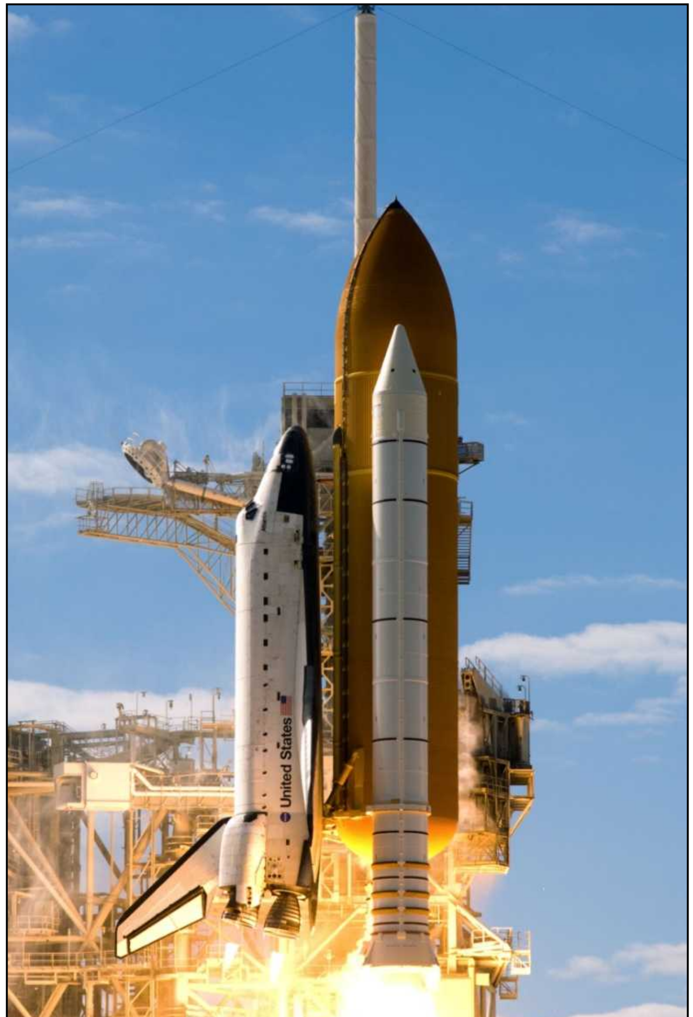
MISSE 7 & 8 Deployment Location



MISSE 7 On the Ground at NRL and KSC



STS-129 Space Shuttle Launch



UNCLASSIFIED
Unlimited Release (SAND 2010-xxxx)

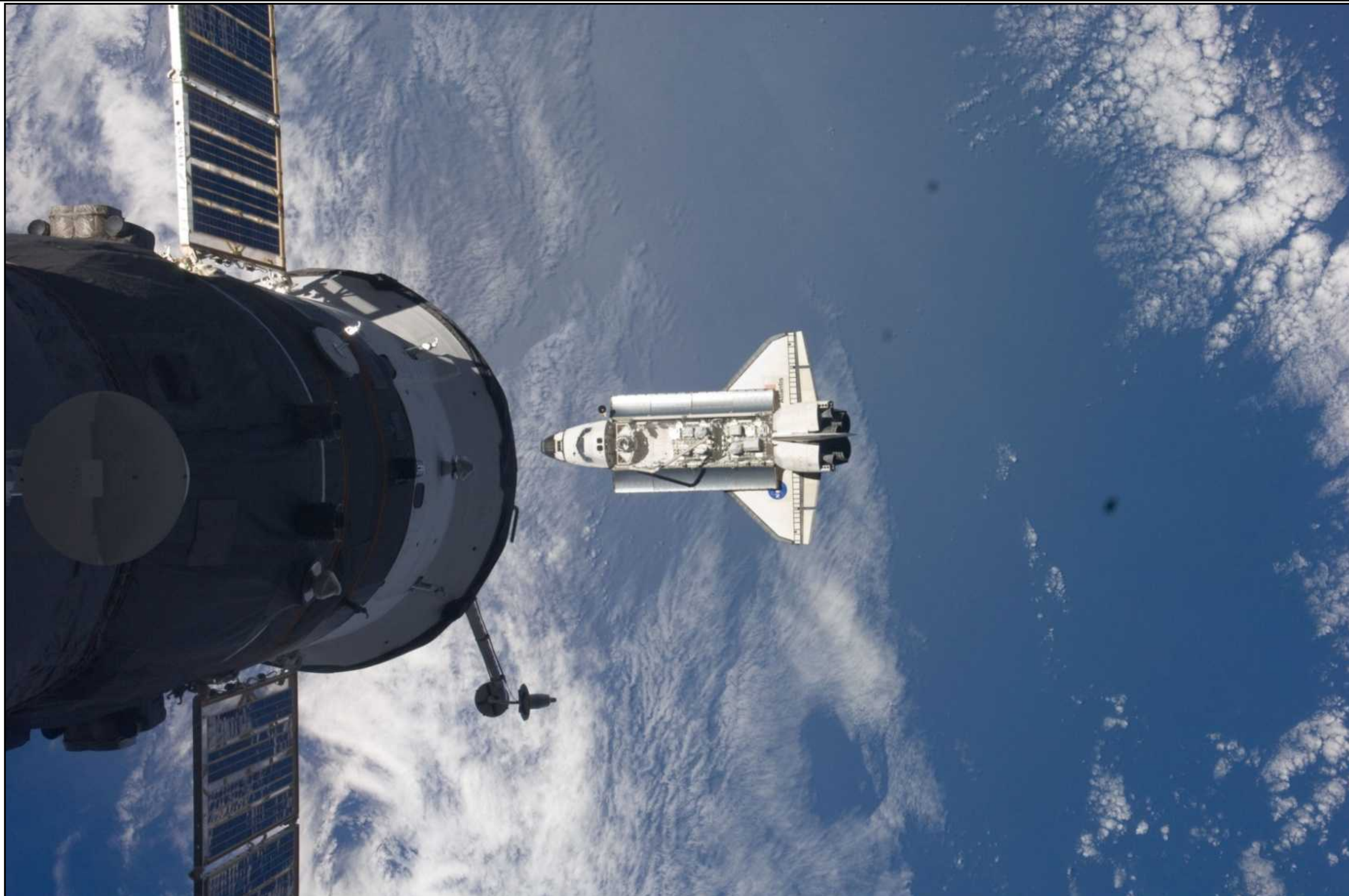
Sandia National Laboratories

STS-129 Launch

STS-129 Launch

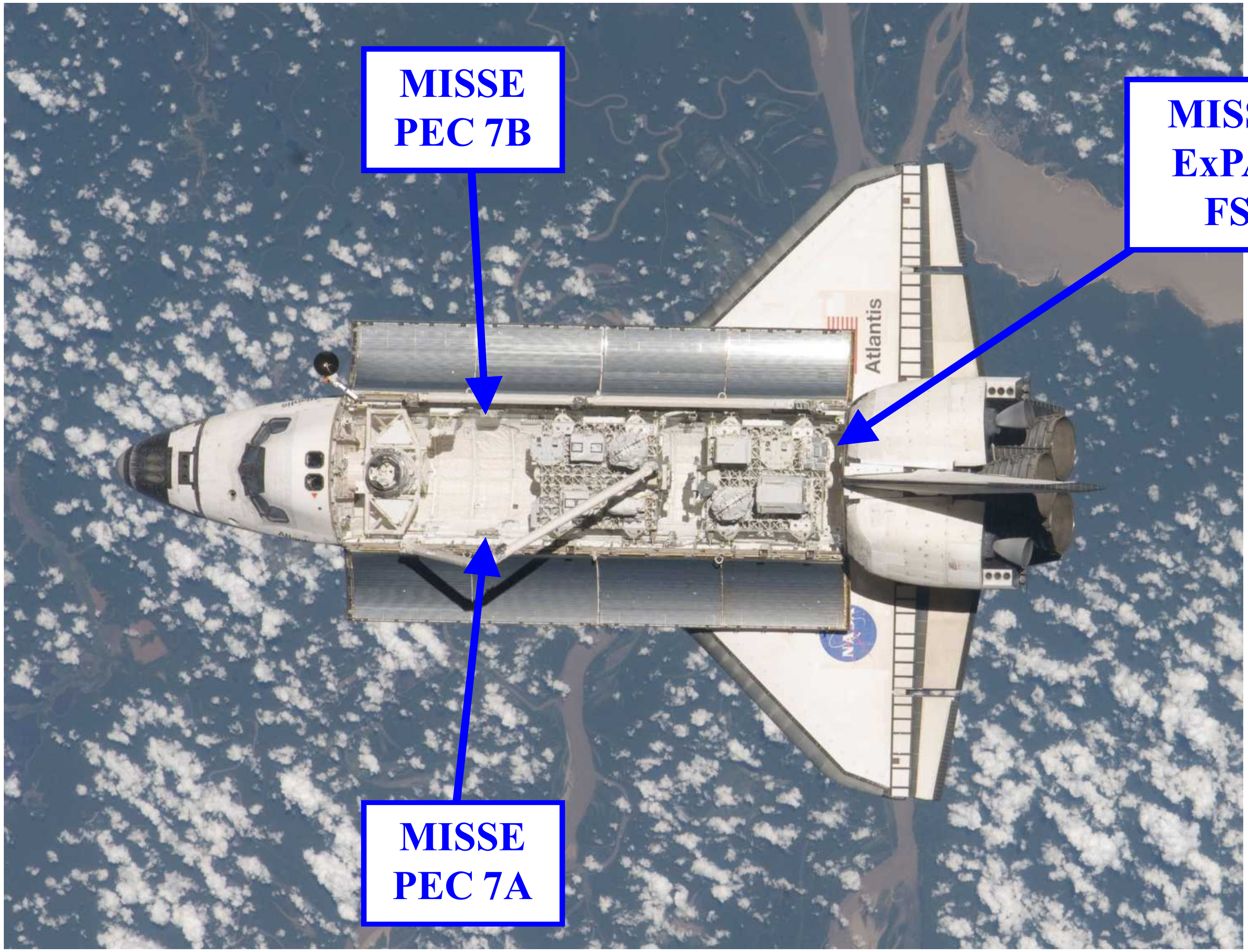
Photo courtesy Carl Carmichael

Shuttle Approach to ISS



ISS021E029809

Shuttle with ELC1 and ELC2(rear)



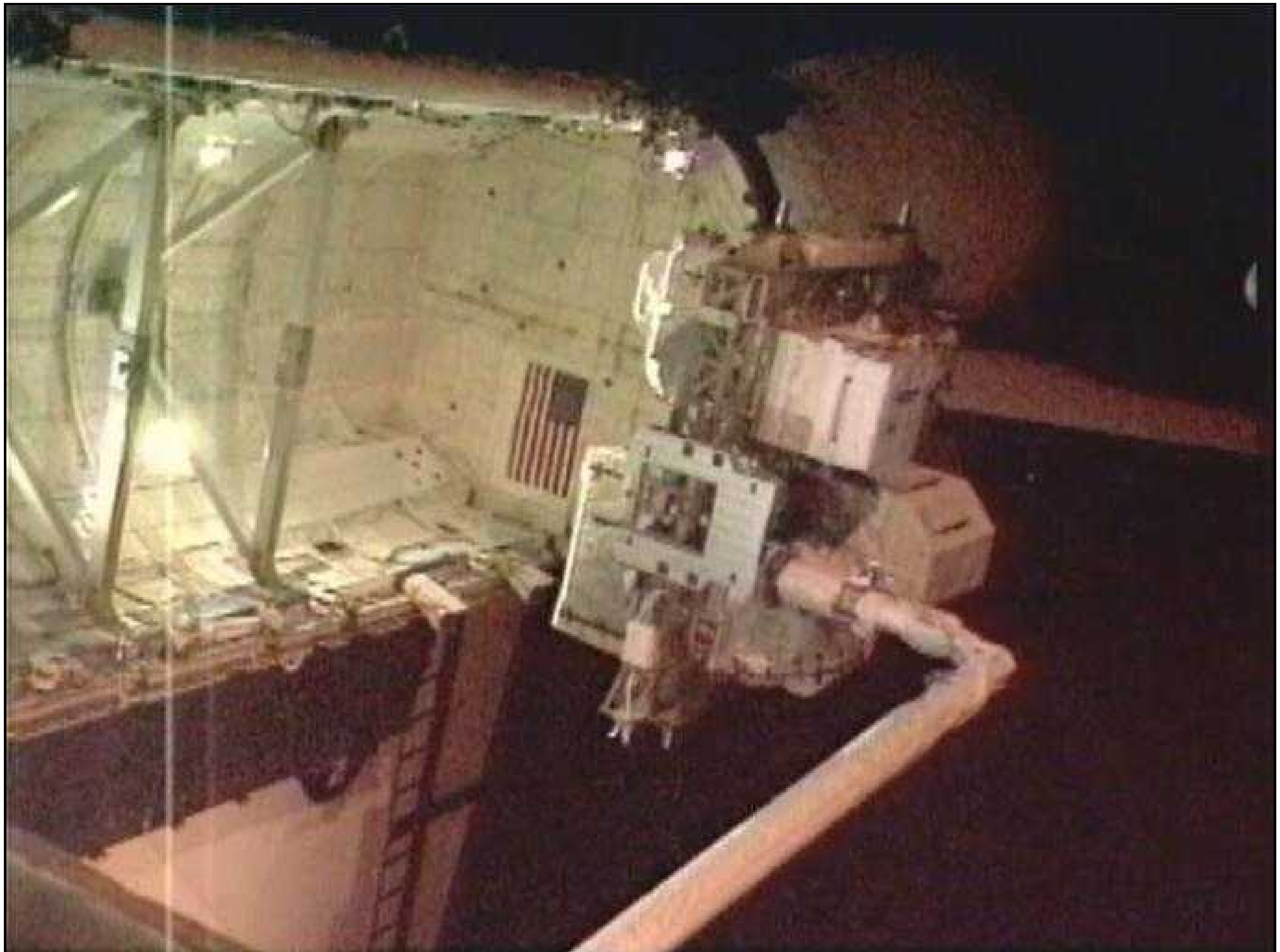
ISS Docking Port

ISS021E028901

ELC2 w/MISSE7-ExPA in Cargo Bay

ISS021E029049

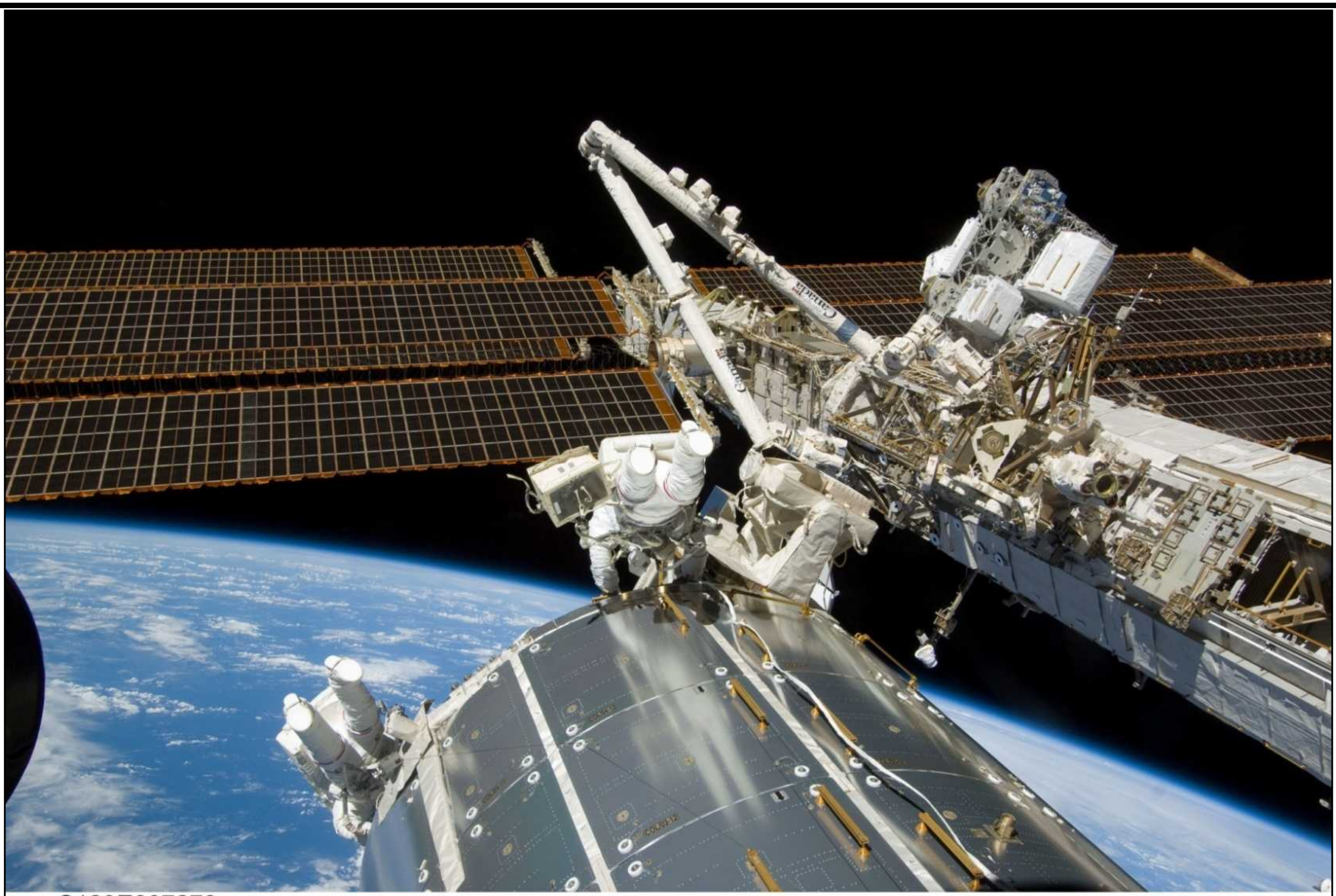
ELC2 Extracted From Cargo Bay (NASA TV)



Station Arm Deploys ELC2

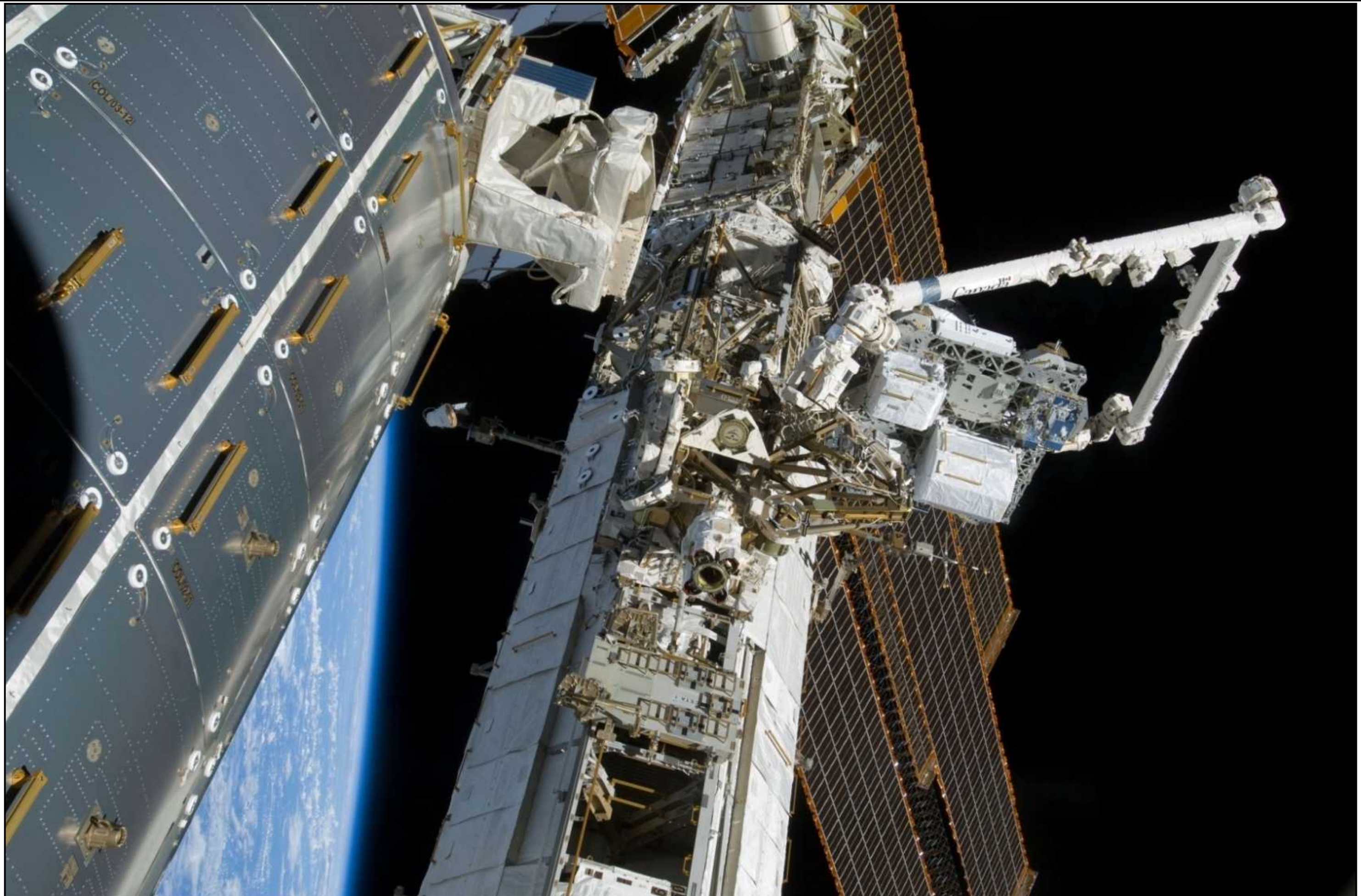
S129E007199

EVA-1 To Attach ELC2 to ISS



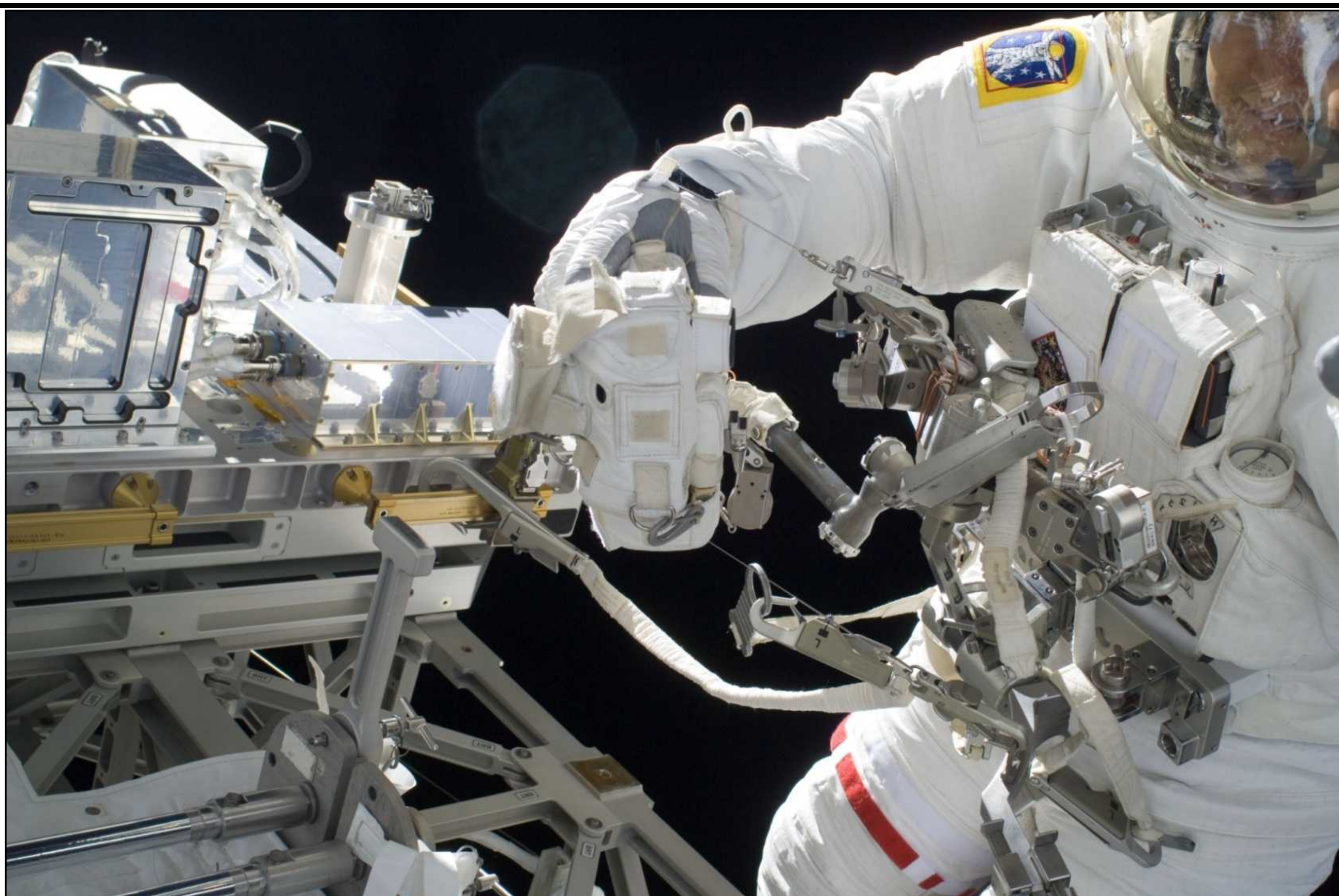
S129E007278

ELC2 w/MISSE 7-ExPA Mounted to ISS



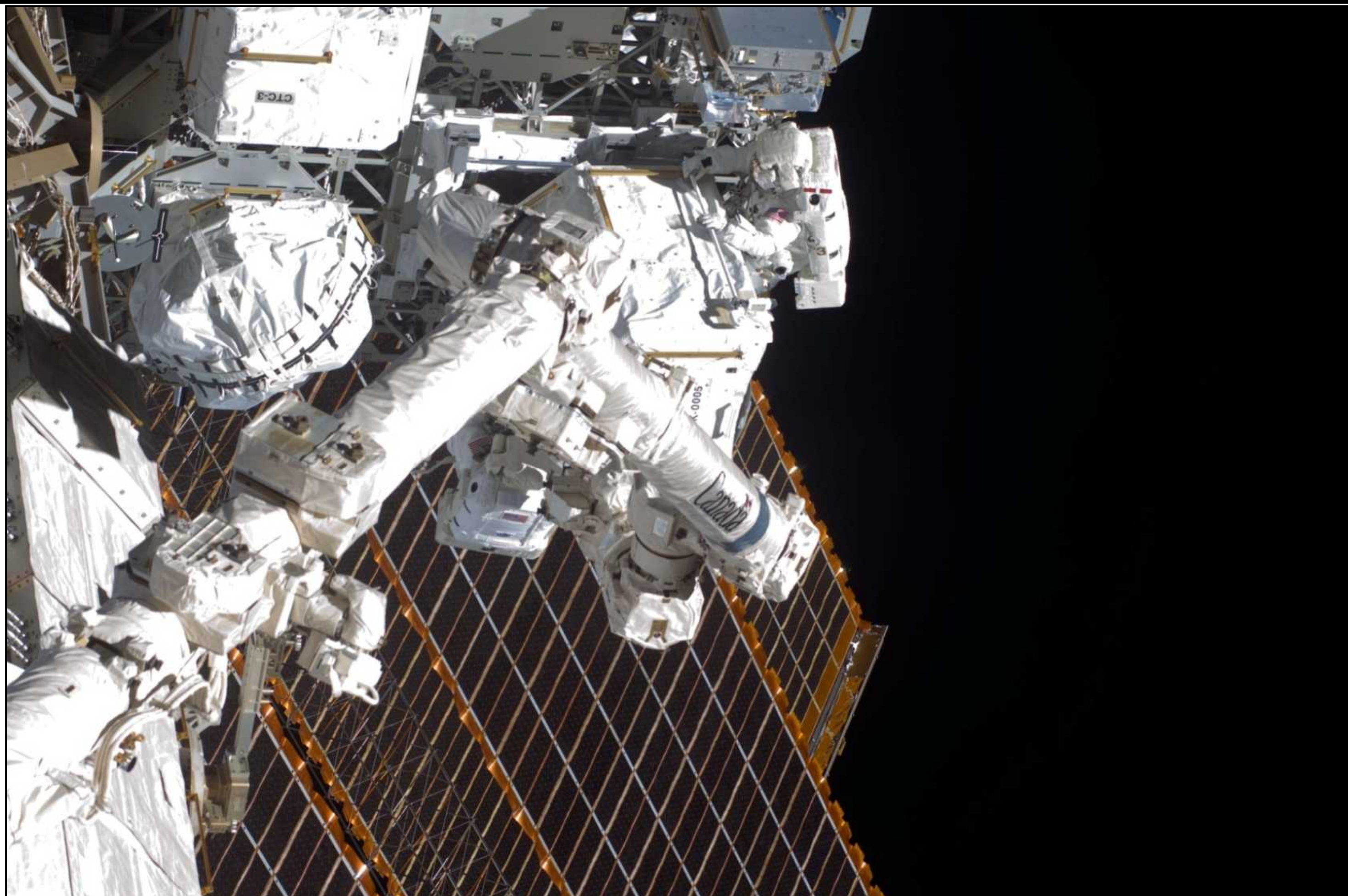
S129E007209

Astronaut with MISSE 7 ExPA
(One of the PEC attachment sockets is shown)



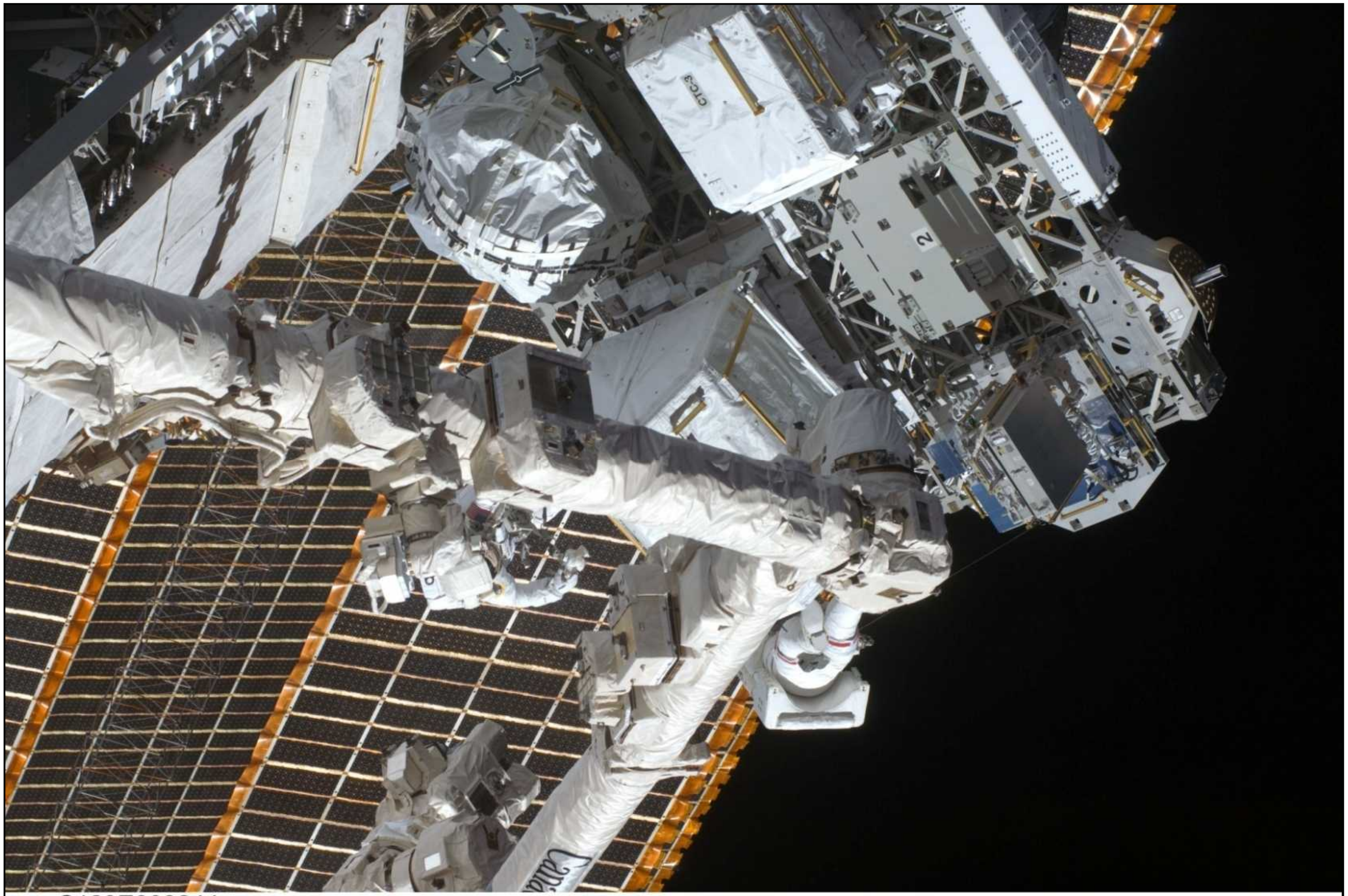
ISS021E031633

EVA-2 to Deploy MISSE 7 PECs (Removing Gas Tank From ELC2)



S129E008246

Stowed PEC A/B Attached to ExPA

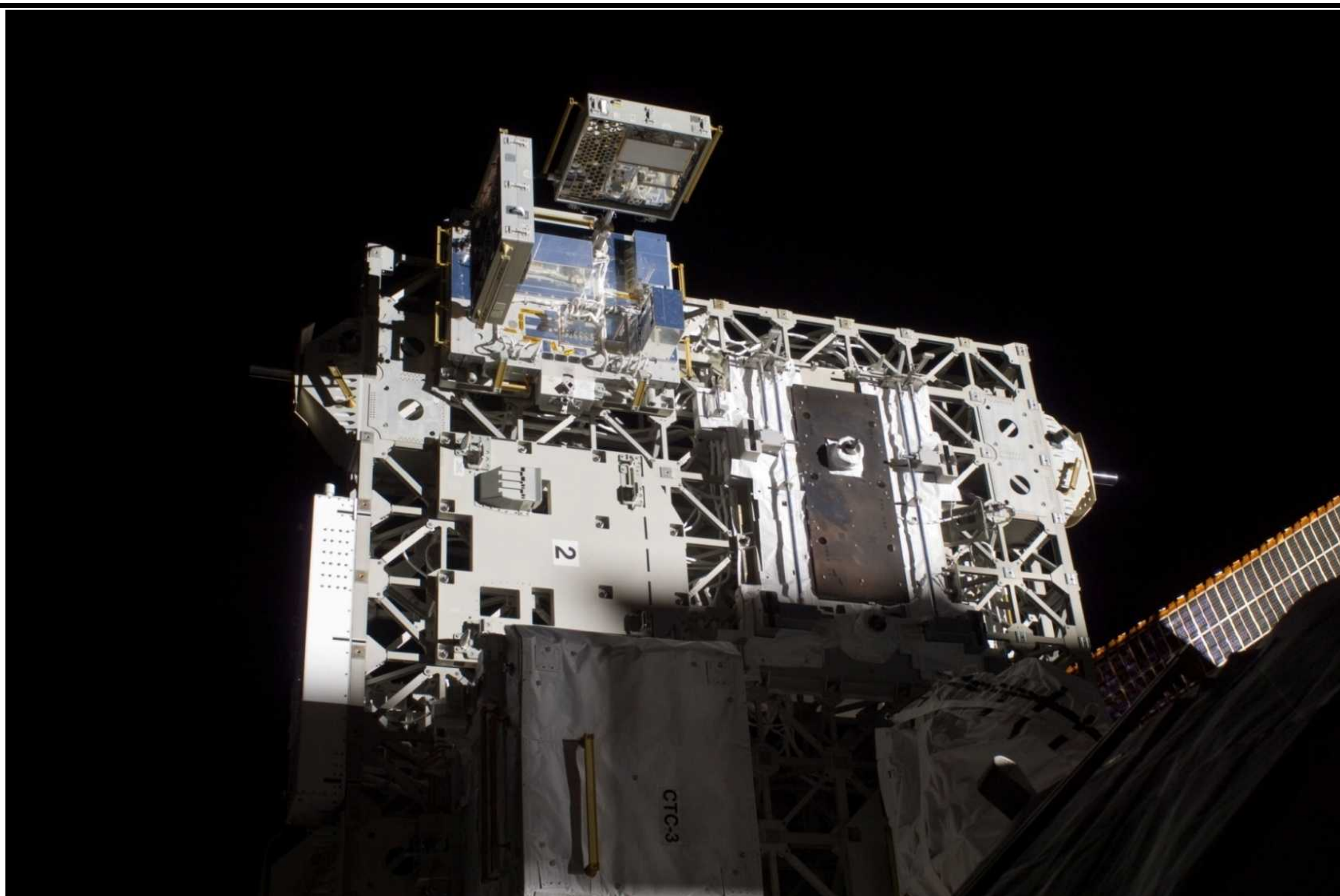


S129E008244

Stowed PEC A/B Before Deployment

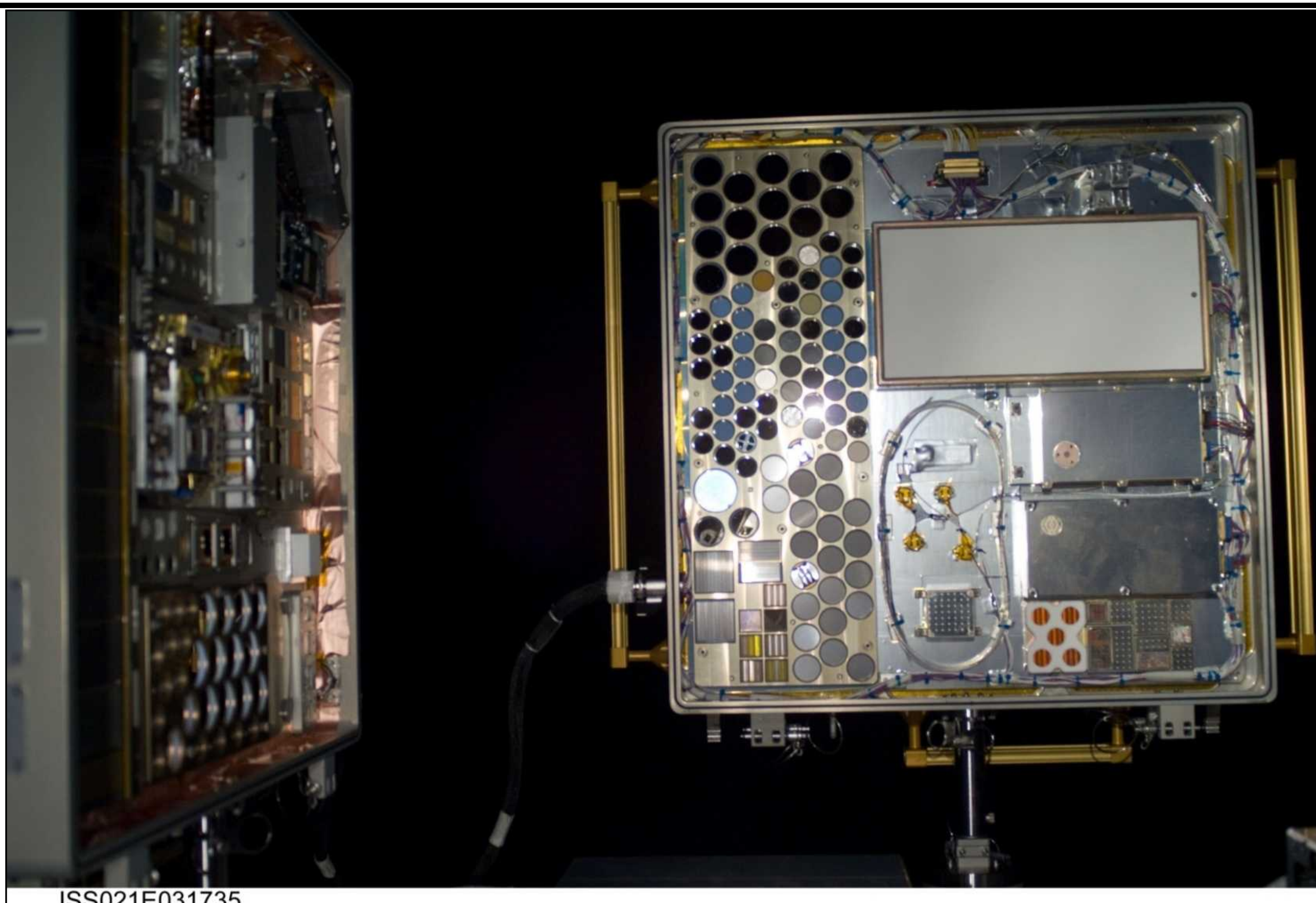
S129E008243

PEC A & B Deployment Completes MISSE 7

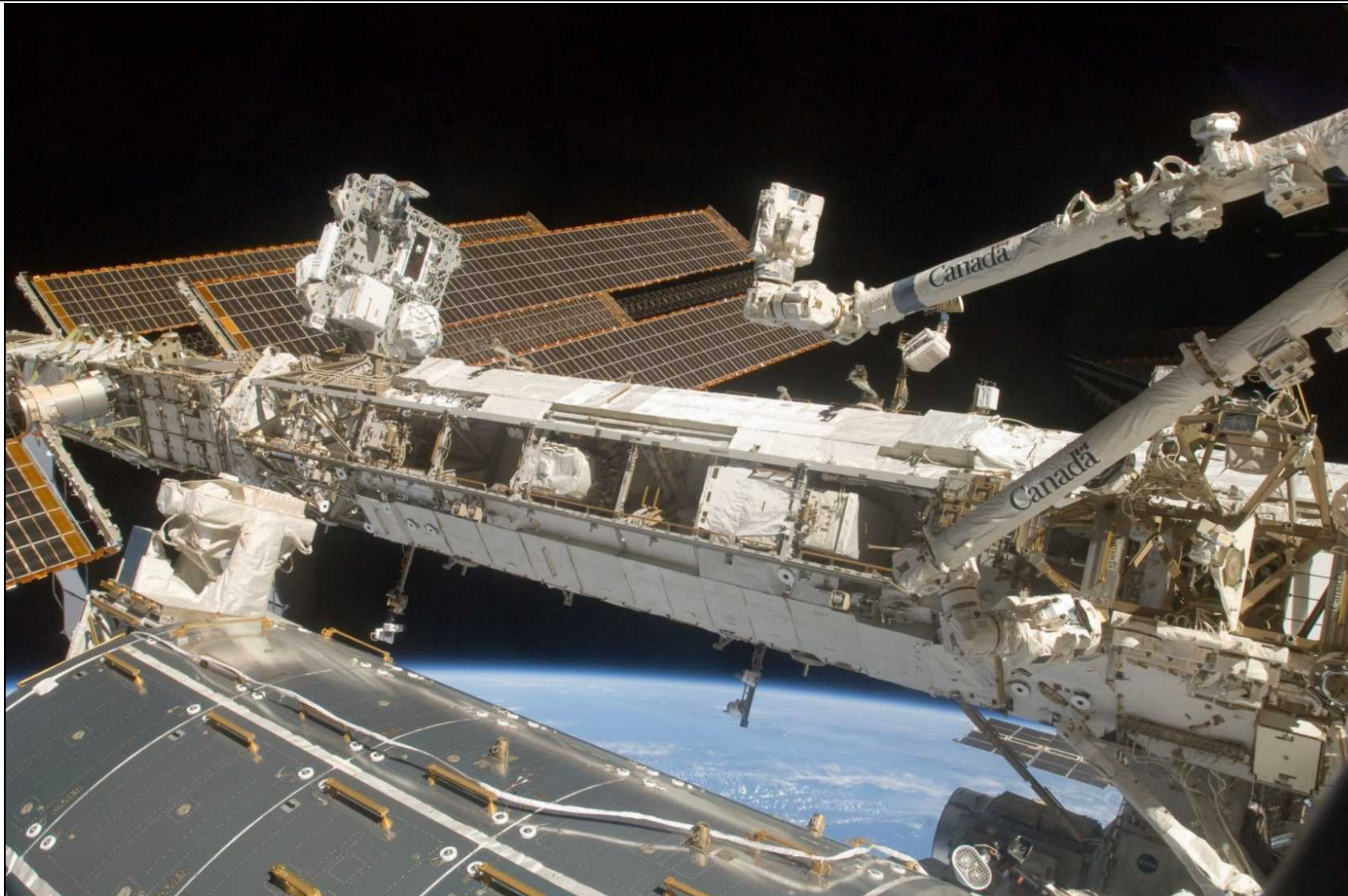


ISS021E031746

Closeup of PEC-A Nadir and SEUXSE/SPIRE

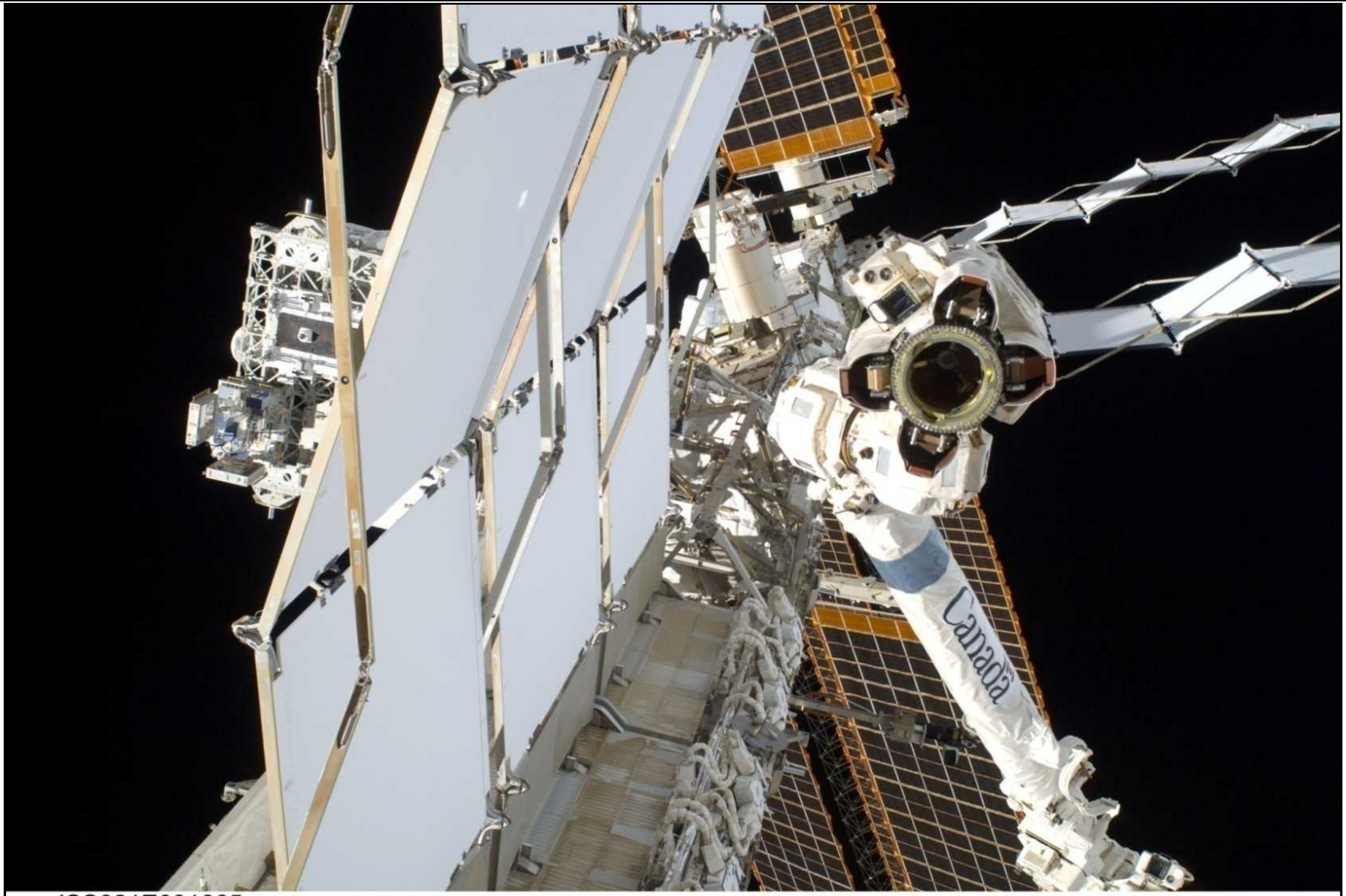


ELC2 Position On ISS
SEUXSE on PEC-A Nadir Face



ISS021E032833

ELC2 with MISSE 7 on ISS



ISS021E031665

ELC2 with MISSE 7 on ISS

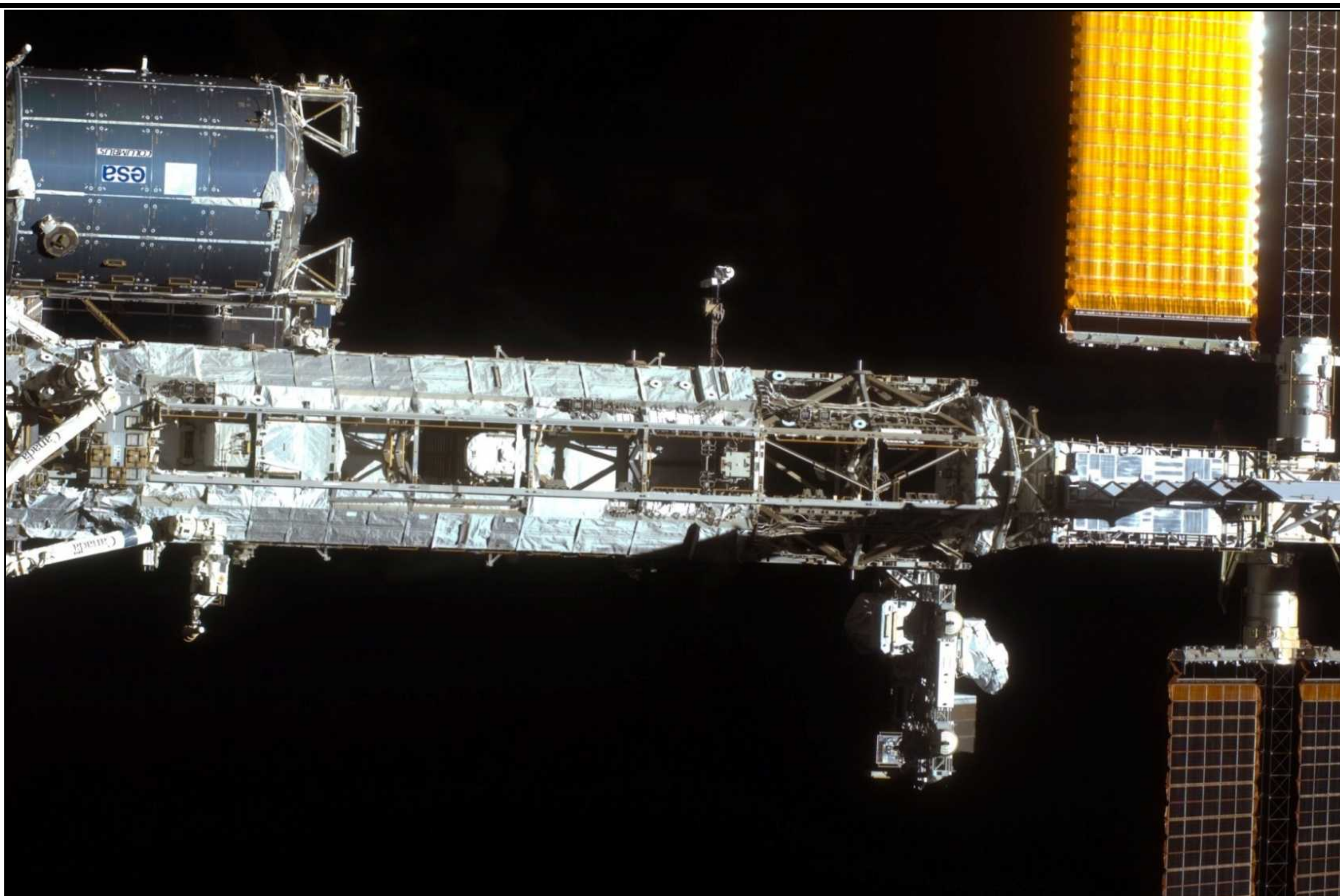
S129E009668

Backside of PEC-A Visible on ISS

S129E009276

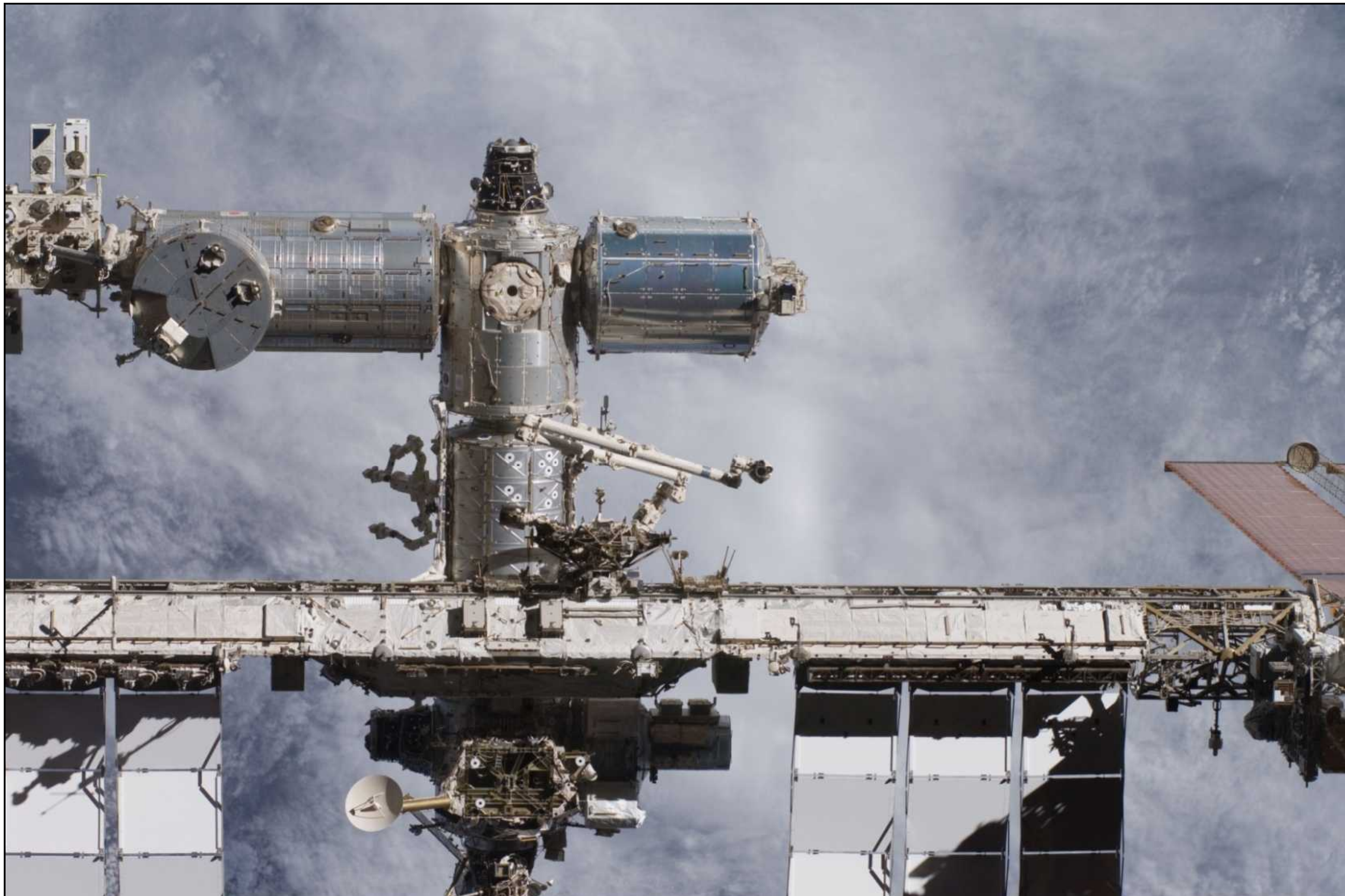
UNCLASSIFIED
Unlimited Release (SAND 2010-xxxx)

Backside of PEC-B Visible on ISS



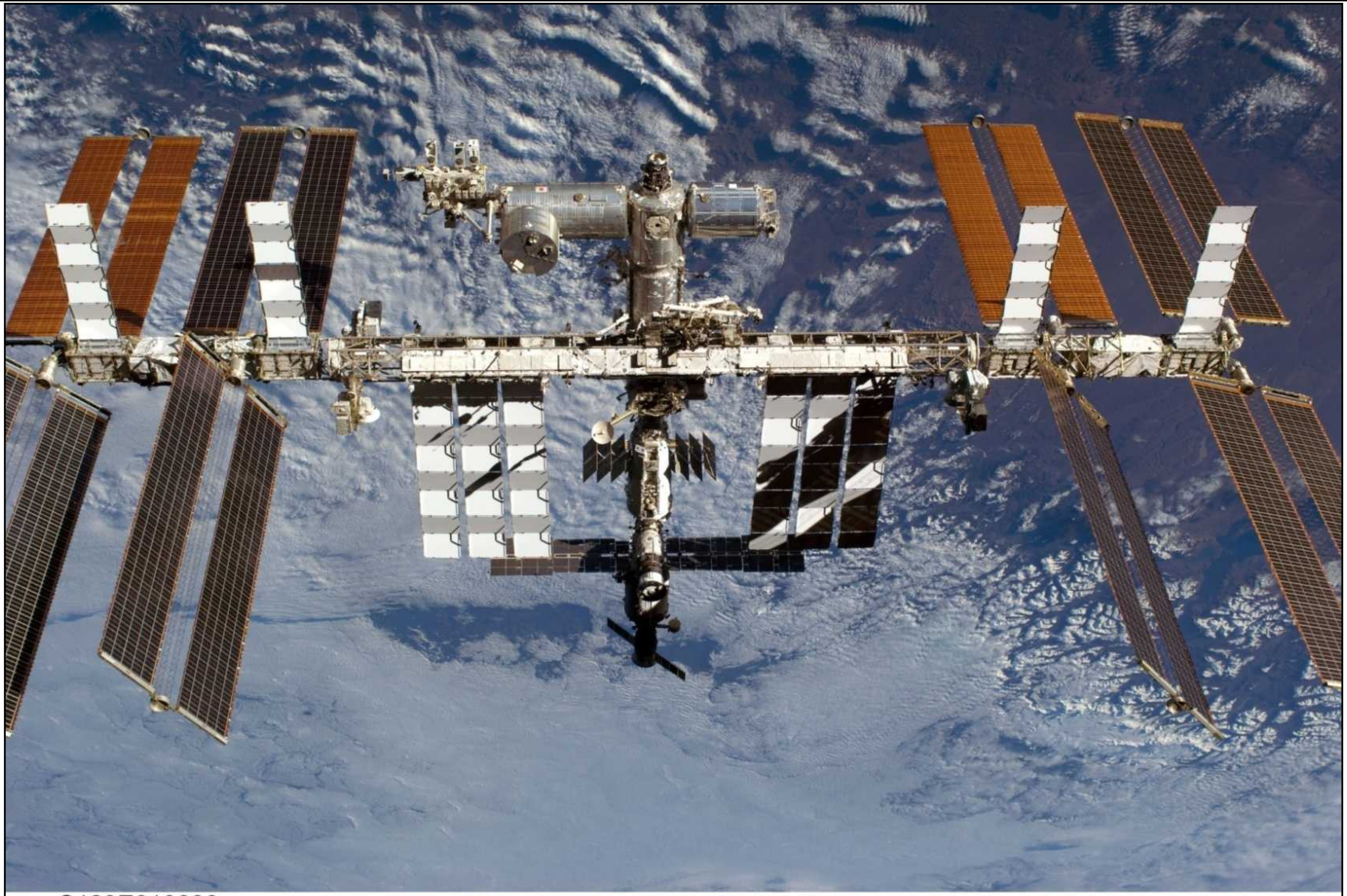
S129E010060

Backside of PEC-A Visible on ISS

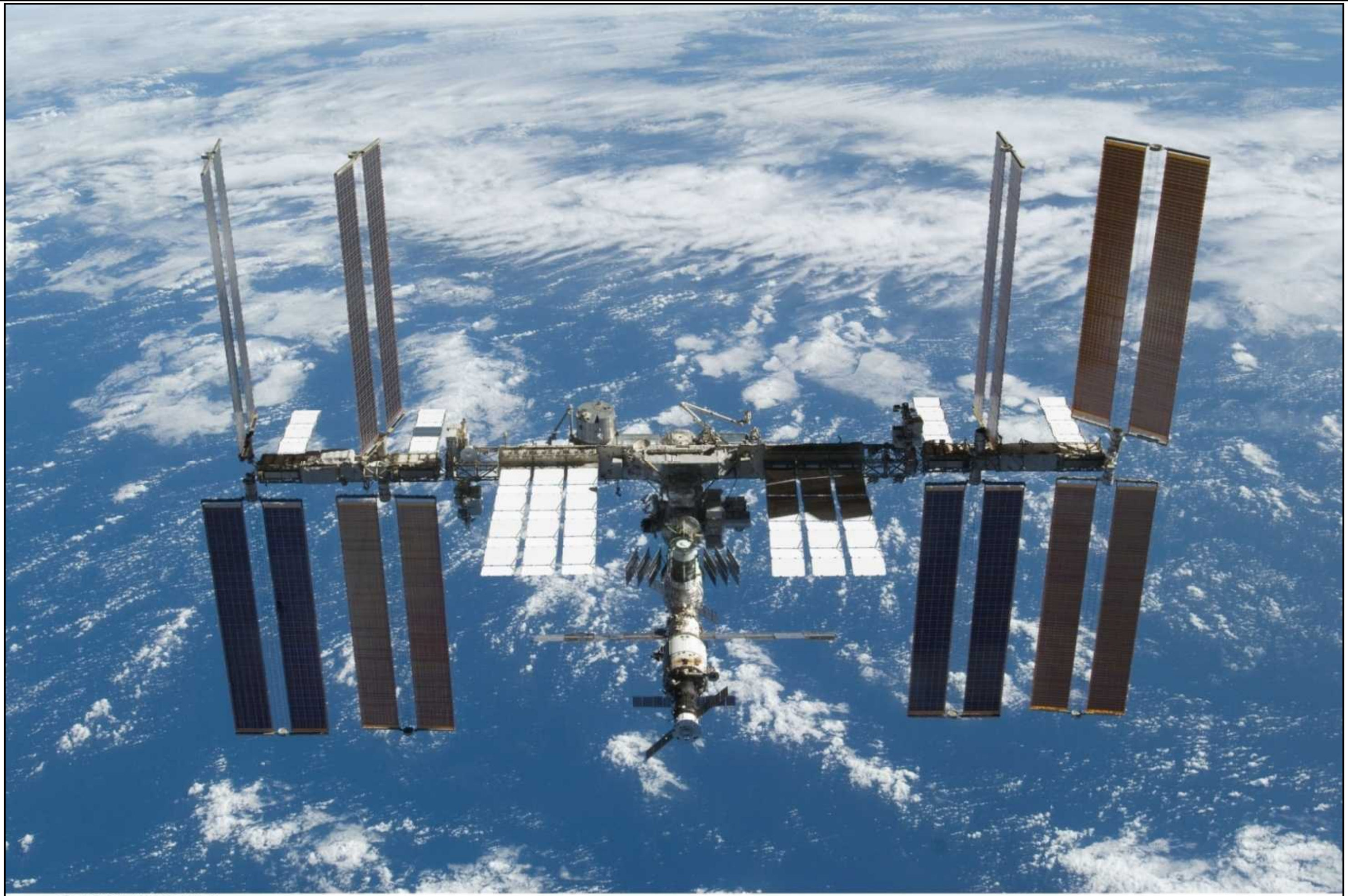


S129E009272

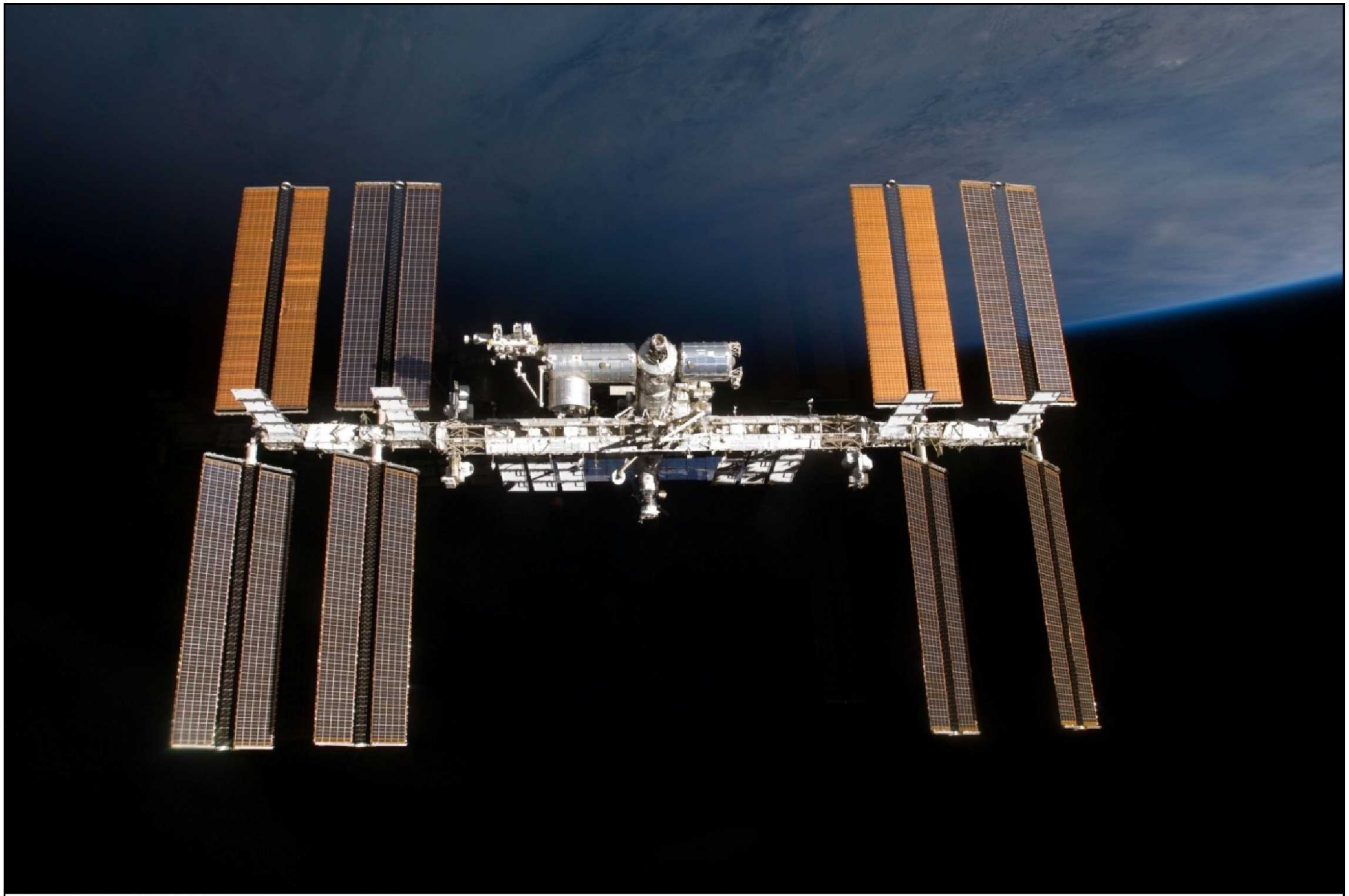
Shuttle Departs ISS


S129E010090

Shuttle Fly Around of ISS


S129E009326

ISS With MISSE 7, SEUXSE, and SPIRE



S129E009225

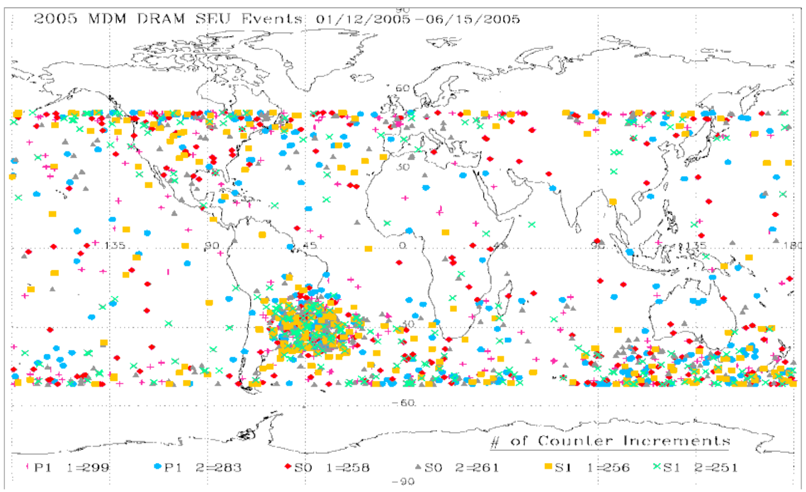
STS-129 Shuttle Atlantis Touch Down

STS-129 Space Shuttle Landing

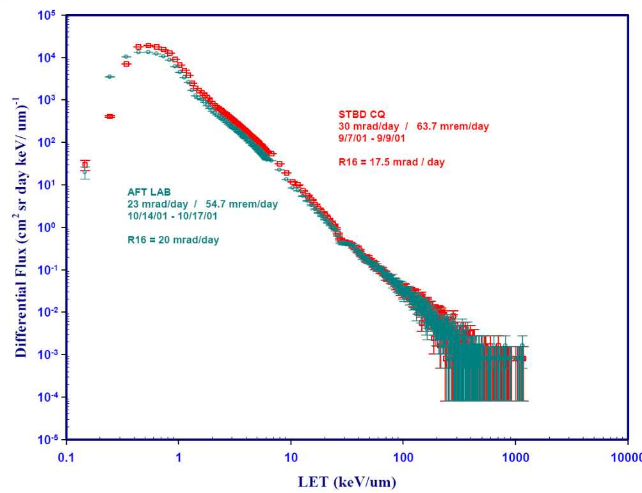
Backup

ISS Radiation Environment

- **ISS environment is suitable for a Single Event Effects experiment**
  - High inclination (51.5°) exposes ISS to higher fluence of trapped electrons and protons and solar and galactic cosmic rays than would be the case in a lower inclination orbit with the same altitude range, largely as a result of the overall shape and magnitude of the geomagnetic field.
  - ISS passes through the South Atlantic Anomaly (SAA).



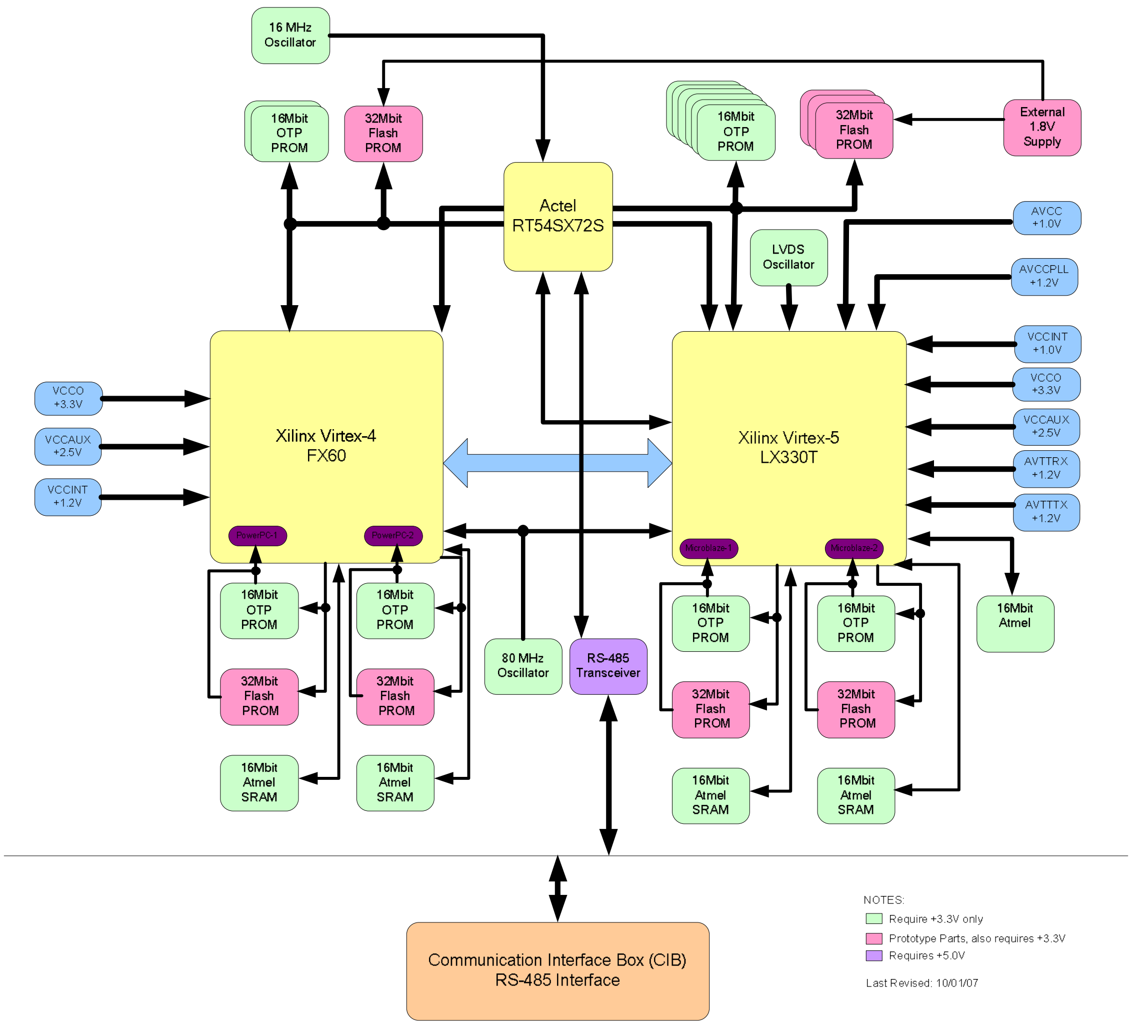
Aggregate MDM DRAM SEU Map (155 days)



ISS Extra-Vehicular Charged Particle Spectrometer (EV-CPDS) Real-time LET measurements

Detected SEUs will be correlated to ISS radiation and environmental monitored data.

SEUXSE Printed Circuit Board Block Diagram



UNCLASSIFIED

Unlimited Release (SAND 2010-xxxx)

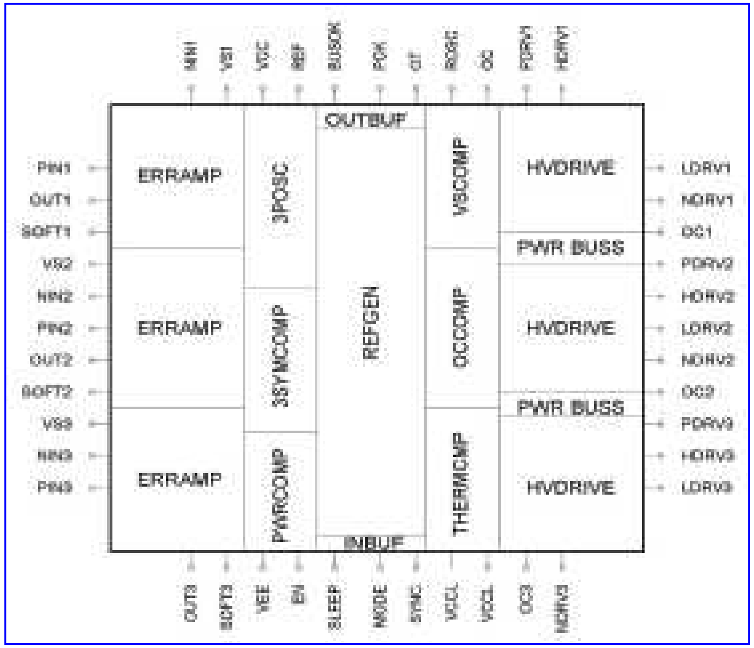
Sandia National Laboratories

MISSE-7 Power System

- Rad-hard point-of-load (RHPOL) power converters to generate the required low voltages
  - 6 POL Converters: +3.3V, +2.5V, 2 at +1.2V, 2 at +1.0V
  - 90% efficiency
- RHPOL controller IC developed at part of internal Sandia research efforts
  - 3 outputs per controller
  - Total-dose tolerant to >1Mrad(SiO_2)
  - Immune to single-event latchup, burnout, and gate rupture
  - No POL output single-event transients to >80MeV-cm^2/mg
- COTS power FETs tested
  - Total-dose tolerant to >30krad(SiO_2)
  - Immune to single-event burnout and gate rupture

POL Controller Development

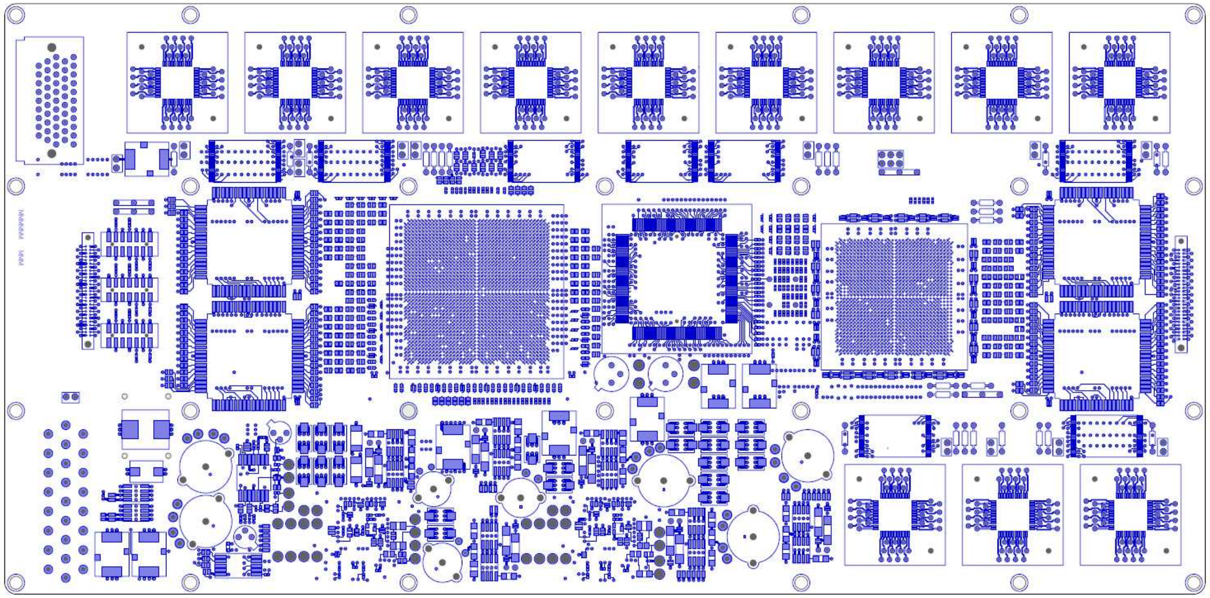
- 3-Output
  - Multi-rail digital parts (e.g. FPGAs)
- Synchronous Buck topology
  - High efficiency > 90%
- High frequency > 300kHz per phase
  - Reduced size
- High gain-bandwidth > 3MHz
  - Improved transient response
- Phase interleaving
  - Reduced size and stresses
- Flexible for varying applications
  - V_{IN} from 4.5 – 13.2 volts
  - V_{OUT} from 0.6 – 5 volts
- Fully protected
  - Over-current
  - Under/Over-voltage
  - Over-temperature



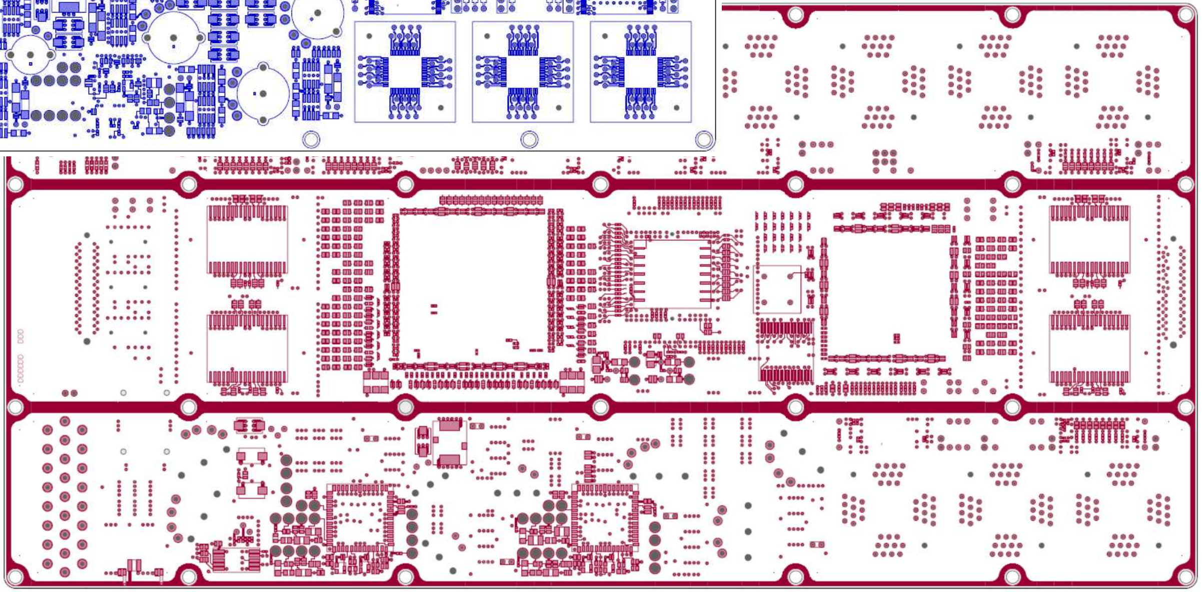
Basic Controller Architecture

- Radiation-Hardened
  - Total-dose > 100krad(SiO_2)
  - SEL, SEGR, SEB immune to LET > 80 MeV-cm^2/mg

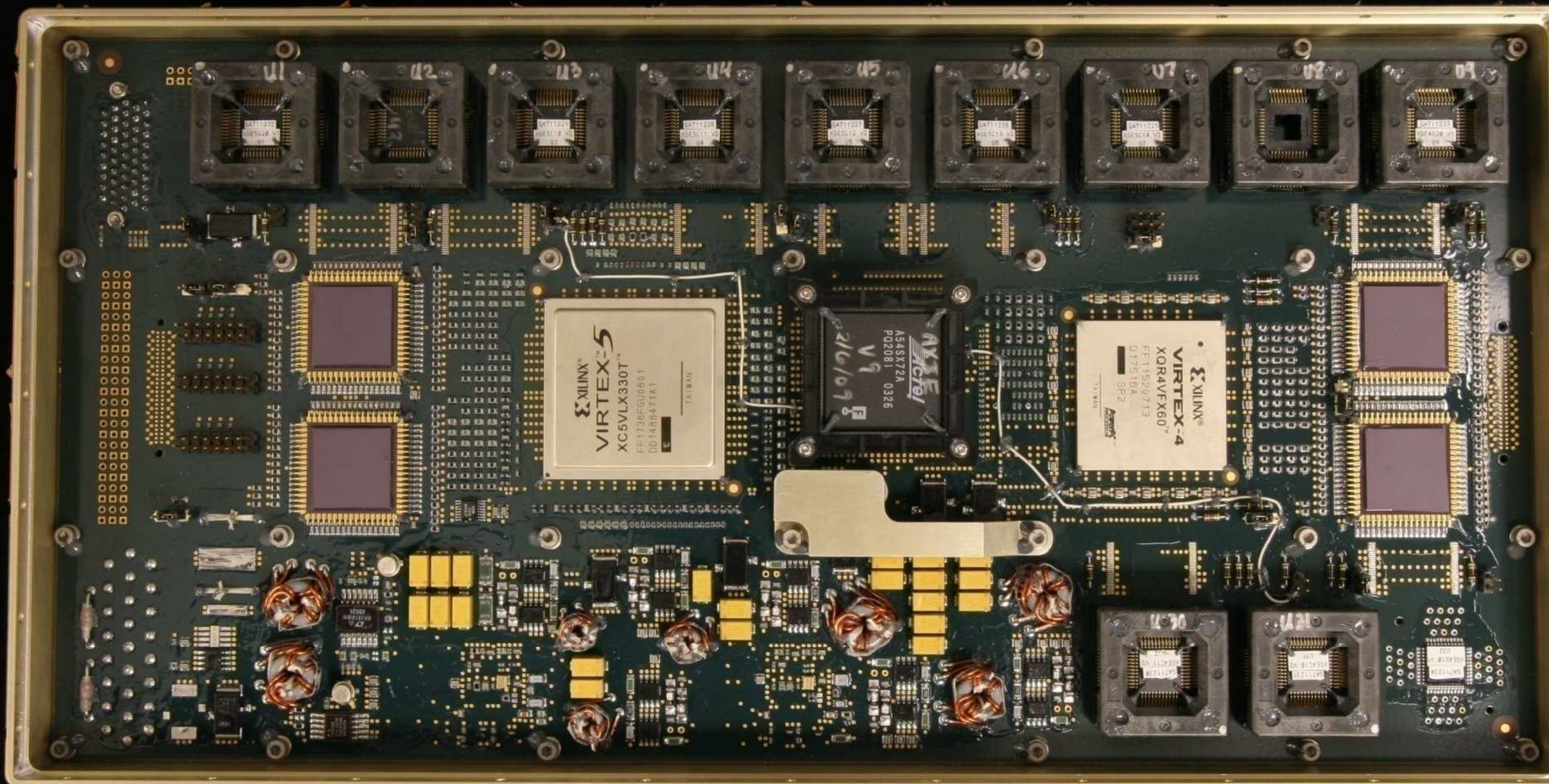
SEUXSE Printed Circuit Board



Top Side View



Bottom Side View


XILINX
VIRTEX-5
XC5VLX330T
XILINX
VIRTEX-4
XQR4VFX60