SAND2013-10538C

Six Generations of ViArray Rad-Hard Structured ASICs

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Abstract: *This paper presents the ten year history of Sandia's ViArray radiation-hardened mixed-signal structured ASIC devices and their evolution from research prototypes into high-reliability product platforms for low-volume government applications. The faster iteration times, lower costs, and reduced risk provided by the ViArray structured ASICs has helped to maintain the relevance of a 0.35-um radiation-hardened foundry.*

Keywords: radiation hardened ASIC; structured ASIC; mask-programmable ASIC; 3D ASIC.

Introduction

In the early 2000s, industry experts projected that structured (or mask programmable) ASICs would gain a sizable share in the electronics market by the end of the decade [1]. With a few notable exceptions [2,3], those predictions did not materialize in the commercial sector due to silicon costs continuing to dominate the economics of high-volume ASIC production in leading-edge foundries [4]. Also in this same time period, a number of radiation-hardened structured ASICs were introduced, with mixed market success, attempting to target low-volume aerospace/military markets [5,6,7,8,9]. This paper describes one of these radiation-hardened devices, the ViArray, the challenges encountered during its development, its evolution into a high-reliability product family, and the economic drivers that have enabled its success [10,11,12,13].

Sandia's ViArray program began in 2004, following an internal study that revealed system customers were increasingly delaying their ASIC development activities until very late in the system design cycle. Their reasons for delaying ASIC work included the following: (1) high NRE costs for realizing a custom ASIC, (2) long lead times for producing a custom ASIC, (3) frequent requirement changes impacting the ASIC design, and (4) the use of commercial FPGAs for early prototype system builds. However, this practice placed an excessive amount of technical, schedule, and cost risks on the custom ASIC that were too frequently realized. A quicker turn, lower cost ASIC technology was needed to bridge the growing gap between commercial FPGA prototyping and production radiation-hardened ASIC devices, and the ViArray was Sandia's proposed solution.

The ViArray structured ASICs are designed for Sandia's CMOS7 foundry technology, which is a radiation-hardened, 3.3-Volt, 0.35-um SOI (Silicon-on-Insulator) process and whose performance parameters can be found in [14]. Like most low-volume foundries that run a wide variety of products, collecting relevant process statistics for low-volume custom ASICs fabricated in the CMOS7 foundry can be a challenge. However, because ViArray base wafers are re-used across multiple low-volume product lots, they reach higher cumulative volumes and improve the ability of the foundry to monitor and control process parameters on production product. In addition, due to the lower cost of fabricating a ViArray ASIC, the number of ViArray wafer starts significantly exceeds that of custom ASICs, improving the statistical confidence of ViArray product.

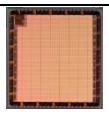
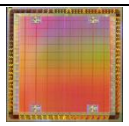
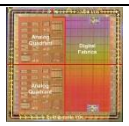
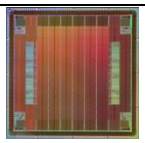
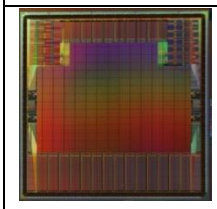
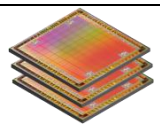
ViArray Device	Specifications	Status
 VA260	Digital Platform 10x11-mm die 4M transistors 170 I/O	Discontinued [functional prototypes tested]
 Eiger	Digital Platform 12x12-mm die 6M transistors 255 I/O	In production for low-volume, high-reliability applications
 Whistler	Mixed-signal Platform 12x12-mm die 3.5M transistors 255 I/O	In production for low-volume, high-reliability applications
 Custom #1	Digital Platform 14x14-mm die 4M transistors 144 I/O	Discontinued [functional prototypes tested]
 Custom #2	Digital Platform 20x20-mm die 18M transistors 346 I/O	Discontinued [functional prototypes tested]
 3D-Eiger	Digital Platform Eiger w/ 3D TSVs 6-18M transistors 256 I/O	Test & Evaluation

Figure 1: ViArray structured ASIC platform summary.

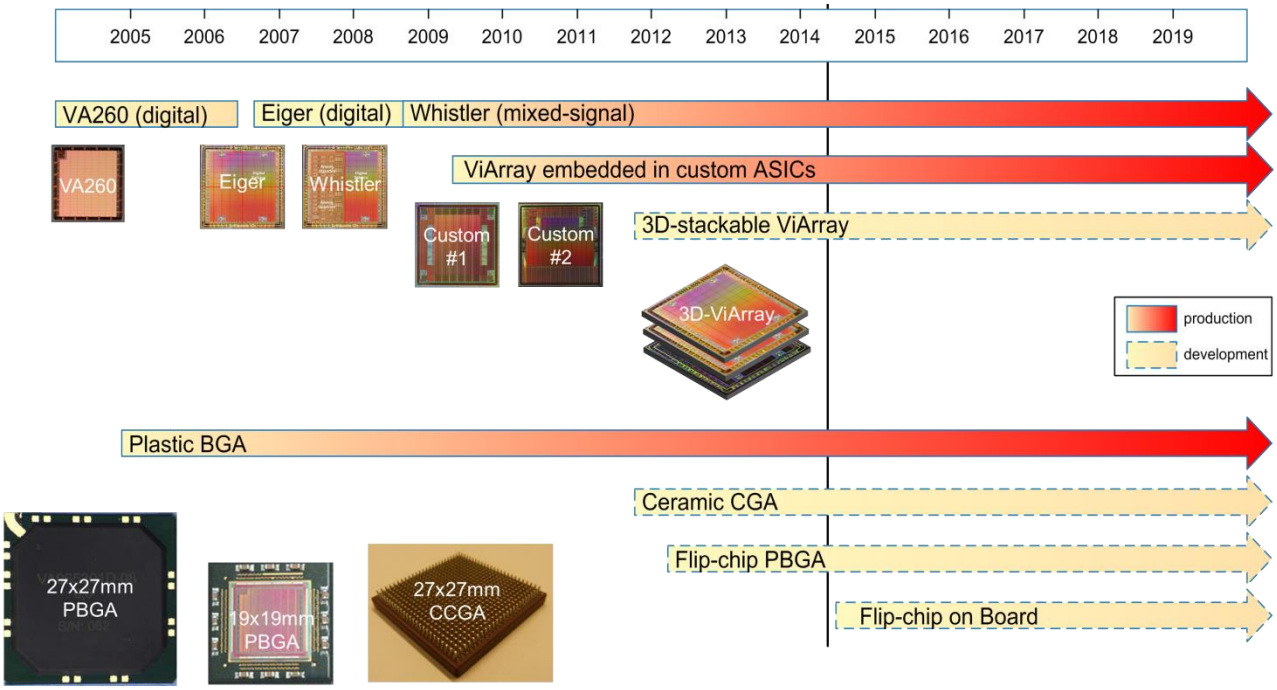


Figure 2: ViArray silicon and package development roadmap.

ViArray Structured ASIC Platforms

Figure 1 summarizes the six generations of ViArray platforms discussed in this paper. All of these devices were designed at Sandia using structured ASIC silicon and tool IP licensed from Triad Semiconductor [3], a leading structured ASIC vendor. The decision to license an industry-proven structured ASIC technology, instead of relying on internal R&D efforts, allowed the ViArray product team to focus immediately on developing ASIC platforms capable of implementing real products, rather than having to demonstrate the viability of the technology with small test structures. Figure 2 shows the ViArray silicon development timeline, along with the associated package roadmap. While additional ViArray platforms continue to be developed to meet unique application needs, the remainder of this section describes only the six platforms that have been verified through silicon testing.

VA260 Platform: This was the first ViArray structured ASIC device, and contained 260K ASIC gates, 354Kb single-port SRAM, 352Kb ROM, 170 CMOS I/O, and an oscillator. Although this platform yielded two first-pass prototype logic designs, several architectural deficiencies were identified, such as the lack of dual-port SRAM and LVDS I/O. However, the most significant defect was the inability to disconnect unused transistors from the power rails, which was an important concern for product yield, reliability, leakage power, and photocurrent generation in radiation environments.

Eiger Platform: This platform included a major re-design of the core ViArray fabric to address all of the deficiencies identified with the VA260 device. In collaboration with Triad Semiconductor, the ability to disconnect all unused transistors from the power rails was incorporated into both the silicon IP and the CAD tool flow. The Eiger device has realized dozens of digital design applications, and has 276K ASIC gates, 368Kb dual-port SRAM, 256Kb ROM, 239 CMOS I/O, 16 LVDS I/O, 4 oscillators, 4 PLLs, and 4 power-on-reset blocks. In addition, the power grid is partitioned into four independent quadrants that can be used for power sequencing and redundancy operations. More detailed technical information on this platform can be found in [12].

Whistler Platform: This platform was derived from the Eiger architecture, but replaces half of the digital resources with analog resources. Its digital resources include 138K ASIC gates, 184Kb dual-port SRAM, 192Kb ROM, 104 CMOS I/O, 16 LVDS I/O, 2 oscillators, 2 PLLs, 4 power-on-reset blocks. Its analog resources include 135 analog I/O, 6 voltage references, 5 current monitors, 4 low-speed ADCs, 4 high-speed ADCs, 8 DACs, 9 32:1 multiplexors, 2 temperature sensors, 64 comparators, 48 amplifiers, 128 analog switches, and 1 analog transient recorder. As described in [12], this platform has greatly simplified mixed-signal ASIC design for instrumentation developers.

Custom #1 Platform: The primary driver for this platform was to develop a ViArray device compatible with legacy low pin count CQFP/PQFP packages, rather than requiring the more advanced (and potentially less mature) high pin count PBGA/CCGA packages employed by the Eiger/Whistler products. This involved re-designing the I/O pads to be universally configurable for CMOS, LVDS, or power/ground as specified by the user. This platform contained 208 universally configurable I/O, 216K ASIC gates, 324Kb dual-port SRAM, 256Kb ROM, 4 oscillators, 4 PLLs, 4 power-on-reset blocks, 6 comparators, 6

amplifiers, 2 voltage references, and 2 DACs. This platform was validated in silicon, but was eventually discontinued due to the maturation of the PBGA/CCGA packages used for the Eiger/Whistler devices and their resulting qualification for high-reliability applications.

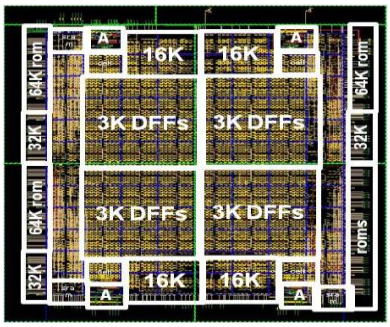
Custom #2 Platform: This platform was developed for digital applications that were too large to fit into the Eiger device. It contained 534K ASIC gates, 712Kb dual-port SRAM, 1.3Mb single-port SRAM, 1.5Mb ROM, 218 CMOS I/O, 64 CMOS or LVDS I/O, 4 oscillators, 4 PLLs, and 4 power-on-reset blocks. The platform was validated in silicon, but ultimately discontinued due to yield and cost concerns.

3D-Eiger Platform: This platform is a 3-dimensional (3D) stackable ViArray device, and is being developed as a lower cost replacement for the Custom #2 Platform. It contains all of the resources that are in the standard Eiger platform and, in addition, contains 42K interconnects on the front and back-side of the die that provide the 3D electrical and power connections. High-density through silicon vias (TSVs) and top-metal bond pads were integrated into the ViArray logic fabric to implement the 3D interconnects. These 3D interconnects were strategically added to empty areas in the 2D Eiger layout so as not to increase its overall die size. This platform has gone through initial 2D and 3D electrical characterization, and further technical details can be found in [13].

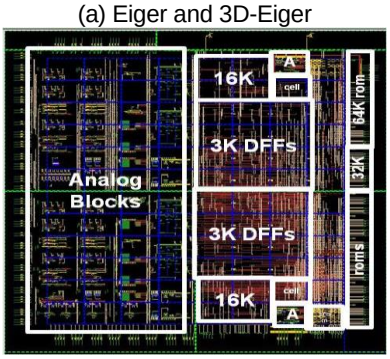
ViArray Platform Qualification

Historically, custom ASIC technologies have required repeated qualification activities for each new ASIC product. The common platform nature of the ViArray, offers further cost and time savings over custom ASICs when faced with product qualification testing. Rather than requiring qualification testing of every unique product design, each of the different ViArray platforms (Eiger, Whistler, etc.) undergoes a rigorous qualification program whose results can be re-used on subsequent product designs. This includes radiation testing, life testing, ESD testing, package testing, etc. While a small number of products may require additional specialized qualification testing above and beyond these generic platform tests, the cost and schedule benefits for leveraging as many of the common platform test results is significant.

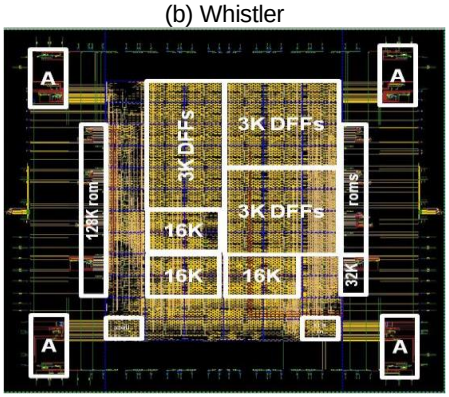
The Common Validation Vehicle (CVV) design is the standard architecture used for ViArray platform validation, characterization, and qualification testing. It is the first design that is implemented on a newly developed ViArray platform, and contains circuits that exercise all of the logic fabric elements and other unique blocks on the platform. In addition, the CVV implements BIST circuits to control the internal flip-flop chains and memories, which helps to standardize qualification testing across platforms. Figure 3 shows the CVV design layouts for five of the six ViArray platforms, illustrating its commonality and scalability across devices with widely differing resources.



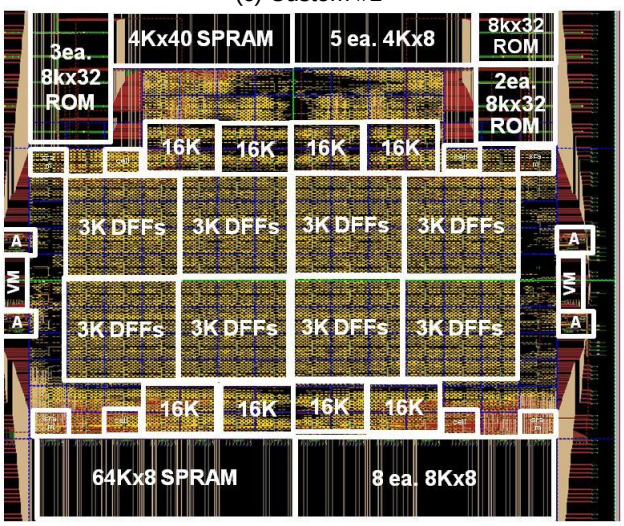
(a) Eiger and 3D-Eiger



(b) Whistler



(c) Custom #1



(d) Custom #2

Figure 3: Common Validation Vehicle (CVV) design layouts used for ViArray platform qualification.

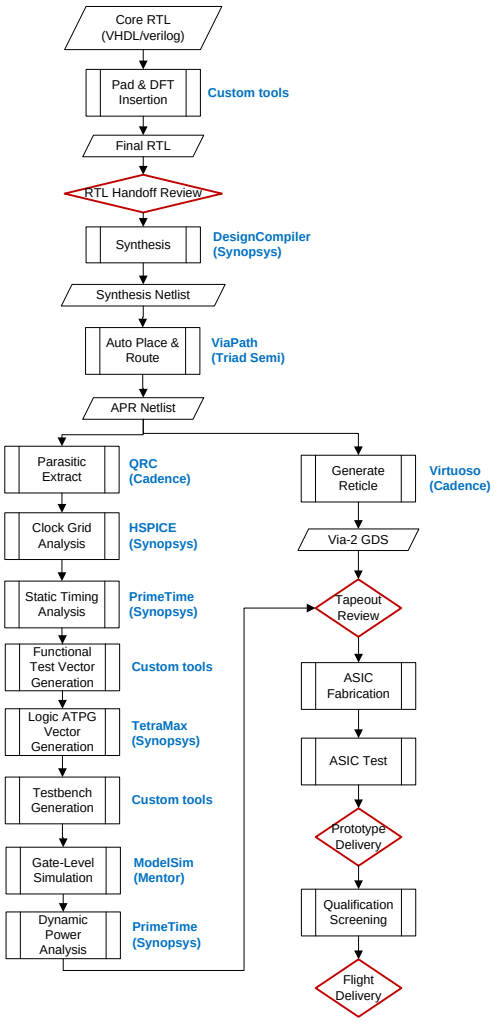


Figure 4: ViArray design and manufacturing flow.

ViArray Platform Infrastructure

Design: The ViArray platforms share a common design environment, which includes standardized design flow scripts, IP cores, and design-for-test architectures. As shown in Figure 4, a combination of commercial and propriety tools are used to implement a ViArray product. ViArray design libraries are regularly updated and checked against silicon characterization data.

Fabrication: Qualified platform wafers are partially pre-fabricated and stored in Sandia's foundry. After a product design has been taped out, the wafers complete their final fabrication steps, which typically takes 2 to 4 weeks. In addition, CVV design wafers are regularly run through the foundry to collect yield data.

Packaging: Although various package types have been developed for the ViArray platforms, the most commonly used are PBGAs for their low-cost and high pin count capability. For hermetic applications, CCGA type packaging is available on select platforms.

Test: Each platform has generic wafer probe cards, package-part load boards, and burn-in boards that are shared across each unique product design. Standardized test programs (stuck-at, IDDQ, delay-fault, etc.) are used to ensure consistent analysis and reporting of yield statistics across designs with a wide range of resource utilizations on the same platform. After adjusting for transistor resource utilization, ViArray ASIC yields are consistent with custom ASIC products run at the same foundry.

Summary

We described six generations of ViArray radiation-hardened structured ASIC platforms that were developed over a ten year period for low-volume, high-reliability government microelectronic applications. These ViArray devices have revolutionized Sandia's approach to ASIC design, fabrication, test, and qualification. The low-NRE and quick-turn properties of the ViArray have greatly reduced risks to system customers, and provided a vehicle to better monitor and predict yield statistics in a low-volume radiation-hardened foundry.

Acknowledgements

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

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