SAND2010-6476C

DARPA/OSD Trusted Foundry Circuit Designers Workshop

Sandia's Trusted Foundry Experience

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Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND2009-0357P

Sandia National Laboratories

Topics

- Sandia National Laboratories and Microsystems and Engineering Sciences Application (MESA) Overview
- IBM Trusted Foundry Design Experience
- FY10 IBM Trusted Foundry Designs
- Trusted Foundry Program Feedback

Sandia National Laboratories and MESA Complex Overview

Sandia National Laboratories

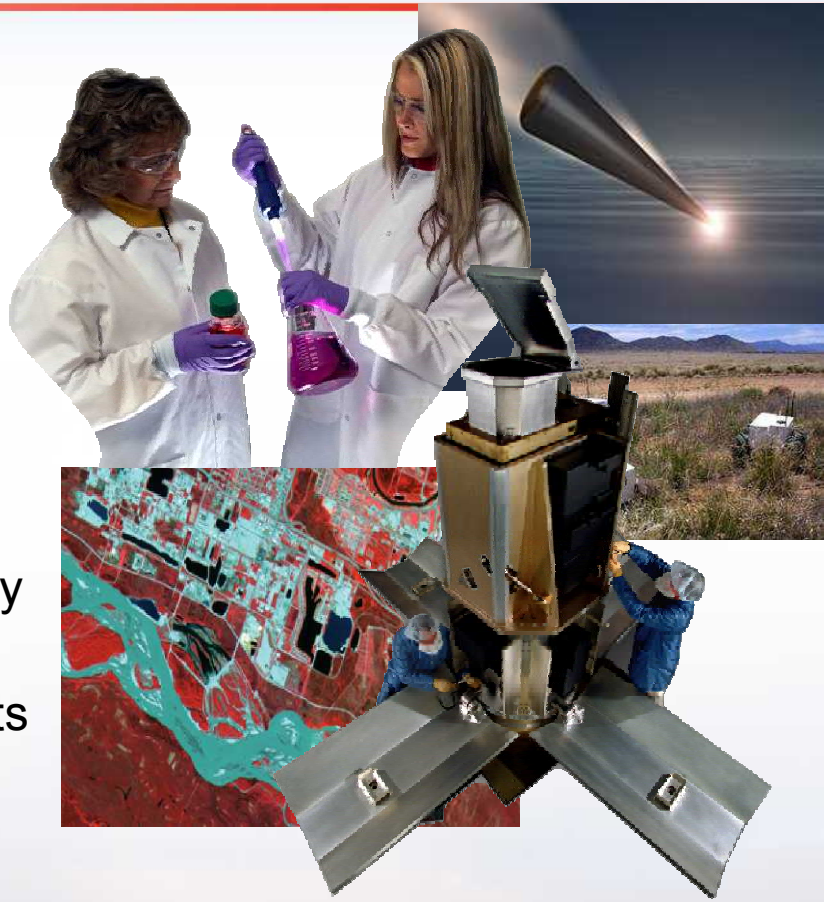
Our Business: National Security

- **Core purpose**
  - to help our nation secure a peaceful and free world through technology
- **Highest goal**
  - to become the laboratory that the United States turns to first for technology solutions to the most challenging problems that threaten peace and freedom for our nation and the globe

Sandia National Laboratories

Technologies for National Security

- **We develop technologies to:**
  - Sustain, modernize and protect our nuclear arsenal
  - Prevent the spread of weapons of mass destruction
  - Provide new capabilities to our armed forces
  - Protect our national infrastructures
  - Ensure the stability of our nation's energy and water supplies.
  - Defend our nation against terrorist threats



Sandia's Administration

- AT&T: 1949–1993
- Martin Marietta: 1993–1995
- Lockheed Martin: 1995–Present

Government-Owned Contractor-Operated (GOCO)

Federally Funded Research & Development Center (FFRDC)

The MESA complex serves a unique role for the U.S. Government

Trusted Systems for National Security Customers


Nuclear Weapons


Non Proliferation Payloads


MicroChemLab-based Sensor system

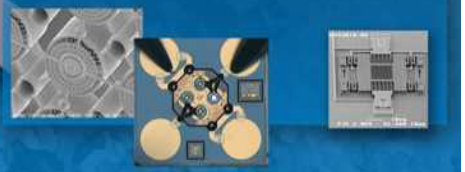
Intelligence Customers

Trusted COTS and Custom Electronic Components

- Assure performance, quality and reliability meet system requirements
- Custom Magnetics, Capacitors, RF, Optical, Interconnects, Transducers, Clocks, connectors & cables

Trusted R&D

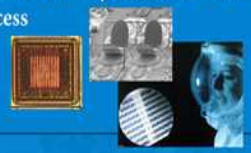
- Chip Scale Atomic Clock
- Ion Traps for Quantum Computing
- Nano-G Accelerometers
- Acoustic Bandgap Science
- Advanced Sensors for Chem/Bio Detection



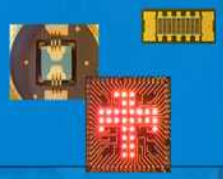
Trusted Fabrication

Custom, low-volume, high-reliability

- Silicon custom & rad-hard process technologies for digital, analog, mixed signal and micromachining
- DOE/NNSA War Reserve Supplier
- Trusted Foundry accreditation in process



- III-V semiconductor Epitaxial Growth and processing
- Photonics, Optoelectronics
- MEMS, VCSELs, Specialized Sensors



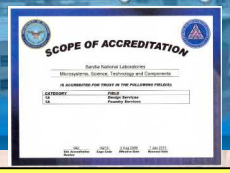
Trusted Design

- Secure design facility with disciplined and trusted design flow and methodologies
- Trusted Structured ASIC
- Design for fabrication at Sandia or at Trusted Foundries: IBM, Honeywell & National

Trusted BEOL

- Advanced Packaging
- 3-D Integration
- Test & Validation
- Failure Analysis & Reliability Physics
- Rad Effects & Assurance
- Anti-Tamper

As part of the DOE NNSA Nuclear Weapons Complex Transformation:
"SNL will be the Center of Excellence for Non-Nuclear Design and Engineering ..."



MESA bridges science to systems, providing an environment where multidisciplinary teams create ***microsystems-enabled solutions*** to the nation's most challenging problems

IBM Trusted Foundry Design Experience

Sandia National Laboratories

Sandia was one of the 1st users of the IBM Trusted Foundry and is a consistent user

- **Sandia was one of the 1st users of the IBM Trusted Foundry**
  - Helped IBM and TAPO define process for using IBM Trusted Foundry
  - One of the drivers behind IBM getting on-shore embedded non-volatile memory (Flash)

- **Sandia has designed a diverse set of ICs at the IBM Trusted Foundry since the start of the TF program**
  - FY07 (and earlier) Designs
    - 5 at IBM CMOS8RF, 130nm technology
    - 1 at IBM CMOS9LP, 90nm technology
  - FY08 Designs
    - 6 at IBM CMOS8RF, 130nm technology
    - 1 at IBM CMOS9LP, 90nm technology
  - FY09 Designs
    - 4 at IBM CMOS8RF, 130nm technology
    - 4 at IBM CMOS9LP/SF, 90nm technology
    - 1 at IBM CMOS10SF, 65nm technology
  - FY10 Designs
    - 3 at IBM CMOS8RF/NV, 130nm technology
    - 1 at IBM CMOS9LP, 90nm technology
    - 1 at IBM CMOS10LPE, 65nm technology
    - 3 at IBM CMOS12SOI, 45nm technology
  - FY11 Projected Designs (so far)
    - 1 at IBM CMOS9LP, 90nm technology
    - 1 at IBM CMOS12SOI, 45nm technology

TAPO

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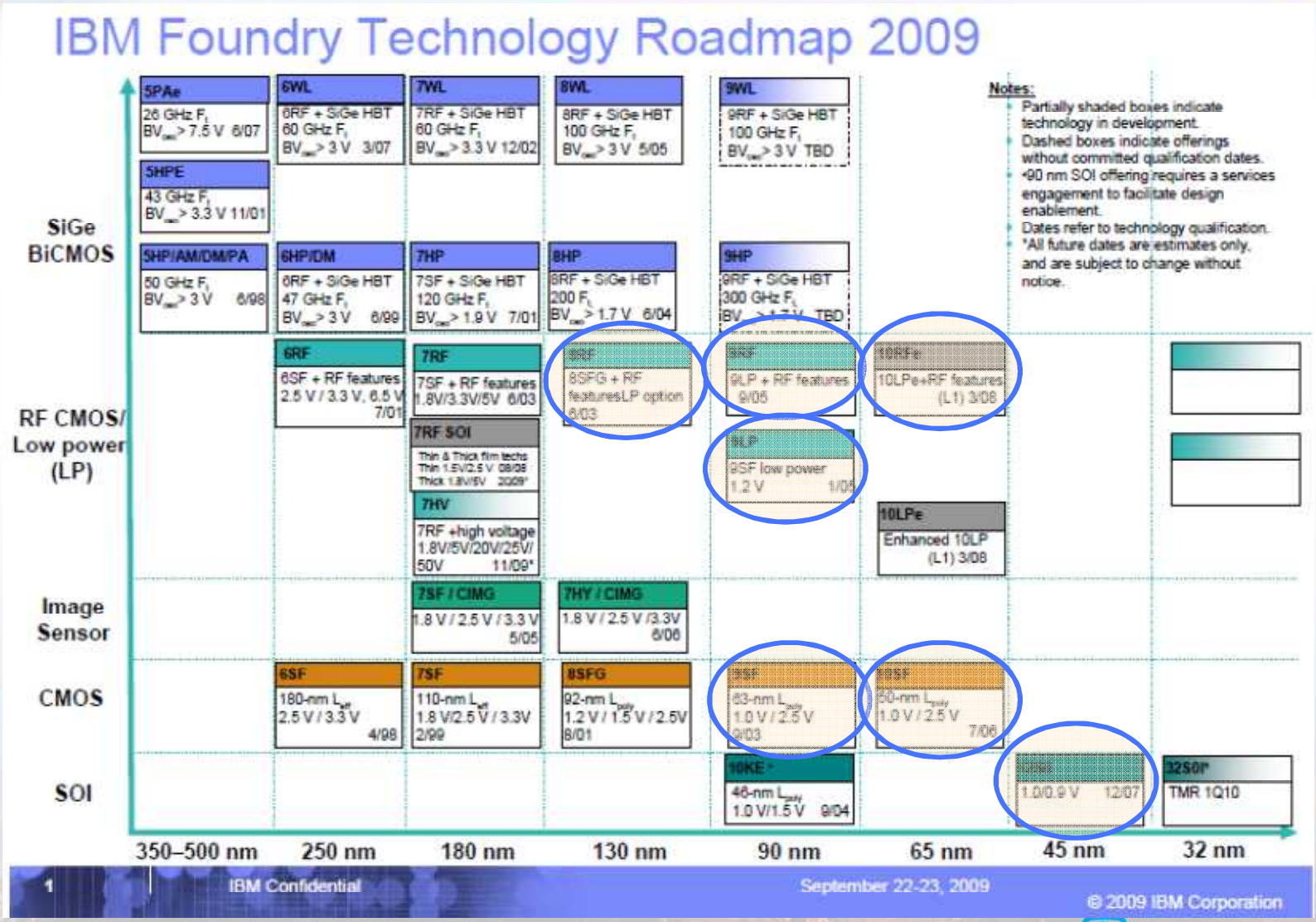
IBM

Sandia has experience at several of the advanced technology nodes



Sandia designs were on a number of IBM TF MPW runs this Fiscal Year

FY10 TRUSTED ACCESS PROGRAM OFFICE 'MULTI PROJECT WAFER SCHEDULE

Technology	FY10 Quarter 1			FY10 Quarter 2			FY10 Quarter 3			FY10 Quarter 4		
	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep
7HP		7HP 10A 2009-11-02							7HP 10B 2010-06-07 2010-11-03			
8RF		8RF 10A 2009-11-16 2010-04-28				8RF 10B 2010-03-15 2010-08-10				8RF 10C 2010-07-01 2010-11-29		
8HP	8HP 10A 2009-10-12 2010-03-26			8HP 10B 2010-01-18 2010-06-16			8HP 10C 2010-04-12				8HP 10D 2010-08-02 2011-01-12	
8NV							8NV 10A* 2010-04-01 2010-08-24					
9SF			9SF 10A 2009-12-01 2010-05-19						9SF 10B 2010-06-28 2010-12-07			
9LP				9LP 10A 2010-01-05 2010-05-28						9LP 10B 2010-07-12 2010-12-07		
10SF												10SF 10A 2010-09-03 2011-03-04
10LPe					10LPe 10A 2010-02-01 2010-07-19							
12SO								12SO 10A 2010-05-10 2010-11-02			12SO Hybrid* 2010-08-16 2011-02-18	
32nm Advance Access												32nm Hybrid 2010-09-15 2011-04-15

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FY10 IBM Trusted Foundry Designs

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Key Data Processor

- **Program Description**

  The Key Data Processor is a System-On-a-Chip processor system designed to securely host the cryptographic algorithms that ensure the integrity, availability and confidentiality of the Military GPS for the Selective Availability Anti-Spoofing Module (SAASM).

- **Program Goal**

  The KDP goal is to provide a secure, NSA-certified, IP block for integration into a single-chip SAASM or other security applications. The KDP can host a wide variety of field-programmable application software packages.

- **Program Sponsor**
  - Department of Defense

KDP-III and KDP-IV Test/Demo Chips

- **Project Features**

	KDP3BTA	KDP4BTA
IBM Process:	CMOS 8RF	CMOS 9LP
Feature size:	130 nm	90 nm
Design size:	24.8 mm^2	19.4 mm^2
Operating conditions:	-55ºC to 125ºC 1.5V ±10%	-55ºC to 125ºC 1.5V ±10%
Gate count:	3.6M	7.2M
Power:	62-200 mA	20-80 mA
Frequency:	48 MHz	48 MHz
Package:	388 PBGA	388 PBGA 416 PBGA

- **History**
  - 7 KDP-III tape-outs from 2007-2009
  - 4 KDP-IV tape-outs from 2008-2010

- **Trusted Foundry IP used in SoC application**

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Bottlecap Program

- **Program Description**

  Develop and fabricate a set of test characterization vehicles (TCVs) in the IBM 130nm (8RF) and IBM 45nm (SOI12SO) technology that

  - allows for the assessment of the basic technology elements and
  - allows for the characterization of the reliability and repeatability of measured electrical parameters.

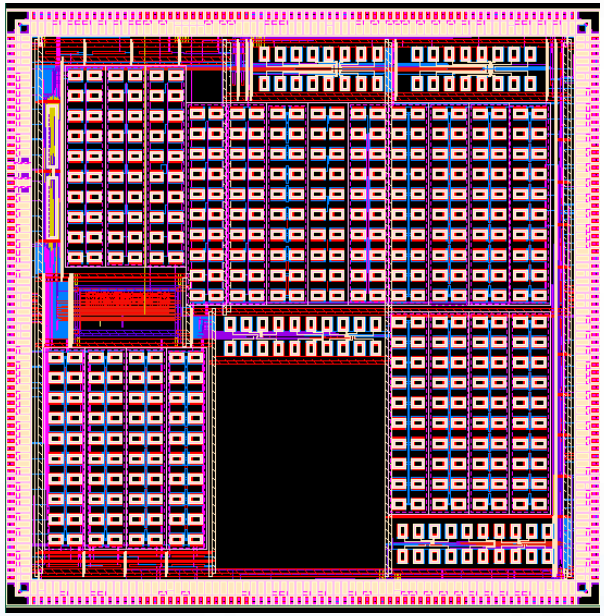
- **Program Goal**

  Enable the trusted design community to develop better assessment methods in the following areas of interest:

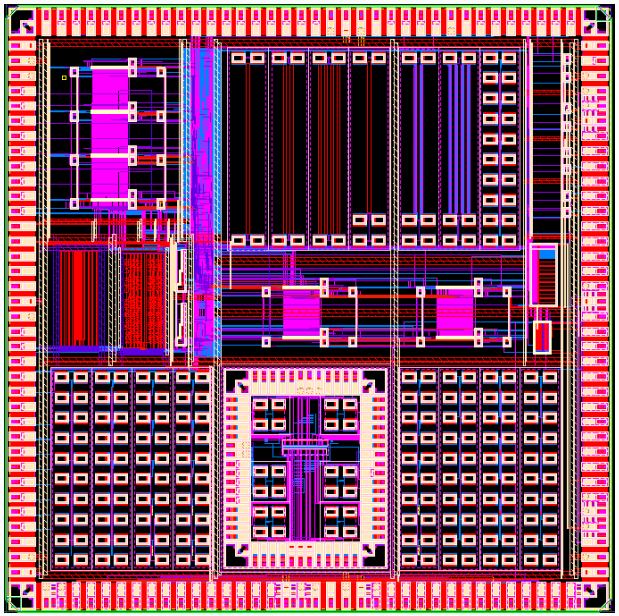
  - Fundamental device responses to various stimulus.
  - Device behavior in various circuit topologies including those that typically apply to amplifier gain-bandwidth and basic gate response.

- **Program Sponsor**
  - Department of Defense

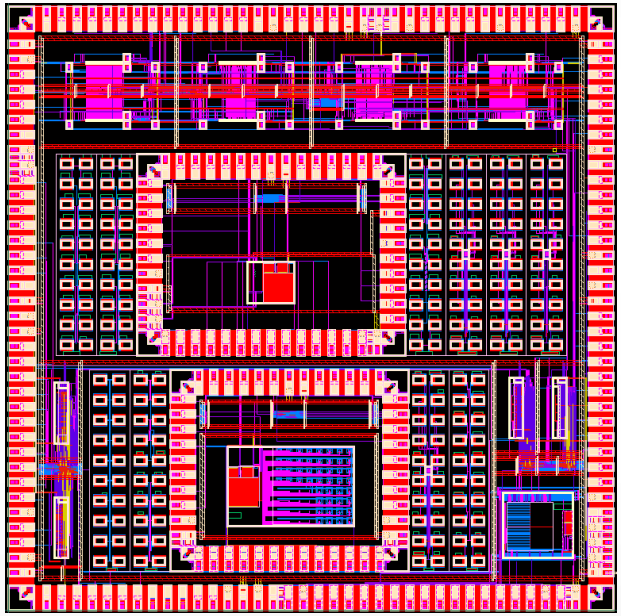
Bottlecap Testchips



- **BCTC1**
  - 8RF09B
  - Artisan RA1SHD, 16k x 8
  - EFUSE, 128 bits
  - Basic analog functions
  - Basic digital functions

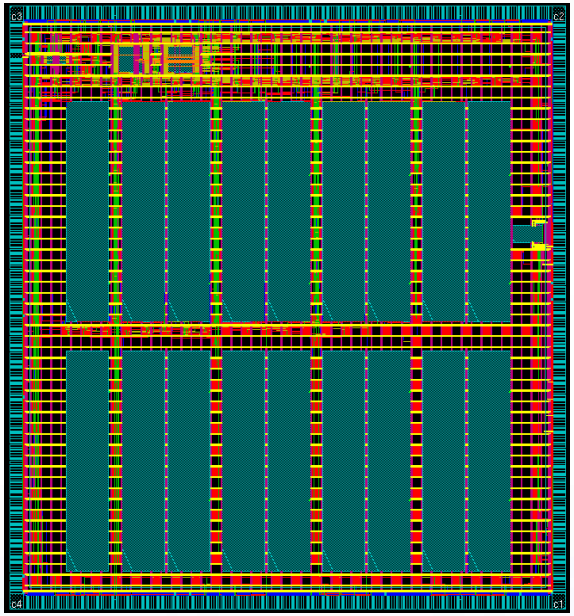


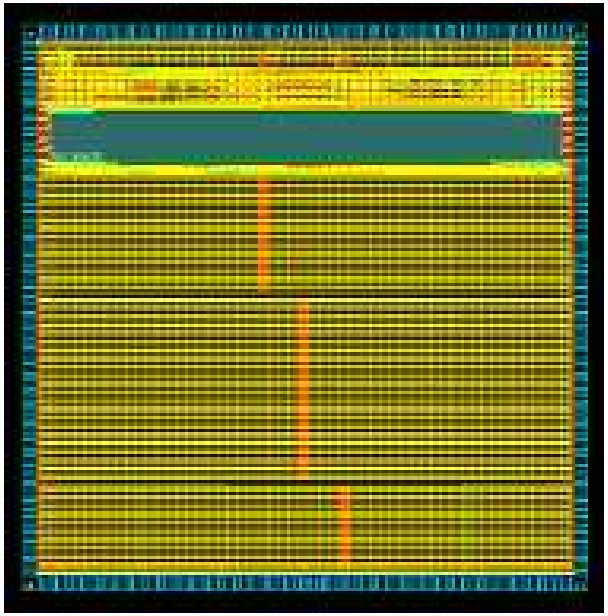
- **BCTC2**
  - 8RF09C
  - Artisan RA1SHD, 16k x 8
  - Custom SRAM, 128 x 8
  - Voltage amplifiers
    - High power
    - High bandwidth
  - 3.3V combinatorial logic



- **BCTC3**
  - 8RF09D
  - Mature analog circuits with digital control
    - EFUSE, 128 bits
    - RF oscillators
    - Analog to digital converters
    - Voltage comparators

Bottlecap Testchips continued evolution





- **BCTC4**
  - 12SO10A
  - IBM SRAM:
    - SRAM1DCUN1638400832 (16k x 8)
  - IBM: EFUSE512
  - Voltage amplifiers
  - Basic digital functions

- **MASH1**
  - 12SO10A
  - Linear Feedback Shift Register
    - High speed pseudo-random bit pattern generator
  - High speed interconnect
  - Transmitter/ Receiver pairs

Memory (MMA)

- ***Program Description***

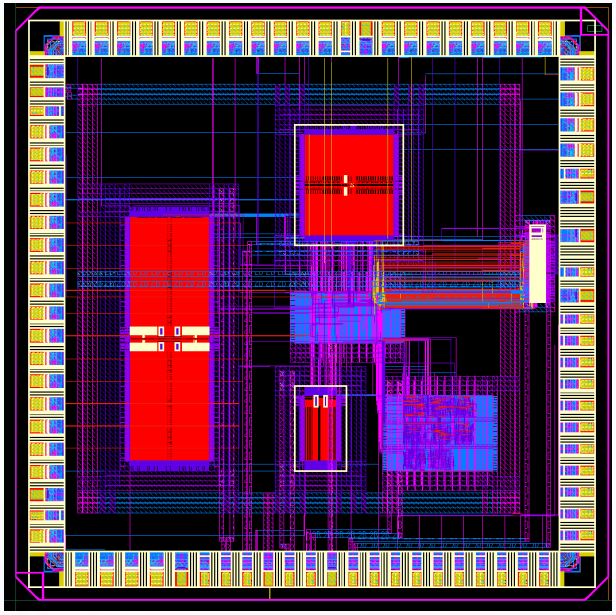
  Develop and fabricate a set of test characterization vehicles (TCVs) in the IBM technologies to analyze and evaluate the various types of memory.

- ***Program Goal***

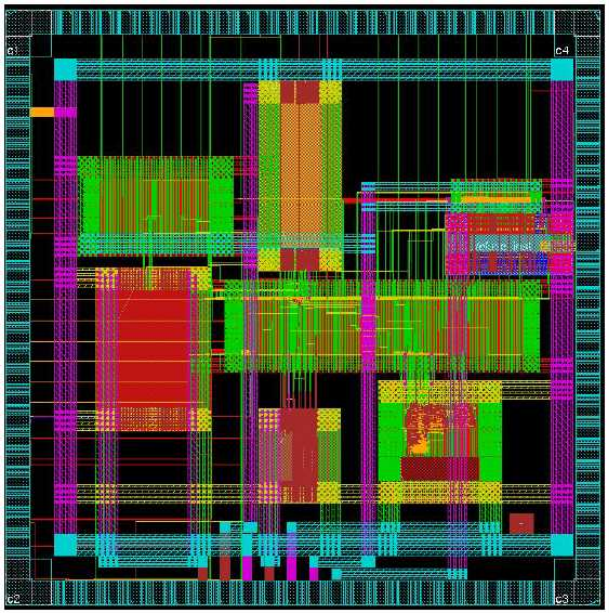
  The MMA program goal is to provide the characterization data to future trusted foundry users.

- ***Program Sponsor***
  - *Department of Defense*

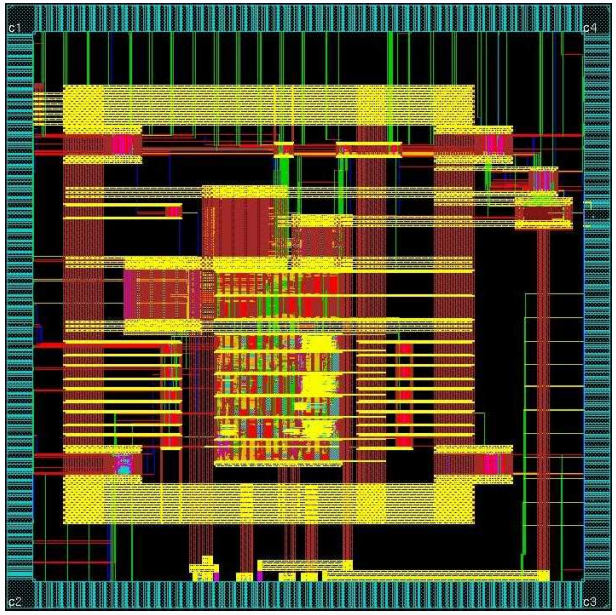
MMA Prototype Chips



- **MMA90**
  - 9LP09A
  - Artisan Single-Port SRAM
  - Artisan Dual-Port SRAM
  - Artisan ROM
  - IBM 128-Bit EFUSE
  - 1K ARM Standard-Cell Register Files
  - ARM IO Cells



- **MMA65**
  - 10LPE10A
  - Virage Single-Port SRAM
  - Virage Dual-Port SRAM
  - Artisan ROM
  - IBM 128-Bit EFUSE
  - 1K Virage Standard-Cell Register Files
  - Aragio IO Cells



- **MMA45**
  - 12SO10A
  - IBM Single-Port SRAM
  - Artisan Dual-Port SRAM
  - Artisan ROM
  - IBM 512-Bit EFUSE
  - 1K ARM Standard-Cell Register Files
  - ARM IO Cells

IBM Trusted Foundry and TAPO Feedback

Sandia National Laboratories

TAPO IBM Trusted Foundry Program Positive Feedback

- Ease of access to modern process nodes has been extremely beneficial.
- Customer was pleased with design validation and accessibility to advanced process nodes.
- Extensive use of IP was very beneficial in the success of this program (PLL's, Memories, Standard Cells, IO, etc).
- Very willing to help out and find answers to problems. Overall it has been a very positive experience.
- TAPO has been very responsive to our inquiries and willing to work with us to meet our schedule and need dates.
- TAPO has been very supportive in obtaining required IP…and providing additional MPW runs to support our program need dates.

TAPO IBM Trusted Foundry Program Areas for Improvement

- CMOS9LP yield has been low, attributed to multiple process issues and design issues in the IBM standard IP offerings.
- CMOS9SF/LP design manual had significantly more errors than other comparable manuals (e.g. IBM 130nm).
- The RTM (Release To Manufacturing) cycle time is often much longer than anticipated, delaying silicon availability. More frequent updates in RTM targets would be helpful.

The End
Thank You