SAND2010-7604C

Flexible Space Computing Architectures and the Role of FPGAs

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Agenda

- Overview
- Hardware development
- Communication standard
- Common development environment
- Early flight opportunities (MISSE)

National Nuclear Security Administration

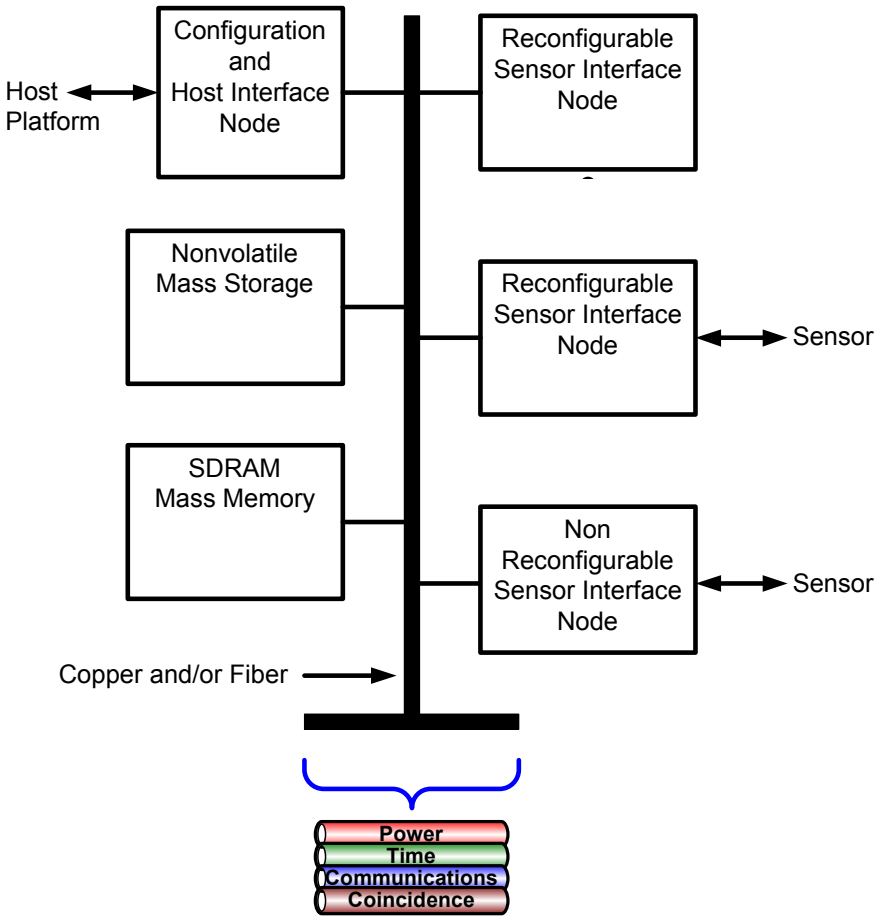
Motivation for JAS

- Sandia and Los Alamos provide sensing and processing systems in support of the NA-222 Space Nuclear Detonation Detection (SNDD) mission
- Develop a standard architecture, supported by both laboratories, that is common to all of NA-222's satellite payloads
- Support a wide range of data communication applications (kbps to Gbps)
- Provide scalable on-board processing to correlate data from many different sensor types
- Provide mechanical flexibility to integrate on a variety of hosts
- Support multiple redundancy options
- Enable common unified approaches to design, fabrication and testing
- Reduce schedule and cost for development, integration, and test
- Provide basic communication and processing infrastructure to enable designers to develop at the application level

Provide SNDD with the flexibility and technology to support its mission (GPS, GEO) and future opportunities (Dem/Val)

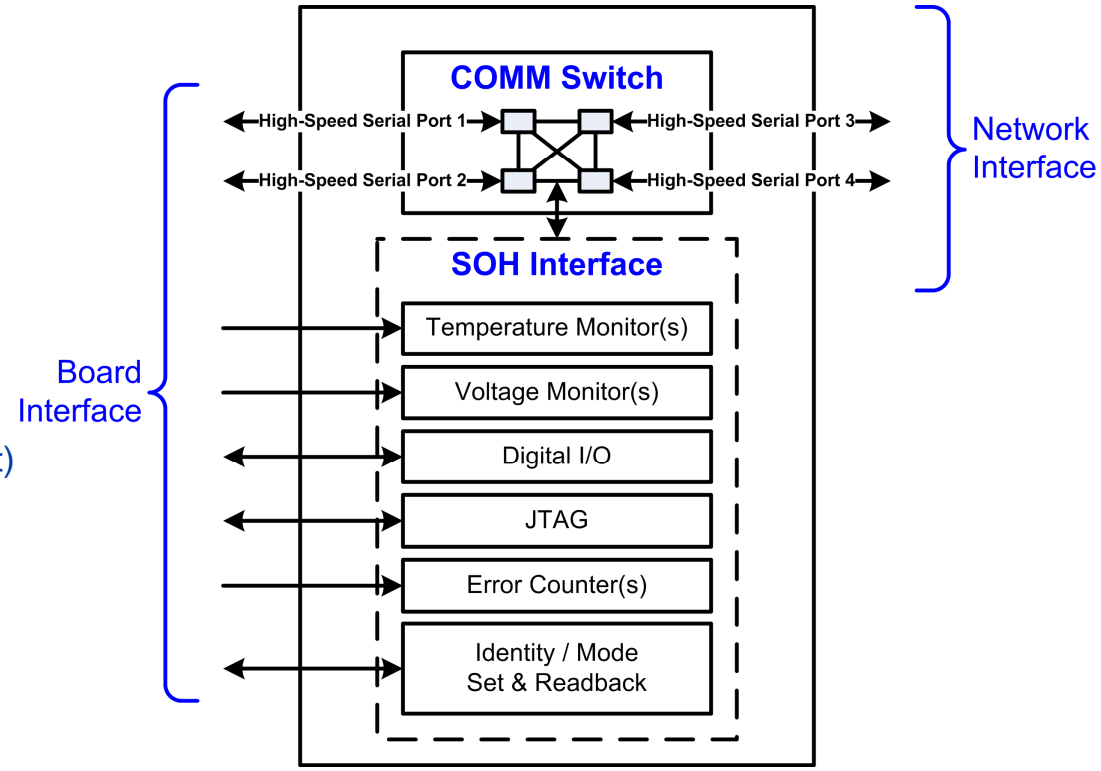
Joint Architecture Standard (JAS)

- Modular, node-based architecture
- Standard HW designs for implementing satellite payload interface, processing and data communication functions
- High-speed serial data interfaces and industry standard protocols
- Numbers and types of nodes determined by system requirements
- All nodes have two common hardware components:
  - System Monitor and Communications port (SMAC)
  - Point-of-Load (POL) Power Converters
- Supports Rad-Hard ASIC processors or FPGA-based soft-core signal processors
- Supports hardware description language (HDL) for custom logic designs
- Includes mass SDRAM and non-volatile memory nodes
- COTS-based development and test environment for rapid system demonstration



Common Node Interface

- SMAC
  - "Always On" to enable all communication traffic and platform management
    - → SOH
    - → Commanding
    - → Mission data
    - → Configuration interface
    - → Board identity/mode
  - Early implementation:
    - → Actel based SpW IP (routed)
    - → Virtex based RapidIO IP (point-to-point)
  - Enhancing technology:
    - → Rad hard switch
    - → Lead to integrated solution
- POL
  - Single Voltage to Node
  - Provides better regulation for low voltage, high current logic
  - Very efficient (approaching 90%)



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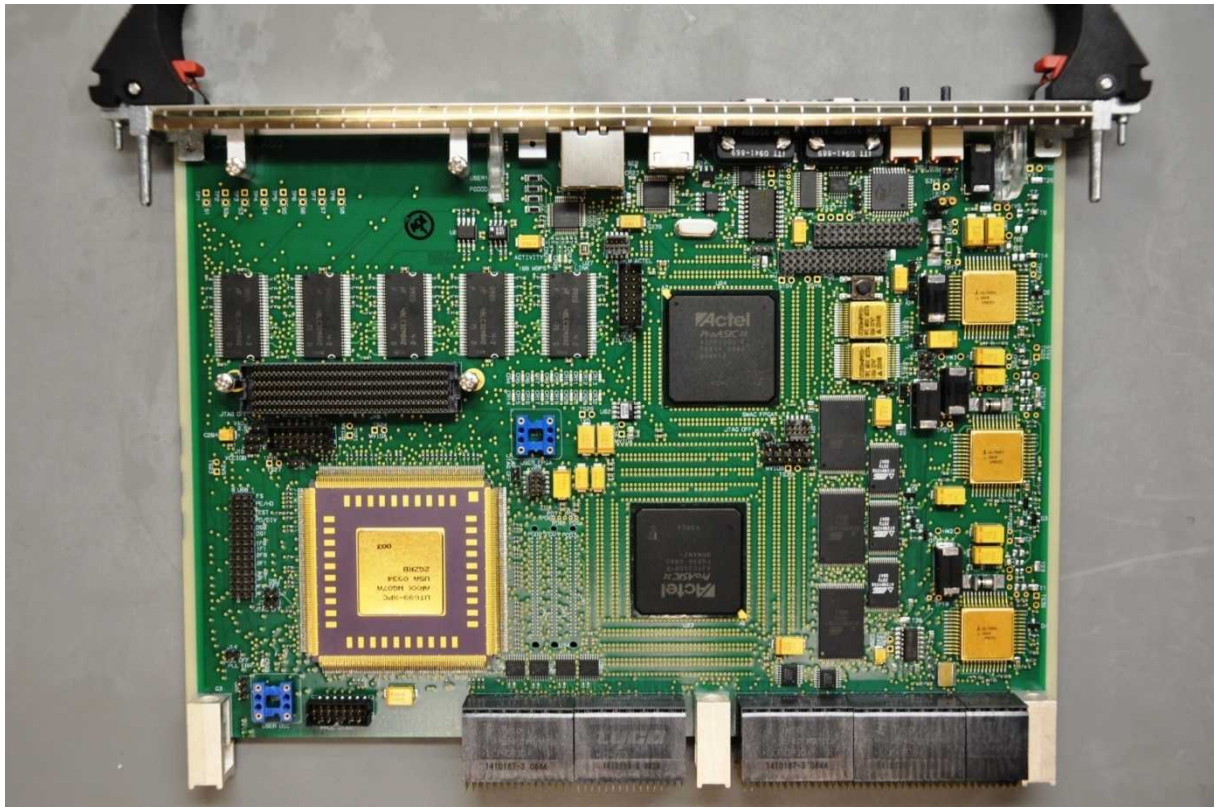
Node Hardware

- 5 node types
  - Rad hard CPU (Leon 3)
  - Reconfigurable FPGA (Xilinx V5QV)
  - One time programmable (OTP) FPGA (Actel RTAX)
  - Non-volatile memory (RTAX memory controller)
  - SDRAM (V5QV memory controller)
- 6U VPX form factor (9.2” x 6.3”)
- Common SMAC and POL devices
- Mezzanine connector for sensor interfaces, memory expansion, etc.
- Soft-core processor support in FPGAs



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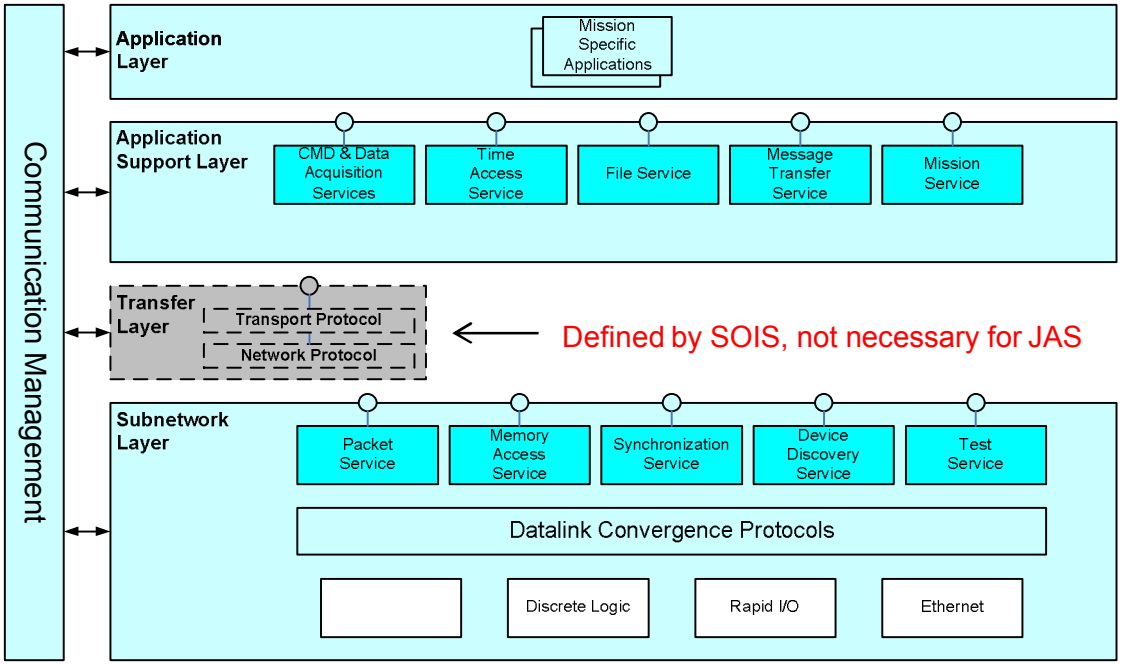
JAS Communications Services Specification

Configures payload devices and communication infrastructure

Monitors payload configuration and responds to changes such as faults

Provides storage of payload state for use by project applications



Project Applications (NDS, …)

Provides a consistent interface to Project Applications

Provides a standard interface to payload hardware and communication interfaces

- This specification is where SNL and LANL will standardize communication interfaces
- Based on CCSDS Spacecraft Onboard Interface Services (SOIS) 850.0-G-1.1
- Common interfaces and data formats to the services promote application reuse
- Services are light-weight which means low resource overhead
- Can be implemented in either hardware (HDL) or software applications
  - Amount of stack implemented is based on application needs

Physical and Data Link Layers

- SpaceWire
  - Intermediate BW protocol (2 Mbps - ~ 400 Mbps)
  - Lower layer protocol definition only (physical layer and data link layer)
  - Needs additional protocols for network and transport layers
- Rapid IO
  - High BW protocol (~600 Mbps – 10 Gbps)
  - Full featured protocol definition up to application layer
  - No additional protocols needed
  - Demonstrated transport of JAS packets over SRIO

SpaceWire Packet Protocols

- SpaceWire requires additional protocols to match Rapid IO capabilities

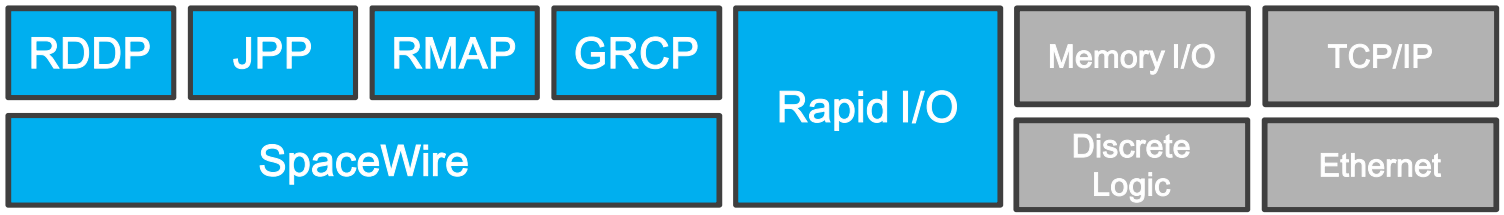
- **Reliable Data Delivery Protocol –** provides "assured" delivery of data across a SpaceWire link
  - Assured delivery includes data retransmission on errors
  - Adds 9 byte header/footer to JAS packet (~2% network overhead)
  - Developed and tested a complete software implementation of the NASA v2.1 spec
  - Partial VHDL implementation has been tested

- **JAS Packet Protocol –** provides "best effort" delivery of data across a SpaceWire link
  - Very simple protocol designed to encapsulate JAS Packets directly into SpaceWire packets
  - Used to transmit less tolerant data streams with less overhead and resource usage
  - Best effort delivery implies limited capabilities such as no retransmission
  - No additional header/footer fields to JAS packet (~1% network overhead)
  - Implemented and tested in software

SpaceWire Memory Access Protocols

- **Remote Memory Access Protocol –** read and write to register-based devices across a SpaceWire data link
  - An example of a register-based device is the SMAC
  - Demonstrated SMAC query in the network using RMAP
  - Tested Leon RMAP interface via PC driver
  - Enabled Leon SW debugging over RMAP
  - Obtained and began testing software library for RMAP

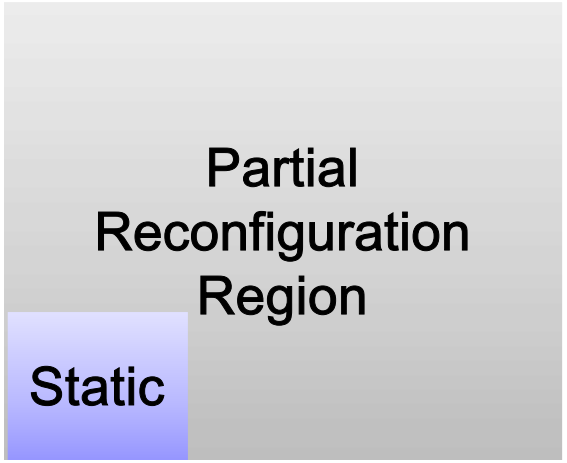
- **Goddard Router Control Protocol –** read and write to configuration registers of Goddard SpaceWire routers
  - Temporary protocol required by current SpaceWire router implementation
  - Goal is to replace current router and standardize on RMAP for register based access
  - Implemented and tested GRCP to discover SpaceWire devices on the network as well as configure them for SpaceWire Logical Addressing (SLA)



Data Link Protocol Stack Summary

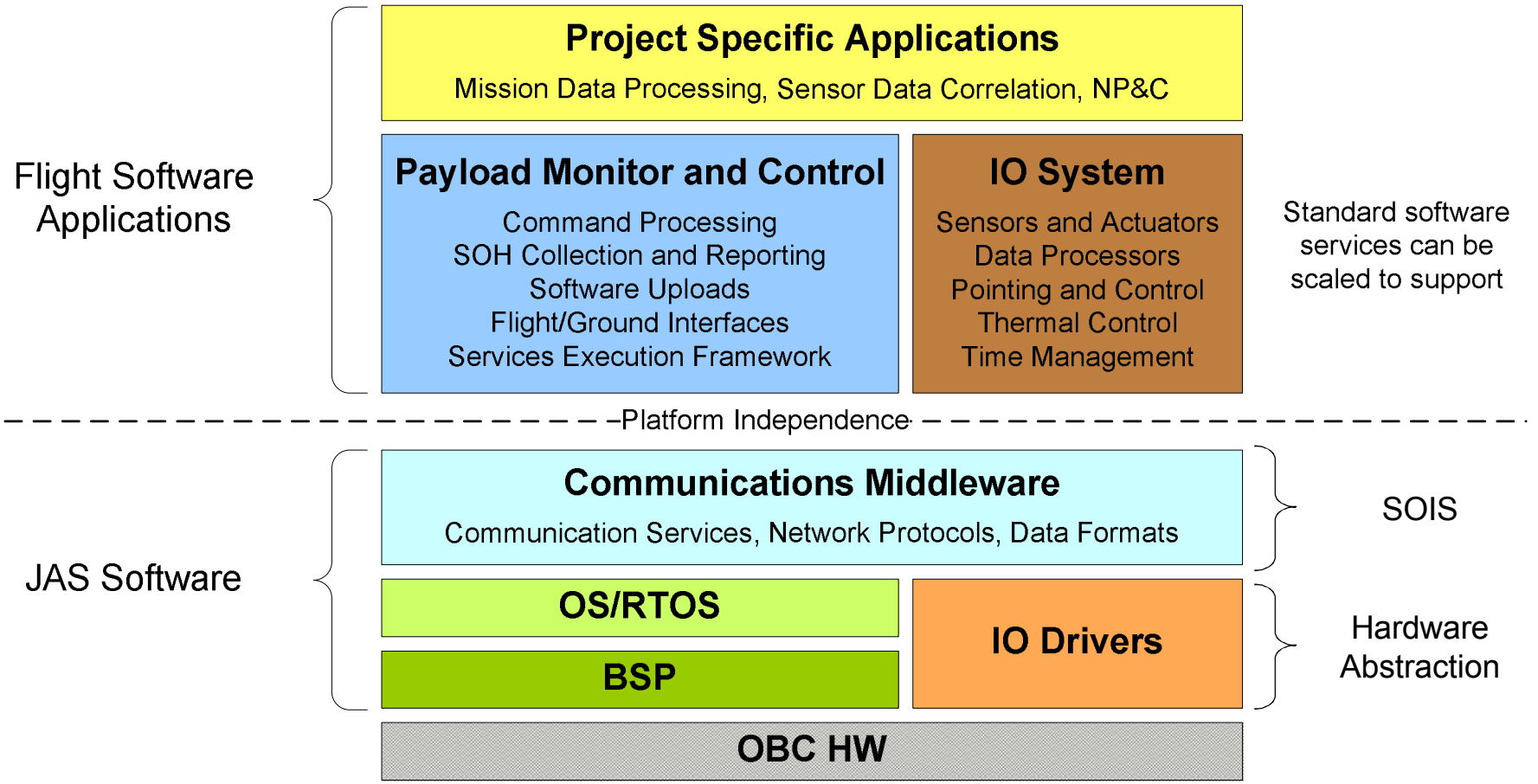
File Service and Partial Reconfiguration

- Partial Reconfiguration
  - Boot RP node from small local static region – configure remotely with partial region bit file
  - Implemented decompression core into static region for use with compressed, partial bit files
  - Bit files are stored remotely on an NV node and are accessed by the CH through the File Service



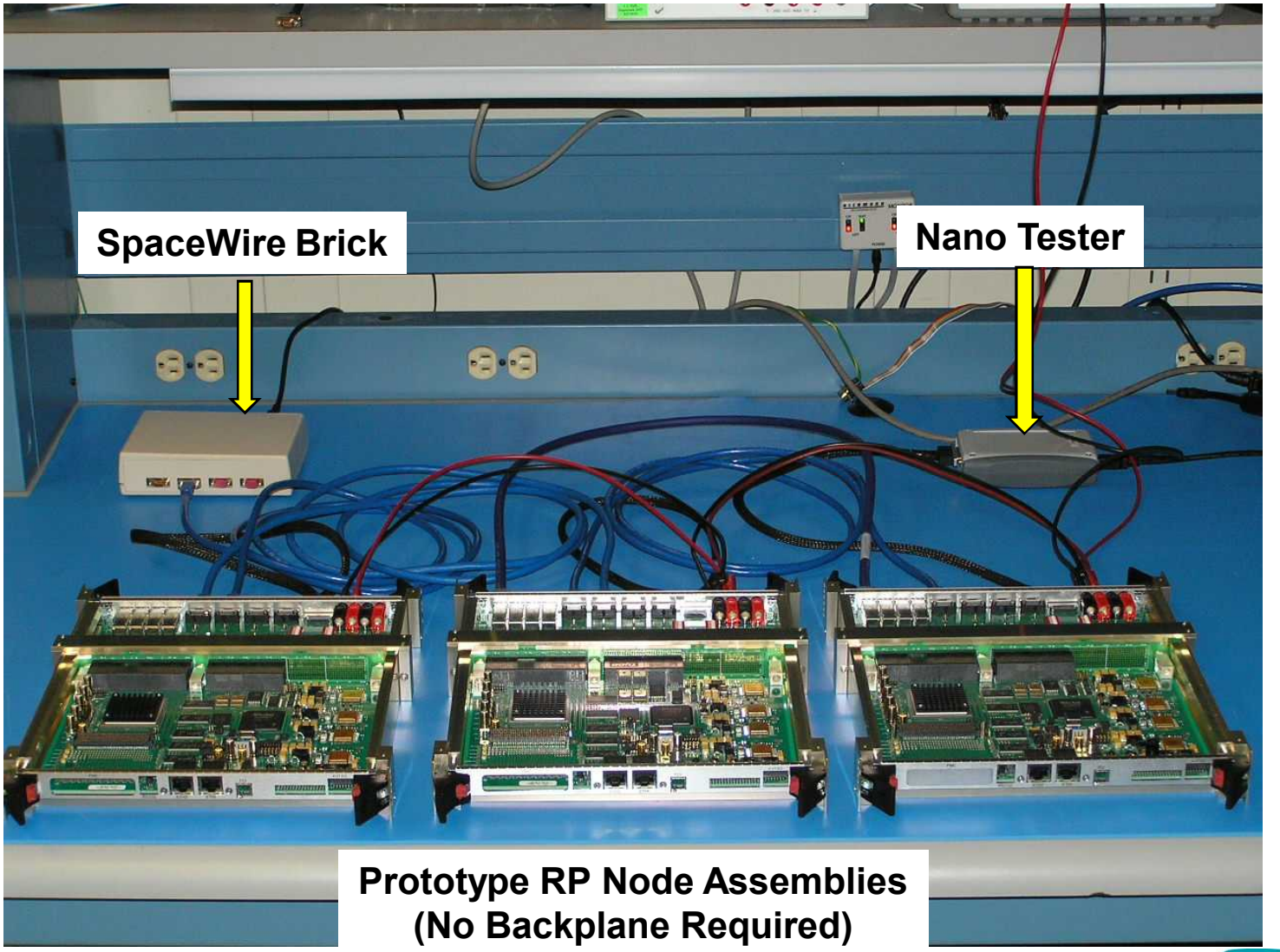
- Demonstrated ability to remotely transfer a VHDL bit file from the CH to an RP node over RDDP and have it load and execute
- Near term goal to integrate remotely accessing the bit file from an NV instead of local Flash

Payload Software Architecture



JAS software provides an abstraction layer between payload hardware and project-specific applications making them more portable

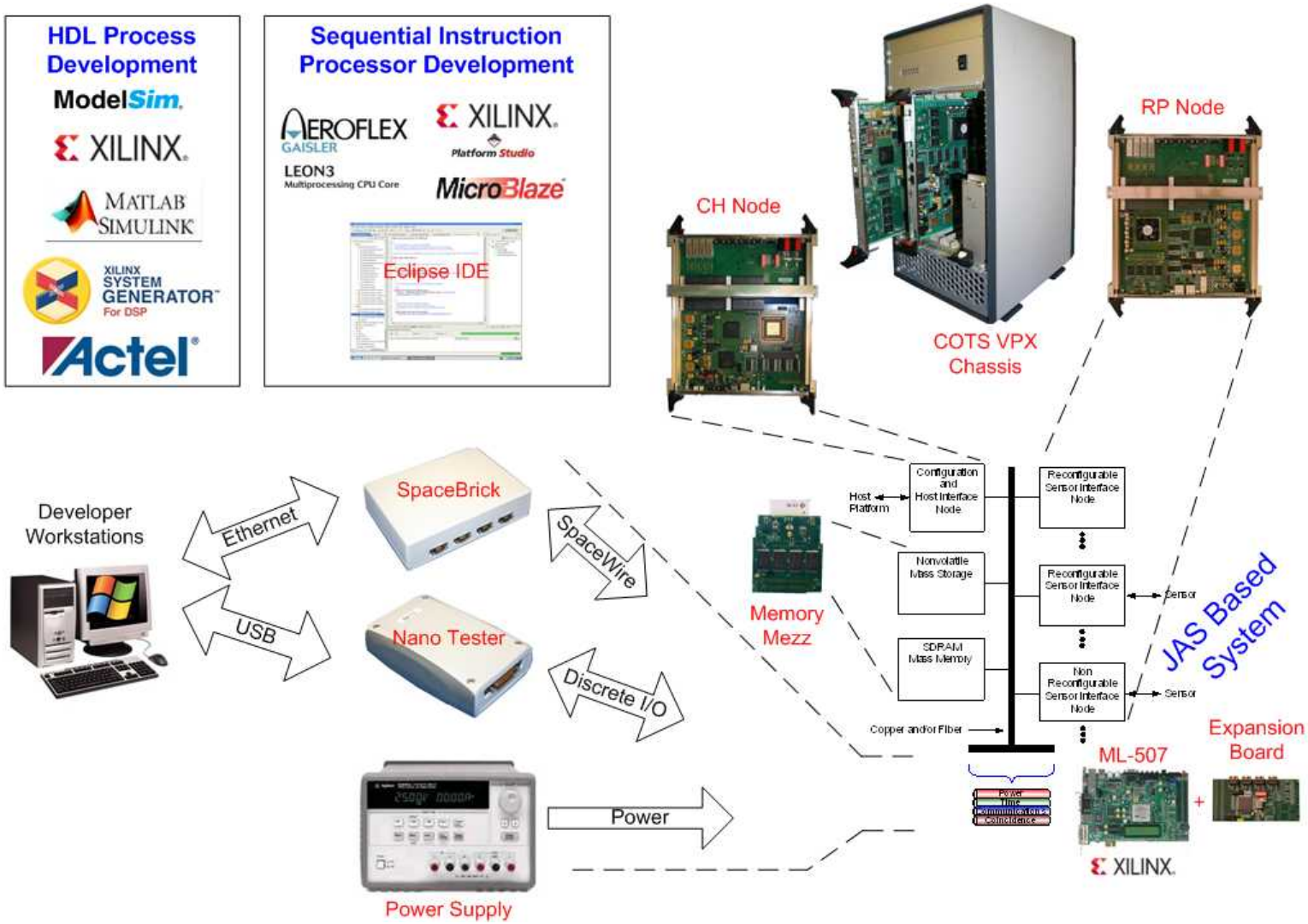
Multi-node Test Bench



Prototype RP Node Assemblies (No Backplane Required)

Unclassified Unlimited Release

JAS Common Development Environment



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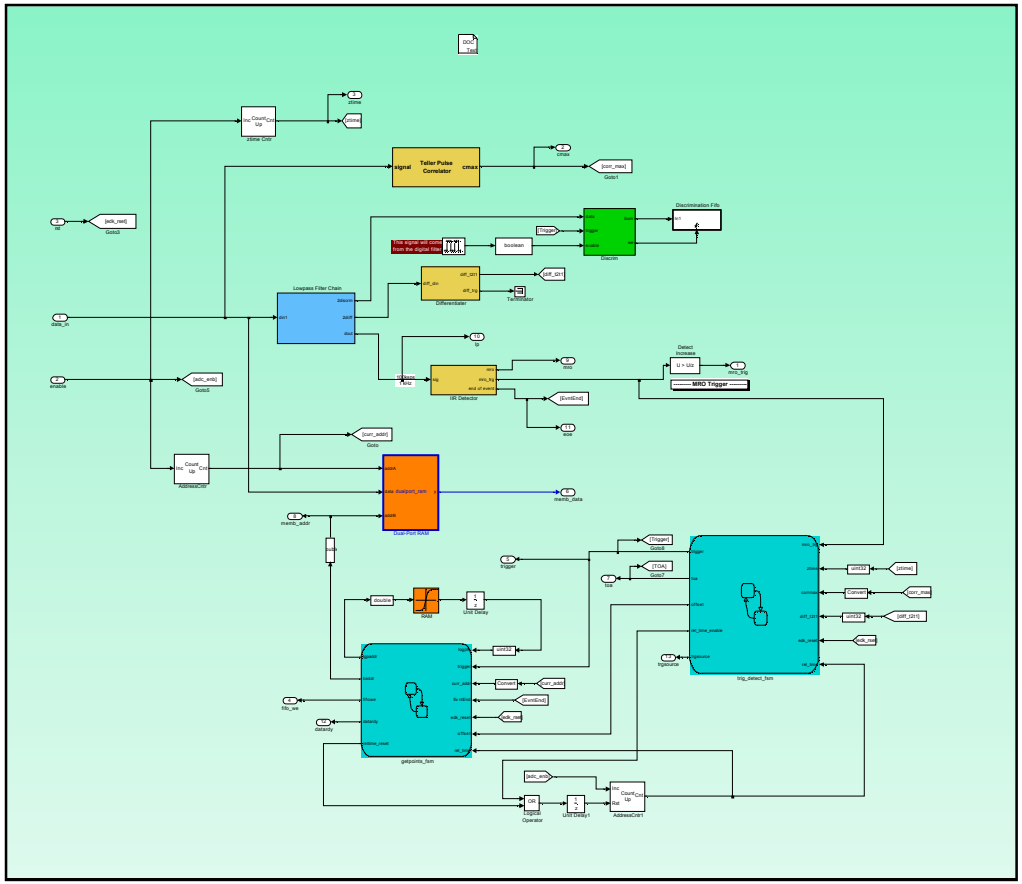
JAS Rapid Prototyping

Step 1: Generate Functional Block Diagram of DSP algorithms (Ex: Discrimination/ Clustering)



Step 2: Build Software Model of same (Ex: in Matlab/Simulink)

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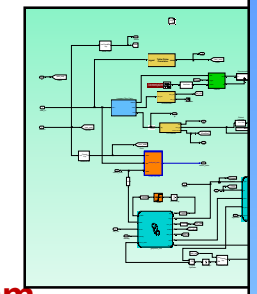
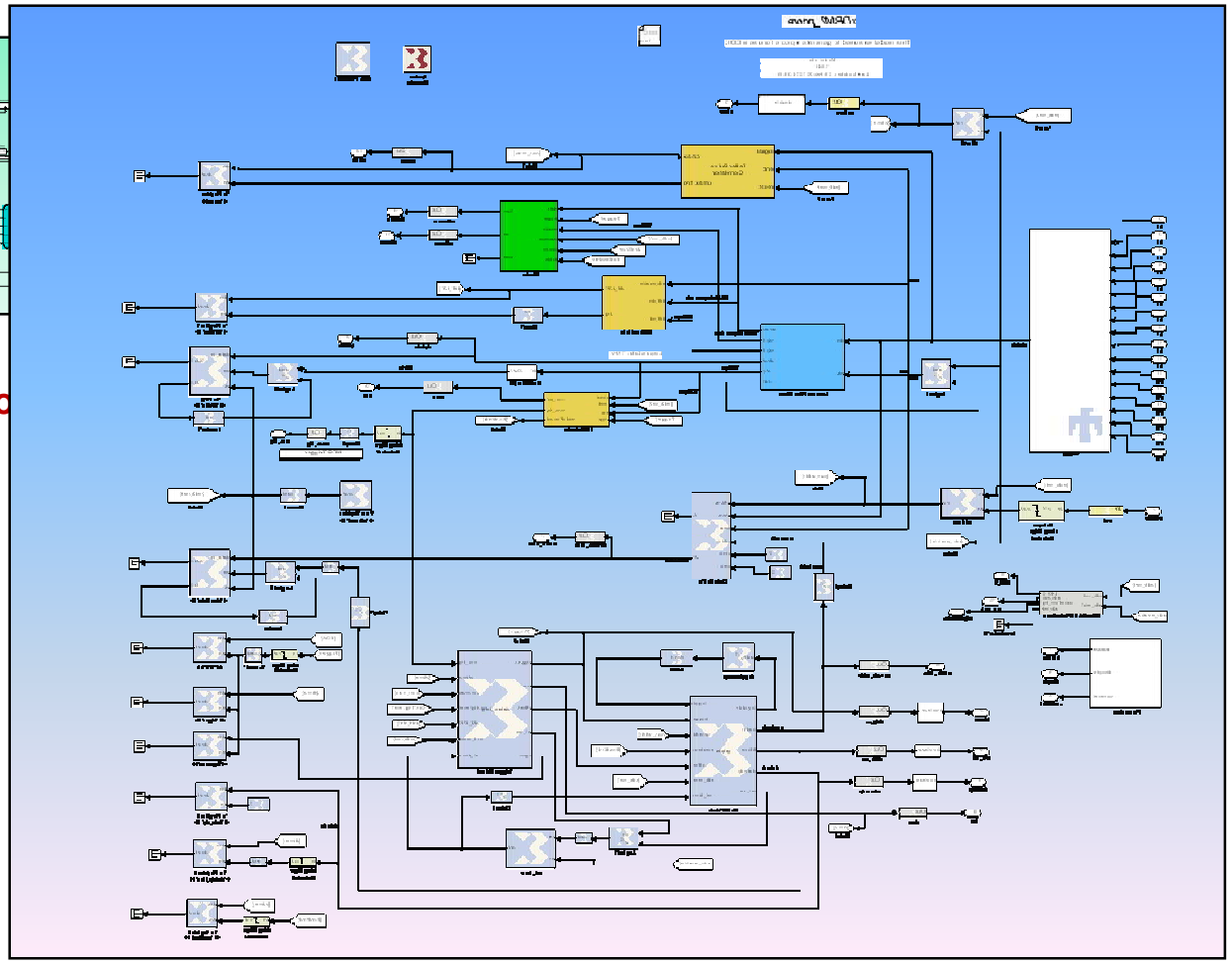
JAS Rapid Prototyping

Step 1:
Block Diagram

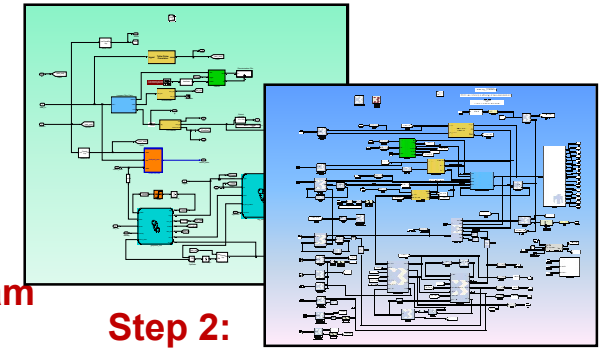


Step 2:
Software mo



Step 3: Generate VHDL code (Ex: from Matlab/ Simulink)

JAS Rapid Prototyping

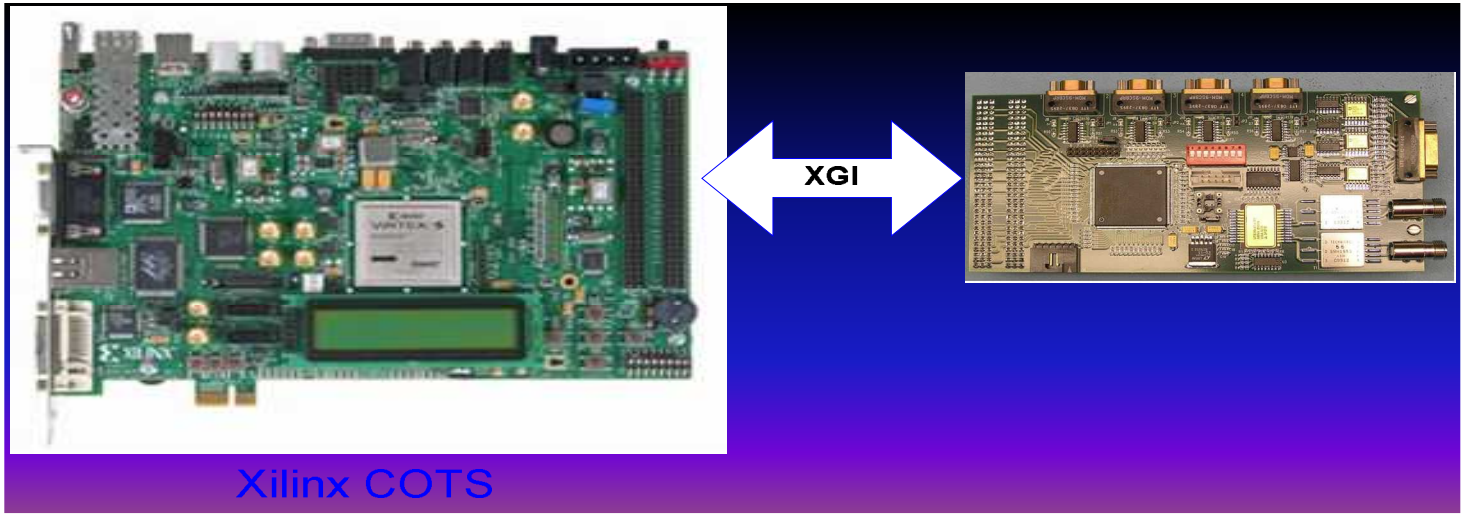


Step 1: Block Diagram

Step 2: Software model

Step 3: VHDL code

different payloads



Step 4: Upload code to XILINX Virtex 5 processor on JAS board (RP node) – Test and verify – Test part shown

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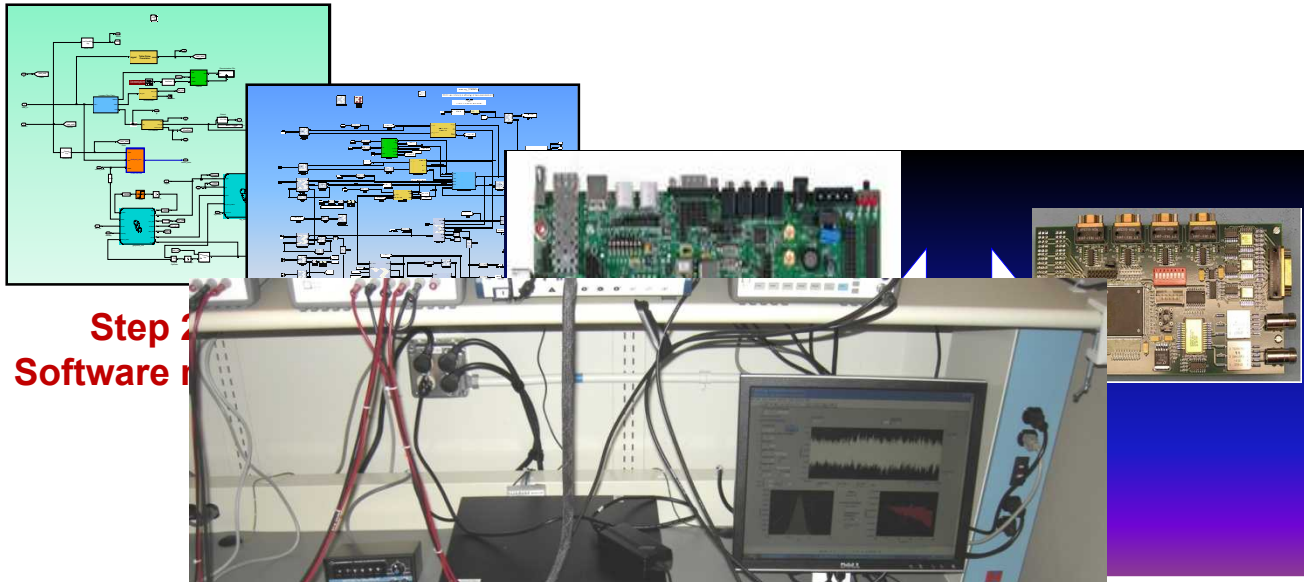
JAS Rapid Prototyping

Step 1:
Block Diagram



Step 2
Software r

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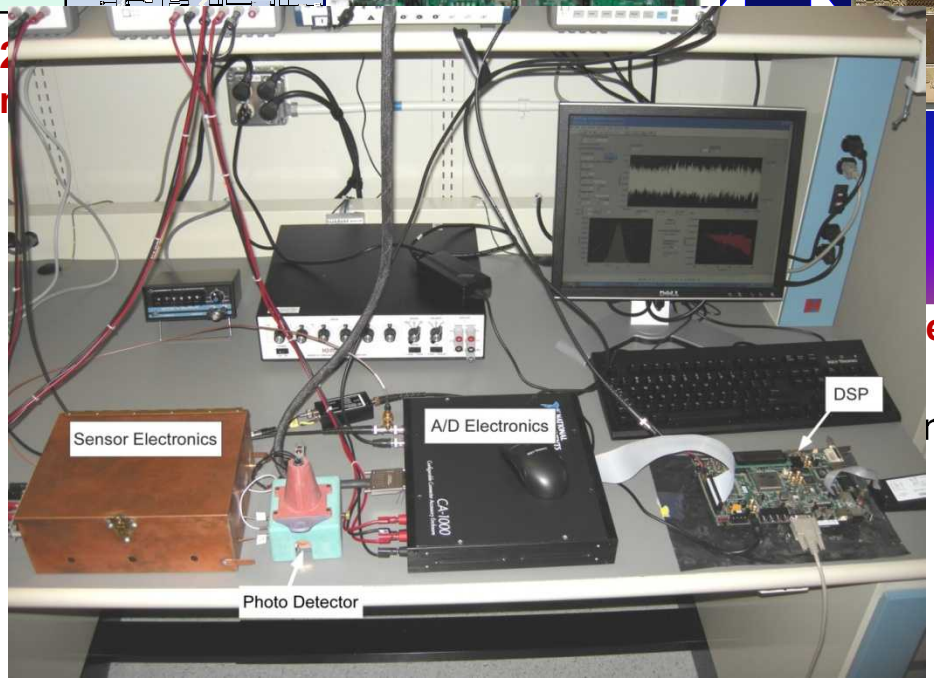

Step 5: Demonstrate End-to-end functionality with Sensor/Analog and JAS interfaces

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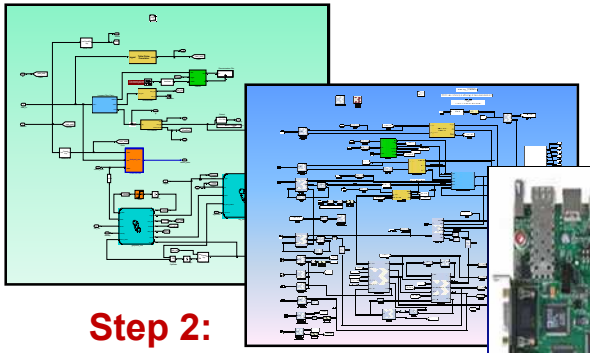
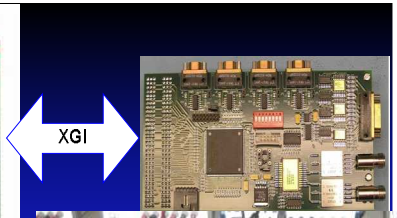
JAS Rapid Prototyping



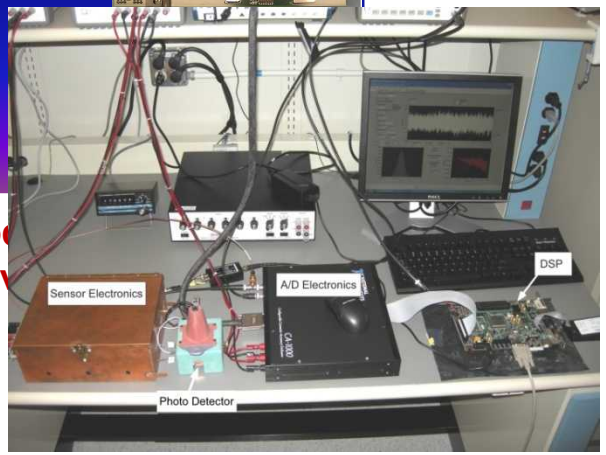
Step 1: Block Diagram

Step 2: Software model

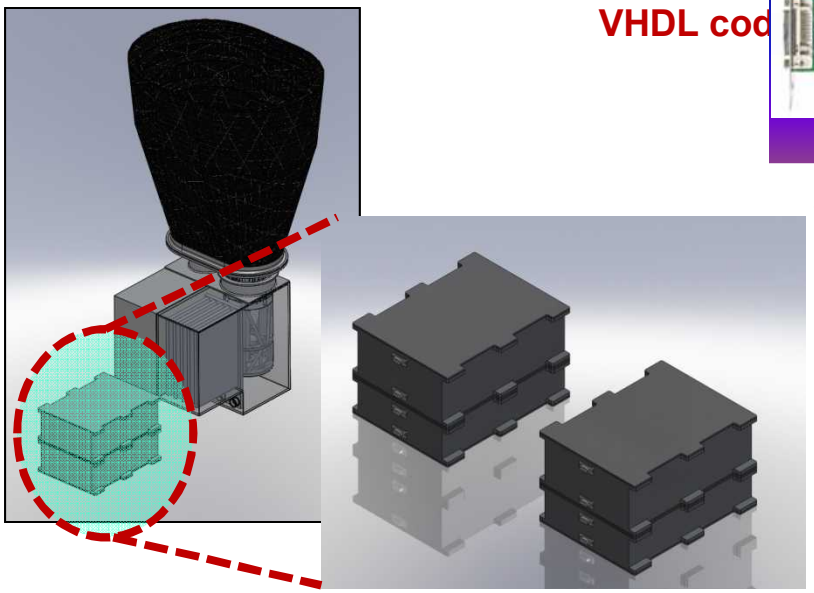
Step 3: VHDL cod



Step 4: Upload co



Step 5: End-to-end functionality demo prior to full implementation



Step 6: Migrate to flight hardware and Integrate

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Single Event Upset Xilinx-Sandia Experiment (SEUXSE)

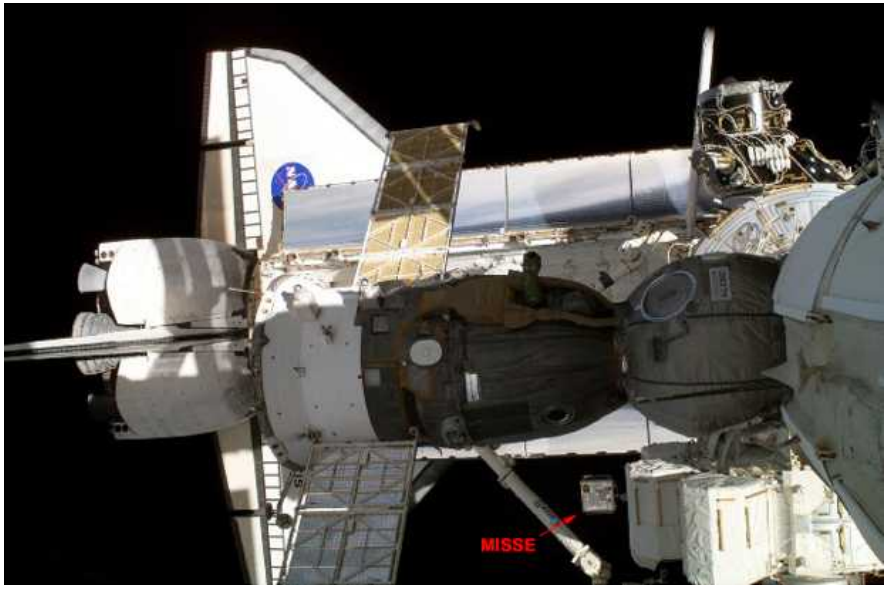
- **Early design, delivery and deployment of technologies relevant to the DOE/NNSA's Joint Architecture Standard (JAS)**
  - Xilinx Virtex-4 and Virtex-5 FPGAs
  - Point-of-Load (POL) power converters
  - Intellectual Property (IP)
  - Demonstrate in LEO space environment on the International Space Station
- **Single Event Upset (SEU) Detection and Characterization Using High Density Xilinx Field Programmable Gate Arrays (FPGA)**
- **Record Time and Bit Value of Each SEU Detected**
  - Continuous scrubbing of Xilinx configuration bits
  - Continuous exercising and monitoring of most functional logic elements within each Xilinx Virtex FPGA
- **Partnered with Xilinx , Xilinx Radiation Test Consortium (XRTC), NRL, NASA, and BYU**

MISSE Overview

- The purpose of the Materials International Space Station Experiment (MISSE) is to characterize the performance of new and prospective spacecraft materials and technologies when subjected to the combined effects of the space environment.
- The MISSE program has a rich history and benefits from six previous on-orbit payloads with substantial legacy hardware and design.
- MISSE 7 (launched Nov. 2009) is the first science payload for the Express Logistics Carrier (ELC) program and carries passive and actively powered experiments.
- One of two MISSE 7 Passive Experiment Containers (PECs) will be replaced by a MISSE 8 PEC (launch February 2011).

MISSE Background

- **Experiments up to 2 years on the ISS**
- **Launched and returned by Shuttle.**
- **Initially passive experiments only – combined UV, AO, radiation.**
- **Active experiments connect to ISS for power, commanding, telemetry.**



- **MISSE 1 & 2 (AFRL/ML)**
  - **Passive material exposures**
  - **Launched 2001, returned 2005**
- **MISSE 3 & 4 (AFRL/ML)**
  - **Passive material exposures**
  - **Launched 2006, returned 2007**
- **MISSE 5 (NRL)**
  - **Self-powered with on-board, two-way comm**
  - **Active solar cell and passive material experiments**
  - **Launched Aug 2005, returned Sept 2006**
- **MISSE 6 (AFOSR)**
  - **Passive and active expts – data loggers**
  - **Launched March 2008, returned Sept 2009**
- **MISSE 7 (NRL)**
  - **Passive and Active experiments (NRL-0602)**
  - **Launched Nov 2009**
- **MISSE 8 (NRL)**
  - **Passive and Active experiments (NRL-0602)**
  - **Launch scheduled for July 2010**

SEUXSE Design

- Xilinx Virtex 4 XQR4VFX60 FF1152 pin BGA
  - 50,560 Flip-Flops, 21 Mbit configuration memory
- Xilinx Virtex 5
  - SEUXSE I: Commercial LX330T FF1738 pin BGA
    - → 207,360 Flip-Flops, 83 Mbit configuration memory
  - SEUXSE II: SIRF FX1 CF1752 pin BGA
    - → 81,920 Flip-Flops, 50 Mbit configuration memory
- Four Embedded Processors Active
  - 2 silicon based PowerPCs, 2 soft core FPGA fabric based processors
  - 2 Mbytes of SRAM for each processor with EDAC
- OTP PROMs (XQR17V16) store FPGA configuration and Processor software
- Radiation Hardened Point-Of-Load (RHPOL) Power Converters
  - Sandia custom ASIC
  - First flight use of these devices
  - Two triple output controllers provide six rails
    - → (3.3 V, 2.5 V, 1.2 V (2), 1.0 V (2))

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SEUXSE Status

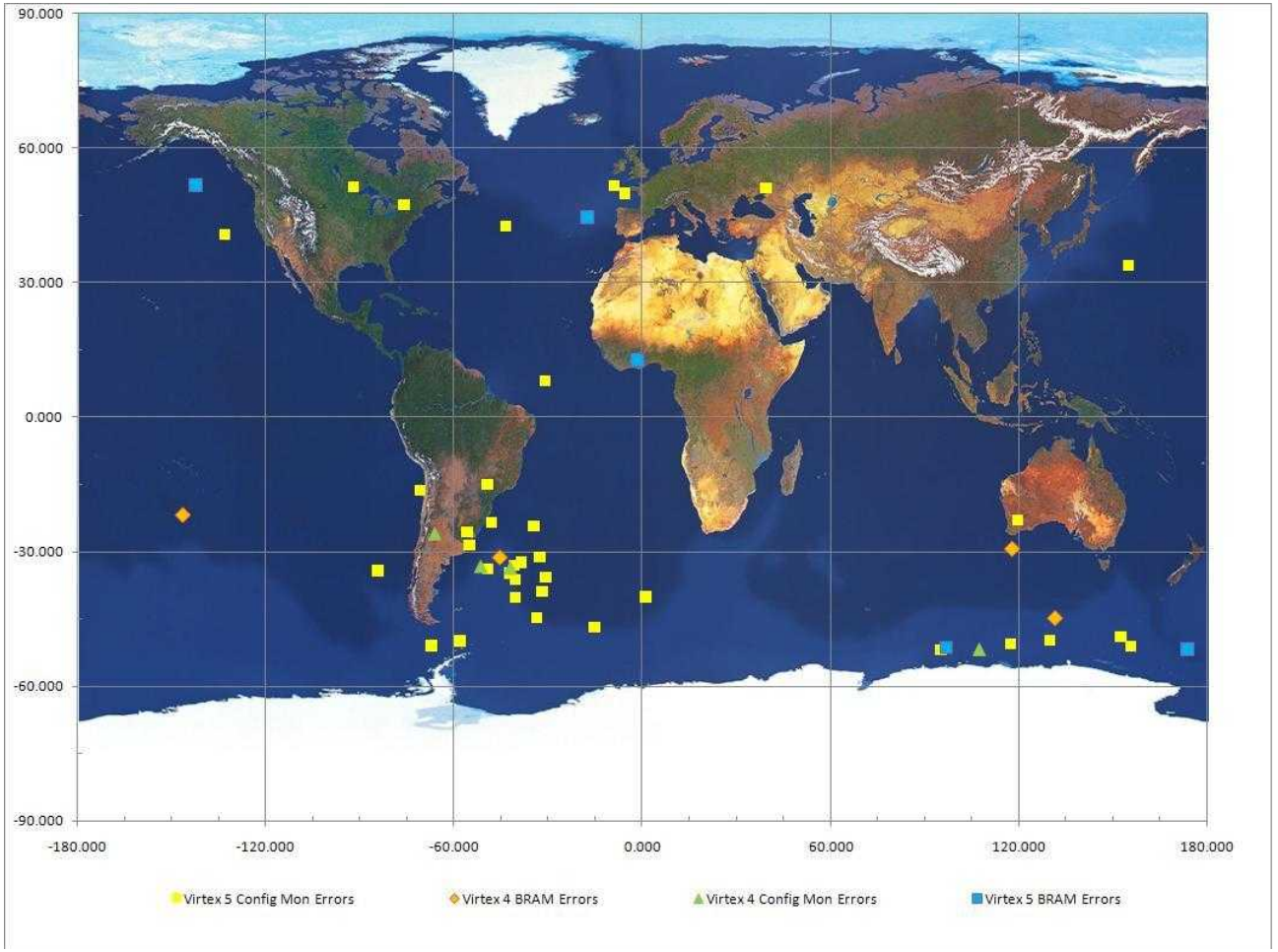
SEUXSE I

- Launched on STS-129 (11/16/09)
- ELC2 and MISSE 7-ExPA Deployed (11/21/09)
- MISSE7 PEC-A (SEUXSE) and PEC-B Deployed (11/23/09)
- As of July 2010, SEUXSE has operated for 199 out of 217 days since deployment. Other MISSE7 thermal issues caused on/off periods
- SEU Upsets as of June 28, 2010
  - No processor watchdog time outs
  - V4 BRAM errors = 12 (1 per 16.6 days)
  - V4 config errors = 29 (1 per 6.9 days)
  - V5 BRAM errors = 29 (1 per 6.9 days)
  - V5 config errors = 111 (1 per 1.8 days)

SEUXSE II

- Delivery to NRL on Feb 1, 2010
- Limited data from NRL shows SEUXSE II performing well after TVAC and vibration
- Passed EMI testing
- Original launch was scheduled for July, 2010, but ISS and shuttle delays caused slip until Feb. 2011
- SEUXSE I will be returned to earth when SEUXSE II is deployed

SEUs on MISSE 7's SEUXSE (2-9-10)



ISS location at SEU events.

Unclassified Unlimited Release

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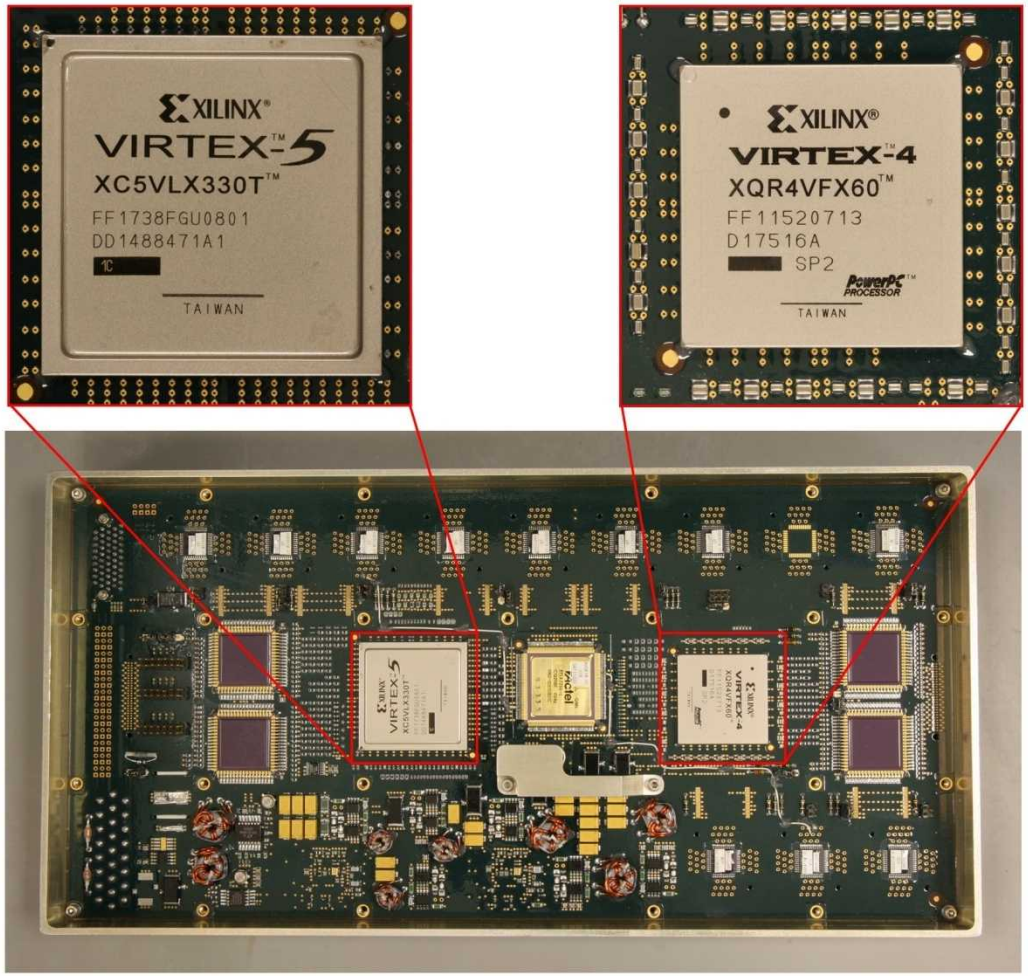
SEUXSE I Hardware



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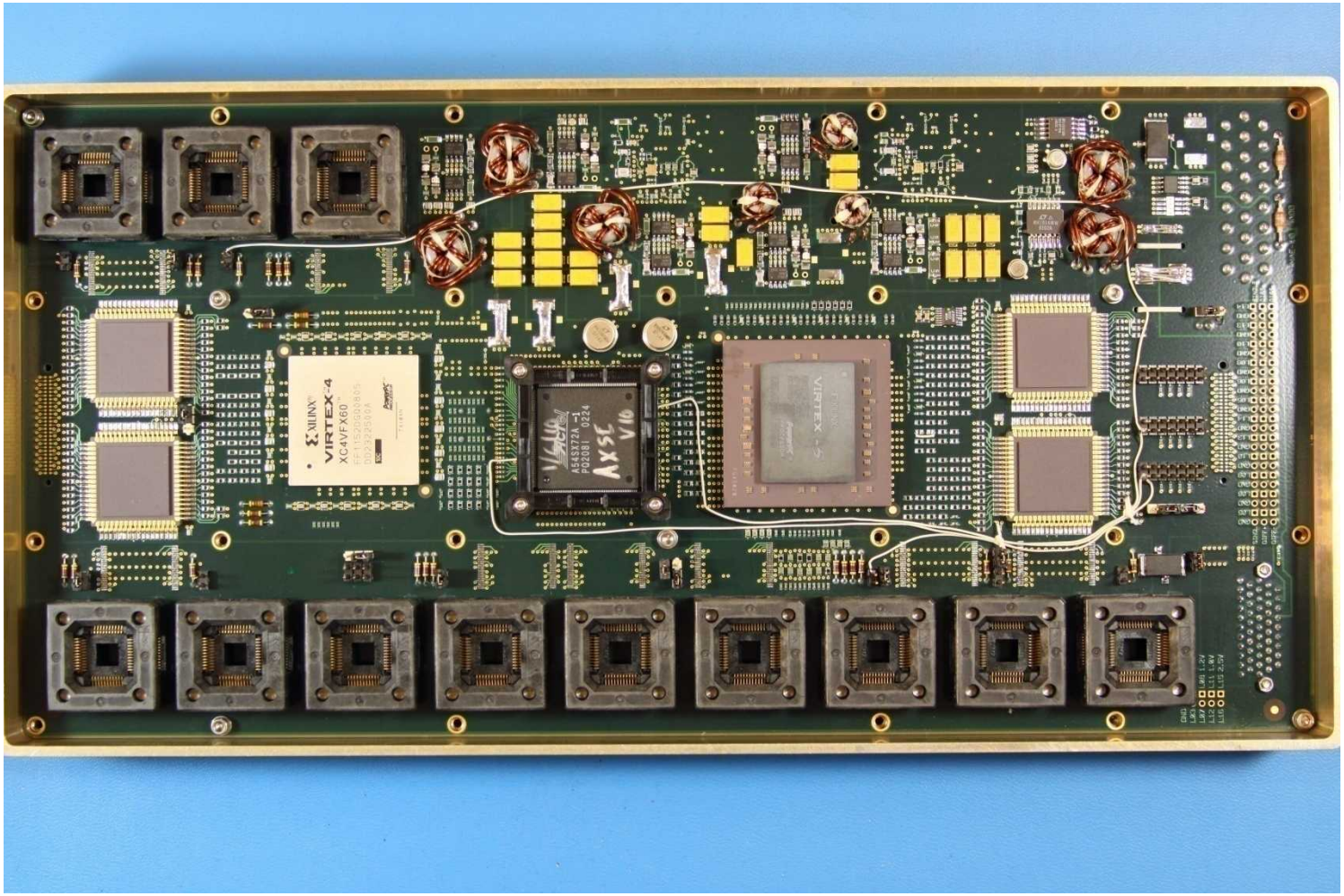
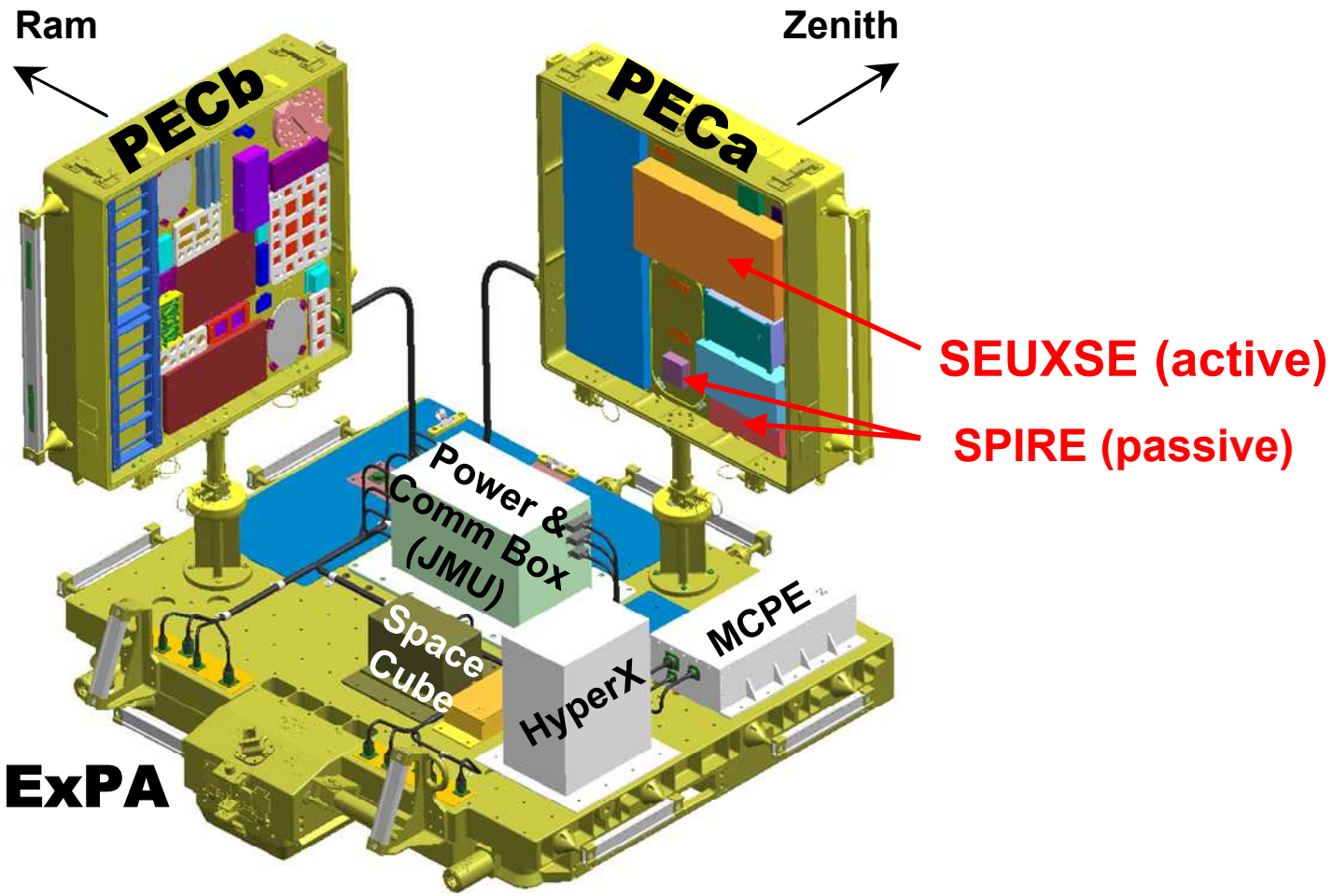
SEUXSE II Hardware

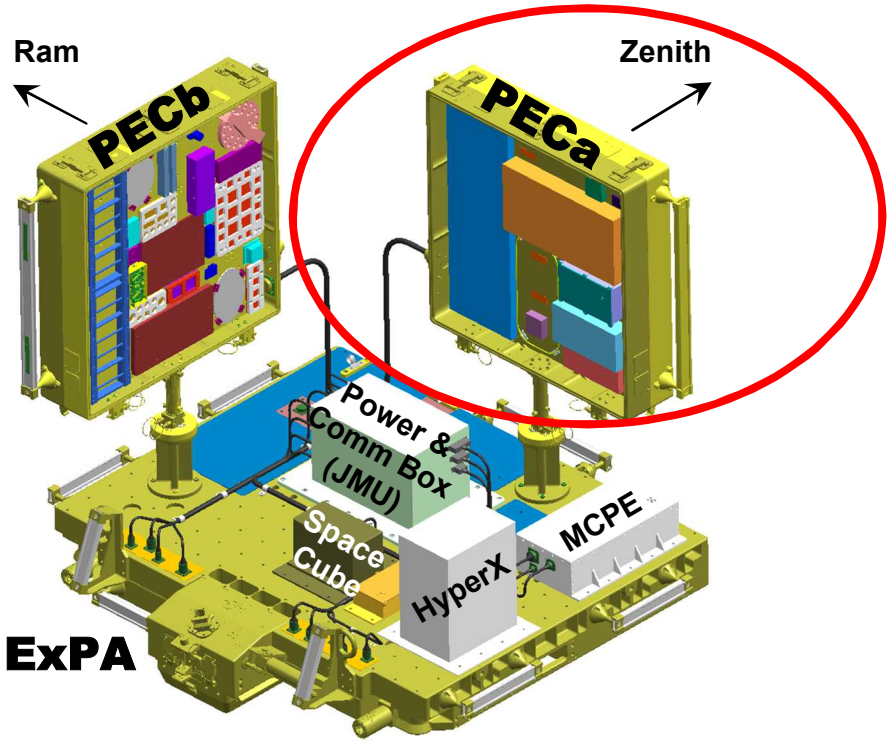


MISSE 7 3D Pictorial View



MISSE 8 Deployment

- MISSE 8 will Re-use MISSE 7 Infrastructure
  - *Single Passive Experiment Container (PEC)*
  - ISS Power
  - ISS Telemetry
- MISSE 8 will be only a single PEC to replace PECa
- MISSE 8 will be an exchange of one of the two MISSE 7 PECs using the same physical, data, and power interfaces



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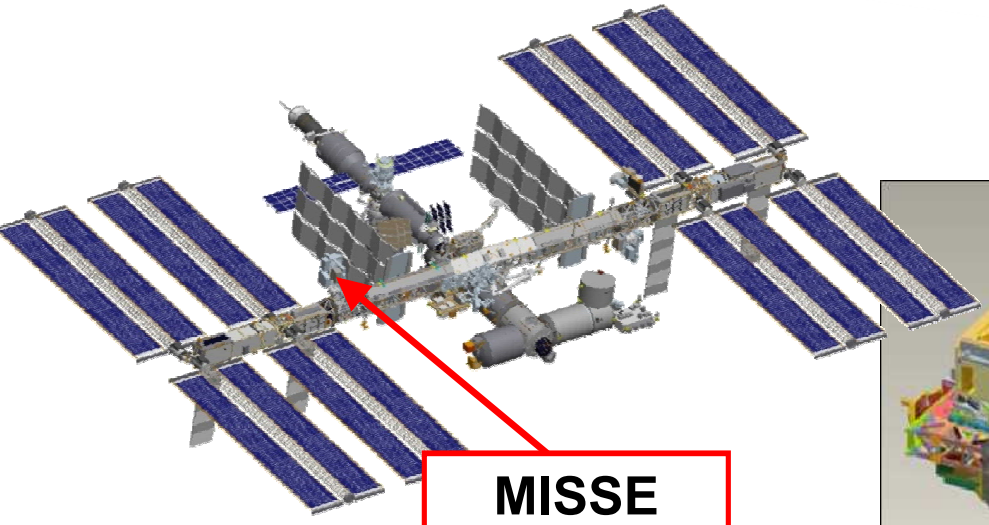
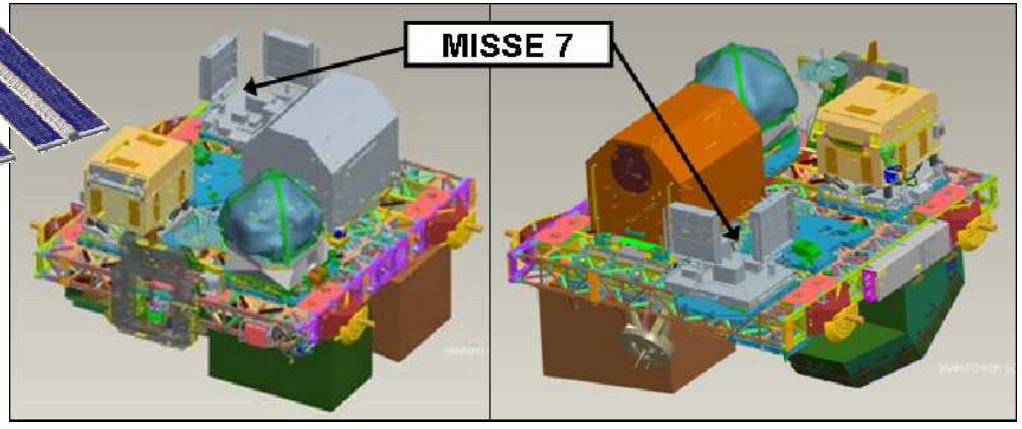
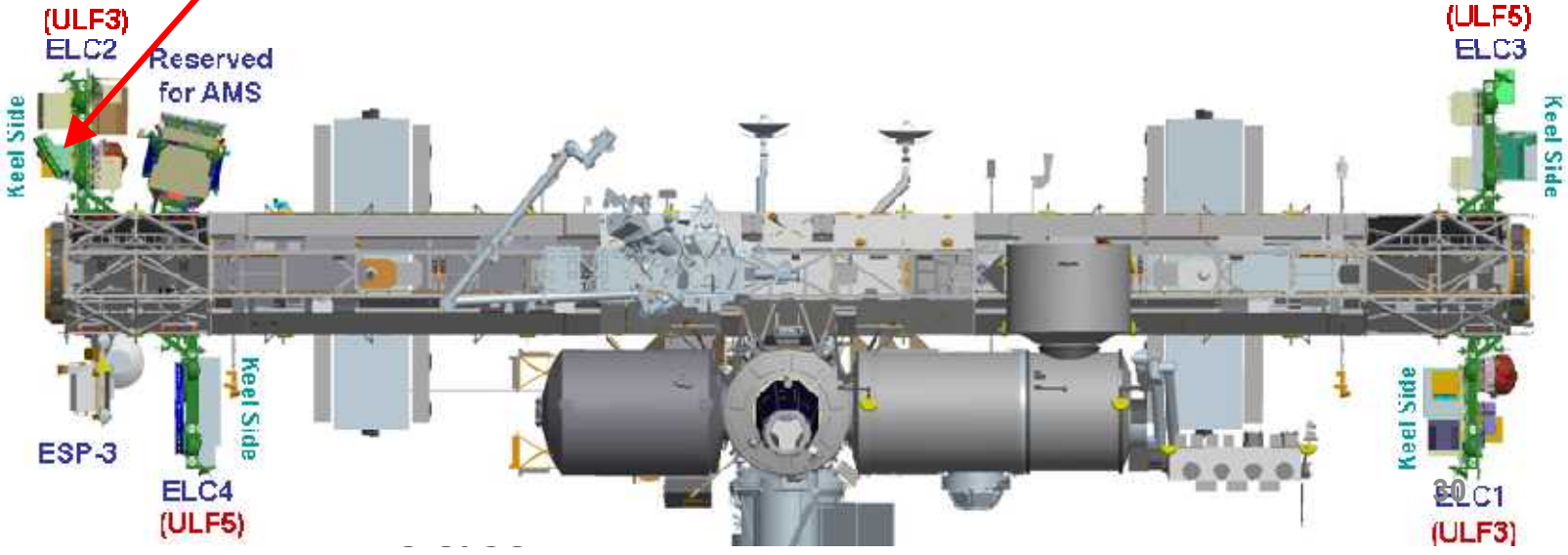
MISSE 7 & 8 Deployment Location







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PEC A & B Deployment On MISSE 7

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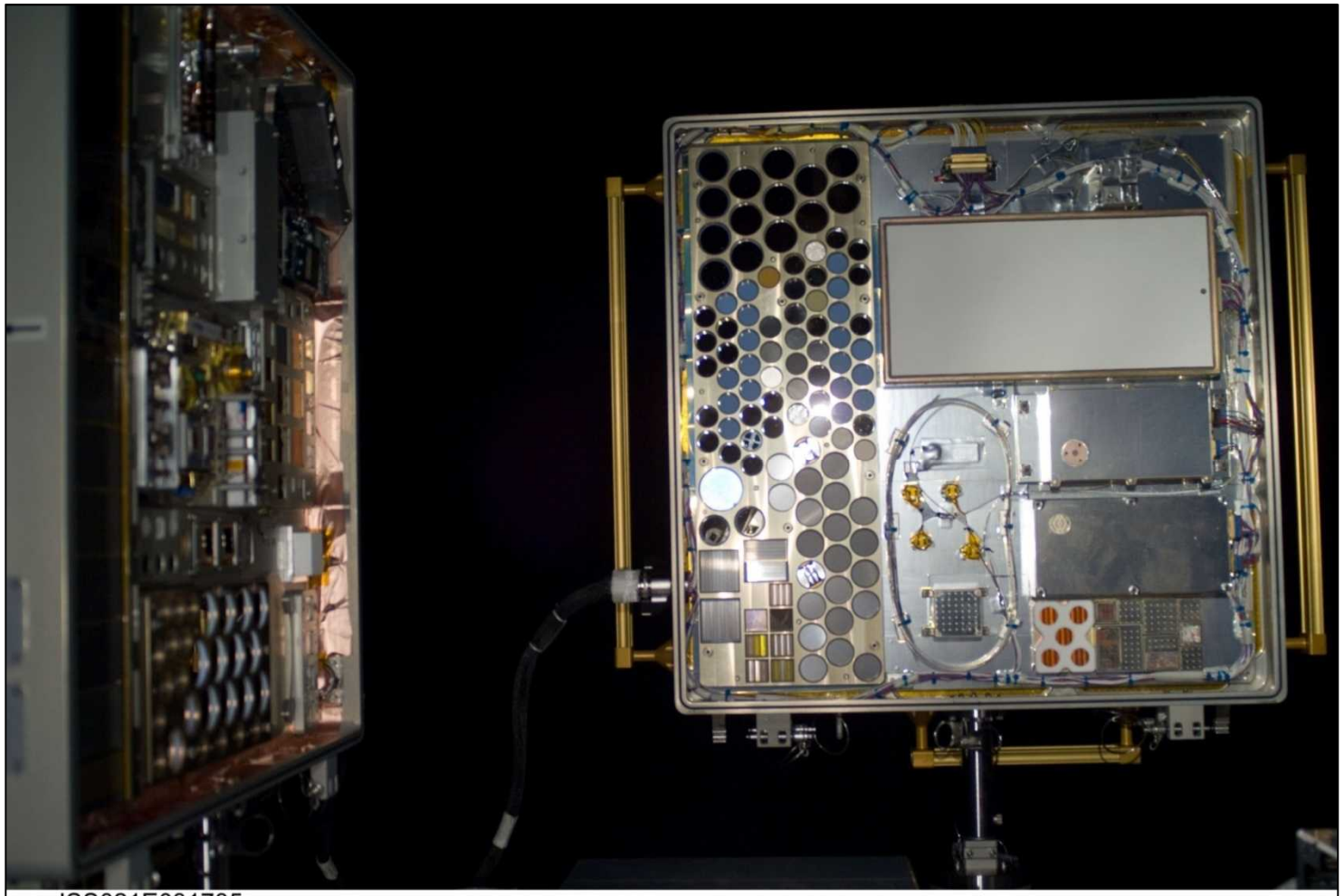
Close-up of PEC-A Nadir and SEUXSE/SPIRE



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Conclusion

- High-speed serial interconnects and FPGAs are the two key enabling technologies for JAS
- Serial interconnects and network communication enables complete modularity, scalability, and flexibility in the architecture
- FPGAs are critical hardware elements of the architecture by enabling:
  - Reuse of hardware building blocks for multiple applications
  - Provide mechanisms for flexible system redundancy and fail-over
  - Robust, power-on ready common network interfaces (Actel RTAX)
  - Reconfigurable high performance on-board computing (Xilinx V5QV)
  - Multi-mission capability through Partial Reconfiguration (Xilinx V5QV)
  - Support both HDL and sequential instruction implementations with the same hardware (soft core processors in Xilinx V5QV, Actel RTAX)
  - Rapid IP development and prototyping with reconfigurable devices (Xilinx V5, Actel ProASIC)